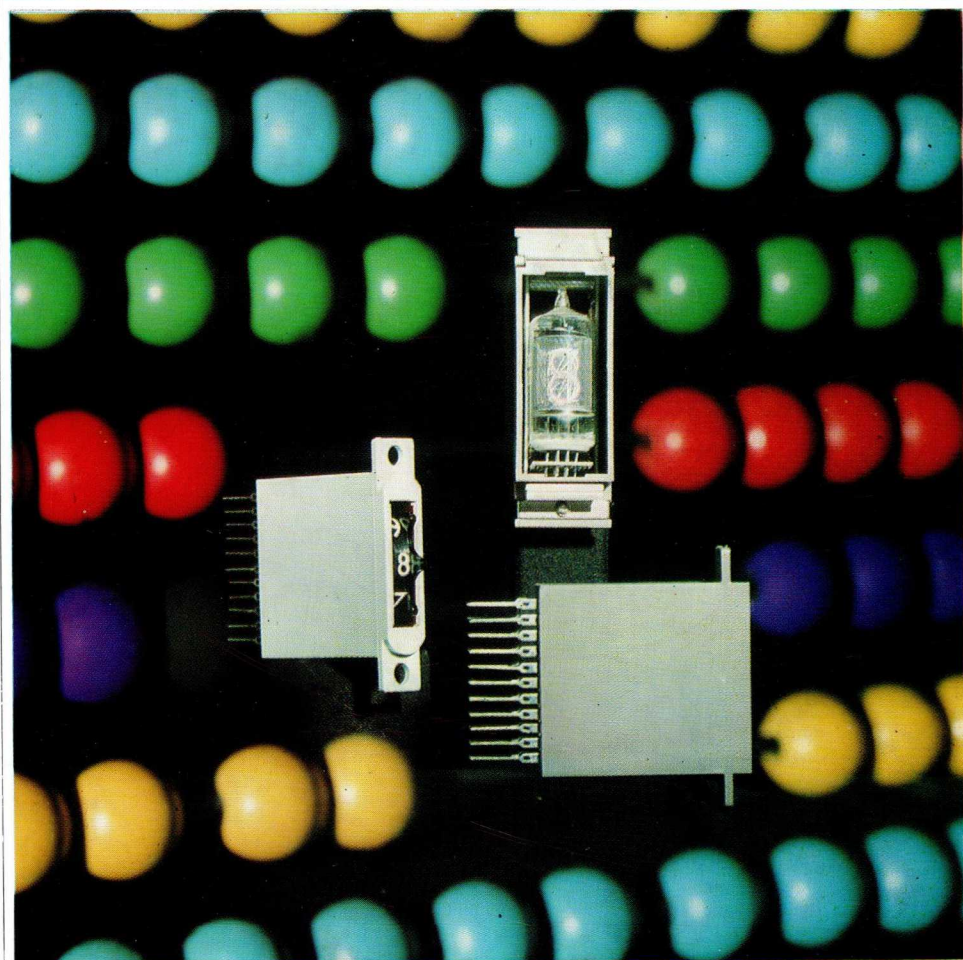


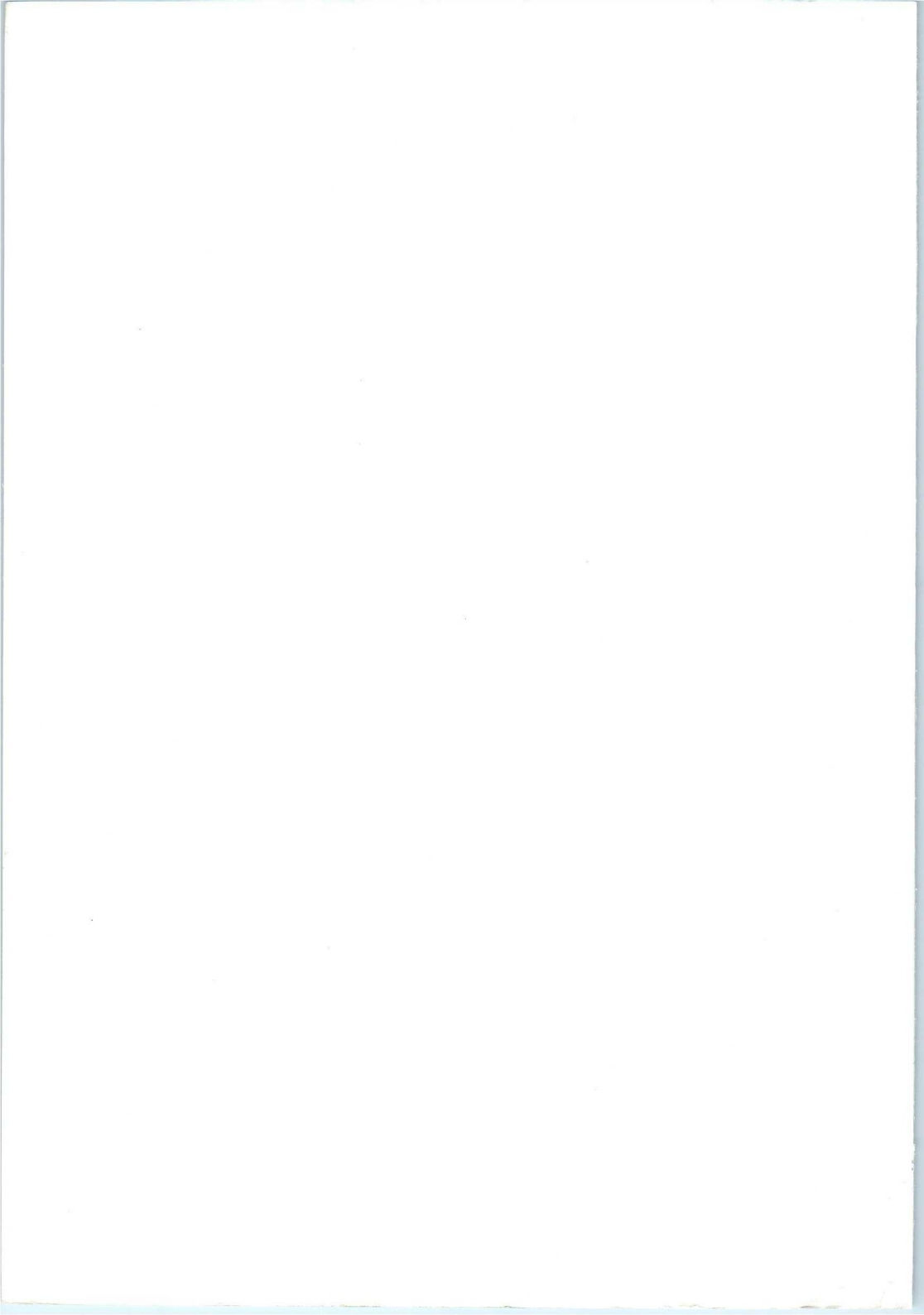
PHILIPS

APPLICATION BOOK

ELECTRONIC COMPONENTS
AND MATERIALS DIVISION

50-SERIES DIRECT DISPLAY COUNTERS





SERVICE CHART

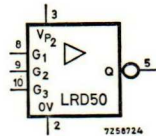
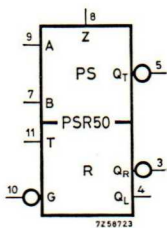
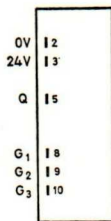
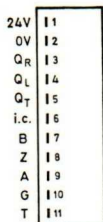
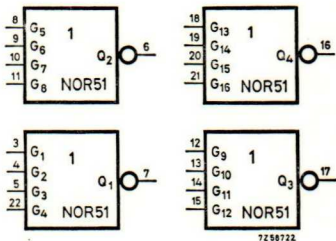
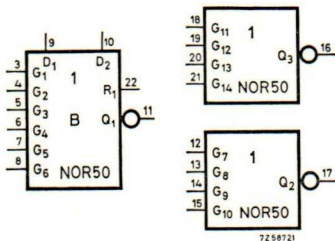
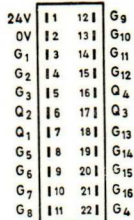
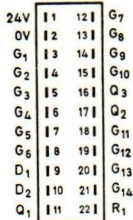
terminal locations

of 50-series direct display counters



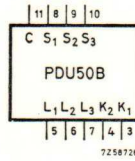
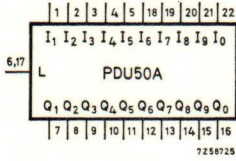
a complete range of modular sub-systems

for preset programmed control



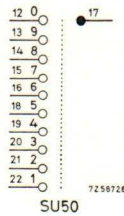
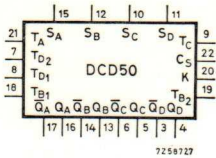
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I ₂	12	13	Q ₇
I ₃	13	14	Q ₈
I ₄	14	15	Q ₉
I ₅	15	16	Q ₀
L	16	17	L
Q ₁	17	18	I ₆
Q ₂	18	19	I ₇
Q ₃	19	20	I ₈
Q ₄	10	21	I ₉
Q ₅	11	22	I ₀

24V	I ₁
0V	I ₂
K ₁	I ₃
K ₂	I ₄
L ₁	I ₅
L ₂	I ₆
L ₃	I ₇
S ₁	I ₈
S ₂	I ₉
S ₃	I ₁₀
C	I ₁₁



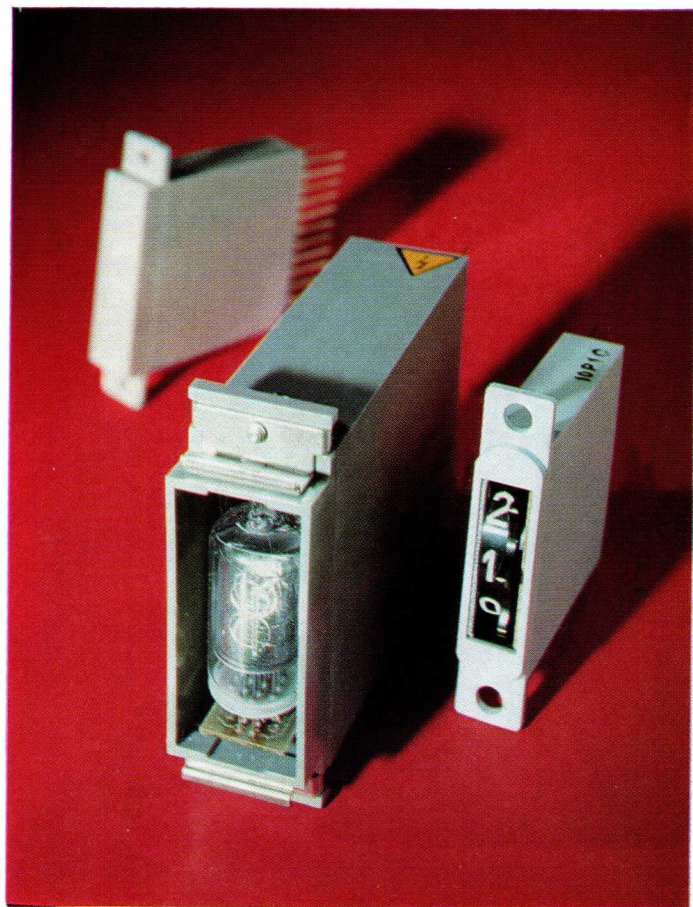
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0V	12	13	Q _B
\bar{Q}_D	13	14	\bar{Q}_B
Q _D	14	15	S _A
Q _C	15	16	Q _A
\bar{Q}_C	16	17	\bar{Q}_A
T _{D2}	17	18	T _{B1}
T _{D1}	18	19	T _{B2}
T _C	19	20	K
S _C	10	21	T _A
S _D	11	22	C _S

12	0
13	9
14	8
15	7
16	6
17	out
18	5
19	4
20	3
21	2
22	1



31-

50-Series Direct Display Counters



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EINDHOVEN - The Netherlands

June 1970

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50-Series Direct Display Counters

edited by **J. Deerson**

PUBLICATIONS DEPARTMENT
ELECTRONIC COMPONENTS AND MATERIALS DIVISION

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50-series specifications are contained in Part 1 of the Components and Materials (green Series) section of the System, to which the reader is referred.

Quality Control and Environmental Test Specifications

A basic design concept for the 50-Series was that the modules remain operating reliably under the most severe conditions, and that they have a long life while remaining inside specified tolerances.

These concepts have been realised by publishing worst-case figures for all component parameters. This means that the module circuits have been designed taking into account not only initial tolerances, but also expected changes in characteristics which will occur over long periods of use.

All quality assessments are of course based to a large extent on sampling tests. Because an occasional module may fail early in life however, the quality control procedures used are designed to minimise this possibility. In addition, batches are regularly taken from the production line and put through worst-case life tests.

The diagram shows the events and processes occurring in the manufacture of the modules, together with the tests which are applied. Tests are carried out both by the factory personnel and by a special independent Quality Control Department.

Applications

Although numerous, many applications for the modules are immediately obvious, and we present here a brief list of some of the more popular ones.

General industrial batch counters, for instance seed batch counters, production line counters.

Dosing machines, for instance control of chemical blending plant.

Control of injection moulding machines.

Control of galvanizing processes.

Synchronizing systems for two shafts, matching both speed and phase.

Tachometers and speed measurers.

Length measuring equipment.

Automatic coil-winding machines.

Control apparatus for copying music tape on tape recorders, and so on.

Introduction

How to use this book. The contents of this book have been arranged in three sections, as follows:

- *Part 1*, Basic Design Considerations;
- *Part 2*, Counting Circuits;
- *Part 3*, Practical Considerations.

In Part 1 are discussed the essentials which the reader who has not worked with 50-Series modules before needs to know. Part 1 covers physical and electrical characteristics applicable to the series as a whole, brief individual functional descriptions, and the drawing symbols used. It explains in a few paragraphs the design philosophy.

In Part 2 are contained all the tried and proven 50-Series circuits — or at least, all the ones we know about. The first seven chapters in this section discuss the flexibility and applications of seven of the modules; subsequent chapters describe input drive circuits, examples of sub-systems such as time-delays and decoders, and examples of systems which can be considered as virtually complete. The circuits described in this section will be found to cover virtually all applications, when combined in the appropriate manner.

Part 3, Practical Considerations, discusses operating speed, loading rules, installation requirements, electrical considerations, and accessories which are available. It should perhaps be mentioned here that all input and output voltages in the 50-Series are matched. The designer has only to check the Loading Table when making schematic diagrams.

At the back of the book is an index which we have made as complete as practicable. As a further aid, the coloured card enclosed gives a handy guide to pin numbers for interwiring.

This book has been written as a practical, more than a theoretical, guide; the designer will in most cases find everything in it necessary to design the counting and display system he requires, from scratch. Full detailed specifications on the modules are not included, however, and for these the designer must make use of our Data Handbook System. The

Preface

The application of counting techniques to industrial automation is now a well-established fact. Their wider adoption has been made possible by the development in recent years of high speed electronic counters embodying transistorized circuits, with greatly increased reliability. Although these counters are now relatively inexpensive, the provision of a numerical display of the count, which is necessary in many applications, has been difficult and costly.

The 50-series range of counting modules solves this problem immediately by having as its basic module a decade counter with integral numerical display.

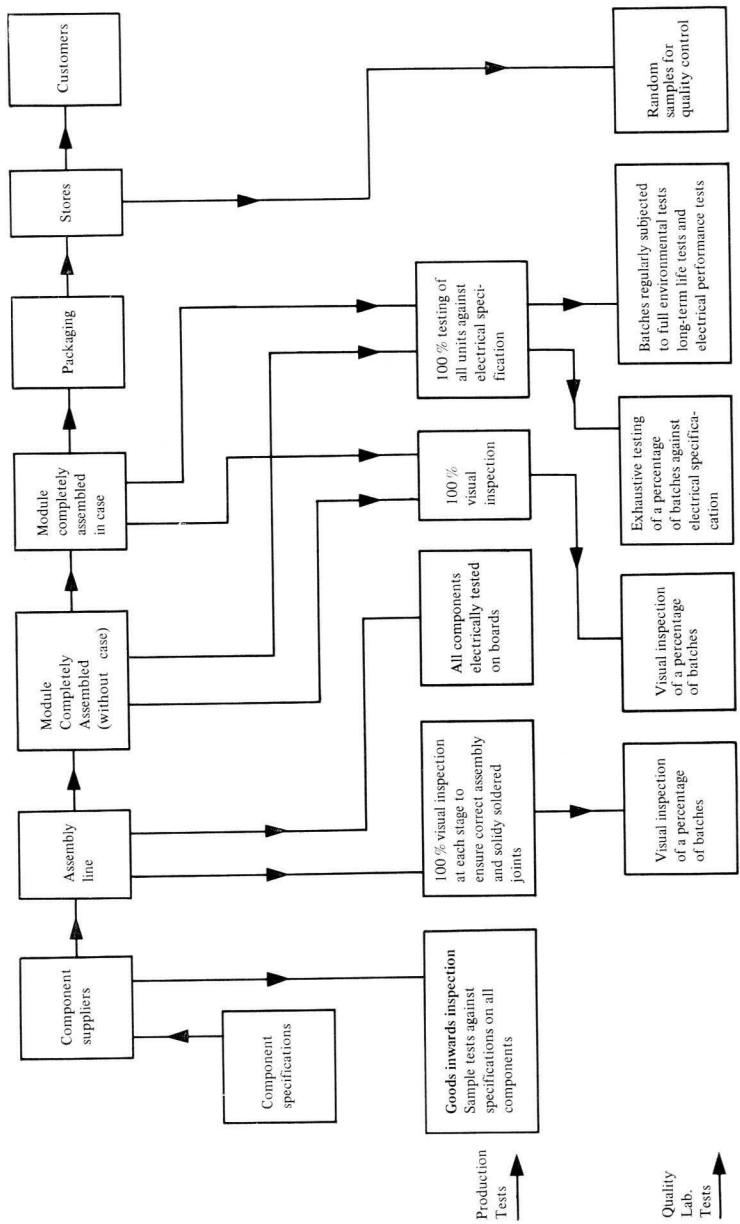
The supporting modules in the range enable preset counting, logic operations, reversible counting and output drive functions to be added as required. Careful attention to details such as pin layout and ease of mounting has greatly simplified interwiring and installation.

A range of compatible input transducers is also available, and the counter modules may be easily integrated with our 60-Series NORbit modules to enable design of more complex control systems.

Acknowledgement

For their valuable contributions and assistance in preparing the book acknowledgement is due to:

A. G. Beresford	Mullard Ltd., Crawley
J. C. Besse	RTC-La Radiotechnique-Compelec, Paris
H. J. M. v. d. Burgt	Elcoma Division, Philips Eindhoven
P. Deerson	Elcoma Division, Philips Eindhoven
R. Dubbe	Valvo GmbH, Hamburg
J. Heuveling	Elcoma Division, Philips Eindhoven,
B. Starr	Mullard Ltd., Crawley



Block diagram of tests and checks carried out on modules during manufacture.

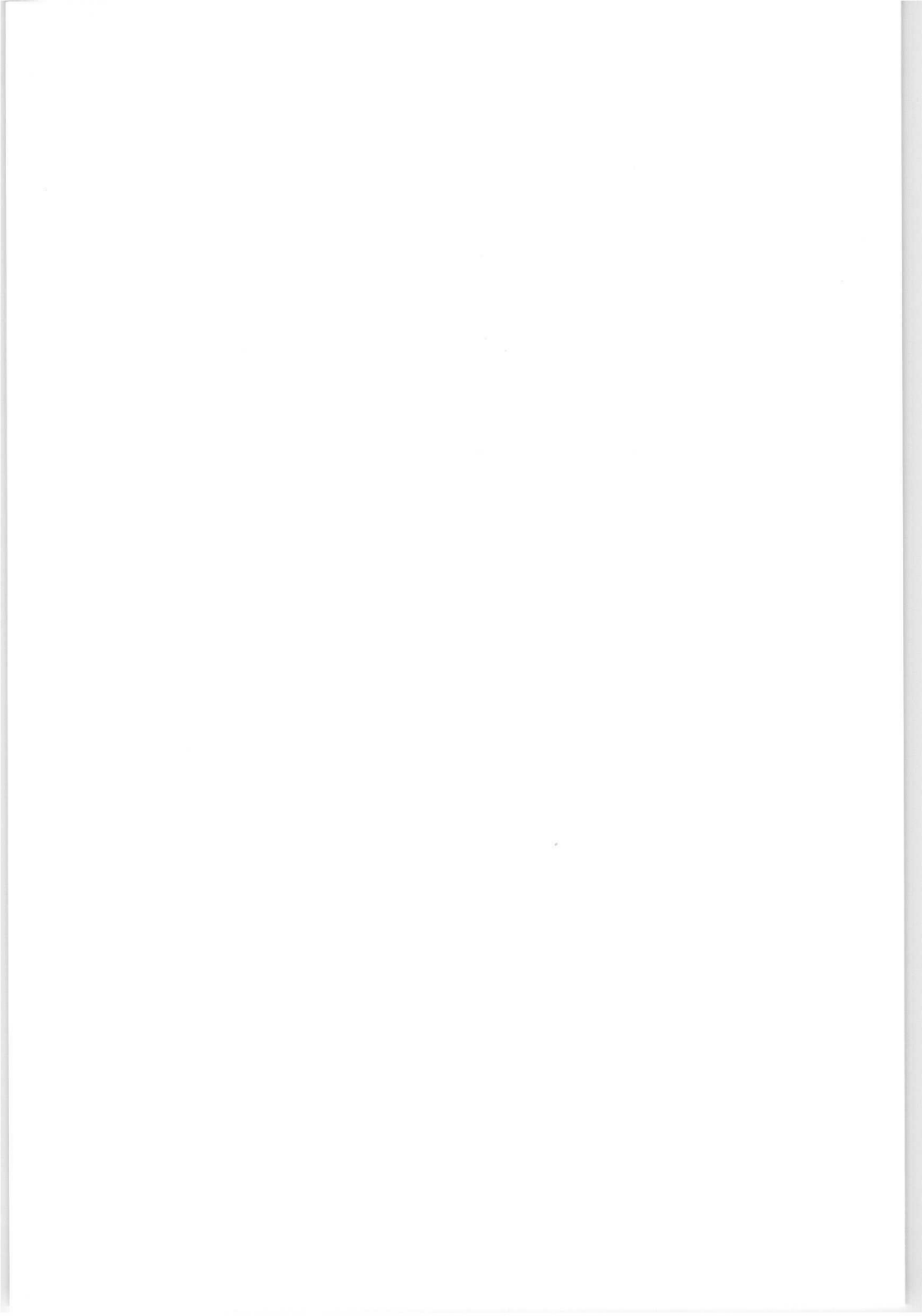


Reaction time measurement

This reaction timer measures physical reaction times, reflex times, operation times, etc., and is used by sportsmen as an aid to training (by courtesy of Ets Bettendorff S.A., Brussels, Belgium).

PART I

General Design Philosophy



1 Characteristics

1.1 Physical Characteristics

Fig. 1-1 illustrates the three types of case in which the range is housed. Type *A* comprises the counting/display modules, type *B* the auxiliary ones and type *C* the preset switches.

1.1.1 PIN CONNECTIONS

The modules have pins mounted in one or two rows at the rear of the case. The pins are suitable for soldered and "wire-wrap" connections. For "wire-wrap" details, please turn to section 17.2.2.

1.1.2 MOUNTING

All three types of housing are designed to be installed from the rear of the mounting panel, simple cutouts being required for types *A* and *C*. These two modules have front façades available in single and multiple sizes up to a maximum of 6.

Fig. 1-2 shows the front façades of modules type *A* and *C* in a three-decade/two-programme counter.

A mounting bar is available for type *B*. Mounting techniques, cutout details etc. are fully covered in sections 17 and 19.

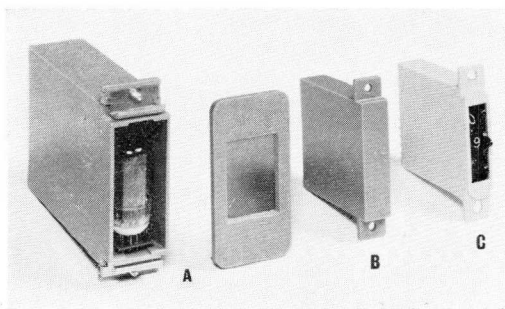


Fig. 1-1. The three case types.

1.2 Electrical Characteristics

1.2.1 COUNTING RATE

Uni-directional:	50 kHz maximum
Bi-directional:	12 kHz maximum

1.2.2 TEMPERATURE RANGE

Operating:	-25 °C to +70 °C
Storage:	-40 °C to +85 °C

1.2.3 SUPPLY VOLTAGE

Logic supply:	single rail +24 V d.c. $\pm 10\%$
Indicator tube supply	single rail +250 V d.c. $\pm 18\%$

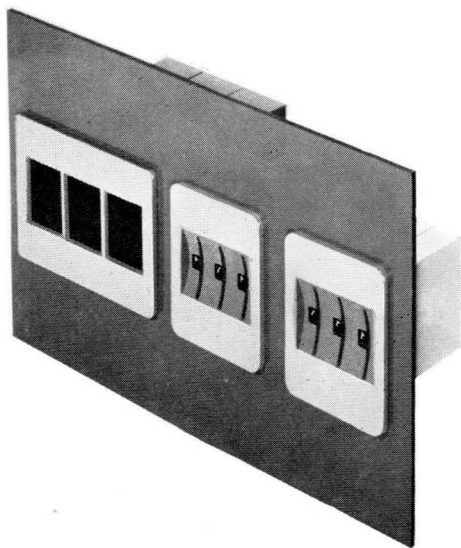


Fig. 1-2. The front façades of modules type A and C in a three-decade|two-programme counter.

2 Functional Description

2.1 Display Modules

2.1.1 NUMERICAL INDICATOR COUNTER NIC50

This module is the basic uni-directional decade counter with direct display of characters 0-9 and decimal point.

Its output is in decimal form, and its symbol is shown in Fig. 2-1 (Type A case).

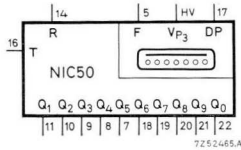
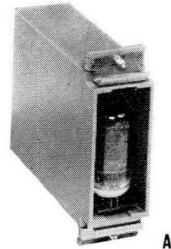


Fig. 2-1. NIC50 symbol.



2.1.2 REVERSIBLE INDICATOR COUNTER RIC50

This module is a bi-directional decade counter with direct display of characters 0-9 and decimal point. Its output is in decimal form, and the symbol is shown in Fig. 2-2 (Type A case).

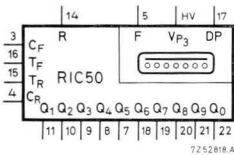


Fig. 2-2. RIC50 symbol.

2.1.3 MEMORY INDICATOR DRIVER MID50

This module is used to store information from the decade counters NIC50 and RIC50. Direct display of characters 0-9 and decimal point is possible; decimal output is available for e.g. printer drive. Its symbol is shown in Fig. 2-3 (Type A case).

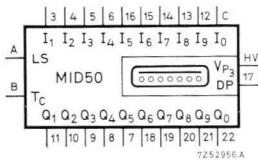


Fig. 2-3. MID50 symbol.

2.1.4 SIGN INDICATOR DRIVER SID50

This module, whose symbol is shown in Fig. 2-4, gives direct display of plus and minus characters. In addition the tube can be brought to the dark condition. The characters *X*, *Y*, *Z* and \sim are also accessible (Type *A* case).

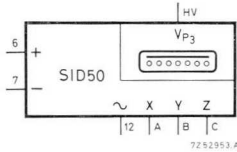


Fig. 2-4. SID50 symbol.

2.2 Auxiliary and Logic Modules



B

2.2.1 TRIPLE NOR MODULE 3NOR50

This module carries a Buffer NOR stage (designed to decode the counter module outputs) and a further two NOR circuits for additional logic, e.g. a memory function. The symbols for the three functions contained in this module are shown in Fig. 2-5 (Type *B* case).

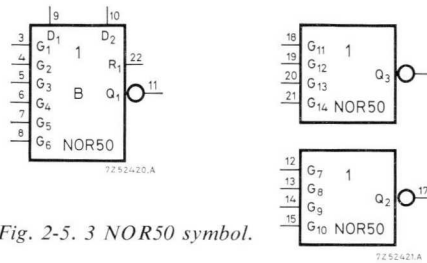


Fig. 2-5. 3 NOR50 symbol.

2.2.2 QUADRUPLE NOR MODULE 4NOR51

Four NOR circuits identical to the logic NOR's of the 3NOR50 module are provided to enable further logic to be performed. Fig. 2-6 shows the symbols for these functions (Type B case).

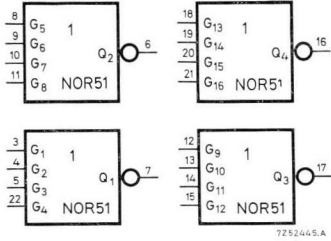


Fig. 2-6. 4NOR51 symbol.

2.2.3 PULSE SHAPER - RESET MODULE PSR50

This dual purpose module provides (a) a pulse-shaping function for transducer inputs to the counter, and (b) a reset function for both counter and logic reset. The symbol is shown in Fig. 2-7 (Type B case).

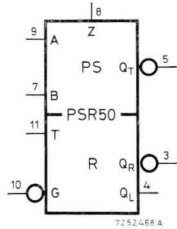


Fig. 2-7. PSR50 symbol.

2.2.4 LAMP-RELAY DRIVER LRD50

This module whose symbol is shown in Fig. 2-8 is capable of driving d.c. loads up to a maximum of 300 mA at 30 V (Type B case).

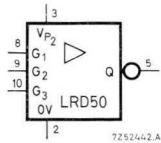


Fig. 2-8. LRD50 symbol.

2.2.5 PRINTER DRIVE MODULES PDU50A AND PDU50B

The modules PDU50A and PDU50B, fed by the decimal output of the NIC50, RIC50 counters or the memory unit MID50, operate as interface stages to drive decimal input printers. The symbols are shown in Figs. 2-9 and 2-10 (Both type *B* case).

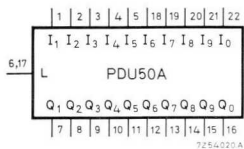


Fig. 2-9. PDU50A.

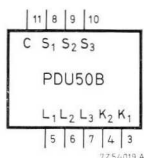


Fig. 2-10. PDU50B.

2.2.6 POWER SUPPLY MODULE PSU50

This module provides +24 V d.c. for the logic and +250 V d.c. for the indicator tubes, sufficient to supply a typical 12-decade system. Mains input can be 110, 220, 230 or 240 V, 45-65 Hz. The PSU50 is shown in the photograph of Fig. 2-11.

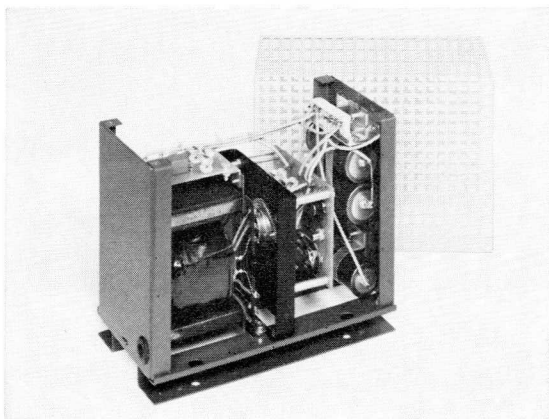


Fig. 2-11. PSU50.

2.2.7 DECADE COUNTER AND DIVIDER, DCD50

The DCD50 provided for non-indicating counting applications contains four separate flip-flops. By interconnecting the correct terminals externally a divider of 2, 3, 4, 5, 6, 8, 9, 10, 12 or 16 can be made. The symbol is shown in Fig. 2-12 (Type B case).

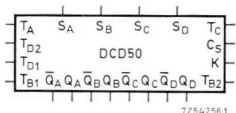


Fig. 2-12. DCD50 symbol.

2.3 The Switch Unit



The switch unit in the 50-Series is a ten-position thumbwheel switch, type 10P1C, termed the Switch Unit, SU50. It is used to obtain variable preset outputs from the counter units. Any similar, good quality, 10-position switch may be used for this purpose. The SU50 has the type C housing. Its symbol is shown in Fig. 2-13.

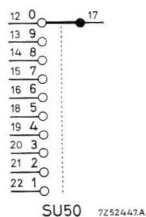


Fig. 2-13. SU50 symbol.

2.4 Accessories

2.4.1 THE EMPTY CASE ASSEMBLY, ECA50

The ECA50 contains an unwired general purpose printed wiring board (see Fig. 2-14) to enable the user to make non-standard circuits and to encase discrete components (Type *B* case).

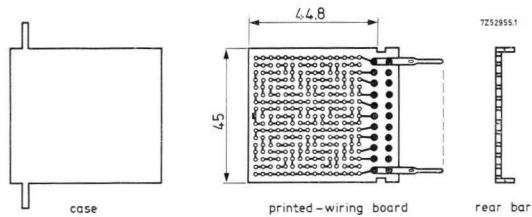


Fig. 2-14. ECA50. Dimensions are in mm.

2.4.2 OTHER ACCESSORIES

Front façades, mounting bar, drawing sticker symbols, and flexible prints are also available (see Section 19).

3 Drawing Symbols

Drawing symbols for 50-series modules appear in two forms: the “sticker” symbols, and schematic symbols.

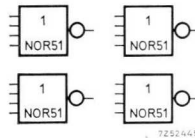
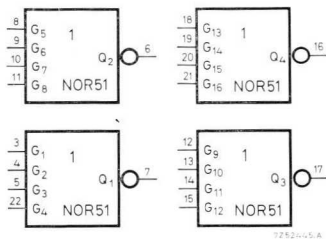
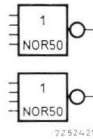
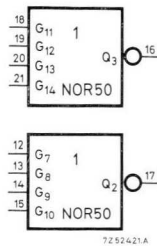
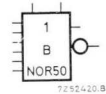
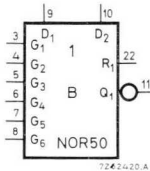
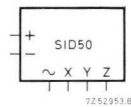
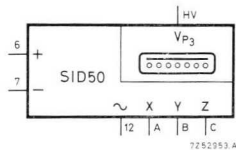
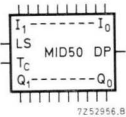
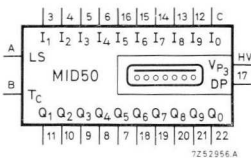
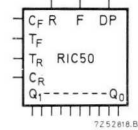
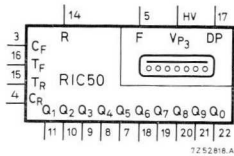
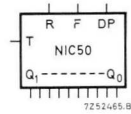
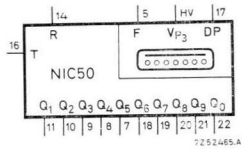
3.1 Sticker Symbols

The sticker symbols are printed on self-adhesive, transparent material, intended as an aid for the circuit designer in preparing detailed diagrams. They are available in sheets, each sticker being detachable from the sheet without cutting (see section 19.2).

3.2 Schematic Symbols

Due to space limitations, the diagrams given in this book have been made using “schematic” symbols. These are smaller and simpler than the sticker symbols described above and contain no terminal numbers. Only a few of the schematic symbols contain terminal letter symbols. Schematic symbols are not available for general use.

Fig. 3-1 compares the two types of symbols (*see next page*).



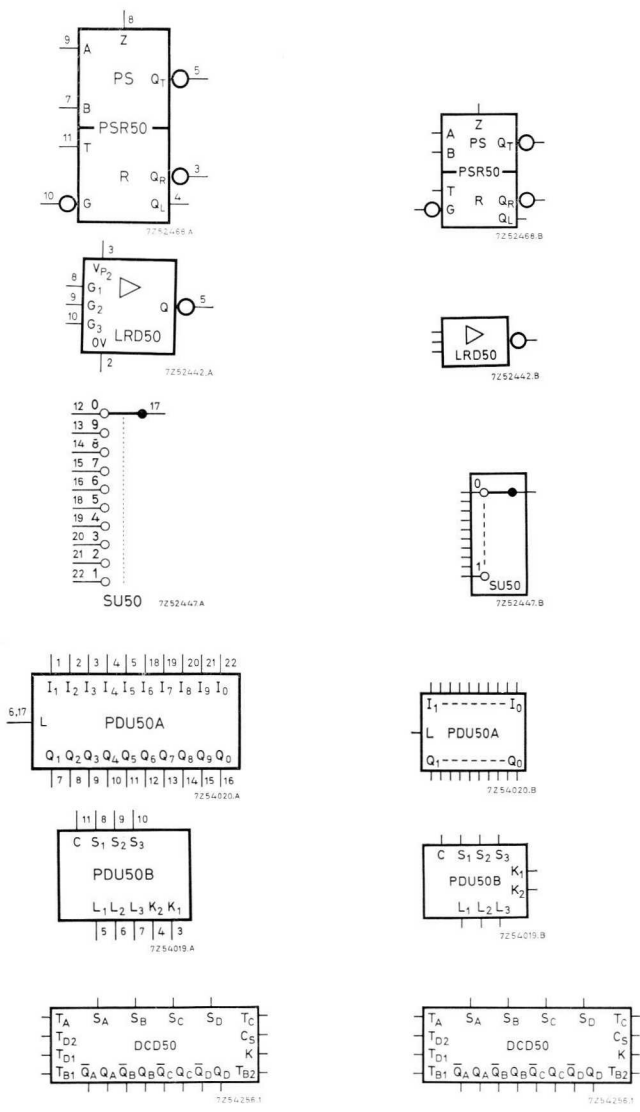


Fig. 3-1. Schematic symbols compared with sticker symbols.

4 The 50-Series Design Philosophy

A brief guide is given here to general principles of design, discussing the basic functions of counting, counting/logic interface, the logic, the output, and finally reset and input principles.

4.1 Counting

The 50-Series has been built up around two modular decade counters, the NIC50 (uni-directional) and the RIC50 (bi-directional). Each contains a ring counter using silicon controlled switches (SCS's) driving directly a built-in indicator tube. They have decimal output, all ten digits being accessible for driving subsequent circuitry. The active digit (the one being displayed) has a LOW output voltage level, i.e. close to 0 V, the other nine digits remaining at HIGH level (a positive voltage). These two levels LOW and HIGH are often represented by *L* and *H*. Although the 50-Series has been designed primarily for systems using up to 6 decades and 6 programmes, larger systems can easily be made, as explained in Part 2 of this book.

4.2 Interfacing with the Logic

Use of SCS's means that the counter output signals must be adjusted to normal logic levels. This is achieved by using a "Buffer NOR" function (one part of the 3NOR50 logic module) as interface. This function must always be interposed between counters and logic. The Buffer NOR performs exactly the same logic function as the normal NOR.

4.3 The Logic System

Logic operations can now be carried out with NOR functions. There are four separate functions in the 4NOR51 module, and two (besides the Buffer NOR in the 3NOR50). The basic logic operations are NOT, AND, OR, and Memory, and all these can be made with various NOR connections, as shown in Figs. 4-1 to 4-4.

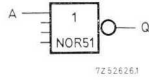


Fig. 4-1. "NOT" operation.

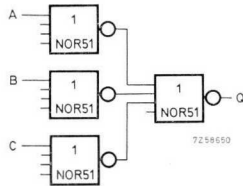


Fig. 4-2. "AND" operation.

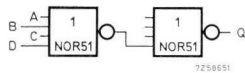


Fig. 4-3. "OR" operation.

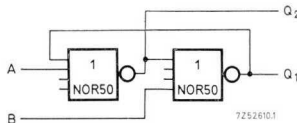


Fig. 4-4. Memory function.

The NOR function operates as follows. If one or more inputs are made HIGH, the output becomes LOW. The fact that the NOR output is LOW can be seen from the symbol for the NOR: a small circle or "state indicator" at the output. (Note that several of the other module symbols also have state indicators; the same rule regarding *L* or *H* level applies). Fig. 4-5 shows the state indicator on the NOR symbol; Table 4-1 shows the result of various combinations of input signal levels.

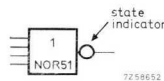


Fig. 4-5. State indicator.

Table 4-1. Truth Table for NOR Function.

A	inputs			D..	output
	B	C	Q		
H	H	H	H	L	
L	H	H	H	L	
H	L	H	H	L	
L	L	H	H	L	
H	H	L	H	L	
L	H	L	H	L	
H	L	L	H	L	
L	L	L	H	L	
H	H	H	L	L	
L	H	H	L	L	
H	L	H	L	L	
L	L	H	L	L	
H	H	L	L	L	
L	H	L	L	L	
H	L	L	L	L	
L	L	L	L	H	

As may be seen from the above, the only input combination for which the NOR output is at *H* level is when *all* inputs are at *L* level.

4.4 Output Drive

An output module, the LRD50, is available for driving lamps and/or relays. It operates as a NOR function, but has an output capability of 300 mA at 30 V.

4.5 Input Requirements

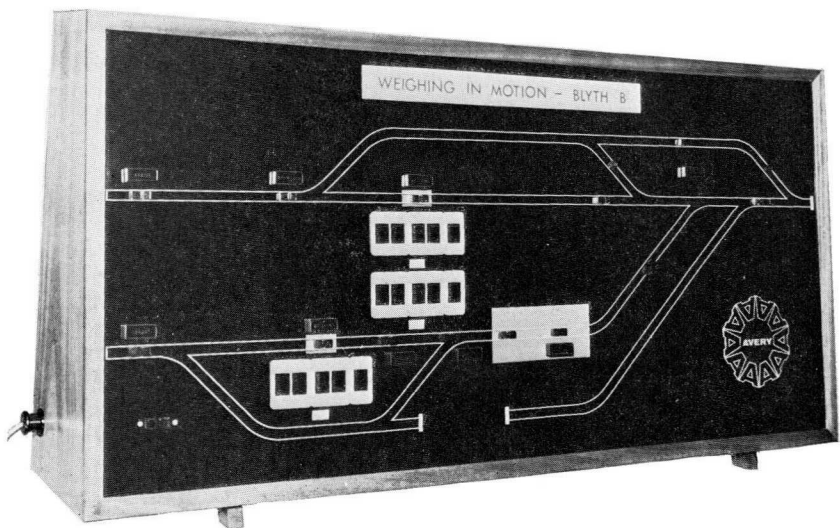
Many types of transducers are available for the purpose of providing input signals for the system. The signals must however conform to the input requirements of the counters, and for this purpose a pulse-shaper circuit is provided.

The module housing the pulse-shaper also contains a reset circuit delivering two output signals, an *L* level resetting the counters to zero and an *H* level resetting the memories in the logic to the original state. The module is termed the PSR50.

4.6 Additional Modules

Other modules available in the series are:

- the memory indicator driver, MID50;
- the sign indicator driver, SID50;
- the 10-position thumbwheel switch, SU50 (type 10PIC);
- the power supply unit, PSU50;
- the decade counter and divider, DCD50;
- printer drivers PDU50A and PDU50B.

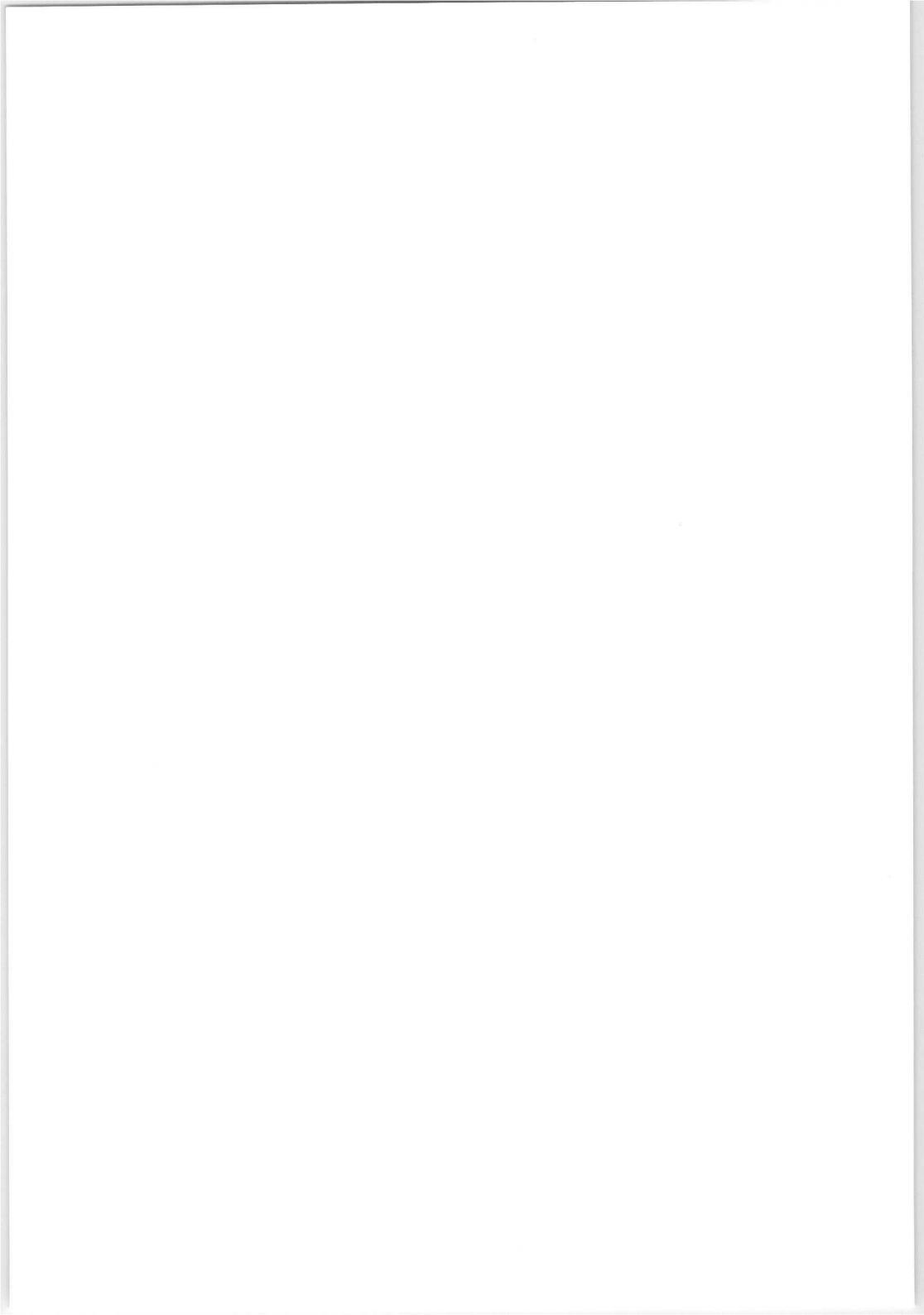


Weighing Wagons in Motion

The installation shown was designed by W. & T. Avery, Birmingham, England, to measure and record the weights of railway wagons passing a certain point. As loaded trains run over the incoming weigh-bridges the individual wagon gross weights are stored in delay-line stores. The system can store the wagon weights of three complete trains each comprising 40 wagons. Gross, tare and net weights are printed out, printing being synchronized by a simple rotor in conjunction with a vane-switched oscillator.

PART II

Counting Circuits



5 Unidirectional Counting with the NIC50

Fig. 5-1 shows the circuit diagram for a simple three-decade, uni-directional counter. Note the following points:

- The input pulses are applied to the pulse shaper section of the PSR50 module; maximum value of R is 39 k Ω . The PSR50 must be used to obtain pulses of the correct form for the NIC50 module. Input transducers are discussed fully in Chapter 12. Fig. 5-2 shows the timing requirements of the pulse-shaper signals; Table 5-1 gives the input data.

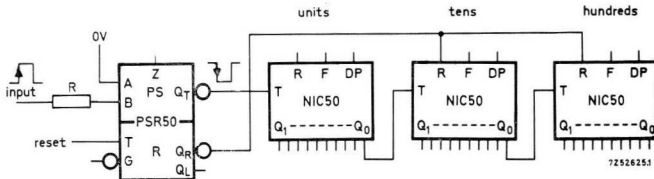


Fig. 5-1. Three decade uni-directional counter.

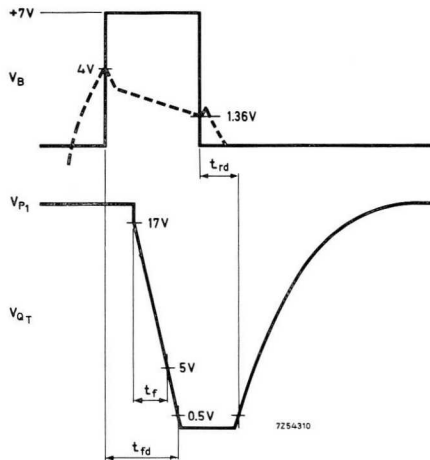


Fig. 5-2. Timing requirements of the pulse-shaper input signals for the counter of Fig. 5-1.

Table 5-1. Input Data for the PSR50.

	high level (operating)	low level (operating)	limiting values
V_B	4.0 V min.	+ 1.36 V max.	+ 7.0 V max. -2.0 V min.
I_B	0.06 mA max.		16 mA max.

- The carry pulse from one decade to the next is taken directly from pin 22, i.e. output Q_0 .
- Resetting is carried out by feeding a positive signal to input 7 of the PSR50 module. Output terminal Q_R will reset up to 6 decades. Due to the special nature of the reset pulse required for the NIC50 modules, a PSR module must always be used for resetting.
- Pure counting systems will work satisfactorily up to 50 kHz, the number of cascaded decades being of no consequence.

Table 5-2 is a Truth Table for the NIC50 outputs. Only the output corresponding to the count is at "0" level; all other nine outputs remain at "1" level.

Table 5-2. Truth Table for the NIC50.

Count	Outputs									
	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_0
1	0	1	1	1	1	1	1	1	1	1
2	1	0	1	1	1	1	1	1	1	1
3	1	1	0	1	1	1	1	1	1	1
4	1	1	1	0	1	1	1	1	1	1
5	1	1	1	1	0	1	1	1	1	1
6	1	1	1	1	1	0	1	1	1	1
7	1	1	1	1	1	1	0	1	1	1
8	1	1	1	1	1	1	1	0	1	1
9	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	0

5.1 Counting with Pre-determined Outputs

5.1.1 FIXED PRE-DETERMINED OUTPUTS

A Single Fixed Output

Fig. 5-3 shows the circuit for obtaining an output pulse at a single fixed count from a three-decade system. At this count (in this case 730) the three inputs to the Buffer NOR are all "0" and its output will change from "0" to "1". This signal change can be made to activate further circuitry. Unused Buffer NOR inputs may be left floating.

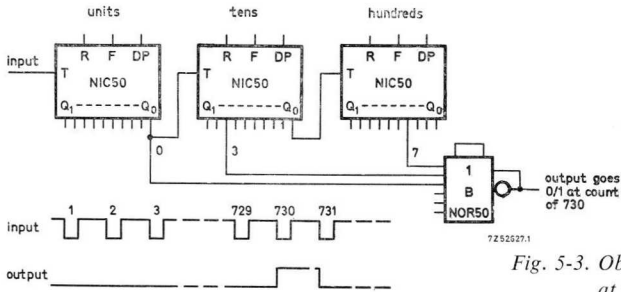


Fig. 5-3. Obtaining a pulse at a single fixed count.

Multiple Outputs

Further fixed outputs may be added as shown in Fig. 5-4. Note that each counter output can drive up to six Buffer NOR inputs.

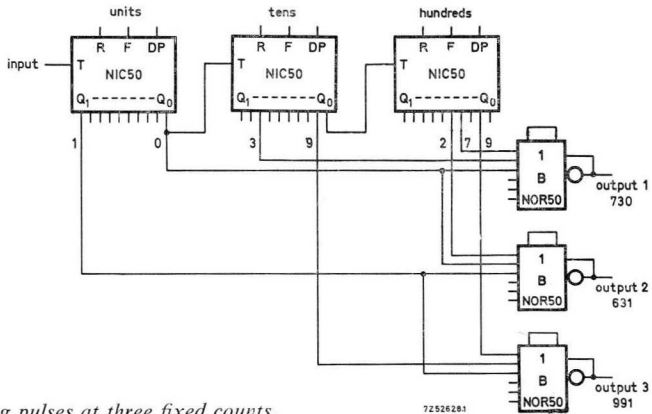


Fig. 5-4. Obtaining pulses at three fixed counts.

5.1.2 VARIABLE PRESET OUTPUTS

A Single Preset Output

Fig. 5-5 shows how the SU50 unit is used to select the particular counter output required to be fed into the Buffer NOR.

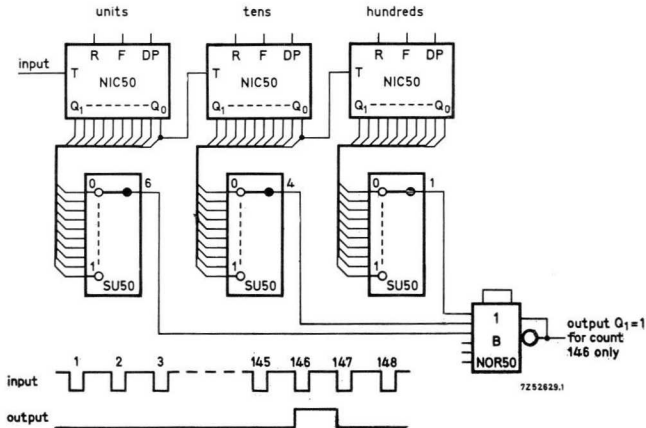


Fig. 5-5. Single preset output with SU50.

Multiple Preset Outputs

Further outputs may be added as shown in Fig. 5-6. Note that a maximum of six preset outputs can be obtained from each counter. The timing diagram is given in Fig. 5-7.

5.2 Using the Pre-determined Outputs

Having obtained an output from the Buffer NOR at the desired count, further circuitry must be added to perform the output functions required.

5.2.1 DIRECT OUTPUT DRIVE

Fig. 5-8 shows how the Buffer NOR output drives the LRD50 module which is then used to drive a lamp or relay. The LRD50 module switches

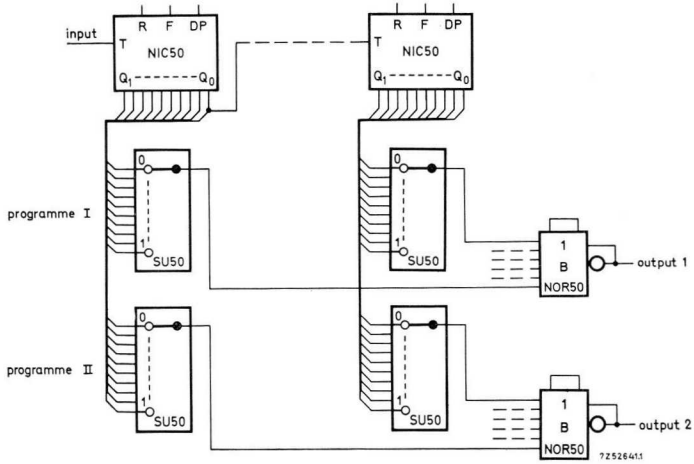


Fig. 5-6. Obtaining two preset counts.

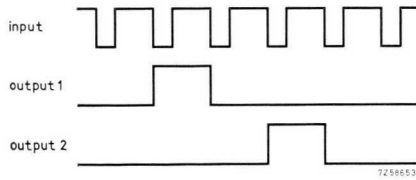


Fig. 5-7. Timing diagram of the circuit in Fig. 5-6.

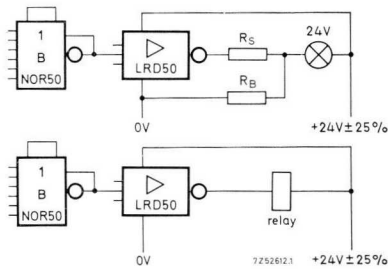


Fig. 5-8. Direct drive of lamp or relay with LRD50.

the load on when its input is “1”, and hence the load is energized for the duration of the chosen count. Note the following points when using the LRD50:

- When driving a lamp load, series- and bleed resistors (whose value can be obtained from Table 5-3) must be provided to protect the output transistor against current surge; R_B should have a rating of 3 W and R_s a rating of 1 W. Lamp supply should be 24 V. I_L in the Table is normal lamp current.

Table 5-3. Values of R_s and R_B for various lamp currents.

I_L (mA)	R_s (Ω)	R_B (Ω)
50	> 0	< ∞
75	>47	< ∞
100	>33	< ∞
150	>22	< ∞
200	>15	≤ 330
250	>12	≤ 270
300	>10	≤ 220

- V_{p2} must be connected to the LOAD supply. This may be the same +24 V logic supply to the counters, or it can be a separate + 24 V $\pm 25\%$ supply of suitable current rating. The latter is recommended, as switching transients are then separated from the logic supplies. The necessary connections for this supply are discussed in section 17.2.3. In either case pin 2, i.e. 0 V should be returned separately to the system central earth point and not commoned with other 0 V connections. It must be realized that the LRD50 supply connections differ from the normal arrangement:
 Pin 1: NOT PROVIDED
 Pin 2: 0 volt
 Pin 3: +24 volt.
- A “1” on any one or more inputs of the LRD50 energizes the load.

5.2.2 OUTPUT DRIVE VIA INTERMEDIATE LOGIC

In many cases the output action required takes longer than the duration of a count period. It is then necessary to use a memory circuit to remember that the count has been reached.

Fig. 5-9 shows a memory circuit which is set by the Buffer NOR output going “0/1” when the count is reached. The LRD50 module is switched on by the memory output, energizing the load.

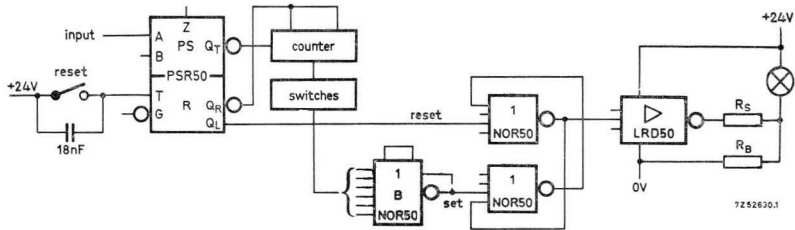


Fig. 5-9. Lamp drive with retention of output (manual reset).

5.2.3 RESETTING

Resetting of the memory may be effected from various sources. A "0/1" signal is required into NOR X, either manually generated via PSR50 module as shown above, or typically from a second pre-determined count as in Fig. 5-10.

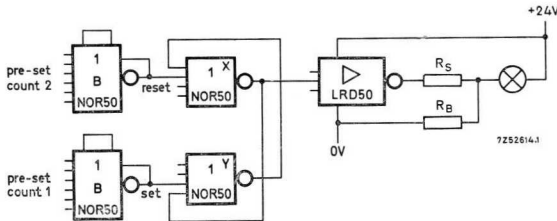


Fig. 5-10. Lamp drive with retention of output (automatic reset).

5.2.4 A TYPICAL EXAMPLE

A typical 3-decade, 3-programme scheme is shown in Fig. 5-11. Operation is as follows. At the 104th count all inputs to Buffer NOR W in programme "1" become "0" and memory 1 is set causing lamp 1 to glow. Note that this memory can be set because memory 2 is still in its reset position supplying a "0" signal to the upper NOR of memory 1. On the count of 256, Buffer NOR X output in programme 2 becomes a "1", thus setting memory 2 and causing lamp 2 to glow. However, memory 2 output (LRD50 input) is now also used to reset memory 1, thus extinguishing lamp 1. Similarly lamp 3 lights and lamp 2 is extinguished at the count of 820. At the 1000th pulse, i.e. Q_0 outputs of the three NIC50 modules at "0", Buffer NOR Z output becomes "1" causing memory 3 to reset and lamp 3 to extinguish.

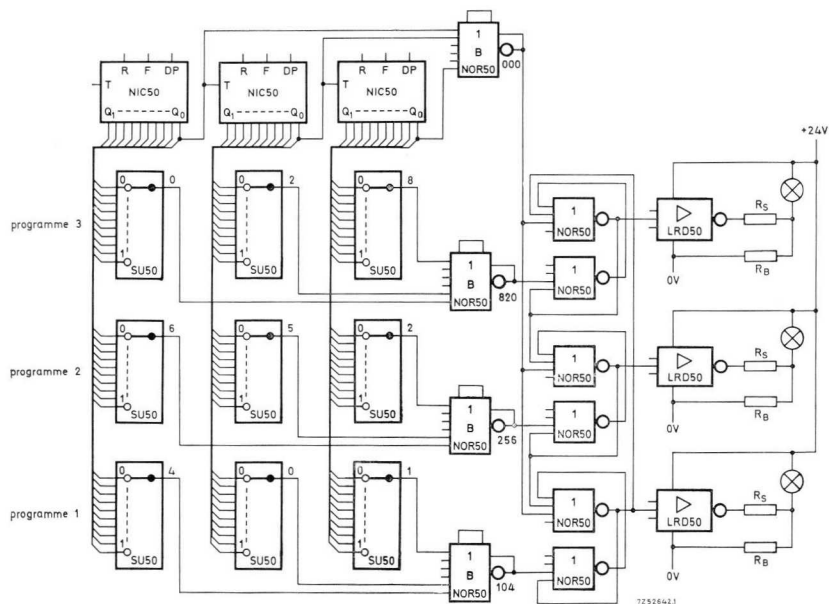


Fig. 5-11. Three-decade, three-programme scheme. Each lamp is extinguished when following lamp lights.

5.3 Sequential Programme Selection

Many applications require sequential opening of decade gates to allow output programmes to operate in a definite order. The NIC50 or SU50 may be used for this function as shown in the following sections.

5.3.1 SELECTION WITH NIC50

Fig. 5-12 gives a scheme for sequential programme selection using the NIC50.

5.3.2 SELECTION WITH SU50

The circuit of Fig. 5-13 gives a scheme in which the SU50 switch may be used to select a particular programme whilst inhibiting all others.

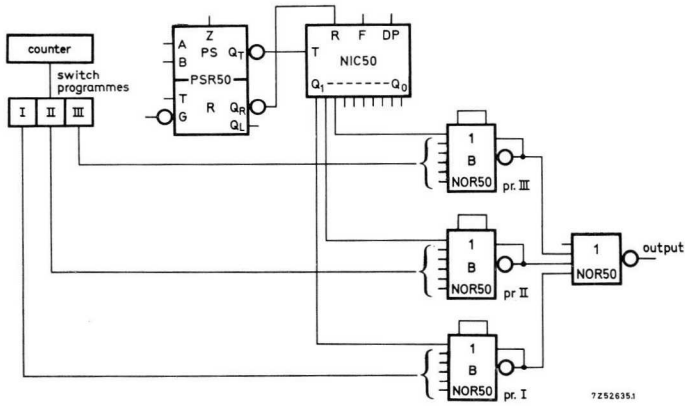


Fig. 5-12. Sequential programme selection using the NIC50.

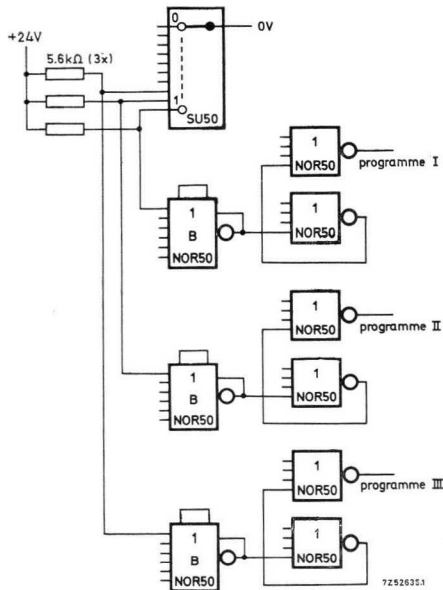


Fig. 5-13. Programme selection using the SU50.

5.4 Variable Scaling

It is sometimes necessary to count to a scale other than 10, e.g. 24 for time indication (number of hours per day). The circuit of Fig. 5-14 shows how this may be achieved.

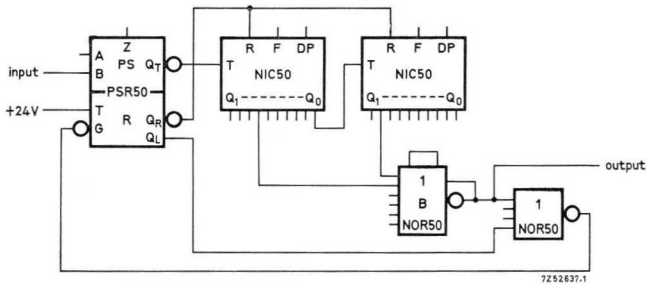


Fig. 5-14. Counting to a scale other than 10.

5.5 Decimal Point Indication

The NIC50 module is provided with decimal point indication which appears on the left of the numerals. It is illuminated by connecting *DP* (pin 17) to 0 V via a switch contact and series resistor of 1 k Ω (see Fig. 5-15a) or as shown in Fig. 5-15b. Variable selection of the decimal point can be achieved by using the SU50 for example, or by using the logic as described in section 13.10.

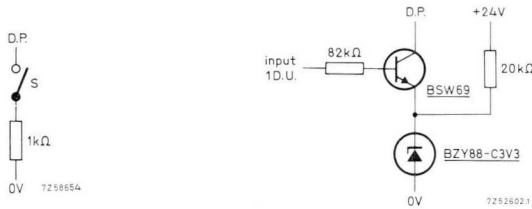


Fig. 5-15. Two methods of illuminating the Decimal Point indication. Fig. 5-15a uses a switch contact, and Fig. 5-15b a logic module drive.

The counting direction is determined by the position of the control switch. Note the following points:

- The control input which is open circuit is inhibited, i.e. an open-circuit condition inhibits in a similar manner to a "1" signal.
- During the operating time of the switch both control inputs are open circuit and thus both trigger inputs are inhibited. It is therefore important that count pulses are not fed to the PSR50 during this period.
- A control input recovery time of 100 μ s must be allowed after each switching action.

6.1.2 CONTROL WITH SEPARATE INPUTS AND A SWITCH

Fig. 6-2 shows a counting system with separate forward and reverse inputs, control of counting direction again being effected by a switch. Points (a), (b) and (c) above apply to this circuit also.

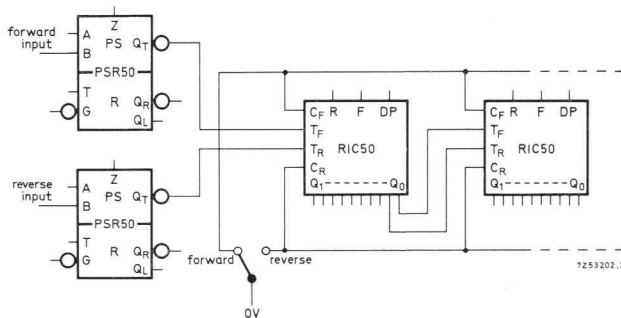


Fig. 6-2. Bi-directional counting — separate inputs, switched control.

6.1.3 CONTROL BY LOGIC

The circuits of Figs. 6-3 and 6-4 show how the control inputs may be driven either by LRD50 modules or NOR units with three inputs in parallel. The LRD50 is capable of driving a maximum of six C_F or C_R terminals, whilst the NOR output is limited to a maximum of two. The circuit of Fig. 6-5 may also be used.

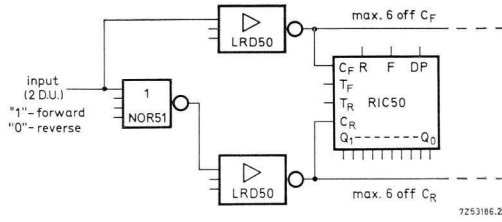


Fig. 6-3. Bi-directional counting with logic input control, using LRD50 modules.

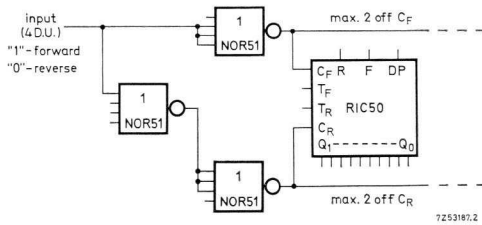


Fig. 6-4. Bi-directional counting with logic input control, using NOR units.

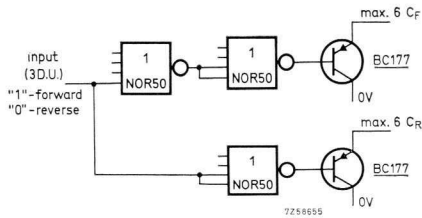


Fig. 6-5. Bi-directional counting with logic input control, using NOR units and transistor drivers.

Up to four decades may be controlled by NOR units with the circuit of Fig. 6-6. The control circuits so far considered require a steady "0" or "1" level at the input in order to hold a particular counting direction. Figs. 6-7 and 6-8 show how the control lines may be driven from memory circuits which will hold a particular direction until set or re-set by a suitable positive-going pulse.

6.2 Counting with Pre-determined Outputs

The output of the RIC50 module is in 10-wire decimal form, and is identical in every respect to the NIC50 module. Its truth table is given in table 6-1, which shows that all outputs are "1" with the exception of the one at which the count is standing.

Pre-determined outputs may be obtained from RIC50 modules in an identical manner to that described in section 5.1 for the NIC50.

Resetting procedures for the RIC50 module are identical to those for the NIC50 as described in section 5.2.3.

Decimal print drive is covered in section 5.5.4.

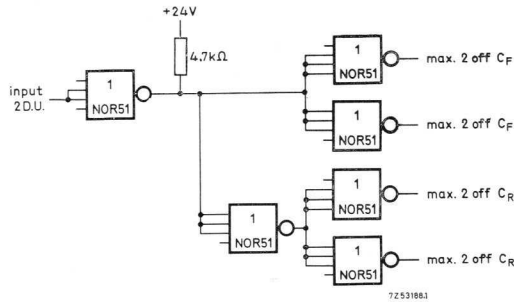


Fig. 6-6. Control of four decades. The input, requiring 9 DU, must be driven by a NOR51 with two paralleled inputs.

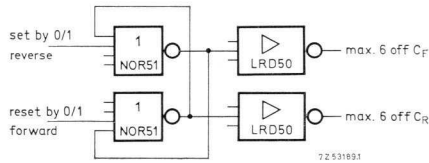


Fig. 6-7. Use of a memory circuit to hold a control line level. Driving capability is 6 decades.

Table 6-1. Truth Table for the RIC50.

count	outputs									
	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	Q ₈	Q ₉	Q ₀
1	0	1	1	1	1	1	1	1	1	1
2	1	0	1	1	1	1	1	1	1	1
3	1	1	0	1	1	1	1	1	1	1
4	1	1	1	0	1	1	1	1	1	1
5	1	1	1	1	0	1	1	1	1	1
6	1	1	1	1	1	0	1	1	1	1
7	1	1	1	1	1	1	0	1	1	1
8	1	1	1	1	1	1	1	0	1	1
9	1	1	1	1	1	1	1	1	0*	1↓
0	1	1	1	1	1	1	1	1	1↑	0**

Trigger signals are: ** forward; * reverse.

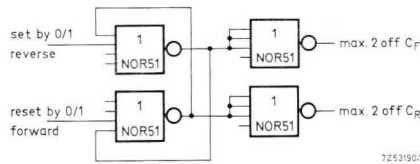


Fig. 6-8. Similar circuit to Fig. 6-7, but with a driving capability of 2 decades.

6.3 Special Requirements of Input Signal Relationships

It is often required that the control inputs C_F and C_R of the RIC 50 be activated by signals of pulse form. In those cases the timing relationships between the control and trigger signals drawn in Fig. 6-9 must be followed for proper operation of the RIC50.

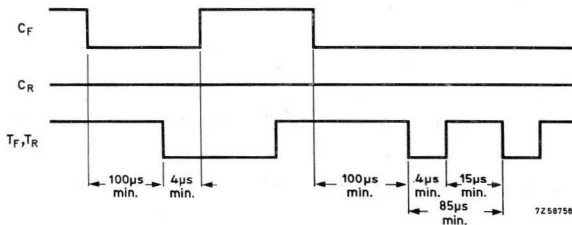


Fig. 6-9. Timing relationships.

7 Sign Indication with the SID50

The SID50 module primarily displays plus and minus signs, provision also being made for a dark condition. This latter condition is obtained whenever + and - inputs are at the same logic level. With complementary signals applied, the sign which has a "1" level at its input will be illuminated.

7.1 Driving the + and - Signs

7.1.1 SWITCHED INPUTS DRIVE

Fig. 7-1 shows how a three-position switch selects the desired state.

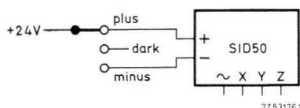


Fig. 7-1. Switch control.

7.1.2 LOGIC DRIVE

Fig. 7-2 shows a single-input control circuit giving, plus for a "1" input and minus for "0" input. Dark position is not available with this circuit. Input requirement is 2 D.U.

Fig. 7-3 shows a memory drive circuit which gives plus indication with the memory set, and minus when reset. If set and reset signals are applied at the same time a dark position can be achieved. Care must be taken that these signals are not removed simultaneously as the memory state would then become indeterminate.

Alternative two-signal input control circuits are shown in Figs. 7-4 and 7-5. All three tube conditions are given in accordance with the truth tables shown.

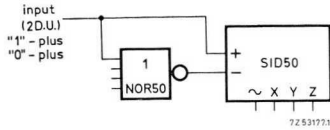


Fig. 7-2. Single-input control.

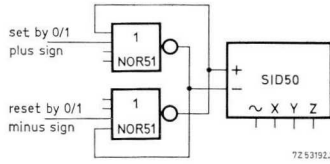


Fig. 7-3. Two-input control with memory.

(Truth Table) Tube conditions.

A	B	sign
1	1	plus
0	1	dark
0	0	minus
1	0	plus

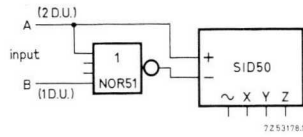


Fig. 7-4. Two-input control.

(Truth Table) Tube conditions.

A	B	sign
0	0	plus
1	0	minus
0	1	dark
1	1	dark

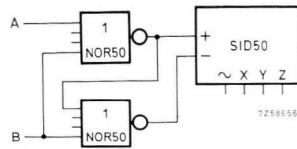


Fig. 7-5. An alternative two-input control.

7.2 Sign Indication and Counting Direction Control

The circuit of Fig. 7-6, besides driving the appropriate sign on the SID50 module, produces the control signals C_F and C_R for the RIC50 module. Consider the series of numbers:

$$+003, +002, +001, +000, -001, -002, -003, \dots$$

It is obvious that despite the fact that one digit is subtracted every time, the RIC50 must operate firstly in the reverse direction to $+000$, then in the forward direction. In Fig. 7-6, it is assumed that a signal A is available to indicate whether subtraction or addition is to take place ($A = "0"$ for subtraction, $A = "1"$ for addition), and that a second signal P is also available to indicate sign ($P = "1"$ for $+$, $P = "0"$ for $-$).

The disadvantage of this arrangement is that the zero indication on the RIC50 is always accompanied by a $+$ or $-$ sign on the SID50, i.e. $+000$ or -000 . To obtain an "un-signed" zero, that is with the SID50 dark when the RIC50 displays 000, the circuit of Fig. 7-7 must be added to produce the input signals A and P .

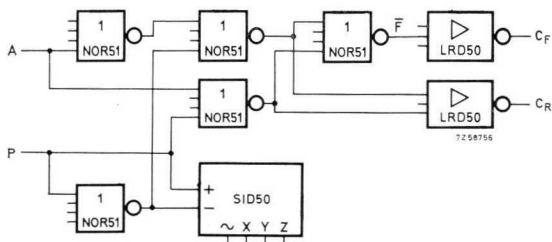


Fig. 7-6. Sign indication and counting direction control.

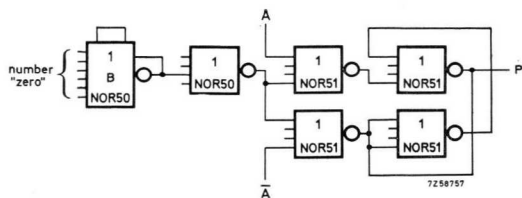


Fig. 7-7. Obtaining an "un-signed" zero in conjunction with the circuit of Fig. 7-6.

7.3 A Typical Example

As an example, a complete scheme for bi-directional counting with the RIC50, incorporating both the previous circuits (Figs 7-6 and 7-7) is given in Fig. 7-8.

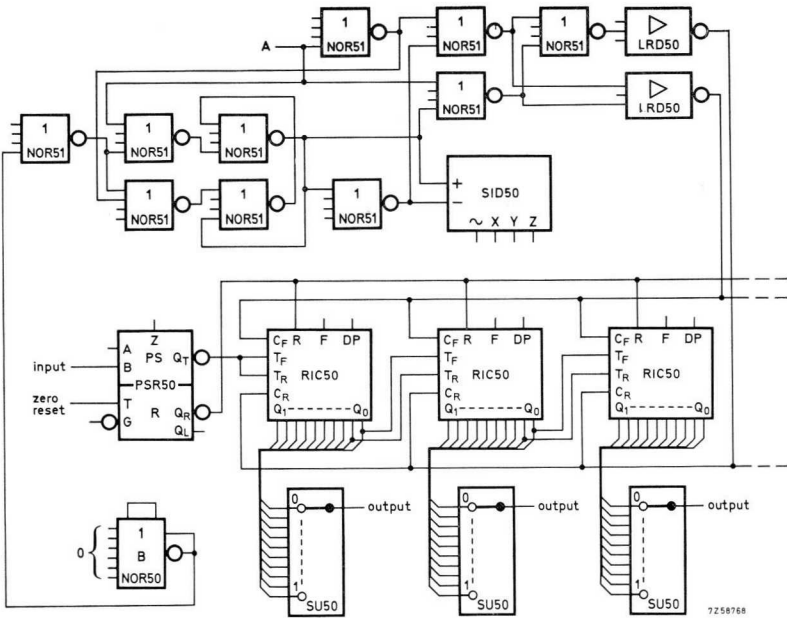


Fig. 7-8. Complete scheme for bi-directional counting with the RIC50.

7.4 Driving the X, Y, Z and ~ Signs in the SID50

The characters X, Y, Z and ~ are also accessible and can be driven with the external circuitry shown in Fig. 7-9.

These characters are illuminated by connecting the corresponding terminal to 0 V, via a switch contact and series resistor of 1 k Ω (see Fig. 7-10). The resistor and switch should be connected as close to each other as possible.

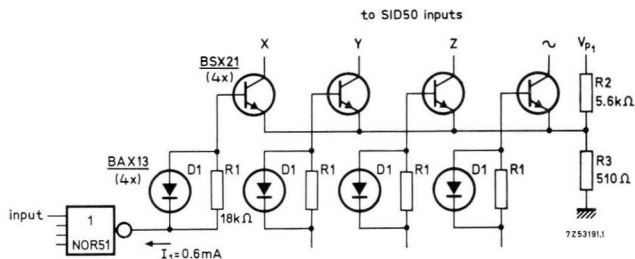


Fig. 7-9. Drive circuitry for the SID50. One input of the NOR51 must always be left floating.

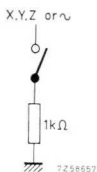


Fig. 7-10. X, Y, Z and ~ sign illumination.

8 Resetting the System with the PSR50

8.1 General

Sophisticated systems can require automatic resetting at a certain count or inhibit of the reset signal during some part of the cycle. The manner in which these functions can be achieved will be more easily understood by considering the resetting action of the PSR50 module in detail.

There are two inputs, T and G , and two outputs Q_R and Q_L . Output Q_R resets the NIC50 modules, output Q_L the logic memories.

The T input is the normal reset input, whilst G is intended to be used as a gate or inhibit input. The waveforms in Fig. 8-1 illustrate their operation.

It will be seen in part A that reset pulses are produced by a "0/1" change on T whilst G is at "0" or floating. Whilst G is at "1" input pulses on T have no effect, i.e. T is being inhibited.

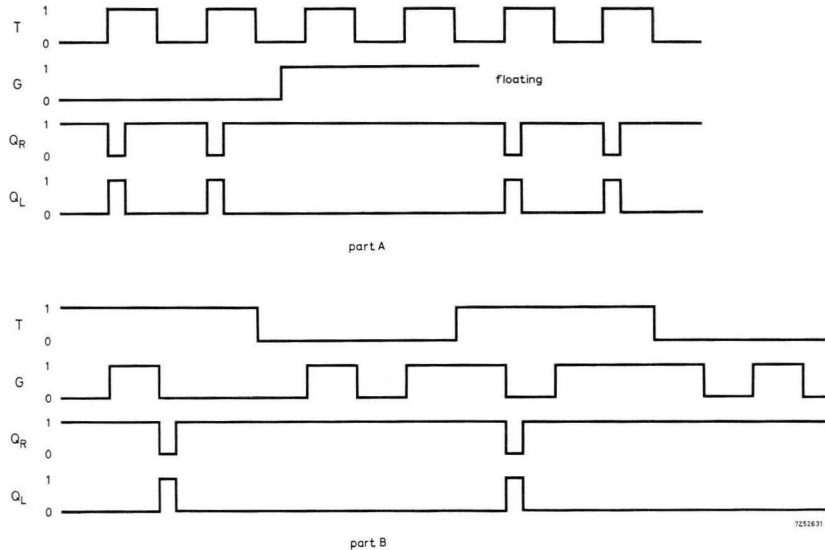


Fig. 8-1. PSR50 input/output relationships.

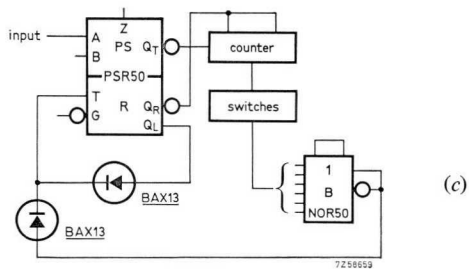
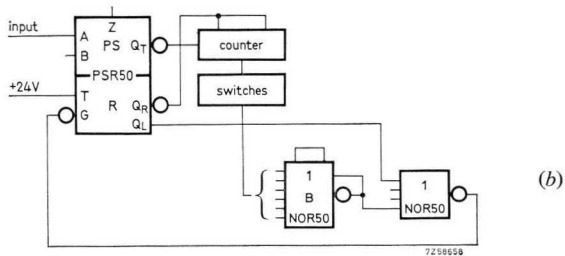
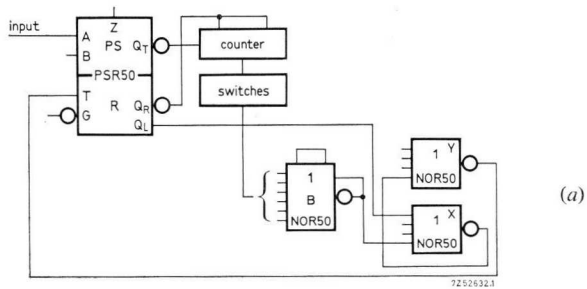


Fig. 8-3a, b, c. Three methods of resetting with PSR50 module.

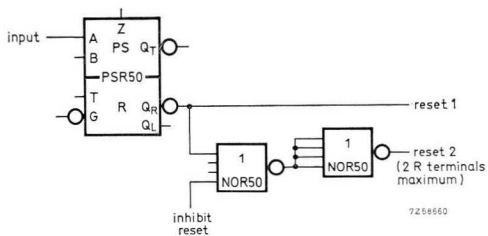


Fig. 8-4. Resetting at different periods.

8.3 Resetting from the Mains

8.3.1 RESETTING AT MAINS SWITCH-ON

When the mains supply is connected, a switch-on reset must be provided to reset both counters and memories; otherwise, random conditions could occur. The circuits of Figs 8-5 and 8-6 show a way to obtain this resetting action.

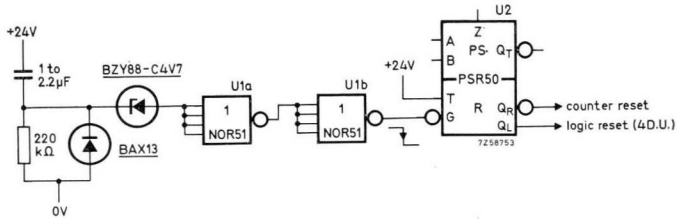


Fig. 8-5. Automatic counter reset at switching on.

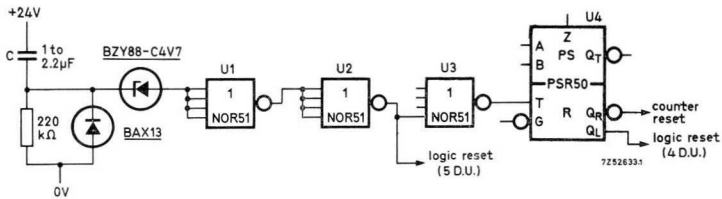


Fig. 8-6. Automatic counter and logic reset at switching on.

In Fig. 8-6, initially capacitor C is discharged and NOR U_1 output is "1", NOR U_2 output is "0" and NOR U_3 output is "1". When the supply is connected, a "1" pulse is fed by the capacitor to NOR U_1 producing a "0" to "1" change from NOR U_2 which resets logic memories. When the capacitor is fully charged NOR U_2 output reverts to "0" and NOR U_3 output changes from "0" to "1" thus producing a counter reset pulse from the PSR50 module U_4 .

A circuit for resetting at mains switch-on of 20 NOR functions is shown in Fig. 8-7.

8.3.2 MAINS SWITCH-ON RESETTING AND MANUAL CONTROL

The circuit of Fig. 8-8 shows a mains switch-on reset circuit which can also be manually operated.

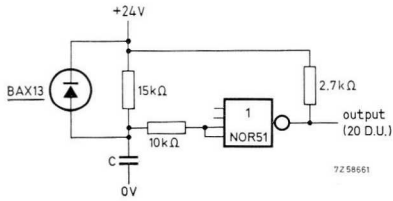


Fig. 8-7a, b, c. Resetting at mains switch-on of 20 NOR functions.

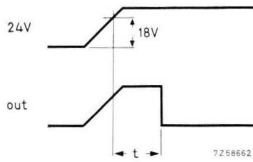


Fig. 8-7b. Showing the timing relationship between mains voltage and resetting pulse.

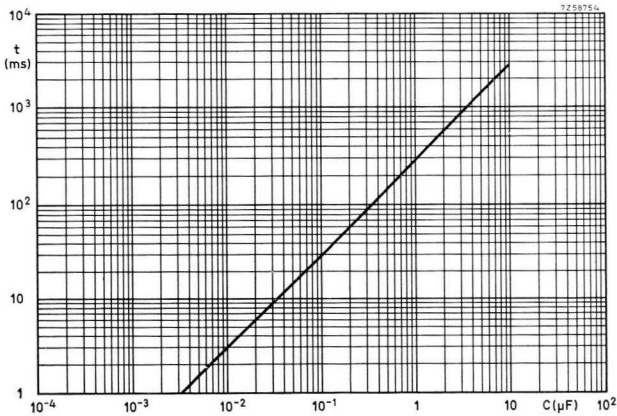


Fig. 8-7c. Showing the relationship between pulse duration "t" and C.

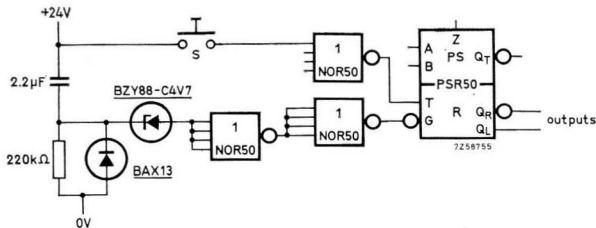


Fig. 8-8. Automatic or manual reset at switching on.

9 Information Storage with the MID50

The MID50 module is a buffer memory which may be used to store information fed from either a NIC50 or RIC50 module or another MID50. For this purpose it has ten inputs I_0 — I_9 which are directly connected to the corresponding outputs Q_0 — Q_9 of the driving module. This connection does not alter the output capability of the driving module. (A maximum of six MID50 modules may be driven from each decade counter, but the maximum wiring capacitance of 200 pF must not be exceeded.)

9.1 Transfer of Informations

Upon applying a suitable transfer pulse to input T_C from either output Q_T or Q_R of a PSR50 module the information in the driving module is transferred to the MID50, where it remains steadily displayed. Fig. 9-1 illustrates the necessary interconnections.

The information is transferred by the positive-going edge of the transfer signal to terminal T_C (see Fig. 9-2). It is therefore important that the times t_1 and t_2 between successive trigger pulses to the counter and the transfer pulse are strictly adhered to in order to avoid malfunctioning of the MID50.

It should be noted that the information stored in the MID50 is removed when a zero level is applied to input terminal T_C .

At the moment of application of the transfer pulse, the MID50 inputs must be at "1" (HIGH) level, except the one at "0" level corresponding to the illuminated digit. As the MID50 uses decimal input, a decoding circuit must be used between the counter and the MID50 if the counter operates on a binary code. A decoder circuit for the 1248 BCD to decimal is given in section 13.5.

9.2 Printer Drive with the MID50

The decimal outputs of the MID50 module may be used for printer drive as well as normal logic purposes. Further information on this application will be found in Chapter 10.

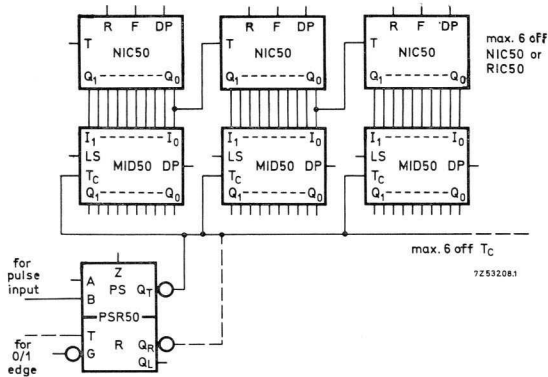


Fig. 9-1. Transferring information to the MID50.

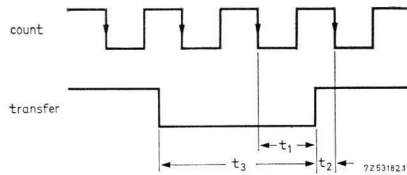


Fig. 9-2. Count and transfer signals $t_1 = 12 + 7(n-1) \mu s$ where n is the number of decades; $t_2 = 8 \mu s$ minimum; $t_3 = 15 \mu s$ minimum.

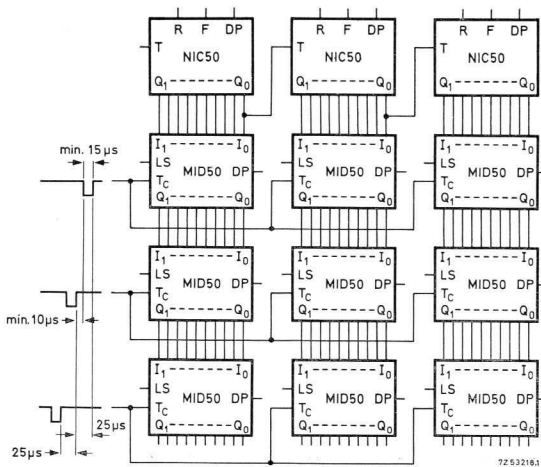


Fig. 9-3. Shift register with MID50.

9.5 Adaptation of the MID50 to Other Systems

The MID50 module can easily be adapted to other logic systems using different logic levels. If such non-standard logic levels, derived from other than the RIC50 or NIC50 modules are fed to the inputs I_0 — I_9 of the MID50, the adaptation can easily be made by connecting a suitable resistor R between LS and V_P and a voltage regulating diode D between LS and 0 V. The MID50 power supply must of course remain at +24 V (V_P). Fig. 9-5 shows the arrangement, and table 9-1 gives suitable R values and D types for systems with logic supplies of 12 V or 6 V.

Table 9-1.

logic level	logic supply	D	R
minimum logic "1" ≥ 5.4 V maximum logic "0" ≤ 1.4 V	12 V	BZY88—C5V1	1.2 k Ω 0.25 W
minimum logic "1" ≥ 3.6 V maximum logic "0" ≤ 0.5 V	6 V	BZY88—C3V3	1.5 k Ω 0.25 W

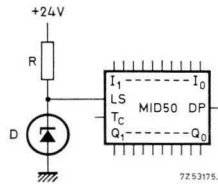


Fig. 9-5. Connection of LS to obtain level shift.

10 Printer Drive with the PDU50A and PDU50B

10.1 General Considerations

The numerical information contained by an electronic counter is often required to be printed out on demand, thus giving a permanent record of the magnitude of the measured quantity at that instant.

A printer drive system for any decimal printer can be simply constructed using the PDU50A and PDU50B modules. These modules are suitable for use with either uni-directional counters (NIC50) or bi-directional counters (RIC50), normally in conjunction with the appropriate buffer memories (MID50). A typical printer drive system employing three decades is described.

Each decade must be accompanied by a PDU50A module (Fig. 10-1). If from four to six decades are employed, two PDU50B modules are required (Fig. 10-2).

The printing mechanism operates by the action of one of ten relay-activated arms, each carrying a digit (0-9). This action is followed by movement of the paper carriage.

In order to print out a number contained by the counter, signals corresponding to the digits of that number must be present at the input terminals of the printer drive modules. The signals are usually transmitted via buffer memories since the actual printing operation can take up to 100 ms per digit, during which time the number held by the counter could change its value. If, however, the counting frequency is sufficiently low or if the counting can be inhibited during the printing operation, the number held by the counter can be fed directly to the input terminals of the printer drive modules (PDU50A).

The printer drive modules and a scanner ensure that the digits are printed in their correct sequence.

10.2 A typical 3-decade Printer Drive Circuit

The circuit of Fig. 10-3 shows a typical system.

The output terminal Q corresponding to the particular digit contained on each decade of the preceding counter (not shown) is LOW, this level being fed to the corresponding input terminal I of the associated MID50 buffer memory.

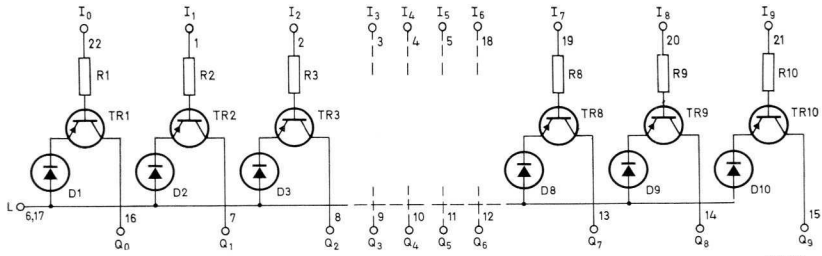


Fig. 10-1. PDU50A module circuit diagram.

7254022.1

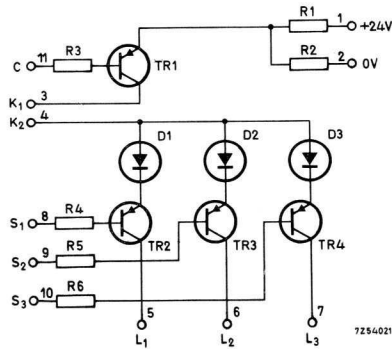


Fig. 10-2. PDU50B module circuit diagram.

7254021.1

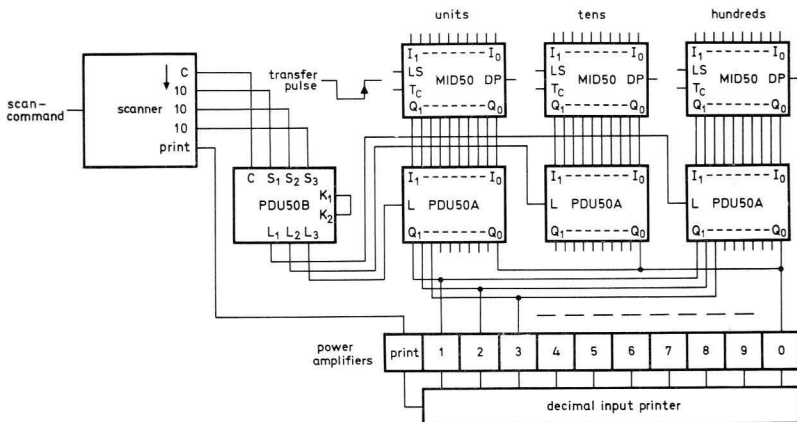


Fig. 10-3. Typical 3-decade printer drive system.

7254024.2

At the positive-going edge of the transfer pulse, the output terminal Q of each MID50 module whose corresponding input terminal I is LOW, becomes LOW, this level being fed to the corresponding input terminal I of the associated PDU50A module.

When both the clock control input C and one of the scan control inputs S_1, S_2, S_3 of the PDU50B module are LOW, a positive shift voltage is applied to the input terminal L of the appropriate PDU50A module. The particular output Q of the latter whose corresponding input level is LOW, then becomes HIGH, switching on the appropriate power amplifier and thus driving the printer.

During the low level of the transfer pulse at pin B (T_C) of each MID50 module, either the clock pulse input C or all three scan inputs S_1, S_2, S_3 of the PDU50B module must be HIGH.

The positive shift voltage to input L of the PDU50A modules is never applied to more than one terminal L of the PDU50A modules at a time, and so the corresponding outputs of all the PDU50A modules can be commoned.

The clock control circuit (TR_1 and associated components in PDU50B) supplies a common clock output pulse C to all drive circuits, so that only one such circuit is required. Thus, in systems containing one PDU50B module, terminals K_1 and K_2 must be connected, but in systems containing two PDU50B modules, terminals K_1 and K_2 of the module to which the clock pulses from the scanner are applied must only be connected to terminal K_2 of the other (see Fig. 10-4).

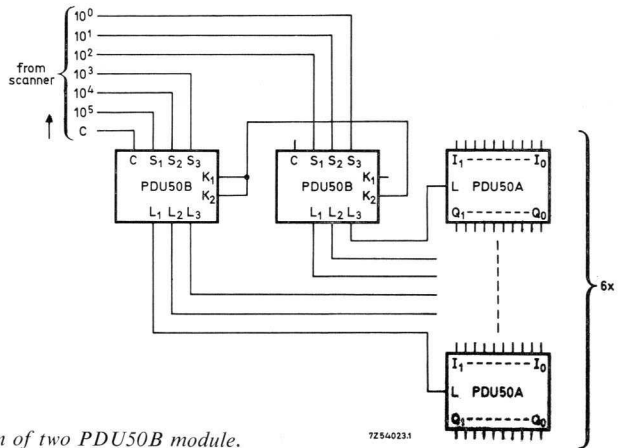


Fig. 10-4. Connection of two PDU50B module.

72540231

The LRD50 power amplifier delivers 300 mA at 30 V as an absolute maximum. Should this be insufficient, the PA60 module (60-series NORbit) can be used giving 1 A at 30 V as an absolute maximum.

10.3 The Scanning Circuit

The function of the scanner circuit is to produce three types of pulses: clock, scan control and print command pulses. The scan control pulses are fed to each PDU50A module in turn, thus setting up the printer unit. The numerical information is then printed out when the print command signal is applied to the printer. Fig. 10-5 shows the scanner circuit, Fig. 10-6 the signal timing diagram.

The signal which activates the scanner, the scan command pulse, resets the memory circuit (two NOR50 units). The NIC50 module is thus reset at the positive-going edge of the scan command pulse, the oscillator being activated at the negative-going edge.

The sequential control pulses from the outputs of the NIC50 module are fed to the PDU50B module together with the clock pulses.

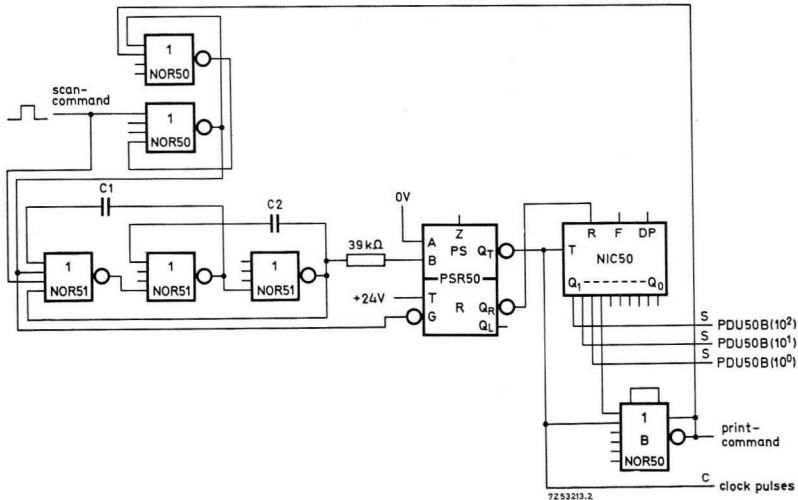


Fig. 10-5. The scanner circuit. Oscillator frequency $f = 5/C_1$, $C_1 = C_2$.

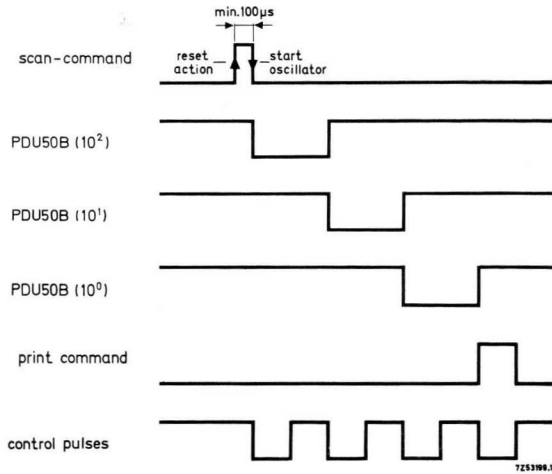


Fig. 10-6. Scanner circuit signal timing diagram.

A "write" command from the PDU50B enables the printer to store the digit corresponding to the output of the printer drive unit concerned.

The Buffer NOR input terminal is connected to the NIC50 output terminal adjacent to that at which the scan control pulse for the least significant digit of the numerical information appears. The output of the Buffer NOR gives the print command, causing the contents of the printer to be printed out.

11 Decade and Divider Circuits with the DCD50

11.1 General Considerations

The DCD50 consists of four flip-flops. By proper interconnection of the terminals, dividers having scaling factors of 2, 3, 4, 5, 6, 8, 9, 10, 12 or 16 can be made.

Each flip-flop is driven by a positive-going pulse. The flip-flops have a common reset input and individual preset inputs, these inputs also being driven by a positive-going pulse. Note that when setting or presetting the DCD50, it is sometimes necessary to apply a HIGH level signal to one of the trigger inputs of the second flip-flop (input *K*) via a diode (see section 11.4).

11.2 DCD50 Terminal Connections for Various Scaling Factors

Table 11-1 lists the input terminal and D.U. required, maximum input pulse repetition frequency, and D.U. available at the output for the ten scaling factors. Sections 11.2.1 to 11.2.10 give the terminal interconnection diagram, truth table, and rear side module wiring diagrams for each of the ten scaling factors. It should be remembered that not all the flip-flops are used for some of the scaling factors.

Table 11-1. Input and Output Data for the DCD50 Module.

divider of	input		max. p.r.f. (kHz)						available output (D.U.)								
	terminal	required (D.U.)	without resistor		with 82 k Ω		with 43 k Ω		Q _A	Q _B	Q _C	Q _D	Q _A	Q _B	Q _C	Q _D	
			1)	2)	3)	1)	2)	3)	1)	2)	3)						
2	21	—			30								6	6			
	9	—			30										6	6	6
	7-8	—			30												
	18	3				22	12.5		30	18							
		2												6	6		
		1	12	6										6	6		
3	8-18	3				22	12.5		30	18				6	6		3
		2												6	6		4
		1		12	6									6	6		5
4	9	—			30						30						6
	21	—						24					6	3	6	6	6
				12									6	4	6	6	6
													6	5	6	6	6
5	8-18	3				22	12.5		30	18				6	6	6	3
		2												6	6	6	4
		1		12	6									6	6	6	5
6	21	—						24			30			6	3	6	3
													6	4	6	6	4
				12									6	5	6	6	5

11.2.1 SCALING FACTOR OF 2

Four dividers of 2 can be made from one DCD50 module.

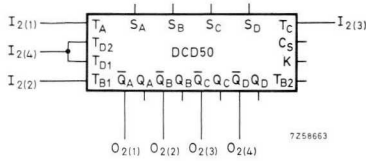


Fig. 11-1. External Connections (sticker symbols).

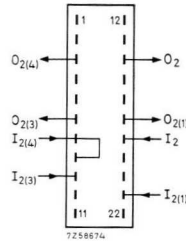


Fig. 11-1. External Connections (module rear view).

Truth Table

input pulse no.	outputs			
	\bar{Q}_A	\bar{Q}_B	\bar{Q}_C	\bar{Q}_D
initial State	1			
1	0			
2 = 0	1			

11.2.2 SCALING FACTOR OF 3

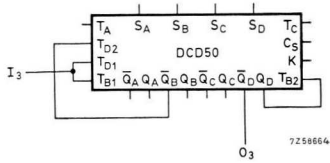


Fig. 11-2. External connections (sticker symbols).

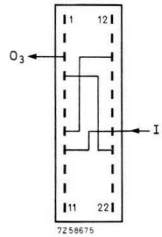


Fig. 11-2. External connections (module rear view).

Truth Table

input pulse no.	outputs	
	\overline{Q}_B	\overline{Q}_D
initial State	1	1
1	0	1
2	1	0
3 = 0	1	1

11.2.3 SCALING FACTOR OF 4

Two dividers of 4 can be made from one DCD50 module.

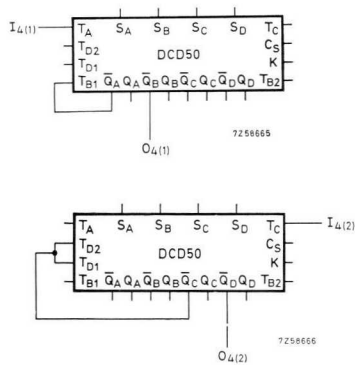


Fig. 11-3. External connections (sticker symbols).

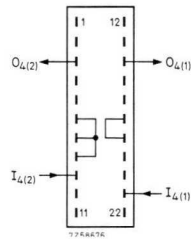


Fig. 11-3. External connections (module rear view).

Truth Table

input pulse no.	outputs	
	\bar{Q}_A	\bar{Q}_C
initial State	1	1
1	0	1
2	1	0
3	0	0
4 = 0	1	1

11.2.4 SCALING FACTOR OF 5

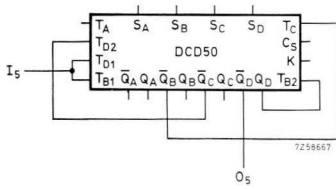


Fig. 11-4. External connections (sticker symbols).

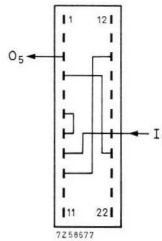


Fig.11-4. External connections (module rear view).

Truth Table

input pulse no.	outputs		
	\overline{Q}_B	\overline{Q}_C	\overline{Q}_D
initial State	1	1	1
1	0	1	1
2	1	0	1
3	0	0	1
4	1	1	0
5 = 0	1	1	1

11.2.5 SCALING FACTOR OF 6

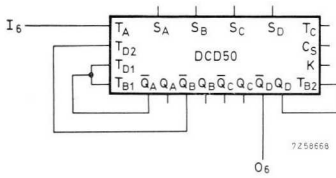


Fig. 11-5. External connections (sticker symbols).

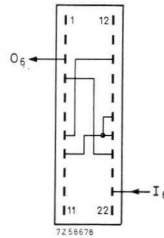


Fig. 11-5. External connections (module rear view)

Truth Table

input pulse no.	outputs		
	\overline{Q}_A	\overline{Q}_B	\overline{Q}_D
initial State	1	1	1
1	0	1	1
2	1	0	1
3	0	0	1
4	1	1	0
5	0	1	0
6 = 0	1	1	1

11.2.6 SCALING FACTOR OF 8

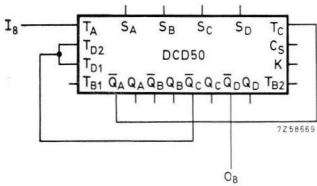


Fig. 11-6. External connections (sticker symbols).

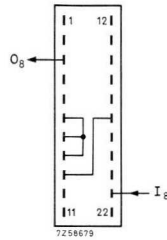


Fig. 11-6. External connections (module rear view).

Truth Table

input pulse no.	outputs		
	\overline{Q}_A	\overline{Q}_C	\overline{Q}_D
initial State	1	1	1
1	0	1	1
2	1	0	1
3	0	0	1
4	1	1	0
5	0	1	0
6	1	0	0
7	0	0	0
8 = 0	1	1	1

11.2.7 SCALING FACTOR OF 9

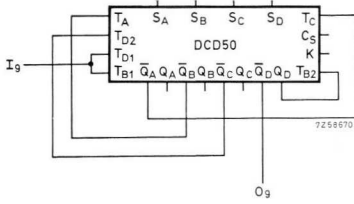


Fig. 11-7. External connections (sticker symbols).

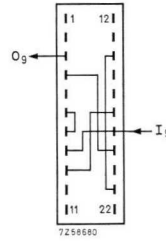


Fig. 11-7. External connections (module rear view).

Truth Table

input pulse no.	outputs			
	$\overline{Q_B}$	$\overline{Q_A}$	$\overline{Q_C}$	$\overline{Q_D}$
initial State	1	1	1	1
1	0	1	1	1
2	1	0	1	1
3	0	0	1	1
4	1	1	0	1
5	0	1	0	1
6	1	0	0	1
7	0	0	0	1
8	1	1	1	0
9 = 0	1	1	1	1

11.2.8 SCALING FACTOR OF 10

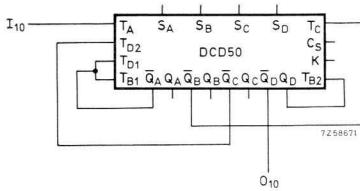


Fig. 11-8. External connections (sticker symbols).

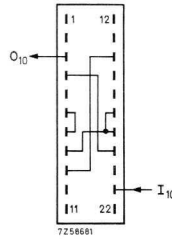


Fig. 11-8. External connections (module rear view).

Truth Table

input pulse no.	outputs			
	\overline{Q}_A	\overline{Q}_B	\overline{Q}_C	\overline{Q}_D
initial State	1	1	1	1
1	0	1	1	1
2	1	0	1	1
3	0	0	1	1
4	1	1	0	1
5	0	1	0	1
6	1	0	0	1
7	0	0	0	1
8	1	1	1	0
9	0	1	1	0
10 = 0	1	1	1	1

11.2.10 SCALING FACTOR OF 16

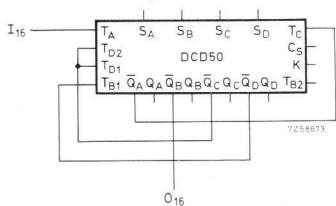


Fig. 11-10. External connections (sticker symbols).

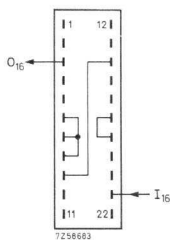


Fig. 11-10. External connections (module rear view).

Truth Table

input pulse no.	outputs			
	$\overline{Q_A}$	$\overline{Q_C}$	$\overline{Q_D}$	$\overline{Q_B}$
initial State	1	1	1	1
1	0	1	1	1
2	1	0	1	1
3	0	0	1	1
4	1	1	0	1
5	0	1	0	1
6	1	0	0	1
7	0	0	0	1
8	1	1	1	0
9	0	1	1	0
10	1	0	1	0
11	0	0	1	0
12	1	1	0	0
13	0	1	0	0
14	1	0	0	0
15	0	0	0	0
16	1	1	1	1

11.3 Trigger Circuit

Normally the PSR50 function must be used to trigger a DCD50 module, as explained below. Triggering is also possible via a NOR function.

11.3.1 TRIGGERING USING A PSR50

Fig. 11-11 shows how the first DCD50 module of a chain is triggered by the pulse-shaper section of the PSR50. The other modules are triggered in their turn by "Carry" signals from the preceding modules (outputs \bar{Q}_D if the modules are connected as decade dividers).

11.3.2 TRIGGERING USING A NOR FUNCTION

Fig. 11-12 shows triggering of a DCD50 module by means of a NOR function. The active part of the NOR input signal is the negative-going edge; this must have a fall time of $\leq 2 \mu\text{s}$. As in Fig. 11-11, it is assumed that the modules are working in a decade mode (carry signal from \bar{Q}_D output).

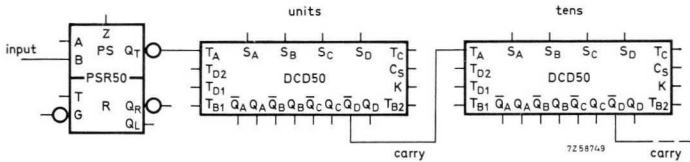


Fig. 11-11. Triggering using a PSR50.

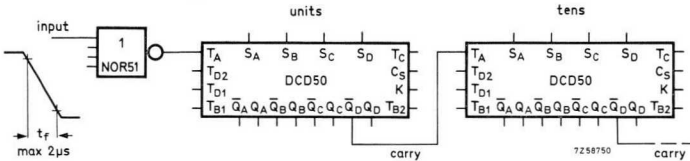


Fig. 11-12. Triggering using a NOR function.

11.4 Reset Circuits

The DCD50 module can be reset (all flip-flop outputs Q at "0" level) (\bar{Q} outputs at "1" level) by applying a pulse of $80 \mu\text{s}$ duration to the C_S terminal. Two resetting circuits are given in the following sub-sections. Note that when a DCD50 is used as a divider of 3, 5 or 9 an inhibit pulse (HIGH or 1 level) must be applied to K (terminal 20) via a diode (type BAX13, cathode to K).

11.4.1 RESETTING OF SIX DCD50 MODULES

The reset pulse duration necessary for n decades is $n \times 80 \mu\text{s}$. Fig. 11-13 gives a method for resetting up to six decades, the reset pulse duration being adjusted according to the number of decades by C . The value of C required for a particular duration can be obtained from the graph of Fig. 11-14.

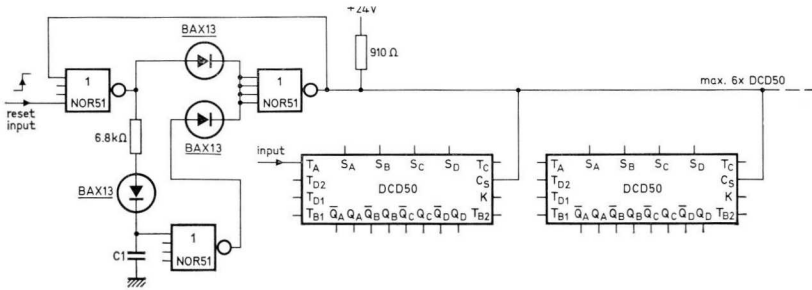


Fig. 11-13. Resetting up to six DCD50 modules.

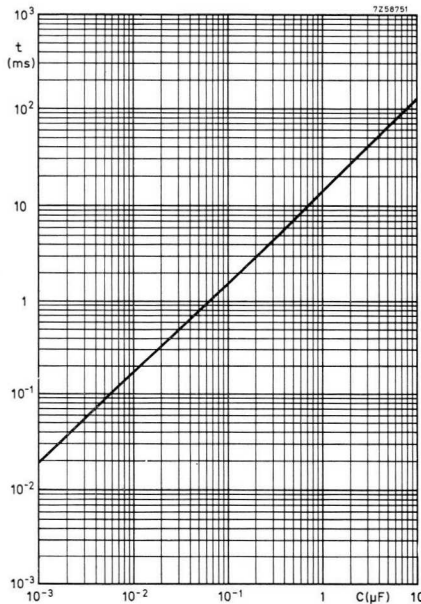


Fig. 11-14. Relation between C and pulse duration in Fig. 11-13.

11.4.2 RESETTING OF EIGHTY DCD50 MODULES

Fig. 11-15 gives a method of resetting up to 80 DCD50 modules, and Fig. 11-16 gives the relation between C in Fig. 11-15 and reset pulse duration. The same general remarks as those of section 11.4.1 apply.

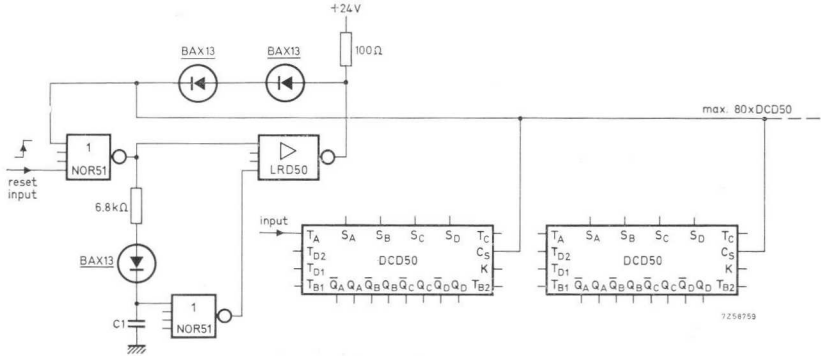


Fig. 11-15. Resetting up to 80 DCD50 modules.

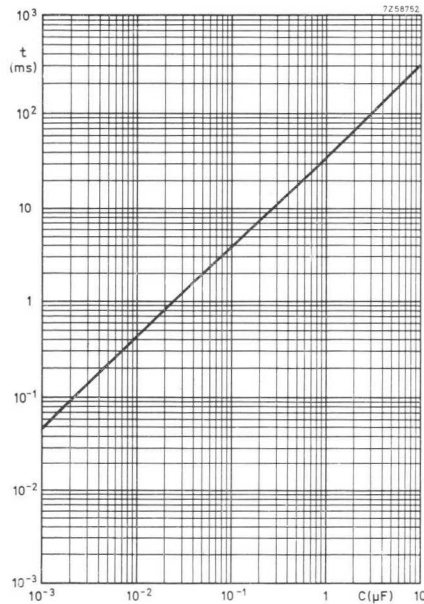


Fig. 11-16. Relation between C and pulse duration in Fig. 11-15.

11.5 Obtaining Preset Output Signals

It is often required that an operation be started or a signal be given at a certain preset number of input pulses. The following sections give methods of obtaining preset output signals from the DCD50 modules. Again, the modules are assumed to be connected in the decade mode. For other scaling factors the principle remains the same.

11.5.1 FIXED PRESET OUTPUT

Fig. 11-17 shows how an output signal can be obtained upon the number of input pulses reaching the fixed preset figure. The number of inputs to NOR U_1 can be extended (up to 24) by using diodes — see section 13.3.1. Table 11-2 shows the DCD50 outputs to which diode inputs to NOR U_1 must be connected for digits 0-9 (DCD50 in decade mode).

The diodes should be mounted as close as possible to the NOR U_1 input(s).

NOR units U_2 and U_3 in Fig. 11-17 form a memory whose output goes HIGH when the desired number (in this case 123) is reached.

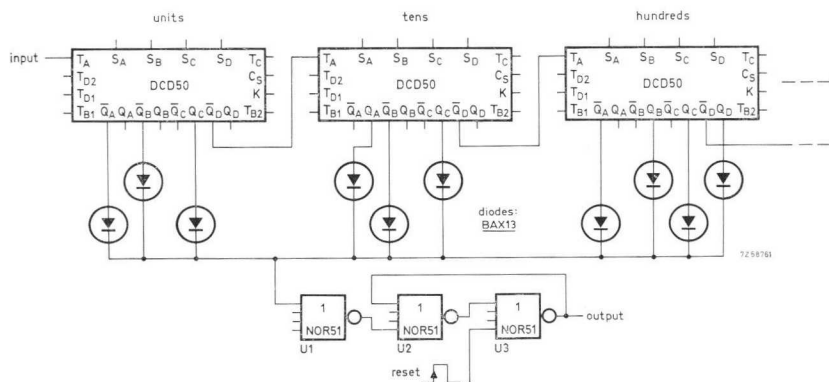


Fig. 11-17. Output at a fixed preset figure.

11.5.2 VARIABLE PRESET OUTPUTS

Fig. 11-18 shows a scheme whereby the preset number can be selected by means of thumbwheel switches, type 1248N. Note that TWS must be connected as shown in the diagram and terminal 12 (internal resistance) left floating. The DCD50 has been connected as a decade counter.

Table 11-12. DCD50 Truth Table and Required Outputs.

decimal digit	truth table (decade mode)				decoding diodes to be connected at:			
	FF-A	FF-B	FF-C	FF-D	FF-A	FF-B	FF-C	FF-D
	\overline{Q}_A	\overline{Q}_B	\overline{Q}_C	\overline{Q}_D	Q_A	Q_B	Q_C	Q_D
0	1	1	1	1	\overline{Q}_A	Q_B	Q_C	Q_D
1	0	1	1	1	\overline{Q}_A	\overline{Q}_B	Q_C	Q_D
2	1	0	1	1	\overline{Q}_A	\overline{Q}_B	Q_C	
3	0	0	1	1	\overline{Q}_A	\overline{Q}_B	Q_C	
4	1	1	0	1	\overline{Q}_A	Q_B	\overline{Q}_C	
5	0	1	0	1	\overline{Q}_A	\overline{Q}_B	\overline{Q}_C	
6	1	0	0	1	\overline{Q}_A	\overline{Q}_B	\overline{Q}_C	
7	0	0	0	1	\overline{Q}_A	\overline{Q}_B	Q_C	
8	1	1	1	0	\overline{Q}_A			\overline{Q}_D
9	0	1	1	0	\overline{Q}_A			Q_D

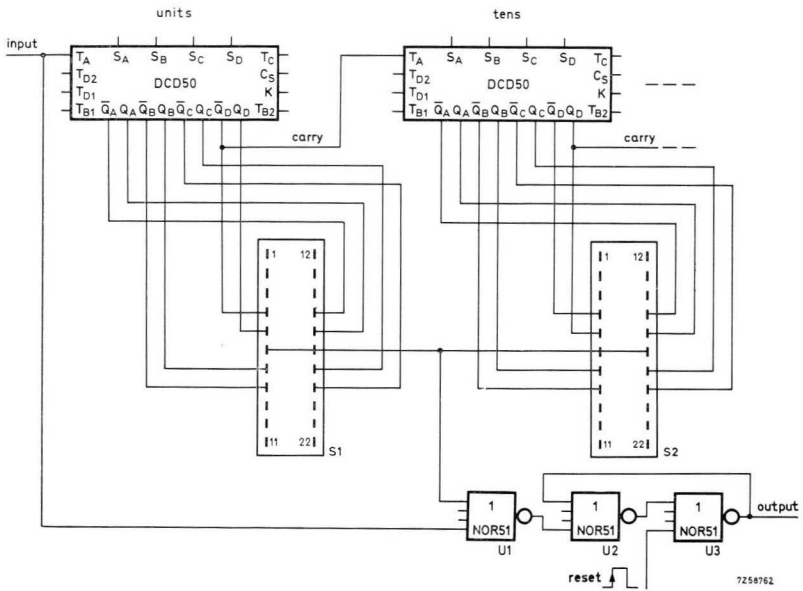


Fig. 11-18. Selection of a preset number.

The circuit of Fig. 11-20 gives the interconnections necessary for presetting DCD50 modules in decade mode.

Note that an Inhibit pulse must be applied to K via a BAX13 diode (cathode to K) if the DCD50 is used as a divider of:

- 3, 5, or 9 when presetting via S_D is required, or;
- 6, 10, or 12 when presetting via S_A and S_D is required.

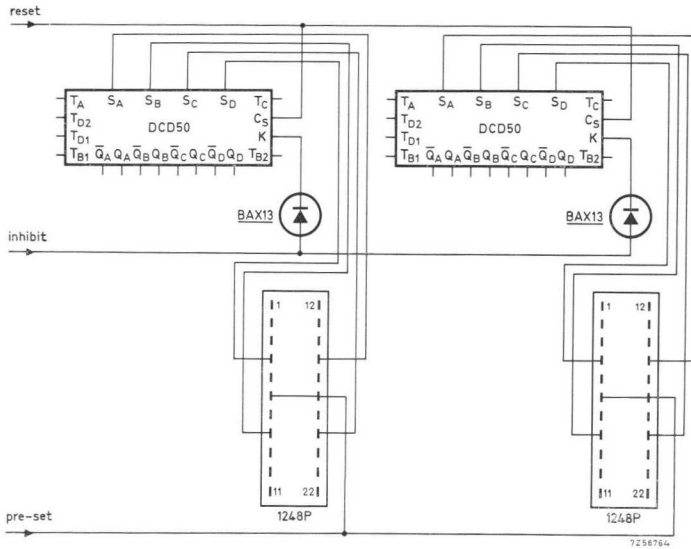


Fig. 11-20. Presetting DCD50 modules in decade mode.

12 Input Drive Circuits

The first two sections of this chapter discuss electro-mechanical and electronic input signal transducers, and sections 3 and 4 give ways of obtaining fixed and variable frequency input signals.

12.1 Electro-mechanical Transducer Interfacing Circuits

12.1.1 RC FILTERS (MAXIMUM SWITCHING RATES 10 Hz AND 100 Hz)

Due to contact bounce problems extreme care must be taken when using this type of input. Switch inputs should never be fed directly to the PSR50 module but via RC filter circuits as shown in Figs. 12-1 and 12-2.

The delay introduced must be sufficient to suppress the contact bounce of the switch used. The frequency of operation of such circuits is limited by the filtering, typical values being given in the diagrams.

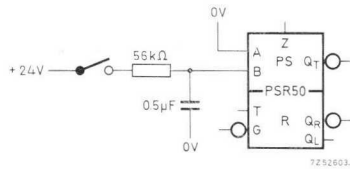


Fig. 12-1. RC input filter circuit (max. switching rate 10 Hz).

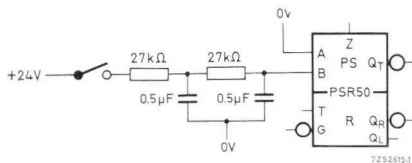


Fig. 12-2. RC input filter circuit (max. switching rate 100 Hz).

12.1.2 RC FILTER WITH A NOR FUNCTION

Better signals are obtained if a NOR function is used with an RC filter, as shown in Fig. 12-3. (PSR50 should always be used in addition, for correct pulses to the counter modules).

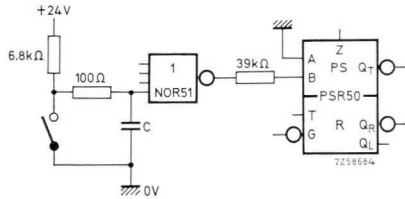


Fig. 12-3. RC input filter with NOR function.

12.1.3 THE SF60 AND PSR50

More reliable switching is obtained when the voltage across the switch contacts is raised. A special filter module in the 60-Series NORbit range, the SF60, is available which will accept high input voltages; the arrangement using the SF60 is shown in Fig. 12-4.

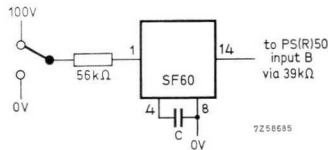


Fig. 12-4. RC input filter with SF60.

12.1.4 CIRCUIT TO NULLIFY CONTACT BOUNCE EFFECTS

Fig. 12-5 gives a circuit using the memory principle to eliminate the effect of contact bounce but requiring a 2-pole contact. Speed is limited by the switch.

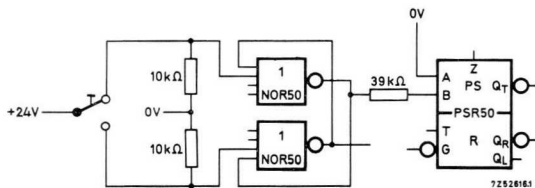


Fig. 12-5. Contact bounce effect elimination using the memory principle.

12.2 Electronic Transducers

This type of transducer is more suitable for use with the 50-Series as the problems of contact bounce and spurious pulses do not occur. Two compatible units are available, as well as light-sensitive, mains and variable frequency inputs.

12.2.1 VANE SWITCHED OSCILLATOR, VSO (Catalogue No.: 2722 031 00001)

This device is operated by passing a metallic vane through the slot at the end of the unit. Its connections are shown in Fig. 12-6. A distance of up to 100 m is allowed between the VSO and the RC filter (see also section 13.9.1).

Note that this unit and the Electronic Proximity Detector (see section 12.2.2) require a $12\text{ V} \pm 5\%$ supply. For single units this may be obtained from the logic supply as shown, or using the circuit of Fig. 12-7 for several units in parallel (up to 30 VSO's).

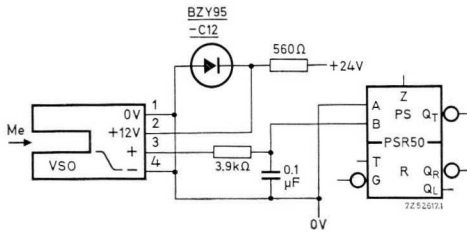


Fig. 12-6. VSO connections.

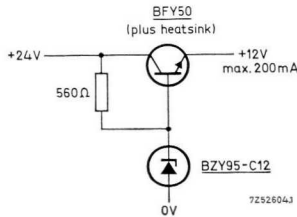


Fig. 12-7. Method of supply for paralleled VSO's or EPD's.

12.2.2 ELECTRONIC PROXIMITY DETECTOR, EPD (Catalogue No.: 2722 031 00021)

This device has a square sensitive end-face and is triggered by the presence of metallic objects. Maximum detection frequency is 1 kHz. Its connections are shown in Fig. 12-8. The 12 V supply shown in Fig. 12-7 can be used to supply up to 24 EPD's.

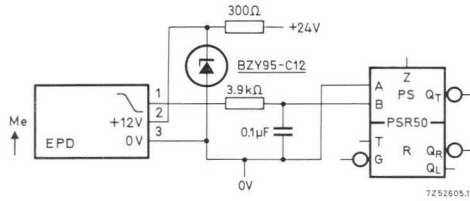


Fig. 12-8. EPD connections.

12.2.3 LIGHT SENSITIVE DETECTORS

The circuit of Fig. 12-9 uses the photodiode BPY68. When the light beam falling on the BPY68 is restored, the output Q_T of the PSR50 changes from "1" to "0", thus providing a trigger pulse for a counter. A capacitor may be inserted at the PSR50 input for filtering purposes. Its value is governed by the required operating speed (10 kHz maximum).

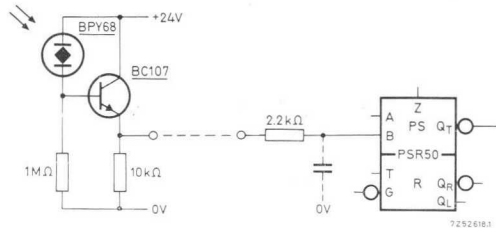


Fig. 12-9. Light sensitive detector using the BPY68.

12.2.4 PHOTO-ELECTRIC DETECTOR, CSPD (Catalogue No.: 2722 031 00041)

A light sensitive detector is available as a complete unit; it has the type designation CSPD. A lamp unit 1MLU (catalogue number 2722 031 00051) is also available. Maximum detection frequency is 6 Hz.

Fig. 12-10 shows how the CSPD can be connected to the PSR50.

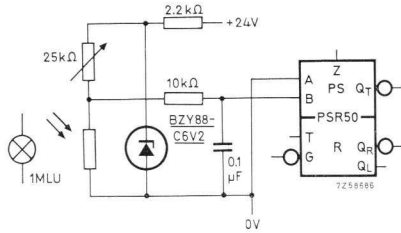


Fig. 12-10. CSPD connections.

12.2.5 LIGHT INTERRUPTION PROBE, LIP1 (Catalogue No.: 2722 031 00081)

Fig. 12-11 shows how the LIP1 can be connected to a PSR50. The maximum detection frequency is at least 10 kHz.

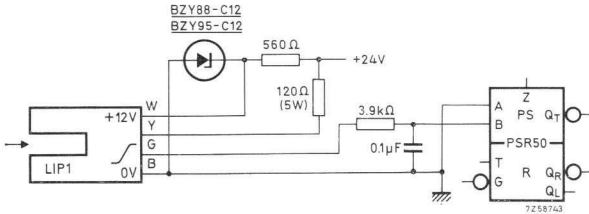


Fig. 12-11. LIP1 connections.

12.2.6 THE IRON VANE SWITCHED REED, IVSR (Catalogue No.: 2722 031 00011)

Fig. 12-12 shows the interconnections between the IVSR and PSR50. The maximum detection frequency is 100 Hz.

The output voltage of the IVSR is high when the vane is present in the gap. The output Q_T of the pulse shaper goes from “1” to “0” level when a metal vane enters the IVSR.

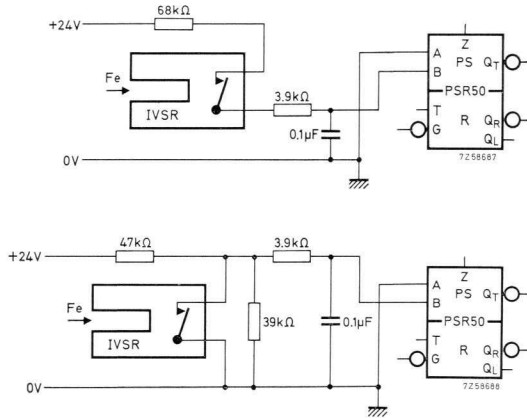


Fig. 12-12. IVSR connections.

12.2.7 GEIGER-MÜLLER RADIATION DETECTOR

The circuit of Fig. 12-13 enables signals from a Geiger-Müller radiation detection tube type 18503 to be fed in a usable form to the pulse-shaper PSR50.

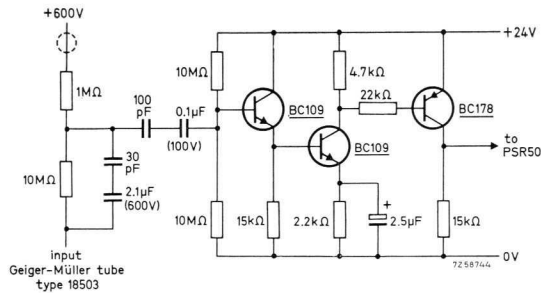


Fig. 12-13. Adapting a Geiger-Müller tube output to the PSR50.

12.3 Mains Frequency Input Circuits

For accurate timing purposes it is often convenient to count 50 or 100 Hz pulses derived directly from the mains supply. The circuits in the following sections indicate how this may be achieved.

12.3.1 CIRCUIT DELIVERING 50 Hz

The circuit of Fig. 12-14 produces output pulses at mains frequency.

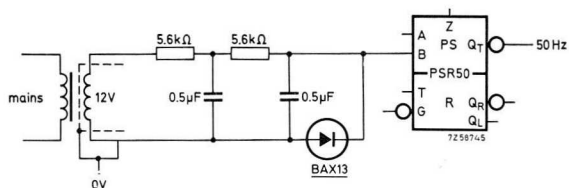


Fig. 12-14. Mains frequency pulse circuit.

12.3.2 CIRCUIT DELIVERING 100 Hz

The circuit of Fig. 12-15 produces output pulses at twice mains frequency, i.e. 100 Hz.

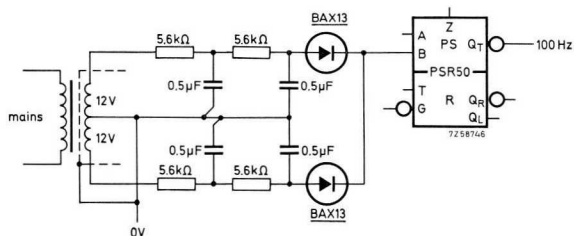


Fig. 12-15. Circuit giving pulses at twice mains frequency.

12.4 Variable Frequency Input Circuits

12.4.1 RC OSCILLATOR USING THE PSR50

A simple oscillator can be constructed with the pulse-shaper section of the PSR50 module as shown in Fig. 12-16a. The relationship between frequency and the value of C is given in Fig. 12-17.

The circuit of Fig. 12-16b can be inhibited by applying 0 V to D_1 or D_2 . If no inhibiting is required, diodes D_1 and D_2 can be omitted.

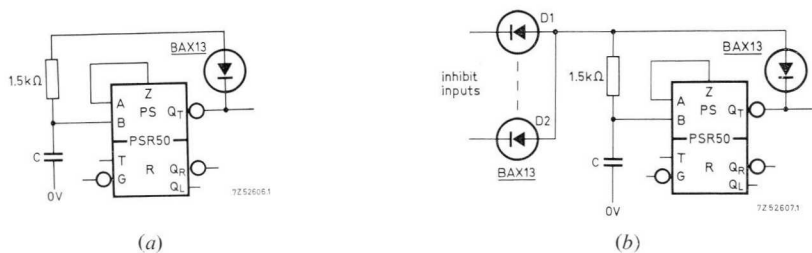


Fig. 12-16a, b. Two RC oscillators.

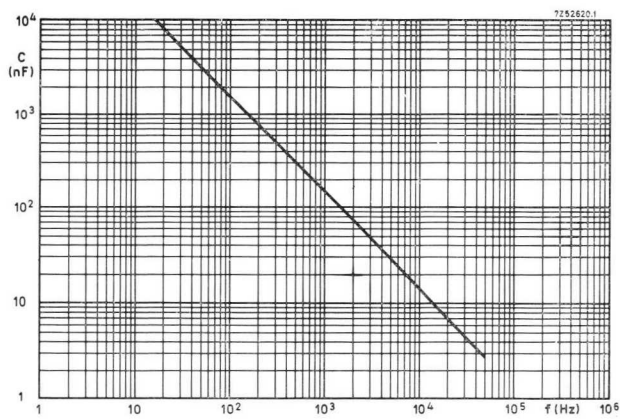


Fig. 12-17. Determination of value of C.

12.4.2 RC OSCILLATOR WITH FREQUENCY CONTROLLED BY LOGIC

The frequency of the output signal f_0 in the circuits of Figs. 12-18 and 12-19 can be controlled by application of the appropriate logic levels to the inputs.

In Fig. 12-18,

$$A \text{ at LOW gives } f_0 = \frac{150}{C_1} \text{ Hz;}$$

$$A \text{ at HIGH gives } f_0 = \frac{150}{C_1 + C_2} \text{ Hz.}$$

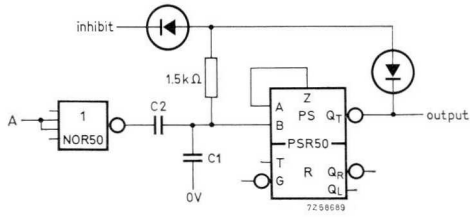


Fig. 12-18. Two-frequency RC oscillator.

In Fig. 12-19,

A at LOW and B at LOW gives $f_0 = \frac{150}{C_1}$ Hz

A at LOW and B at HIGH gives $f_0 = \frac{150}{C_1 + C_2}$ Hz

A at HIGH and B at LOW gives $f_0 = \frac{150}{C_1 + C_3}$ Hz

A at HIGH and B at HIGH gives $f_0 = \frac{150}{C_1 + C_2 + C_3}$ Hz

All capacitor values in μF .

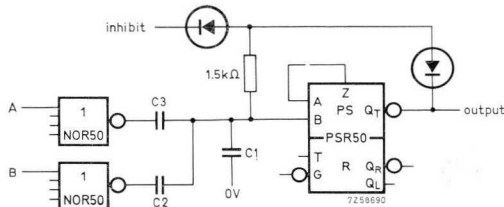


Fig. 12-19. Four-frequency RC oscillator.

12.4.3 RC PULSE GENERATOR USING NOR UNITS

Fig. 12-20 shows the circuit. For an equal mark/space ratio, C_1 and C_2 should be equal. The frequency is approximately equal to $5/C$, ($C=C_1=C_2$ in μF), but is also dependent on loading of the output, and supply voltage. Increased load raises the frequency, and increased

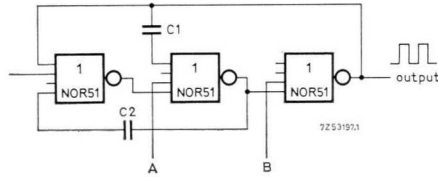


Fig. 12-20. RC pulse generator.

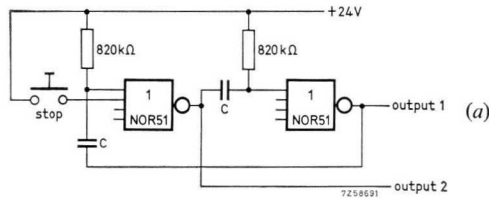


Fig. 12-21. RC pulse generator.

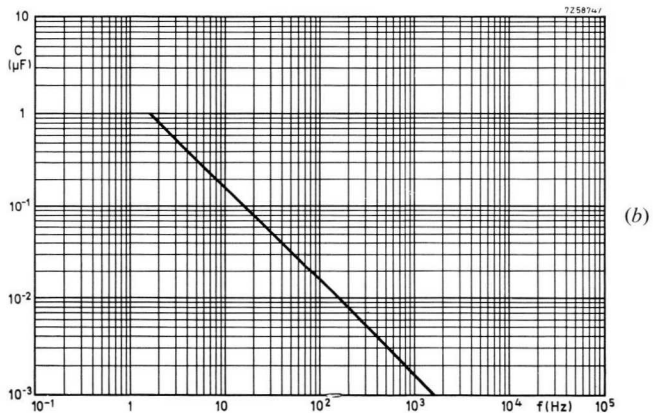


Fig. 12-21. Determination of value of C .

supply voltage lowers it. *A* at HIGH level and *B* at LOW level makes the output a steady HIGH, and *B* at HIGH makes the output a steady LOW. The circuit is self-starting when supply is connected.

A second RC pulse generator using only 2 modules is shown in Fig. 12-21a. The output is sufficient to drive a flashing light. The relation between frequency and value of *C* is shown in Fig. 12-21b.

12.4.4 CRYSTAL OSCILLATOR OF 10 KHZ

The circuit of Fig. 12-22 shows a 10 kHz crystal oscillator using the PSR50 module and crystal Cat. No. 4322 131 00021. The voltage at terminal *Z* of the PSR50 must not rise above 12.5 V as damage to the crystal might otherwise occur.

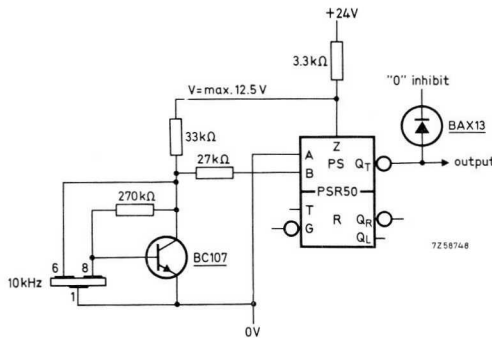


Fig. 12-22. Crystal oscillator.

13 Subsystem Examples

In this chapter we discuss techniques and circuits for various commonly required subsystem functions. Included are

- time delays circuits;
- direct-coupled monostable circuits;
- methods for obtaining extra output capability from NOR functions;
- divider circuits with the NIC50;
- decimal/binary code converters;
- additional drive circuits with the PDU50A;
- decimal/binary decoding for tape punches;
- output interface circuits;
- long-distance input signal transmission method;
- sign shift and decimal point shift in the indicator modules;.

13.1 Time Delays

13.1.1 DELAY OF NEGATIVE-GOING SIGNAL

Fig. 13-1 shows a method of delaying a negative-going "1/0" change. With $R = 15 \text{ k}\Omega$ the time delay obtained varies from approximately 2-20 ms maximum for $C = 1 \text{ to } 10 \mu\text{F}$. Up to 2 D.U. may be taken from output Q . Fig. 13-2 shows the time relationships.

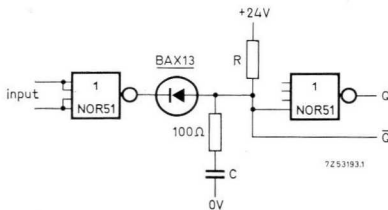


Fig. 13-1. Delay of negative-going signal.

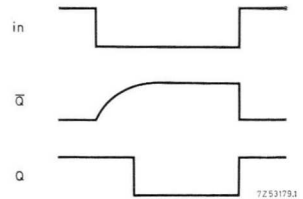


Fig. 13-2. Time relationships.

The graph of Fig. 13-3 shows the exact relationship between the value of C and the delay t , for various loadings of the output. The numbers alongside the curves refer to the value of R which must be used for various output loadings, as follows:

- Curve 1: load, 1 D.U.; $R = 47 \text{ k}\Omega$
- Curve 2: load, 2 D.U.; $R = 22 \text{ k}\Omega$
- Curve 3: load, 3 D.U.; $R = 15 \text{ k}\Omega$
- Curve 4: load, 4 D.U.; $R = 12 \text{ k}\Omega$
- Curve 5: load, 5 D.U.; $R = 8.2 \text{ k}\Omega$
- Curve 6: load, 6 D.U.; $R = 6.8 \text{ k}\Omega$

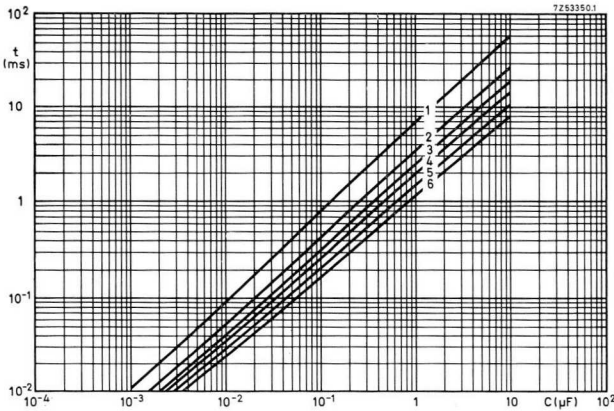


Fig. 13-3. Determination of the value of C .

For delays of more than 100 ms, a module from the 60-Series NORbit range should be used. The module is termed the Timer Unit TU60; Fig. 13-4 shows a suitable arrangement. Delay t is then equal to $R \times C$ seconds, if R is in $\text{M}\Omega$ and C in μF (capacitor C should be a low leakage, non-electrolytic type).

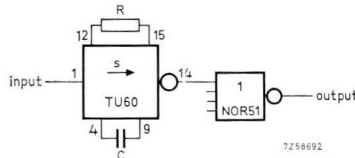


Fig. 13-4. Delays of more than 100 ms.

13.1.2 DELAY OF POSITIVE-GOING SIGNALS

A "0/1" change may be delayed as shown in Fig. 13-5. When the signal is applied the output of NOR (A) goes to "0" and the diode becomes cutt off. The capacitor then discharges into the driven units. The time delay thus depends on output \bar{Q} loading. Typical figures are 15 to 150 ms for

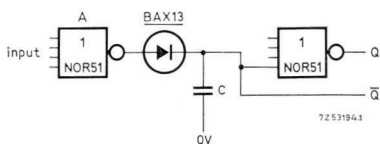


Fig. 13-5. Delay of positive-going signal.

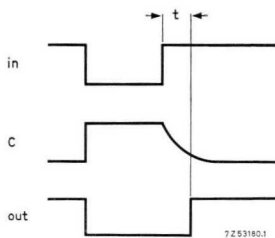


Fig. 13-6. Time relationships.

$C = 0.1 \mu\text{F}$ to $1.0 \mu\text{F}$ for a loading of 1 D.U.; time relationships are shown in Fig. 13-6. The graph of Fig. 13-7 shows the relationship between C and t , for various output loads. The curve numbers refer to the various loads as, follows:

- Curve 1: load, 1 D.U.
- Curve 2: load, 2 D.U.
- Curve 3: load, 3 D.U.
- Curve 4: load, 4 D.U.
- Curve 5: load, 5 D.U.
- Curve 6: load, 6 D.U.

For positive-going delays of more than 100 ms, the 60-Series NOR-bit module TU60 should be used, as shown in Fig. 13-8. The same remarks as given for the TU60 in section 13.1.1 apply.

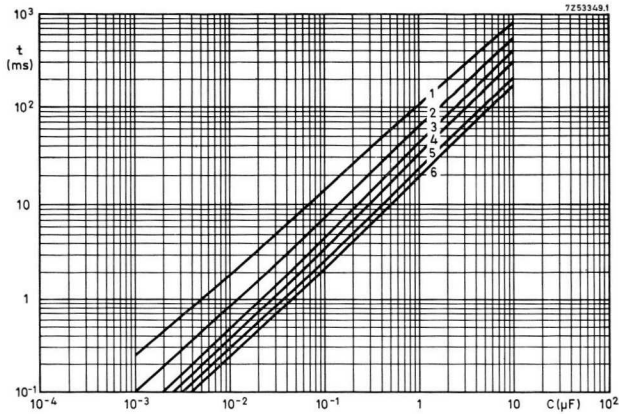


Fig. 13-7. Determination of the value of C .

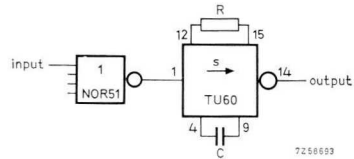


Fig. 13-8. Delay of more than 100 ms.

13.2 Direct-coupled Monostable Circuits

13.2.1 OUTPUT PULSE DURATION LESS THAN INPUT

A monostable circuit which can be triggered by a negative-going input signal is shown in Fig. 13-9. The input signal duration must be greater than the output pulse duration t (max. 100 ms) as shown in Fig. 13-10; t is determined by C , the relationship being given in the graph of Fig. 13-11.

If a longer output pulse duration is required, the circuit of Fig. 13-12, which uses a 60-Series module TU60, can be used. See section 13.1.1 for remarks regarding the TU60.

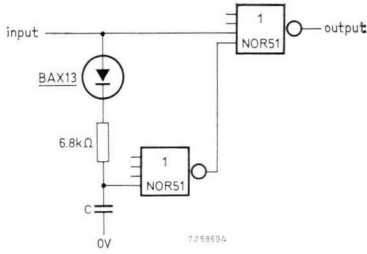


Fig. 13-9. Monostable circuit triggered by negative-going input signal.

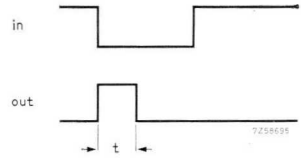


Fig. 13-10. Time relationships.

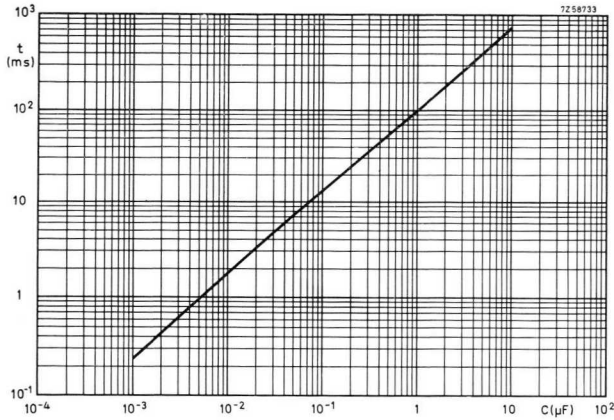


Fig. 13-11. Relationship between t and C .

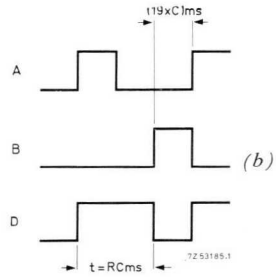
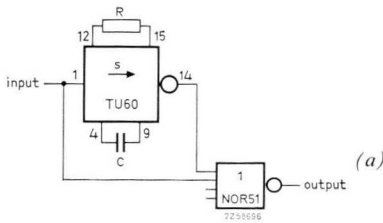


Fig. 13-12. (a) Monostable circuit giving longer output pulse duration. (b) Time relationships.

13.2.2 OUTPUT PULSE DURATION GREATER THAN INPUT

The circuit of Fig. 13-13 shows how a positive-going input can be used as trigger. Because the output is fed back to the input of a memory circuit, the input signal duration can be made very short (down to $10 \mu\text{s}$). Fig. 13-14 gives the relationship between the input and output signals; Fig. 13-15 illustrates how t varies with C .

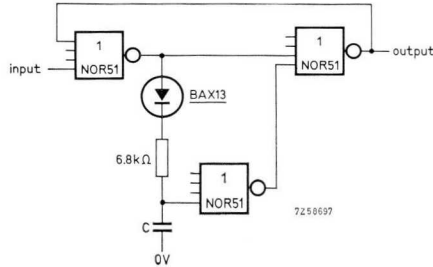


Fig. 13-13. Triggering with positive-going pulses.

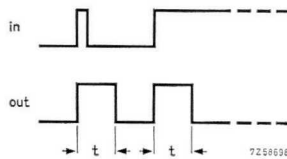


Fig. 13-14. Time relationship.

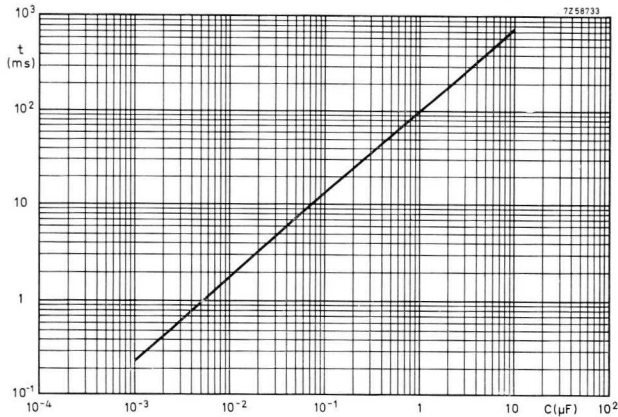


Fig. 13-15. Relationship between t and C .

For a longer output pulse duration, a 60-Series module (the TU60) can be used as in Fig. 13-16. See section 13.1.1 for further remarks regarding the TU60.

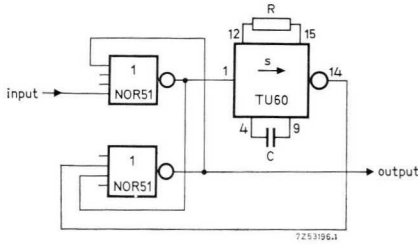


Fig. 13-16a. Long output pulse duration.

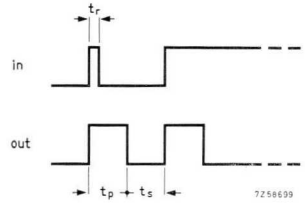


Fig. 13-16b. Time relationship.

13.2.3 CHAIN OF MONOSTABLE CIRCUITS

The circuit of Fig. 13-17 shows how various delays may be obtained with monostable circuits coupled in series. Note that the trailing edge of one pulse occurs simultaneously with the leading edge of the next pulse (see Fig. 13-18).

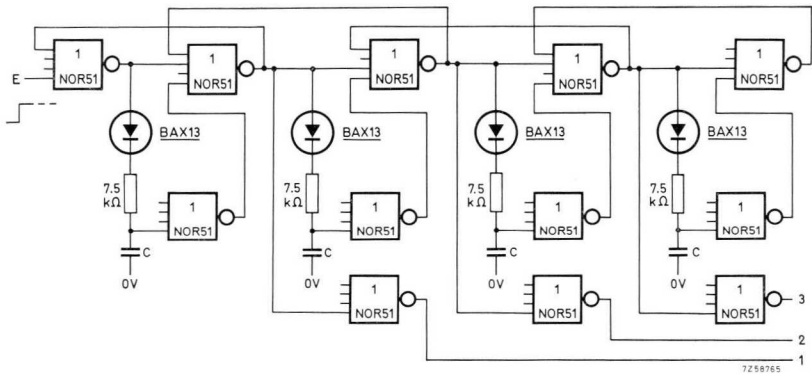


Fig. 13-17. Series connection of delay-circuits.

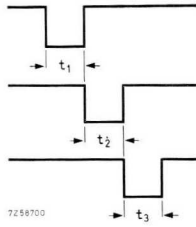


Fig. 13-18. Time relationship.

13.3 Extra Capability from NOR Functions

13.3.1 ADDITIONAL NOR INPUTS

The basic NOR function has four inputs, and although this is usually sufficient, extra inputs can be created by using diodes in the manner of Fig. 13-19. The number of extra inputs obtainable in this way is limited to 6 per input; above this number the total leakage current of the diodes can be sufficient to overload a driving unit. Alternatively, a maximum of 24 diodes may be mounted on one input, the others being left unconnected.

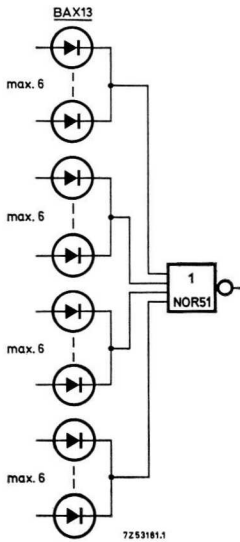


Fig. 13-19. Increasing NOR fan-in.

13.3.2 PARALLELING NOR-INPUTS

The sensitivity of a NOR function can be greatly increased by paralleling the inputs. The effect of paralleling the inputs is illustrated by the following (see Fig. 13-21):

- 2 inputs paralleled: HIGH: 7.75 V;
- 3 inputs paralleled: HIGH: 4.4 V;
- 4 inputs paralleled: HIGH: 3.0 V;
- (single input; HIGH: 13 V).

13.3.3 INCREASING OUTPUT CAPABILITY

Fig. 13-20 shows how the output capability of a NOR can be increased by using an external resistor R_{EXT} to the V_P (+24 V) supply. However, several inputs must be connected in parallel to keep the maximum "0" level output voltage within its specification. Fig. 13-21 gives the relation between R_{EXT} and the output in $D.U.$, together with the number of inputs that must be paralleled.

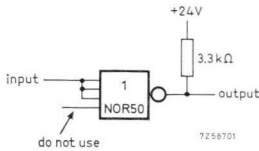


Fig. 13-20. Increasing NOR fan-out.

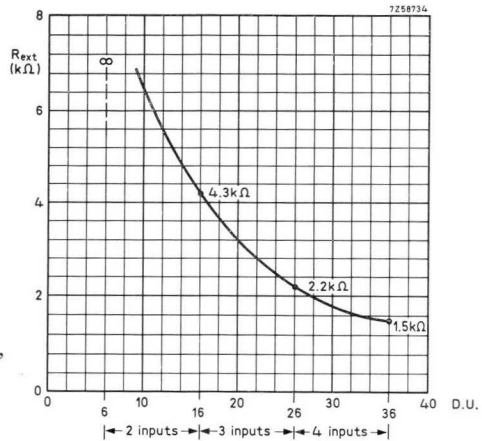


Fig. 13-21. Relation between R_{EXT} , $D.U.$, and paralleled inputs.

13.3.4 DRIVING BUFFER NOR FUNCTIONS FROM A NOR FUNCTION

Up to 6 Buffer NOR functions can be driven from a normal NOR function if required. Up to 3 B-NOR functions can driven together with one normal NOR. Figs. 13-22 and 13-23 show the two possibilities.

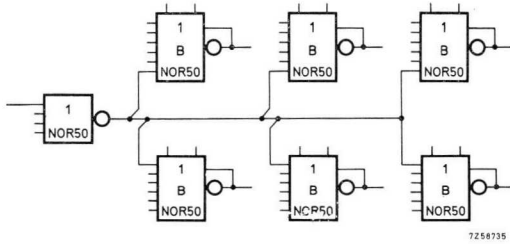


Fig. 13-22. NOR driving Buffer NOR's.

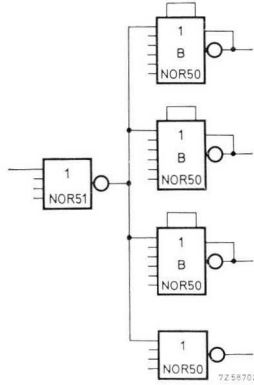


Fig. 13-23. NOR driving B-NOR's and NOR.

13.3.5 OBTAINING AN OUTPUT FROM MORE THAN 6 DECADES

In decoding a number one Buffer NOR input per decade is required. Thus for more than 6 decades Buffer NOR units should be paralleled as shown in Fig. 13-24.

Note that Q_1 should be connected to R_1 on one unit only. A maximum of three Buffer NOR's may be connected in parallel.

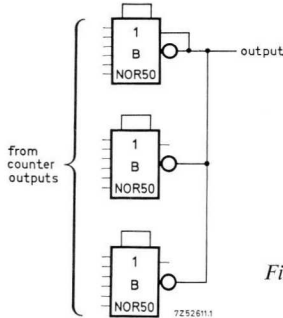


Fig. 13-24. Paralleling of Buffer NOR outputs.

13.4 Dividing Circuits using the NIC50

13.4.1 DIVIDER WITH SCALING FACTOR OF 2

The circuit of Fig. 13-25 shows the outputs which must be used in order to obtain a divider of 2 with the NIC50.

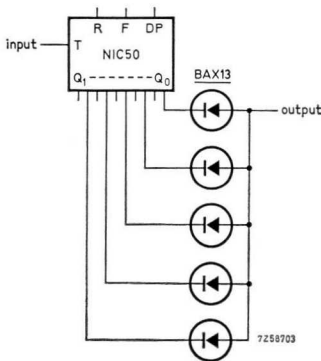


Fig. 13-25. Scaler of 2.

13.4.2 DIVIDER WITH SCALING FACTOR OF 5

Fig. 13-25 shows the arrangement for a divider of 5 using the NIC50.

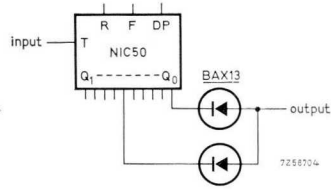


Fig. 13-26. Scaler of 5.

13.5 Code Conversion Methods

13.5.1 DECIMAL TO BINARY CODE CONVERSION

This section gives four examples of converting a decimal number to a number expressed in binary code. These are:

- Using Buffer NOR functions (one circuit required per decade);
- Using PDU50A modules (one circuit required per decade);
- Using PDU50A modules plus scanner (only one circuit required — independent of number of decades — plus scanner);
- Using LRD50 modules for tape punch drive (one circuit per decade).

Decimal to Binary Code Converter using B-NOR's

The circuit is shown in Fig. 13-27. Decimal input to the converter can be directly from a NIC50 or RIC50 module.

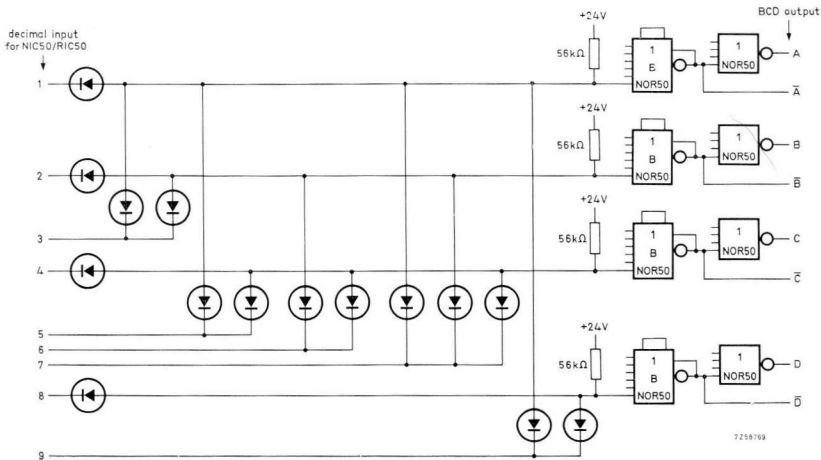


Fig. 13-27. Decimal to Binary Code Converter.

Decimal to Binary Code Converter using PDU50A Modules

The circuit of Fig. 13-27 given previously uses four B-NOR functions per decade. In some cases, a more economical solution is to use one PDU50A module per decade as shown in the scheme of Fig. 13-28. The decoder circuit is shown in Fig. 13-29.

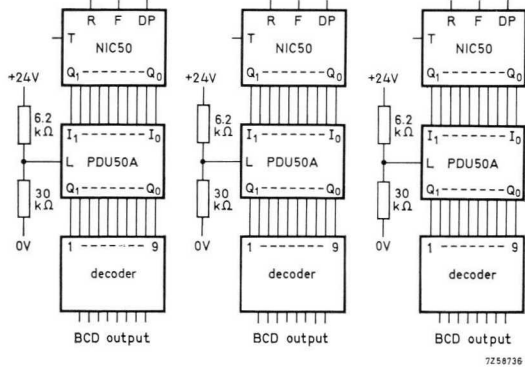


Fig. 13-28. Decimal to Binary Code Converter.

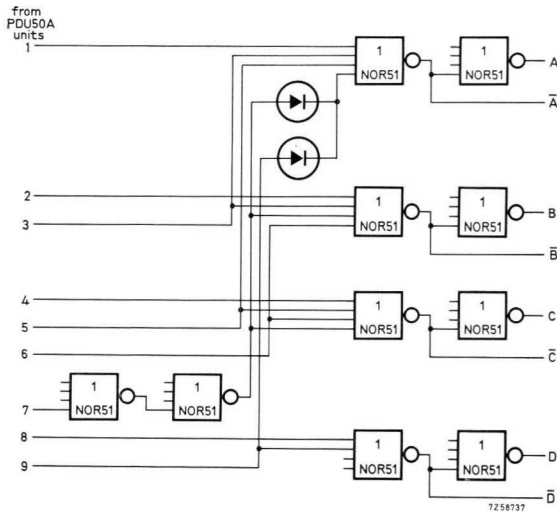


Fig. 13-29. Decoder.

Decimal to Binary Code Converter using PDU50A Modules, plus Scanner

Where a number composed of many decades is required to be converted, a single decoder plus a scanning circuit might prove more economical than the arrangement given previously. Fig. 13-30 shows a typical arrangement for 3 decades; the decoder circuit is that of Fig. 13-29. The scanner circuit is discussed in section 10.3.

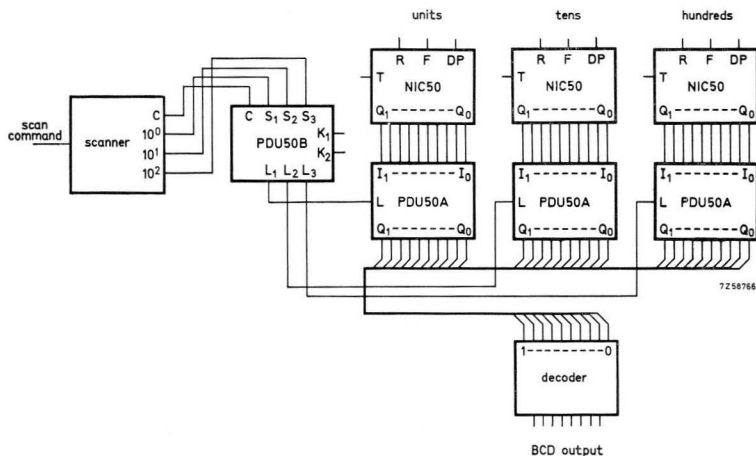


Fig. 13-30. Decimal to Binary Code Converter with Scanner.

Decimal to Binary Code Converter for Tape Punch Drive

Fig. 13-31 shows how the decimal number to be punched is converted from decimal to BCD code and fed to the tape punch via the power amplifiers. Parity checking is incorporated. Each digit is punched in sequence. The number of inputs of the LRD50 may be increased as shown in order to make full use of the facilities incorporated in the tape punch.

13.5.2 BINARY TO DECIMAL CODE CONVERSION

A circuit for converting binary code to decimal code, for instance converting the output of the DCD50 module to a suitable input for the MID50 module, is shown in Fig. 13-32.

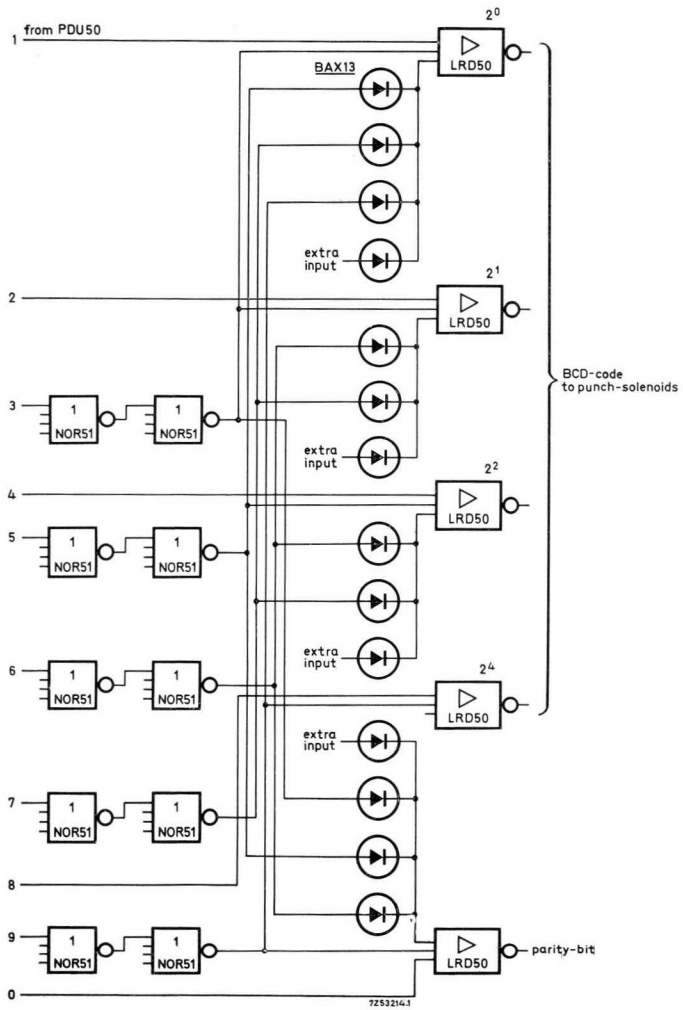


Fig. 13-31. Tape punch drive.

13.6 Additional Drive Circuits with the PDU50A

13.6.1 OUTPUT LEVEL MODIFICATION

The PDU50A module can be advantageously employed in comparator systems in which the output levels of the NIC50 or RIC50 decade counters are required to be modified to the normal logic levels. (HIGH: $0.62 V_{p1}$ to V_{p1} ; LOW: 0.3 V maximum).

In this application, the PDU50A module replaces ten Buffer NOR units from the 3NOR50. Terminal *L* of the PDU50A modules must be connected to a suitable positive voltage as shown in Fig. 13-33.

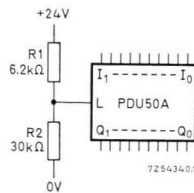


Fig. 13-33. Level conversion with PDU50A.

13.6.2 SEQUENCE REGULATION

The sequence regulator shown in Fig. 13-34 functions as a scan pulse generator. It can be thought of as a stepping switch of 30 positions, or a pulse distributor. The ten *Q* outputs of the first NIC50 are connected to the ten *I* inputs of each PDU50A module. At the first input pulse (from an oscillator for example), inputs *I*₁ of all three PDU50A modules are driven to HIGH level, but only *Q*₁ of PDU50A-I produces an output because only *Q*₀ of NIC50-II is at low level (thus producing shift signal *L*₁). At the tenth input pulse, *Q*₁ of NIC50-II becomes LOW in turn, and the ten outputs of PDU50A-II are subsequently activated in sequence. At the twentieth pulse, PDU50A-III comes into operation.

The thirtieth input pulse, which appears as an output pulse on *Q*₀ of PDU50A-III, could be used to reset the NIC50-II so that subsequent input pulses cause the whole cycle described above to be repeated. A larger number of outputs could be obtained simply by adding PDU50A

and PDU50B modules. Separation of the output pulses (in time) can be done by connecting the input signal to terminal *C* of PDU50B. With terminal *C* connected to earth, the output pulses are joined in time, that is, the start and finish of two pulses at adjacent outputs is coincident.

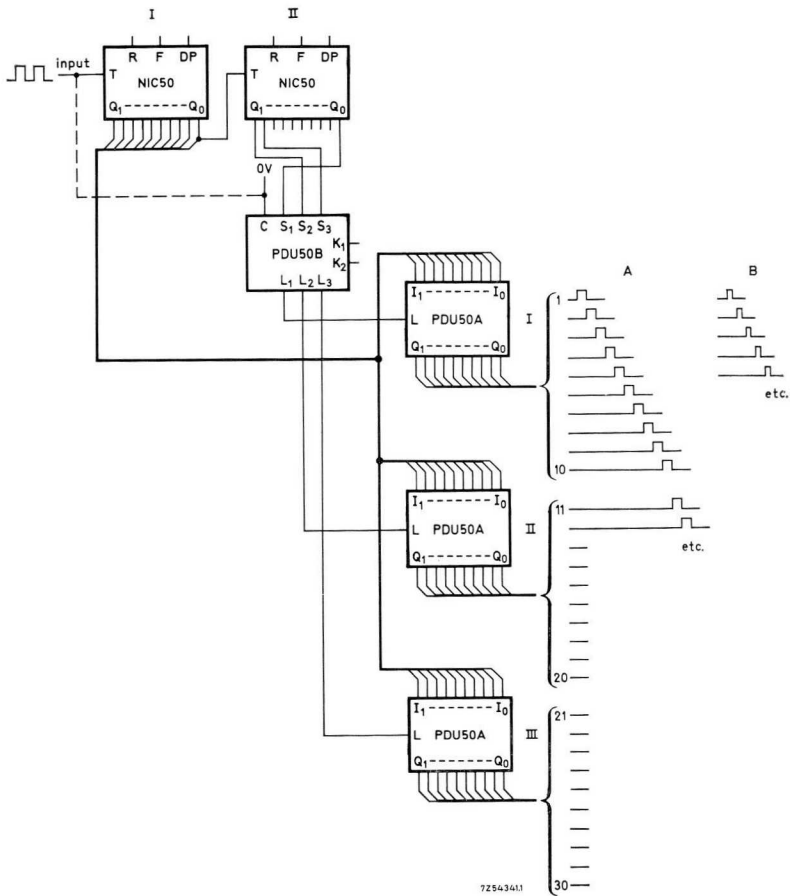


Fig. 13-34. Sequence regulator.

13.6.3 CONTROL OF MORE THAN 6 PROGRAMMES

The NIC50/RIC50 can drive up to 6 programmes. Increased output (max. 20) can be obtained by using PDU50A modules and additional power amplifiers like the IA60 (half of the 2.IA60 60-series module) at the output, as shown in Fig. 13-35.

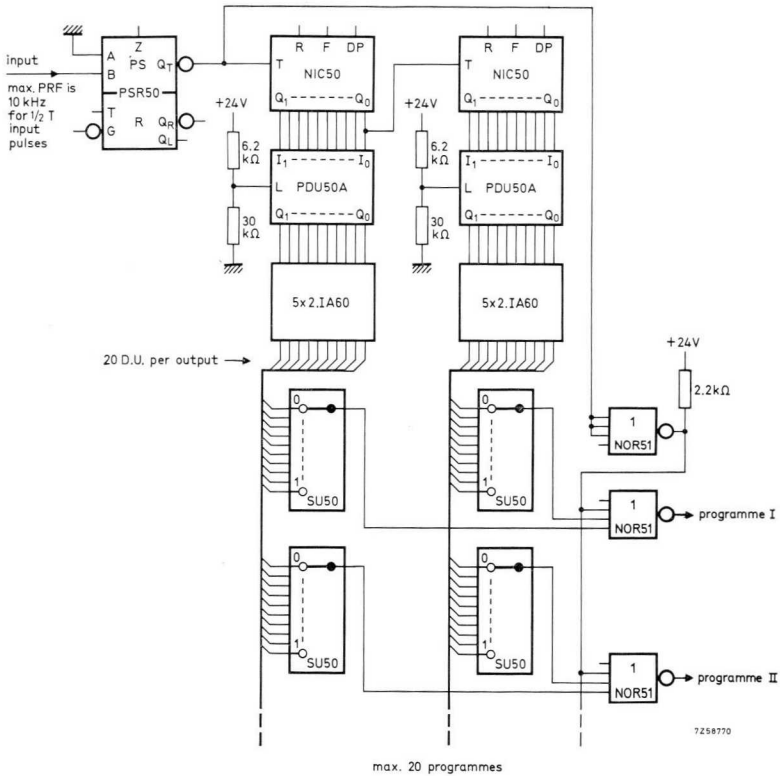


Fig. 13-35. Driving up to 20 preset programmes.

13.7 Precautions against Supply Failure

13.7.1 PREVENTION OF SUPPLY FAILURE

The circuit of Fig. 13-36 shows how an auxiliary Ni-Cd storage battery can be connected to the normal power supply so as to maintain system supply in the event of a mains failure. Battery capacity should be matched to system requirements. With the arrangement shown, the battery is continuously trickle-charged when mains supply is available.

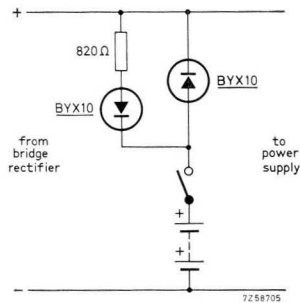


Fig. 13-36. Battery supply at mains failure.

13.7.2 RE-STARTING AFTER LOSS OF SUPPLY

It is usually necessary to ensure that memories in the logic system take on a definite state when re-starting after loss of supply. The circuit of Fig. 13-27 shows how a reset pulse can be obtained upon switching on the supply; that of Fig. 13-38 shows an arrangement by which the memory states at supply failure are retained until after the supply is again available.

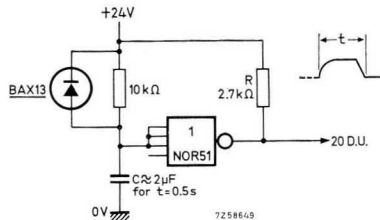


Fig. 13-37. Resetting at mains switch-on.

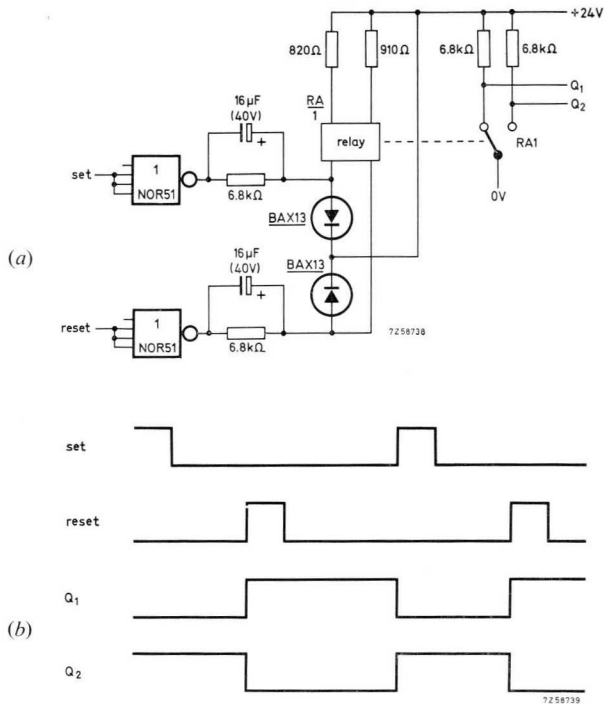


Fig. 13-38. Restart after loss of supply.

13.8 Output Interface Circuits

This section gives methods by which the logic system outputs can be used to drive warning signals or operate machines.

13.8.1 0.3 A, 1 A OUTPUT DRIVE

For loads up to 300 mA, the LRD50 module is available. It can be connected directly to the 50-Series logic NOR outputs, and has a maximum output capability of 300 mA at 30 V supply. For loads of up to 1 A, a power amplifier in the 60-Series NORbit range, the PA60, is available. Its maximum output capability is 1 A at 30 V and can also be directly connected to a 50-Series NOR output.

13.8.2 2 A OUTPUT DRIVE

The circuit of Fig. 13-39 shows a way in which a load of up to 2 A can be driven by an LRD50 module. When the LRD50 input is at LOW level, current will flow in the load. Inductive loads should be paralleled with a diode (in opposite direction to current flow through the load).

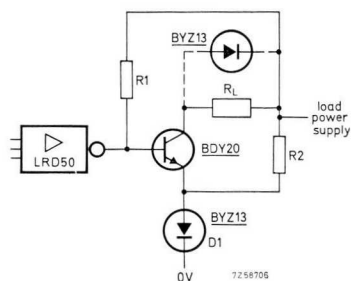


Fig. 13-39. 2 A output drive.

13.8.3 A.C. RELAY DRIVE

Fig. 13-40 shows a circuit suitable for driving an a.c. relay. The LRD50 is used to trigger a BTY94 DIAC which activates the relay. A maximum of 25 A at 220 V can be handled.

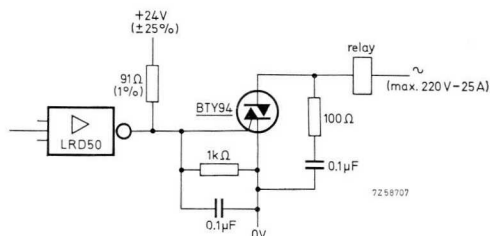


Fig. 13-40. A.C. relay drive.

13.8.4 THYRISTOR DRIVE

An electro-magnetic clutch with brake is an application for this circuit; when the brake is not activated then the clutch must be driven. Fig. 13-41 shows the circuit, where LRD50's control a level-driven thyristor flip-flop. The value of the commutation capacitor C is given by:

$$C \geq 1.4 \times t_q \times I/E \mu\text{F}$$

where

t_q = Max. turn-off time of the SCR in μs .

I = Max. load current (in A) at the moment of commutation.

E = Min d.c. supply voltage.

Capacitor C can be made of two solid aluminium-type electrolytic capacitors and two diodes as shown in Fig. 13-42. The max. rated forward current of the diodes must be greater than the max. load current at the moment of commutation. Inductive loads should be reverse-paralleled by diodes as shown.

Care should be taken to ensure that the power supply to the load can only be switched on when the logic power supply is present. A circuit providing this feature is shown in Fig. 13-43. The value of R depends on the trigger current of the thyristor used; for the BTY79 the value is 690 Ω .

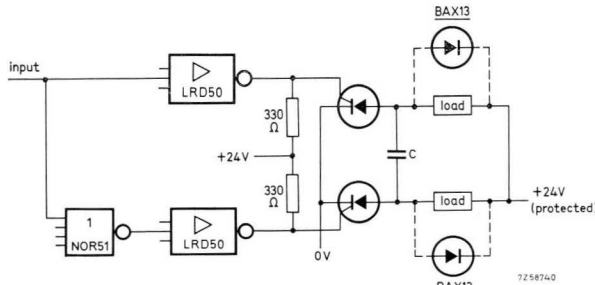


Fig. 13-41. Thyristor drive.

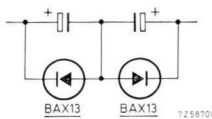


Fig. 13-42. Capacitor connections.

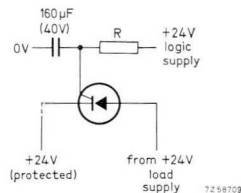


Fig. 13-43. Output transistor protection.

Thyristor Switching of Full-Wave Rectified A.C.

Fig. 13-44 shows how LRD50's are used to trigger thyristors in a full-wave rectified a.c. circuit. The capacitor *C* across the load turns off the thyristor as the supply voltage approaches zero by placing a negative voltage on the thyristor anode. For reliable switching the time constant of the load and capacitor should be at least 25 times the frequency of the a.c. supply. The supply voltage may of course be higher than 24 V, but should be isolated from the a.c. mains.

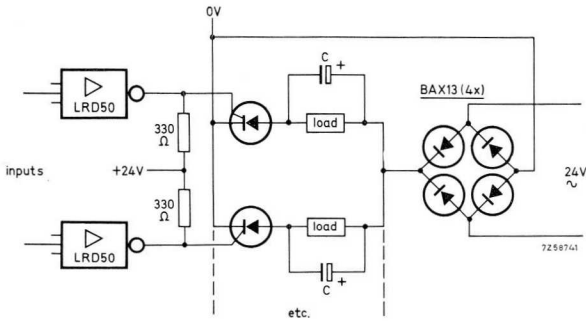


Fig. 13-44. Full-wave rectifier circuit.

13.9 LONG-DISTANCE INPUT SIGNAL TRANSMISSION (OVER 100 M)

The circuit of Fig. 13-45 can be used where signals must be transmitted over distances of more than 100 m.

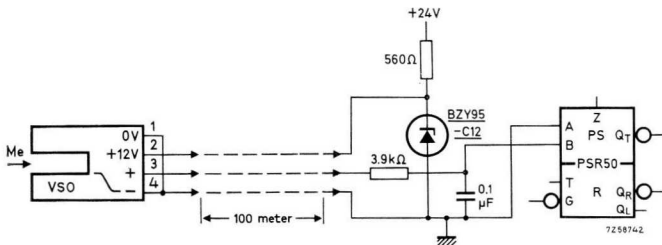


Fig. 13-45. Long-distance signal transmission.

13.10 Sign Shift and Decimal Point Shift

13.10.1 SIGN SHIFT WITH SID50

When using the MID50 in the shift register mode (see section 9.3) it may be necessary to shift sign information in synchronism. Fig. 13-46 gives a suitable circuit, which operates as follows.

Assume NOR (1) has a "1" level input thus giving a plus sign on SID50 (A). When the shift signal is applied, both inputs to NOR (3) will be "0", setting memory (4-5) such that NOR (4) output is at "1" level and NOR (5) at "0", illuminating "plus" on SID (B). The sign of SID50 (B) is transferred to (C) in a similar manner, the memory state being determined by the signals from NORs (4) and (5). In such a register staggered pulses must be provided in order to achieve correct operation. The circuit of Fig. 9-4 is suitable.

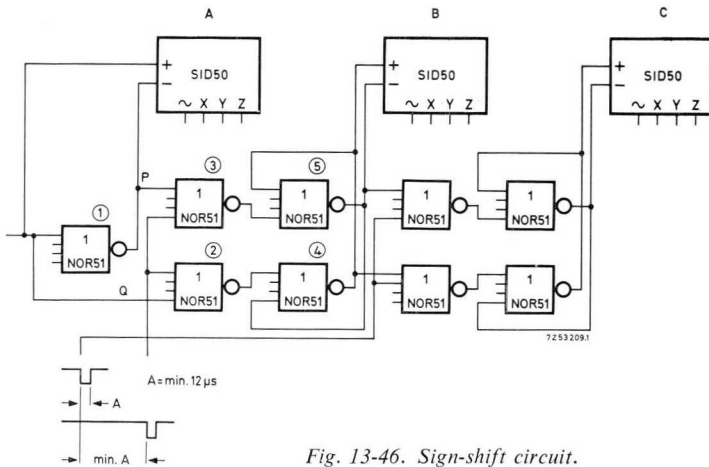


Fig. 13-46. Sign-shift circuit.

13.10.2 DECIMAL POINT SHIFT

The decimal point may be shifted in a similar manner to that described for the plus and minus signs, providing that it is driven as shown in Fig. 13-47. Inputs *P* and *Q* control the setting of the memory as before.

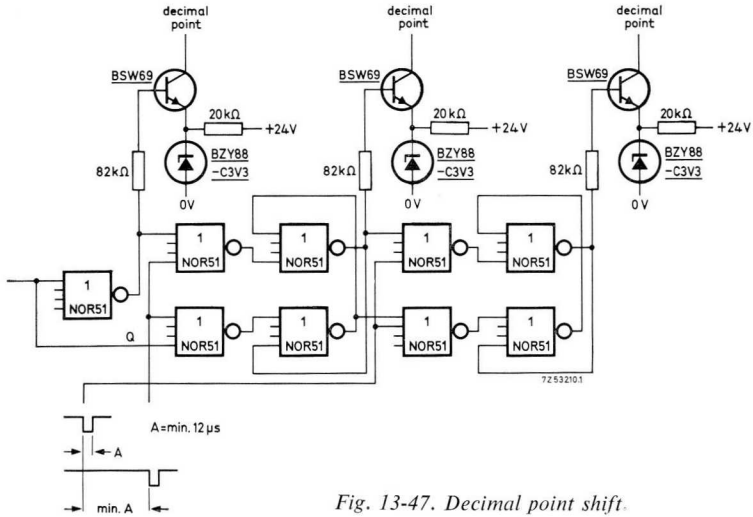


Fig. 13-47. Decimal point shift.

14 Examples of Virtually Complete Systems

We shall now examine the way in which complete or virtually complete systems can be built up by using the subsystems described in Chapter 13 and the basic techniques discussed earlier. Although some of the systems discussed in this chapter are for special applications, in reality the uses to which the modules can be put is limited only by the imagination of the designer. It is easy to see for instance that the "Chemical Blending Plant Control" system described in the following pages could readily be adapted to control many other processes besides the blending of chemicals.

14.1 A Counting System for the Batching of Components

This section gives a description of a counting and batching machine which was developed by a manufacturer. Before arrival at the machine, the capacitors are attached, evenly spaced, by their leads to a tape. The manufacturer's request was for a machine to cut the leads so that the capacitors feed into a box, fill the box with a certain quantity of units, and automatically transfer the flow to another box upon reaching that quantity. The first box meanwhile having been emptied, the flow was to be returned to it after the filling of the other box, and so on.

The machine described (and in service) performs all these operations, and incorporates interlocks to prevent mishaps due to operator error. The input circuitry, which at first glance might seem rather complicated, has in fact been designed to guarantee accurate operation at over 70 000 capacitors per hour. A detailed description of the logic is given under the heading "Circuit Description"; below is a general account of the actions involved.

Fig. 14-1 is a photograph of the control unit. It should be noted here that quality tests, such as capacitance value measurements, are carried out on the capacitors before they reach the batching machine. For this reason gaps sometimes occur on the tape, where particular capacitors have been removed after failing a test.

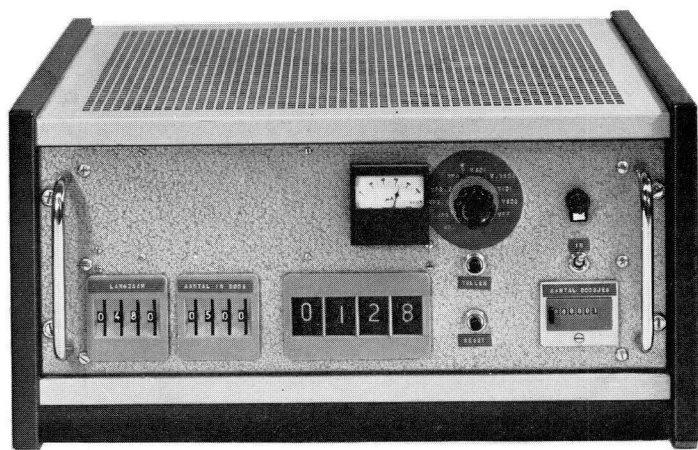


Fig. 14-1. Control unit.

The tape carrying the capacitors by their leads comes from the left and the capacitors trip a probe which triggers a VSO "presence switch" (VSO₂ in Fig. 14-2).

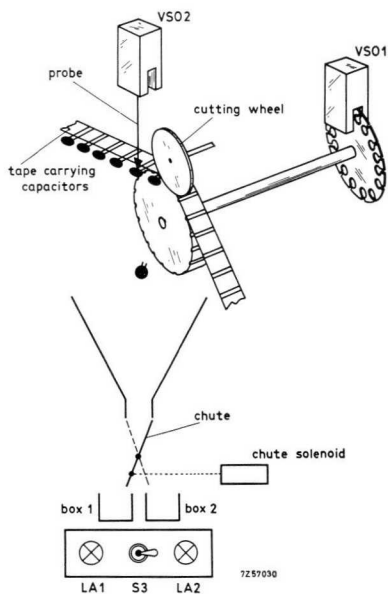


Fig. 14-2. Mechanical arrangement of the machine.

A gapped wheel inside the machine, rotating in synchronism with the tape, passes the jaws of a second VSO (VSO₁), each gap in the wheel indicating the place of a capacitor on the tape. If a below-standard capacitor has been removed from the tape, then the first VSO blocks the counting, by preventing the second VSO from registering a capacitor for that position. With this method of counting the capacitors, high speeds are possible.

The circular cutting blade slices off the capacitors from the tape, and the capacitors, with their leads now trimmed to the correct length, fall through the chute and into a box at position 1. To prevent variations in the number of components in the box due to the delay caused by mechanical inertia, the motor speed is substantially reduced just before the box is filled to the required quantity. The number of capacitors

which must pass into the box before speed reduction occurs can be set on Programme 1; this is just a few less than the total number per box, set on Programme 2. Let us assume that the numbers are 490 and 500 respectively. (Up to 9999 can be set on each programme.) Fig. 14-3 shows the block diagram of the system. Motor speed (normal, slow, or stop) is dependent on three conditions: chute direction, position of switch S_3 , and the preset numbers.

When the 500th capacitor is delivered to Box 1, the "Box 1 Full" lamp (LA_1) burns, and the chute is automatically directed to Box 2. The machine delivers capacitors, at normal speed, to Box 2.

Meanwhile, the operator sees that LA_1 is alight so he replaces the full Box 1 with an empty, and switches over S_3 to the "Box 2" position. Switching over S_3 extinguishes lamp LA_1 .

Box 2 continues to receive capacitors until 490 have been delivered. The machine then automatically slows down until the 500th capacitor is received in the box, whereupon the "Box 2 Full" lamp (LA_2) lights up. This tells the operator to replace Box 2 with an empty one.

The chute now swings back to Box 1 and capacitors are delivered to

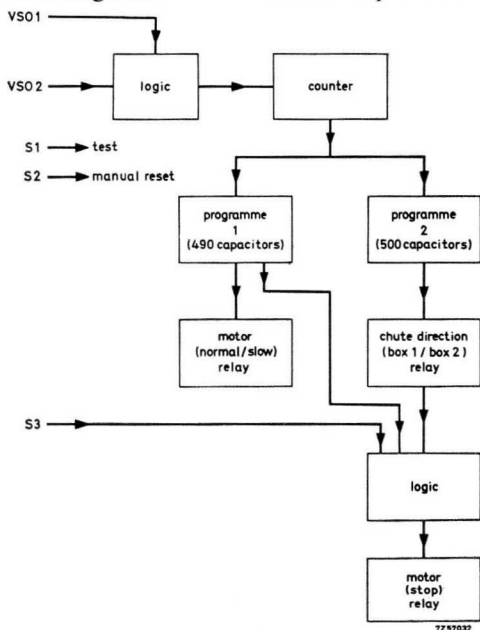


Fig. 14-3. Block diagram.

Box 1 again at normal speed. If, however, the operator has forgotten to remove the full box at position 2, and has therefore not switched S_3 to "Box 1", then the machine will stop after 490 capacitors have been delivered to Box 1. This prevents more capacitors being delivered to the already-full box.

Circuit Description

Figs 14-4 to 14-8 show the circuit diagram. Pulses from VSO_1 (see Fig. 14-4) via the logic circuit formed by U_1, U_2, U_3, U_4 and U_5 , and the pulse-shaper half of the PSR50, activate the four-decade counter (four NIC50 units). With no capacitors available VSO_2 prevents the VSO_1 signals reaching the pulse shaper; with capacitors present, i.e. the probe vane not in the jaws of VSO_2 , VSO_1 can deliver "1" level signals to the PSR50 "B" input.

The memory (U_4 and U_5) ensures that only one count pulse per capacitor is delivered to the PSR50, despite the fact that the VSO_2 vane probe reacts to each of the two capacitor leads. The timing diagram of Fig. 14-5 shows this.

Programme 1 Buffer NOR (U_{28}) output (see Fig. 14-6) goes "1" when all the SU50 outputs of Programme 1 go to "0", that is, at the 490th pulse. LRD50 (U_{25}) activates the "motor normal/slow" relay (see Fig. 14-7) and the motor decelerates to slow speed, if S_3 is at "Box 1" position and the chute is in the Box 1 position.

The motor continues to work, at slow speed, and finally the 500th component is counted, causing the Buffer NOR of Programme 2 (U_{27}) to give a "1". This causes the outputs P and Q of the bi-stable circuit in Fig. 14-8 (U_{20} to U_{23}) to change and as result the "chute/box 1/box 2" solenoid changes to the other position, that is, Box 2. With S_3 being at the "Box 1" position, lamp LA1 will light because $Q = "1"$ (U_{10} output = "1"). The I/O output change from U_{19} which activates the bi-stable also activates the Reset section of the PSR50 (Fig. 14-4) via U_{18} which produces a signal $D = "1"$. The reset pulse C from the PSR50 terminal Q_L has the correct shape and duration to reset NOR memory U_{16}, U_{17} ; terminal Q_R of the PSR50 delivers, at the same time, a reset pulse B to the four NIC50 units.

The memory (U_{16} and U_{17}) being reset causes LRD50 (U_{25}) to deliver "0" and thus the "motor normal/slow" relay contacts switch back to "normal". Operation then continues in the manner described above.

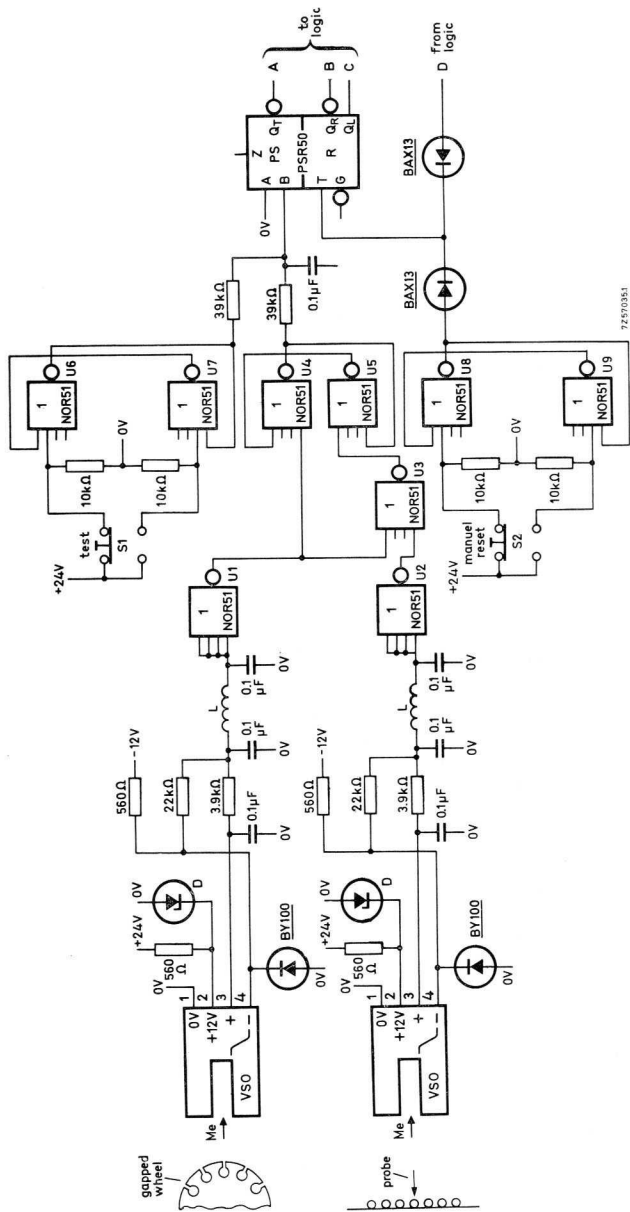


Fig. 14-4. Input circuit. Voltage regulator diodes D are type BZY95-C12 chokes L have the cat. No. 4312 020 36690.

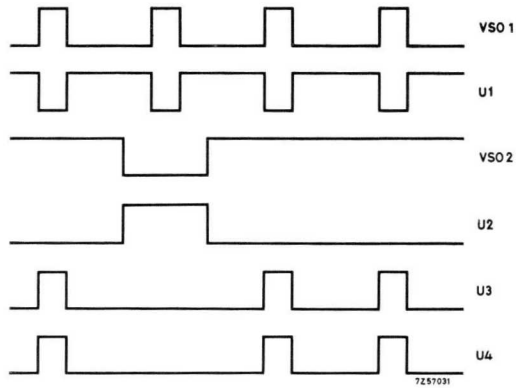


Fig. 14-5. Timing diagram of output signals from input circuit.

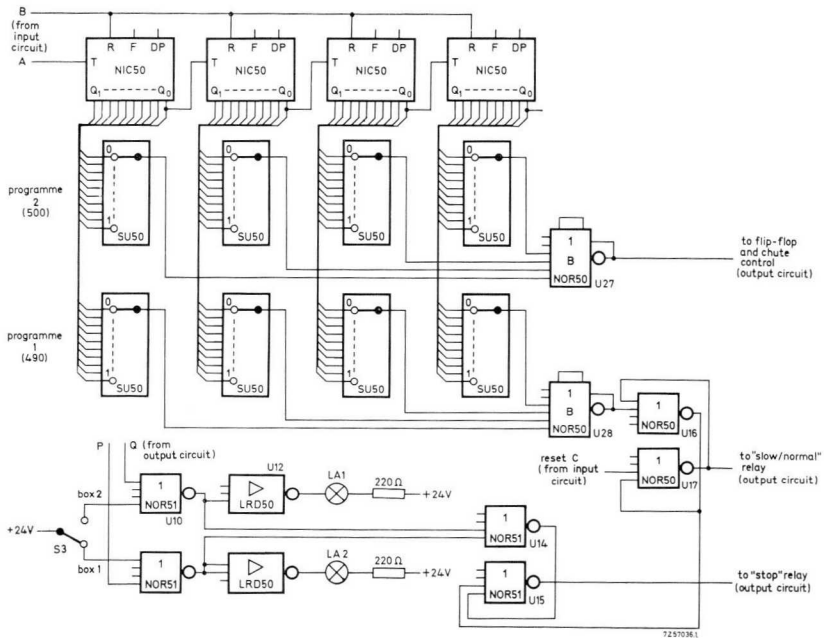


Fig. 14-6. Count control circuit.

14.2 Chemical Blending Plant Control

This section gives a description of a control circuit for blending three chemicals in a specified sequence. A block diagram of the system is shown in Fig. 14-9. The chemicals which are to be blended are stored in tanks *A*, *B* and *C*, being fed sequentially into the main processing tank via the flowmeter. A suitable time interval t_1 must elapse before liquid *C* is added in order to allow liquids *A* and *B* to complete their required reaction. For the same reason, a further interval t_2 must also elapse after the addition of liquid *C*. Valve *D* is then opened in order to discharge the main processing tank. During the above process the flowmeter produces digital electronic pulses at a rate which is directly proportional to the rate of liquid flow through it, and digital pulses are produced by an oscillator in the control circuitry.

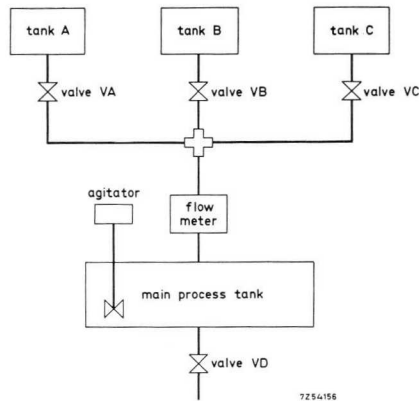


Fig. 14-9. Block diagram.

The five measuring operations, that is of the three liquid quantities and the two time intervals, are initiated and terminated by means of various control functions, the complete process taking place in two automatic sequences separated by an inspection interval. The sequence of operations occurs in seven steps.

Step 1. Depressing the “start” button closes valve *D* and opens valve *A*. Liquid is measured from tank *A* and when the required quantity is reached, valve *A* closes.

Step 2. Valve *B* opens, the agitator starts, and liquid is measured from tank *B*. When the required quantity is reached, valve *B* closes.

Step 3. Timing signals start, the reaction time t_1 is measured, and the timing signals cease.

Step 4. An alarm bell is activated and a “Check” lamp illuminated. Depressing the “Alarm Accept” button silences the alarm bell and extinguishes the “Check” lamp.

An operation check is now carried out.

Step 5. If the results of the inspection are satisfactory, the operator depresses the “Restart” button, valve *C* opens and liquid is measured from tank *C*. When the required quantity is reached, valve *C* closes.

Step 6. Timing signals start, the reaction time t_2 is measured and the timing signals stop. The agitator also stops.

Step 7. Valve *D* opens, the alarm bell is activated and the “Process Complete” lamp illuminated, and liquid is discharged from tank *D*. Depressing the “Alarm Accept” button silences the alarm bell and extinguishes the “Process Complete” lamp.

The Control Circuitry

A single electronic counter is used to measure the five quantities involved in the measuring operations, the magnitude of each quantity being selected by means of the appropriate group of three thumbwheel switches.

The counter, which is reset to zero before each measuring operation, is supplied - with digital measuring pulses produced either by the flowmeter or by the oscillator, depending on whether a liquid quantity or a time interval is being measured.

Each control function (or group of functions) is implemented by the setting or resetting of one of the nine memories. When a particular counter programme has been executed, signals produced by the counter

are used to set the memory which implements the control functions necessary to initiate the next measuring operation. At the same time, the memory which implemented the function (or functions) necessary to initiate the completed operation is reset, thus terminating that operation. The setting signals are applied to a particular memory in conjunction with a gating signal from the previous memory so that the measuring operations take place in the required sequence.

Functional Description

The circuit diagram is shown in Fig. 14-10. When the mains supply is connected, the switch-on reset circuit U_{33}/U_{34} produces a "1" input which resets the nine memories U_{13}/U_{14} to U_{29}/U_{30} .

Step 1. When the "Start" button is depressed by the operator, the 0 V connection to the input of U_{13} is replaced by a "1" level which sets memory U_{13}/U_{14} . This "1" level is also used to reset the three NIC50 decade counters U_4 to "0" via NOR U_2 and the reset section of PSR50 (U_1).

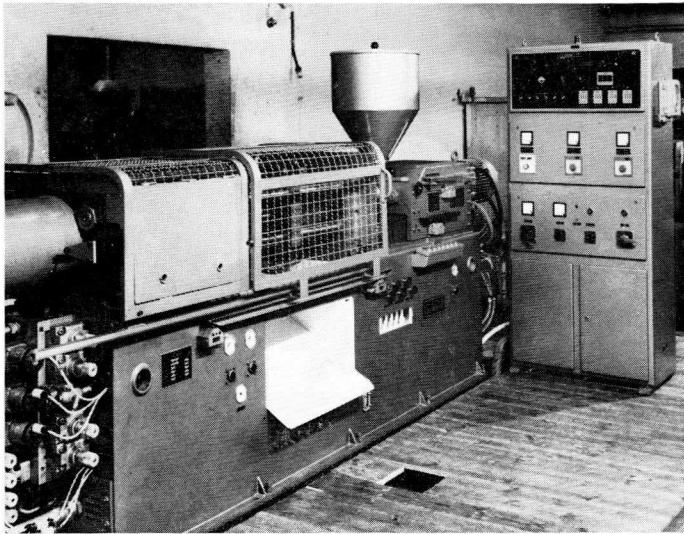
The "1" output from U_{14} is fed to a power amplifier PA60 (U_{39}) which operates relay RA , opening valve VA . The "0" output from U_{13} is used as a gating signal for NOR U_6 of the next memory, all other Buffer NORs being inhibited by "1" levels from their respective previous memories.

With valve VA open, digital measuring pulses are produced by the flowmeter directly proportional to the quantity of liquid through it, and fed via NOR U_3 to the pulse shaping section of PSR50 (U_1). The positive-going output pulses are counted by the three NIC50 decades U_4 until the value which has been set on U_5 (bank of three SU50 switches) is reached.

At this moment, the output signal from Buffer NOR U_6 changes from "0" to "1", setting memory U_{15}/U_{16} .

The "1" output from U_{16} resets memory U_{13}/U_{14} , thus closing valve VA . This signal is also used to reset decades U_4 to zero.

Step 2. The "1" output from U_{16} is used to activate relay RB and open valve VB . This signal also sets memory U_{17}/U_{18} , the "1" output from U_{18} being used to activate relay RE and start the agitator to mix liquids A and B .



Injection Moulding

Electronics oust electro-mechanical devices in this injection moulding control system. 50-Series modules are used to build up signal processing component assemblies incorporating such functional sequences as closing, injection, ejection, opening etc. on individual insert cards. Output signals from the modules are fed via amplifiers to final control elements (solenoid valves and motors).

(by courtesy of Dr. Ing. Fritz Sommer Nachf., Lüdenscheid, W. Germany)

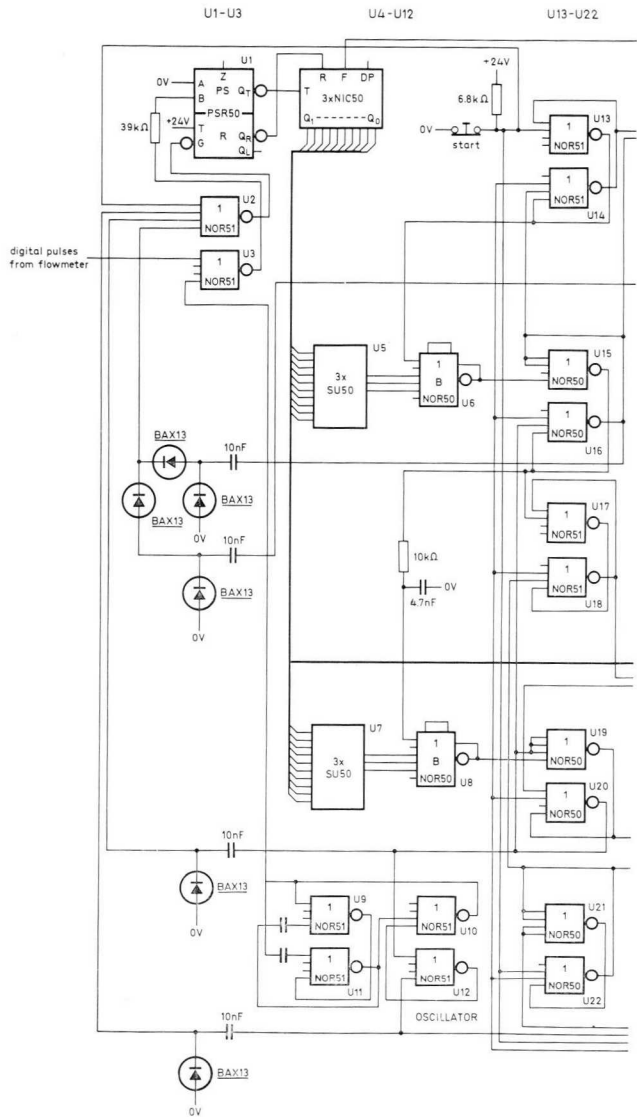


Fig. 14-10. Control circuit.

The "0" output from U_{15} is used as a gating signal for Buffer NOR U_8 , after a small time delay created by the $10\text{ k}\Omega/4.7\text{ nF}$ network which then allows the next programme to be initiated. With valve VB open, pulses from the flowmeter are counted by U_4 until the value which has been set on U_7 is reached. At this moment, the output signal from Buffer NOR U_8 changes from "0" to "1", setting memory U_{19}/U_{20} . The "1" output from U_{20} resets memory U_{15}/U_{16} , thus closing valve VB . This "1" level is also used to reset U_4 to zero.

Step 3. The "1" output from U_{20} is applied via NOR U_{12} to oscillator U_9 , U_{10} , U_{11} , which then feed timing pulses to U_4 via NOR U_3 and the pulse shaping section of PSR50 (U_1). The "0" output from U_{19} is used as a gating signal for Buffer NOR U_{36} so that when the value which has been set on U_{35} (time " t_1 ") is reached by the counters, the output signal from U_{36} changes from "0" to "1", setting memory U_{27}/U_{28} .

The "1" output from U_{28} resets memory U_{19}/U_{20} , and so the oscillator U_9 , U_{10} , U_{11} no longer produces timing pulses.

Step 4. The "1" output from U_{28} is used to activate the alarm bell, and also illuminate the "Check" lamp LA_1 .

When the "Alarm Accept" button is depressed by the operator, a "1" level is produced which resets memory U_{27}/U_{28} thus silencing the alarm bell, and extinguishing the "Check" lamp.

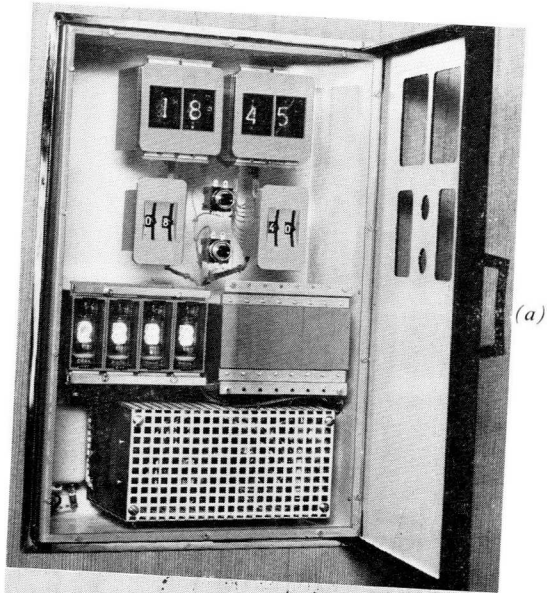
Step 5. When the "Restart" button is depressed by the operator, a "1" level is produced which sets memory U_{25}/U_{26} .

The "1" output from U_{26} is used to reset U_4 to zero and also to activate relay RC and open valve VC . Pulses from the flowmeter are then counted by U_4 .

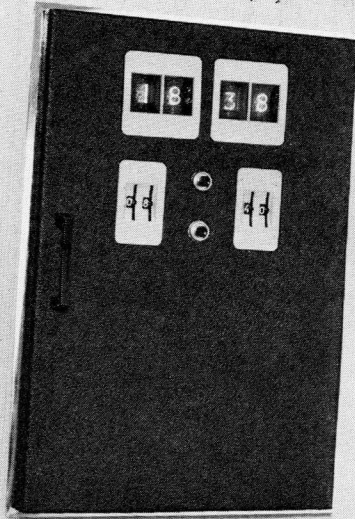
The "0" output from U_{25} is used as a gating signal for Buffer NOR U_{32} , and so when the preset value on U_{31} is reached by the counter, a "1" output is produced by U_{32} , setting memory U_{23}/U_{24} . The "1" output from U_{24} resets memory U_{25}/U_{26} , thus closing valve VC . This "1" level is also used to reset U_4 to zero.

Step 6. The "1" output from U_{24} is applied via NOR U_{12} to the oscillator U_9 , U_{10} , U_{11} which then produces timing pulses which are counted by U_4 .

The "0" output from U_{23} is used as a gating signal for Buffer NOR



(a)



(b)

Digital clock of section 14.3.2. (a) Front view, (b) Interior view.

U_{38} , and so when the preset number on switches U_{37} (time " t_2 ") is reached by the counter, a "1" level is produced by U_{38} , setting memory U_{21}/U_{22} .

The "1" output from U_{22} resets memory U_{23}/U_{24} , and so the oscillator no longer produces timing pulses. This "1" level also resets memory U_{27}/U_{28} , thus stopping the agitator.

Step 7. The "1" output from U_{22} is used to activate relay RD and open valve VD . This "1" level also sets memory U_{29}/U_{30} . The "1" output from U_{30} is used to activate relay RF and again operate the alarm bell, and to illuminate the "Process Complete" lamp LA_2 .

When the "Alarm Accept" button is depressed by the operator, memory U_{29}/U_{30} is reset, thus silencing the alarm bell, and extinguishing the "Process Complete" lamp LA_2 .

Valve VD is closed when the "Start" button is depressed by the operator at the beginning of a subsequent blending process.

14.3 Clock circuits

Clocks frequently form an important part of process control systems. Two examples are given.

14.3.1 CLOCK WITHOUT SETTING FACILITY

This is a simple type, requiring a 1 Hz signal source. Fig. 14-11 shows the circuit diagram. The 1 Hz pulses at the left of the diagram are shaped by the pulse-shaper section of the PSR50, and pass to NIC50 (U_1). Units U_1 and U_2 form a frequency divider of 60, indicating seconds, but are reset in a different manner to that described for the units of the circuit of 14.3.2. Output Q_6 of NIC50 (U_2) is taken to Buffer NOR (U_7); on reaching the 60th pulse, Buffer NOR (U_7) output goes "1" and immediately a reset pulse from terminal Q_R of the reset section of the PSR50 (U_8) is produced. The correct reset pulse duration is obtained via the diode feedback from Q_L to T .

NIC50 (U_3) receives, as a consequence, 1-minute pulses. Buffer NOR (U_9) output goes "1" when NIC50 modules U_3 and U_4 register 59 minutes but, due to the time necessary to charge C_1 the input to NOR (U_{10}) does not reach the "1" level immediately. During this time one of the inputs to NOR (U_{11}) has received a "0" reset pulse from the PSR50 because

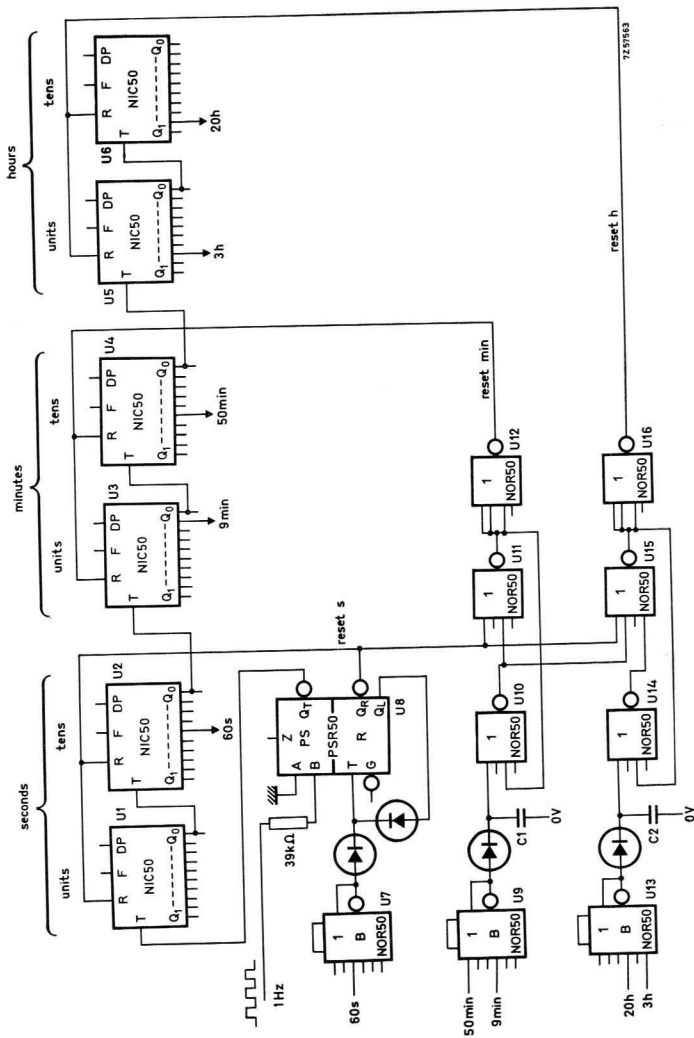


Fig. 14-11. Clock circuit. Capacitor $C_1 = C_2 = 3.9 \text{ nF}$.

NIC50 modules U_1 and U_2 have just registered 60 seconds. Memory (U_{10} — U_{11}) is not able to set, however, because NOR (U_{10}) output is still “1”. At the 60th minute, that is 59 minutes plus 60 seconds, another reset pulse is received at the other input to NOR (U_{11}) and NOR (U_{11}) output becomes “1”. NIC50 modules U_3 and U_4 are reset via NOR (U_{12}).

A similar reset method is used for the modules registering hours, NIC50s U_5 and U_6 . These modules are reset every 24 hours, i.e. 23 hours plus 59 minutes plus 60 seconds.

14.3.2 CLOCK WITH MANUAL SETTING FACILITY

This circuit has provision for manual setting with thumbwheel switches if, for example the supply should fail.

The circuit is shown in Fig. 14-12. A mains full-wave rectifier (not shown) delivers 100 Hz pulses to input B of the pulse-shaper section of PSR50 U_{13} (see Fig. 14-12*b* on p. 136). The trigger output Q_T delivers shaped 100 Hz pulses to input T of NIC50 (U_1). The four display counters U_1 — U_4 act as a frequency divider of 6000. At the 5999th pulse, all four inputs to Buffer NOR (U_{14}) go to “0”. The 6000th pulse causes B-NOR (U_{14}) output to return to “0” and this generates a negative-going reset pulse at Q_R and positive-going at Q_L from the reset section of PSR50 (U_{13}). (Terminal T is held at “1” level). The four NIC50 modules are thus reset to zero and the first pulse appears at input T of NIC50 (U_5) via PSR (U_{15}) and the “set time” push-button which is in the released (“normal”) position.

Further pulses appear at 1-minute intervals. NIC50 modules U_3 and U_4 actually indicate seconds. However, these modules were blocked off in the unit in Fig. 14-12, as they have little practical use and lead to needless complication in this case. (Units U_1 to U_4 can also be replaced by four DCD50 modules which perform the same function as the NIC50 modules but have no indicator tubes).

The NIC50 modules U_5 and U_6 register up to 59 minutes, at which time B-NOR (U_{16}) output goes “1”. It returns to “0” and thus resets NIC50 (U_5 , U_6) to zero at the 60th minute, similarly to the frequency divider of 6000. Output Q_0 of NIC50 (U_6) subsequently going from “1” to “0” triggers T of U_7 . Units U_7 and U_8 register up to 23 hours, operating similarly to NIC50 modules U_5 and U_6 .

The “set time” circuitry operates as follows. The time to be set is entered on the thumbwheel switches SU50 (U_9 and U_{10}) — units and tens

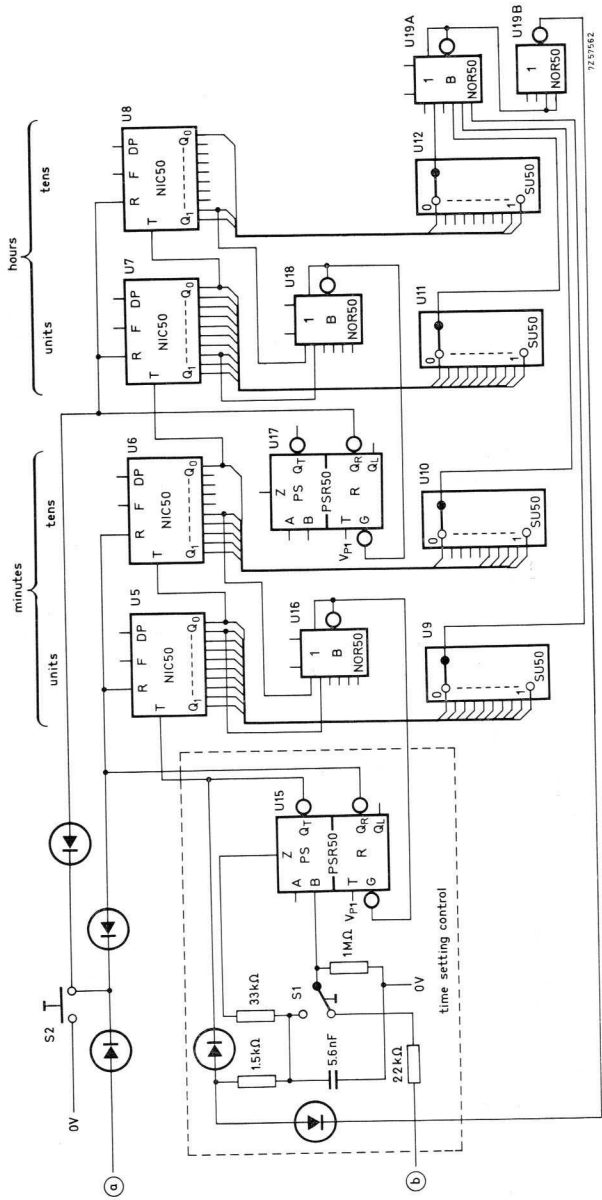


Fig. 14-12a. Clock circuit. Points a and b on this drawing correspond to those on Fig. 14-12b.

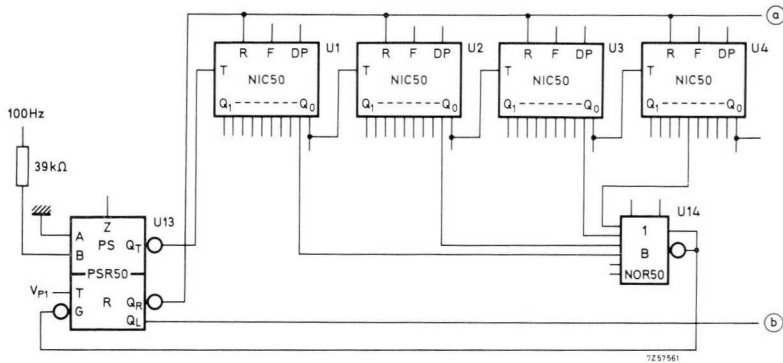


Fig. 14-12b

of minutes, and SU50 (U_{11} and U_{12}) — units and tens of hours. Upon pushing the “set time” push-button S_1 , the pulse-shaper section of U_{15} delivers an oscillating signal of approximately 50 kHz. This signal — enabling the 24 hours to be displayed in about 1 second — is inhibited when the counters NIC50 (U_5 to U_8) reach the preset time. All inputs to B-NOR ($U_{19}A$) are then “0”, its output is “1”, and NOR50 ($U_{19}B$) delivers “0” which is used to block the oscillator. The NIC50 modules will then read the preset time. No further changes occur until the push-button is released, at which normal operation is resumed. The “set zero” push-button facility (S_2) can be included if it is desired to measure elapsed time after an event. Depressing the push-button before the event applies “0” to all NIC50 reset “R” terminals and all NIC50 modules will display zero. Releasing the push-button at the event enables the units to resume counting.

14.4 Serial Insertion of Count Pulses

In some applications it is necessary to insert a pre-determined number of pulses into the counters before commencing normal counting. Fig. 14-13a shows how this can be achieved. NOR’s U_1 and U_2 and the pulse-shaper section of PSR50 form an oscillator. Before the preset count is reached input G_5 on NOR U_2 is “0”, and input G_{16} on NOR U_3 is “1”. Thus normal input pulses are inhibited and oscillator pulses will be fed into the counters. Upon reaching the preset count the Buffer NOR output goes “0/1” and sets the memory. This puts NOR U_2 input (G_5) to “1” and NOR

14.5 Insertion of Preset Numbers

14.5.1 SERIAL INSERTION OF A PRESET NUMBER

Certain applications of preset counting are best fulfilled by inserting a preset number into a reversible counter, and then subtracting down to zero, thus giving a fixed final position. Fig. 14-14 shows how the preset number is fed into T_F on the first RIC50, whilst the counting input is fed to T_R . The mode of operation is as follows.

NOR's U_1 and U_2 form a memory circuit. After an insert command the PSR50 oscillator starts, gate inputs C_F are opened and C_R inhibited. When the correct number is reached the Buffer NOR output goes to "1" level and sets the memory, which in turn stops the oscillator, and allows the reverse count input to function. In a multi-decade system two alternative approaches are possible. Firstly, the counters may be coupled in the normal manner, and the forward count inserted into the first decade, as above. This is the most economic solution, but can require quite a long insertion time for large numbers, e.g. 500 000 at 10 kHz maximum gives an insertion time of 50 seconds.

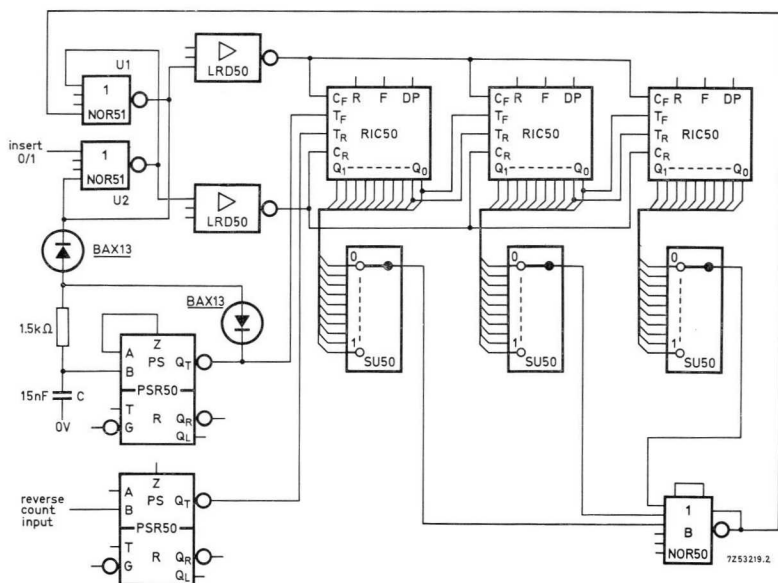


Fig. 14-14. Serial insertion of a preset number.

The second solution inserts pulses into each decade separately, and hence the maximum insertion time is 10 times the oscillator period, i.e. 1 ms at 10 kHz. This system is described in the next section.

14.5.2 PARALLEL INSERTION OF A PRESET NUMBER

Fig. 14-15 depicts a scheme for three decades. The memories are reset by push-button R , thus opening gate inputs C_F of the three RIC50 modules, and inhibiting the C_R inputs. The pulse generator formed from the PSR50 at the top of the figure now starts, due to the "1" level at D_1 . Pulses are then fed to all the T_F inputs and drive each RIC50 until its preset count is reached. The associated memory is then set, and the corresponding C_F input is inhibited. When all memories are set, all inputs to NOR U_1 becomes "0", and inputs C_R are brought to "0", thus enabling the input count pulses to drive the counters in the reverse direction (sequentially). The pulse generator can drive up to 6 decades. For details on how to increase the number of inputs to NOR U_1 see Section 13.3.1.

14.6 Count Position Detection

When using reversible counters it is often necessary to take action when the count goes above or below a preset number. Fig. 14-16 shows a circuit which signals these conditions. When supply is switched on, the whole system must be reset. NOR U_6 output goes to "1". At the preset count the Buffer NOR output goes to "1", and the output of NOR U_1 to "0". The output of NOR U_2 becomes "1" and hence NOR's U_5 and U_6 outputs become "0". Depending on which of the control inputs A or B is at "0" level, the memory formed by NOR's U_3 and U_4 will feed a "1" level to one of the two inputs of NOR's U_5 and U_6 . For example, if input A , the forward or adding input, is at "1", NOR U_5 output becomes "1", because NOR U_2 delivers a "0", as does NOR U_4 . If A remains at "1" while continuing to count forward NOR U_1 output goes "1" when the RIC50 modules move off the preset count and the memory output remains as before, because both memory inputs are now at "0".

14.7 Frequency Measuring Circuit

Fig. 14-17 shows the circuit diagram of a simple frequency or speed measuring circuit. Pulses of 50 Hz are fed to a two-decade counter system. (NIC50 modules are shown here to illustrate the operation, but as

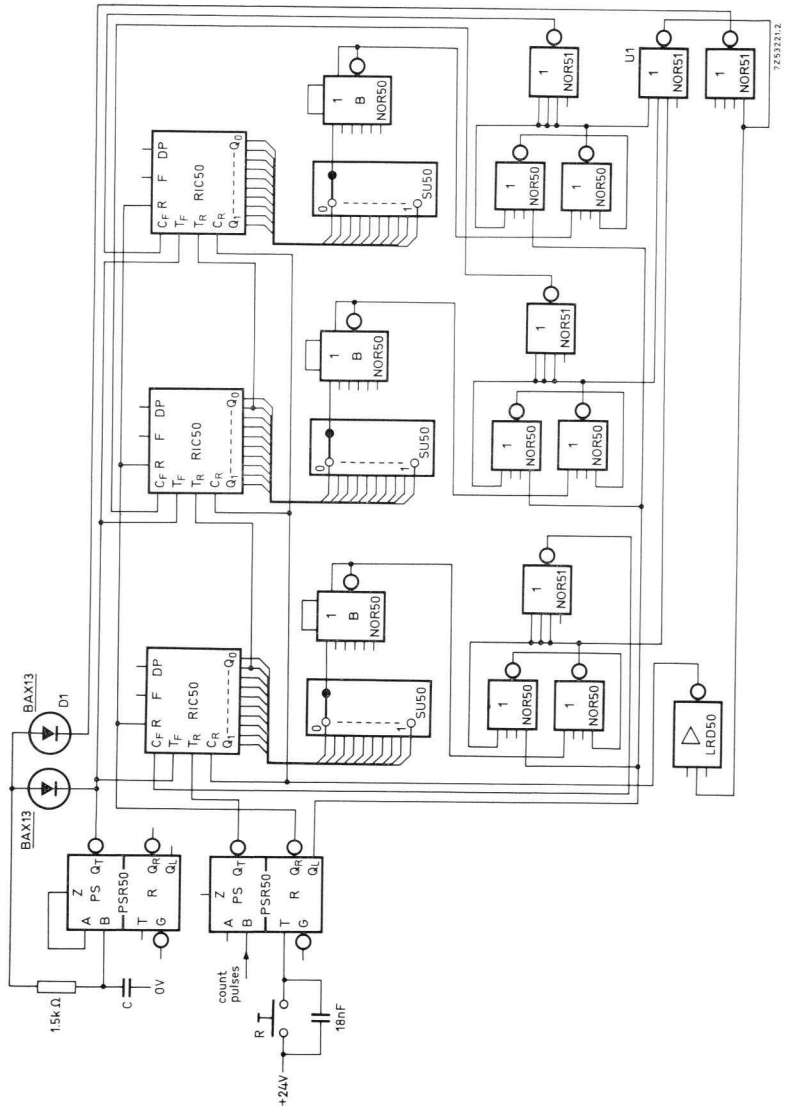


Fig. 14-15. Parallel insertion of a preset number.

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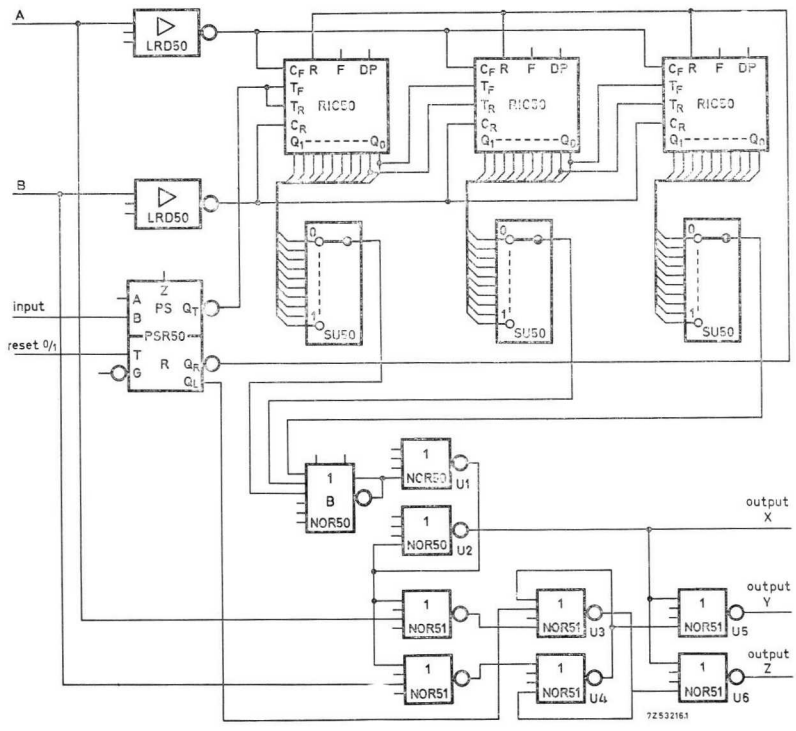


Fig. 14-16. Count position detection.

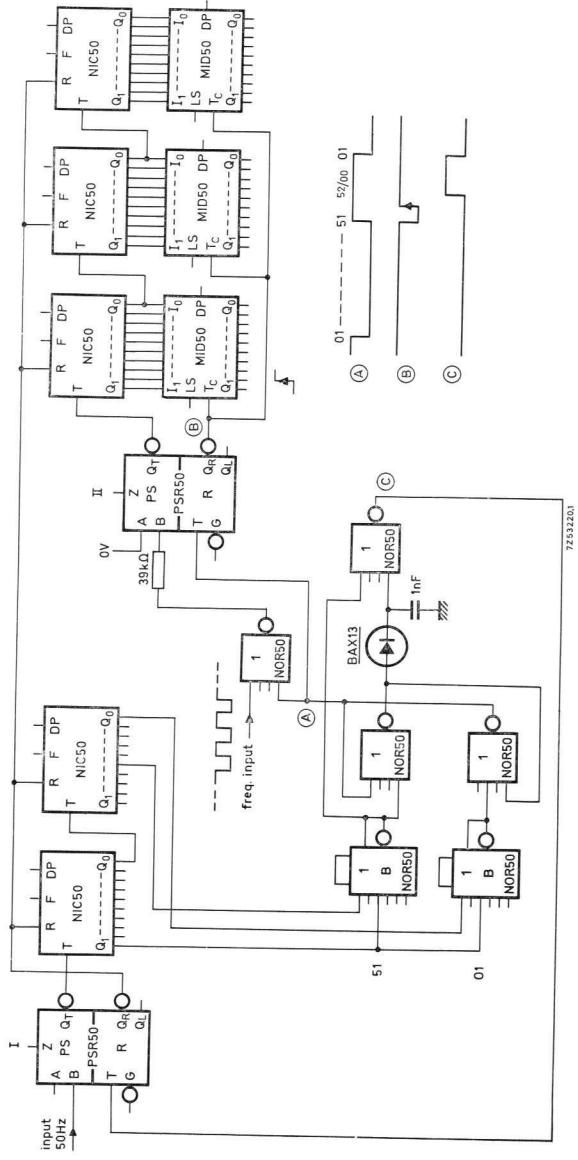


Fig. 14-17. Frequency measuring circuit.

the display is not necessary in this case the NIC50 modules can be replaced by DCD50 modules). Counting is designed to take place in the interval from 01 to 51 pulses, as this has been found to give the most economical solution in terms of components, and avoids resetting problems. It should be noted that when no input pulses are applied the input to NOR U_8 must be kept high.

At the count of 01 from the interval timer U_2-U_3 , Buffer NOR U_5 output goes to "1", setting the memory circuit NOR's U_6-U_7 . The output of U_7 goes to "0" which opens NOR U_8 . Frequency or speed measuring now takes place. After exactly 1 second i.e. at the 51st pulse from the interval timer, B-NOR U_4 output goes to "1" which resets the memory NOR U_6-U_7 . The "1" level output from U_7 inhibits the NOR-gate U_8 and at the same time triggers the reset section of PSR50 U_9 , producing a transfer pulse from output Q_R which is delivered to the MID50's. At the count of 52 from the interval timer, one of the inputs to B-NOR U_4 goes to "1", giving "0" levels at both the inputs of U_{10} . The "1" level output from U_{10} then resets the interval timer to 00 via PSR50 (U_1). The "0" level from B-NOR U_4 which resets the interval timer also produces a "1" level at the NOR U_6 output, and after a time-delay makes one of the NOR U_{10} inputs go to "1". The resulting "0" level output from NOR U_{10} removes the interval timer reset signal and allows another frequency or speed measurement to be made.

14.8 Automatic Bi-directional Revolution Counting

Counting the number of passes of an object and indicating direction of motion is a common requirement in practice. Fig. 14-18a shows the scheme of a circuit giving the basic requirement of "total revolutions" indication (total forward minus total reverse revolutions) and Fig. 14-18b that of a circuit giving, in addition, indication of the direction at a given instant. Input signals are supplied by a PHILIPS transducer type PE2270 (see Fig. 14-18c). A multiplier-by-4 increases the counting accuracy by raising the maximum pulse repetition frequency to 10 kHz. Counting direction of the RIC50 is controlled via two LRD50's by the direction discriminator. Fig. 14-19 shows the complete diagram; its operation is explained with the timing diagram of Fig. 14-20. Sign indication is provided by a SID50, and zero detection is carried out by a Buffer NOR.

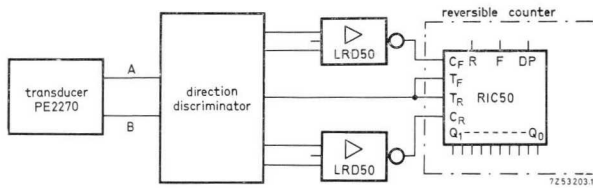


Fig. 14-18a. Revolution counter.

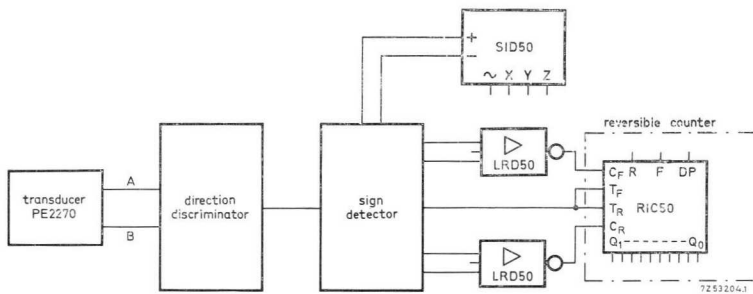


Fig. 14-18b. Revolution counter with indication of direction.

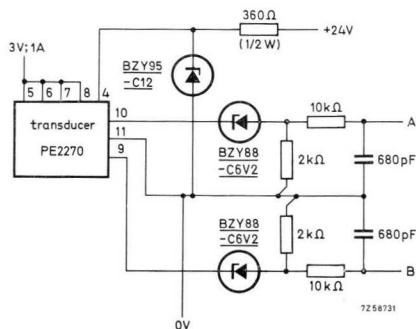


Fig. 14-18c. Input circuitry.

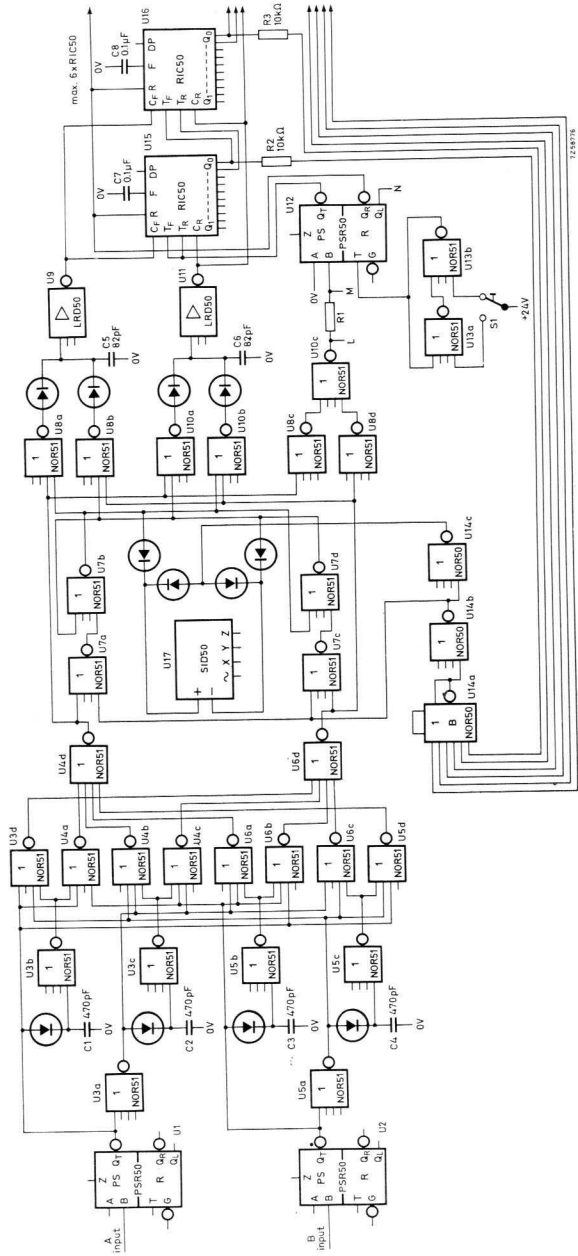


Fig. 14-19. Composite circuit diagram.

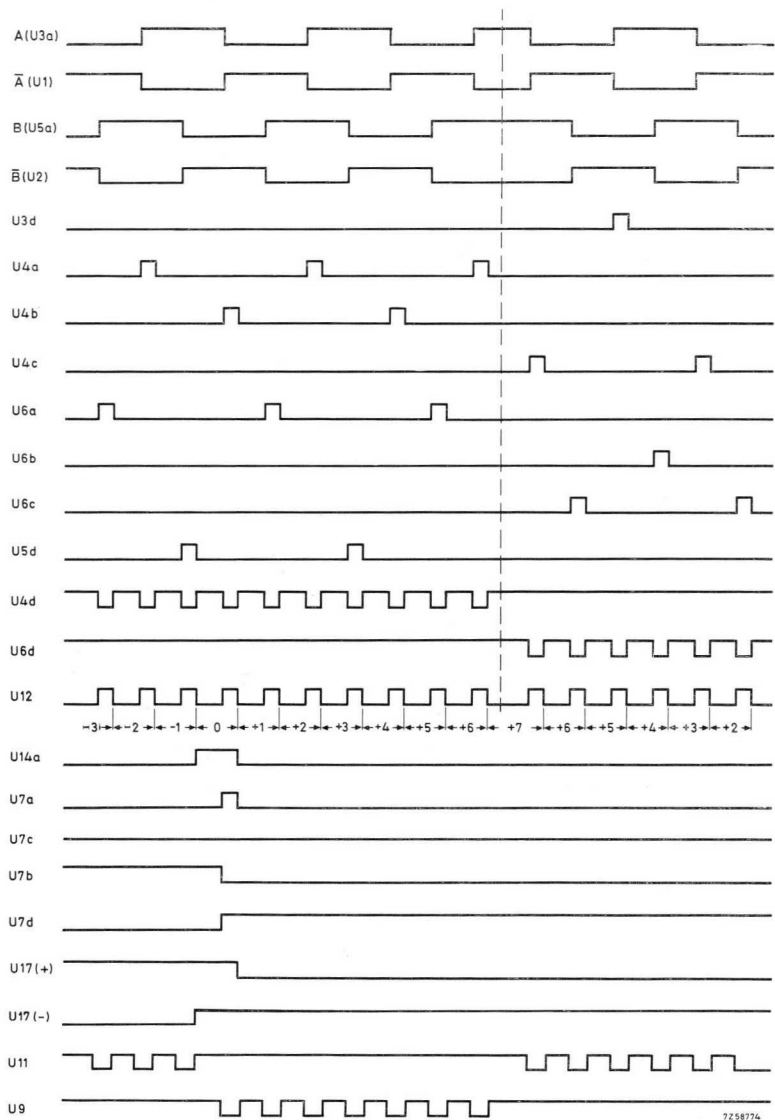


Fig. 14-20. Pulse diagram.

The alarm circuit of Fig. 14-21a may be used to give:

- a flashing signal when approaching the maximum p.r.f. that can be counted.
- a steady light indication when the maximum permissible p.r.f. has been exceeded i.e. when the contents of the counter no longer correspond with the input information.

The timing diagram of Fig. 14-21b shows the operation of the alarm circuit.

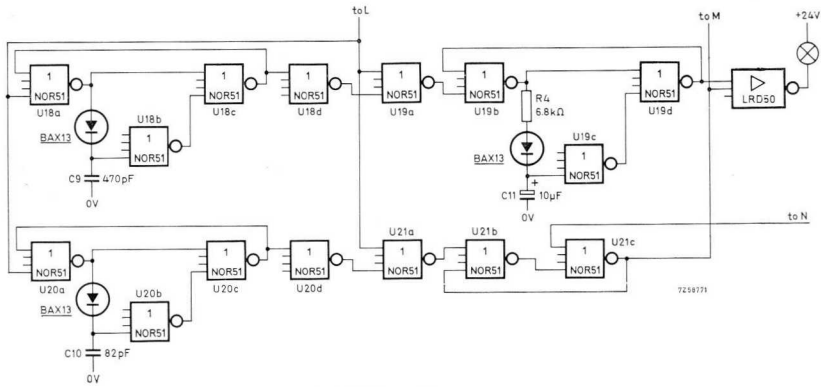


Fig. 14-21a. Alarm circuit.

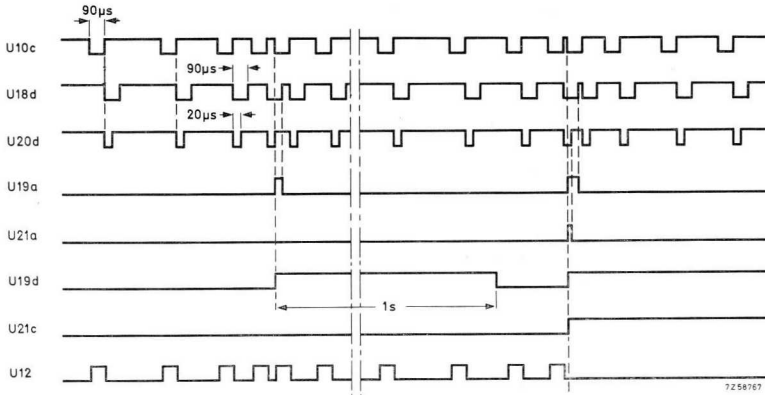


Fig. 14-21b. Pulse diagram.

14.9 Indication of difference between two independent pulse sources

Co-ordination between two independent processes requires a compensation procedure applied to one or both; the situation is encountered in, for example, attempting to keep horizontal a beam lifted by two cranes. The circuit of Fig. 14-22 provides a means of making this compensation by indicating the difference (positive or negative) between the number of pulses received from the two sources. Pulses of $10\ \mu\text{s}$ from the wave-shapers $U_1-U_2-U_3$ and $U_4-U_5-U_6$ set memories $U_{11}-U_{12}$ and $U_{14}-U_{15}$ respectively. Complementary pulse-trains from the 5 kHz pulse generator $U_7-U_8-U_9$ reset each memory alternately and simultaneously specify the counting direction by levels on the inputs C_R and C_F of the RIC50's. A low-going signal from the reset memory produces, via pulse circuit $U_{16}-U_{17}$ or $U_{18}-U_{19}$ an $80\ \mu\text{s}$ pulse at the trigger inputs of the RIC50's. The use of memory circuits reset by anti-phase signals means that simultaneous input signals will produce pulses $100\ \mu\text{s}$ apart at the RIC50 trigger input, thus ensuring unambiguous input conditions to the RIC50.

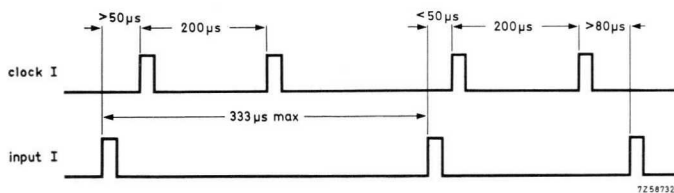


Fig. 14-22. Time relations of input signals.

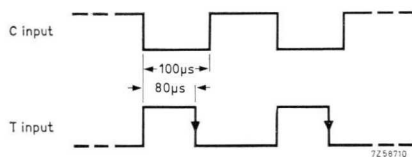


Fig. 14-22. Time relations between C and T inputs of RIC50.

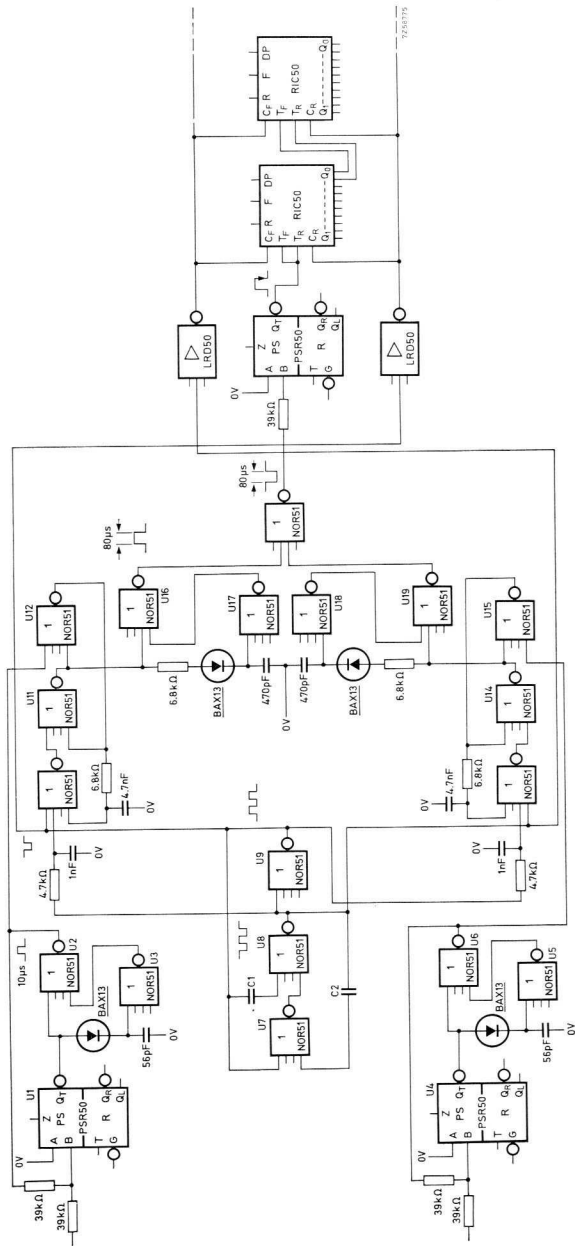
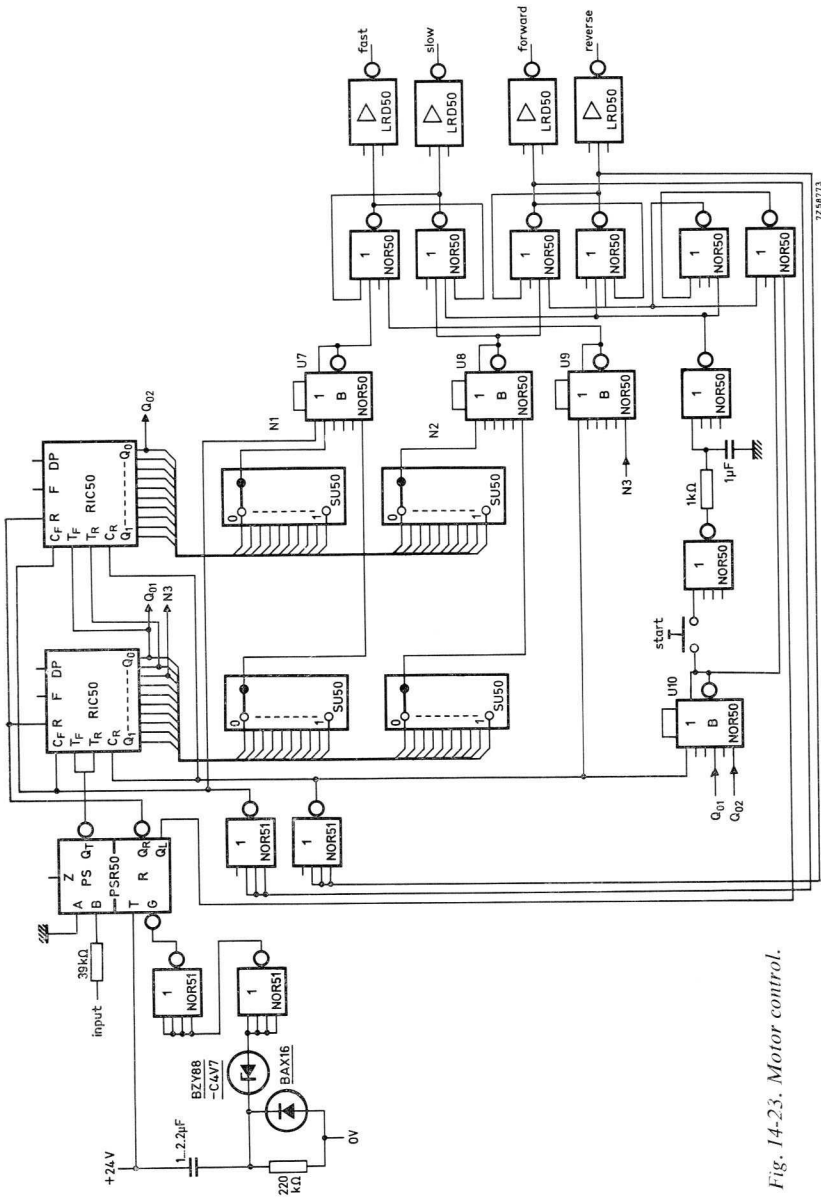


Fig. 14-22. Difference indication.

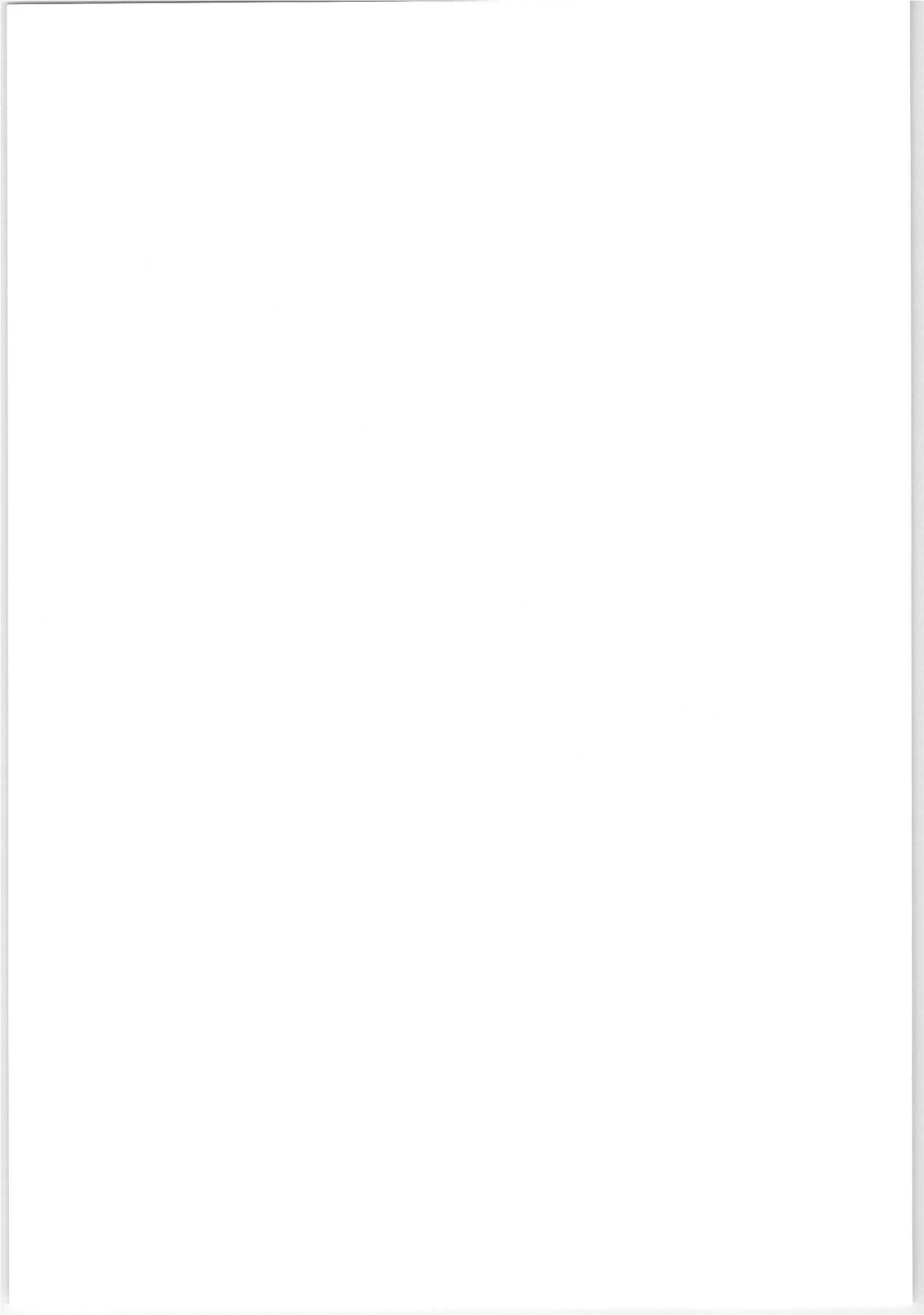
14.10 Automatic Motor Control

Fig. 14-23 shows a circuit designed to control the number of revolutions of a motor in both directions. Pulses from the motor revolution transducer are fed via a PSR50 to RIC50 counters. When the count N_1 (preset on SU50's) is reached, a "slow" command is given via U_7 . On reaching the preset count N_2 , a signal from U_8 stops the forward count, gives a "reverse direction" command and starts the reverse count. On reaching the preset count of N_3 a signal from U_9 gives a "slow" command, and at the count of 0, U_{10} stops the motor. A new cycle will commence on pressing the "Start" button.



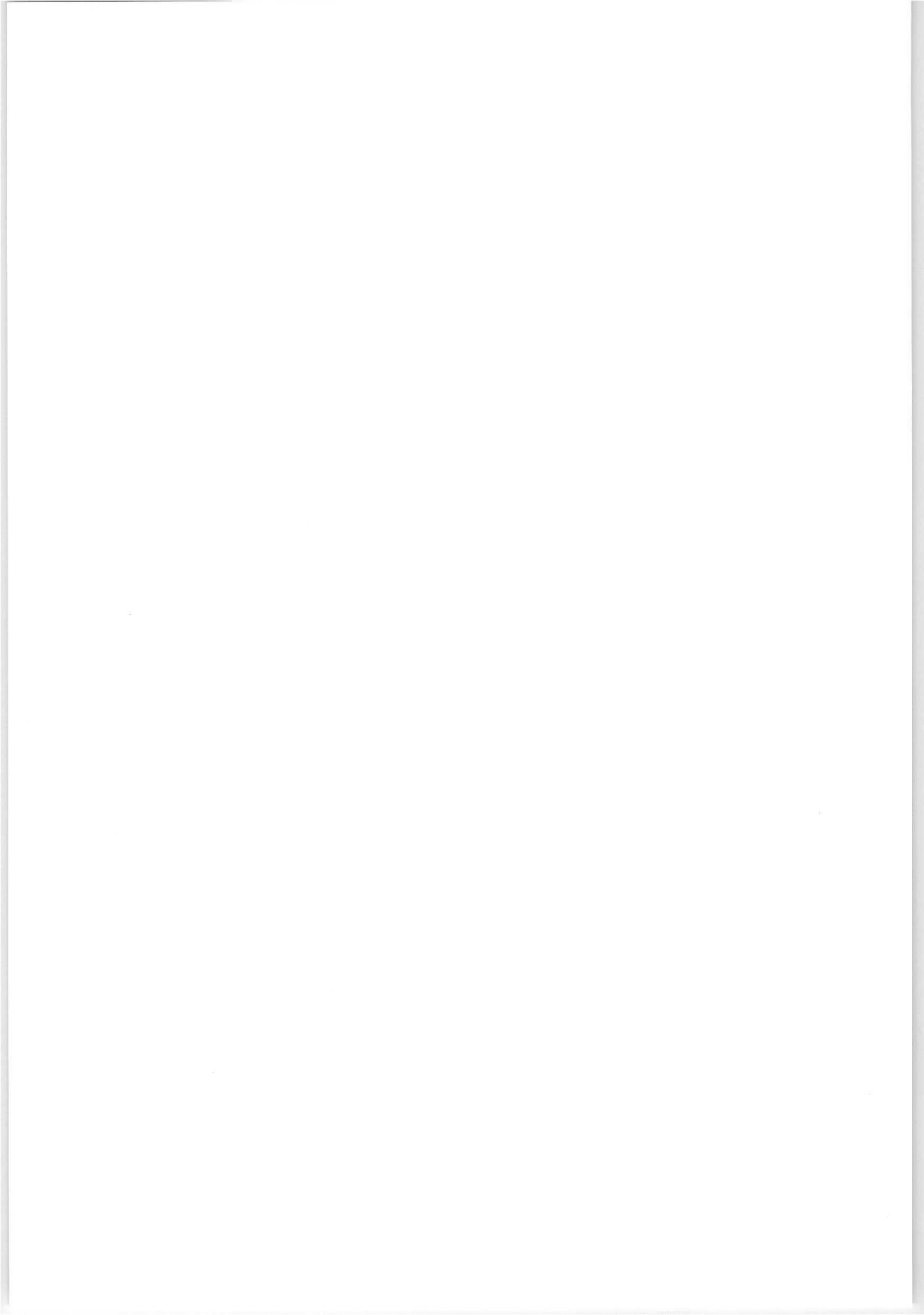
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Fig. 14-23. Motor control.



PART 3

Practical Considerations



15 Operating Speed

Pure counting systems will work at up to 50 kHz. However the introduction of preset outputs slows the maximum operating speed due to an intentional delay built into the Buffer NOR module. This is necessary to suppress spurious output pulses which could occur during the transition from, for example, 499-500 at the transit counts of 490 and 400, supposing that these had been selected as preset outputs.

This delay of maximum value 18 μs , is produced by connecting D_1 and D_2 (pins 9 and 10) on the 3.NOR50 module and it is recommended that this practice be observed whenever more than one NIC50 module is used.

This maximum value of 18 μs may be reduced to 5 μs by inserting a suitable capacitor between D_1 and D_2 (see Data Sheets).

The maximum time taken for the NIC50 module to step between numbers is 4 μs . Thus spurious signals to the Buffer NOR cannot last longer than this time, and as the Buffer NOR delay is longer the system will function safely. However, in a counting system longer delays occur due to counters switching in sequence when carry pulses are generated, e.g. in the transition from 99 to 100.

The maximum delay thus introduced will be $n \times 4 \mu\text{s}$ where n is the number of counter modules in the system. Assuming that the number to be decoded is the one immediately following this delay, the total delay introduced could be, worst case, $(4n + 18) \mu\text{s}$. Allowing $Z \mu\text{s}$ for the Buffer NOR output to switch further logic the complete delay introduced will be $(4n + 18 + Z) \mu\text{s}$ and the maximum operating speed:

$$\frac{10^6}{4n + 18 + Z} \text{ Hz.}$$

Thus for a worst case calculation for the circuit of Fig. 15-1 the maximum speed would be:

$$\frac{10^6}{12 + 18 + 12} \text{ Hz} = 23.8 \text{ kHz,}$$

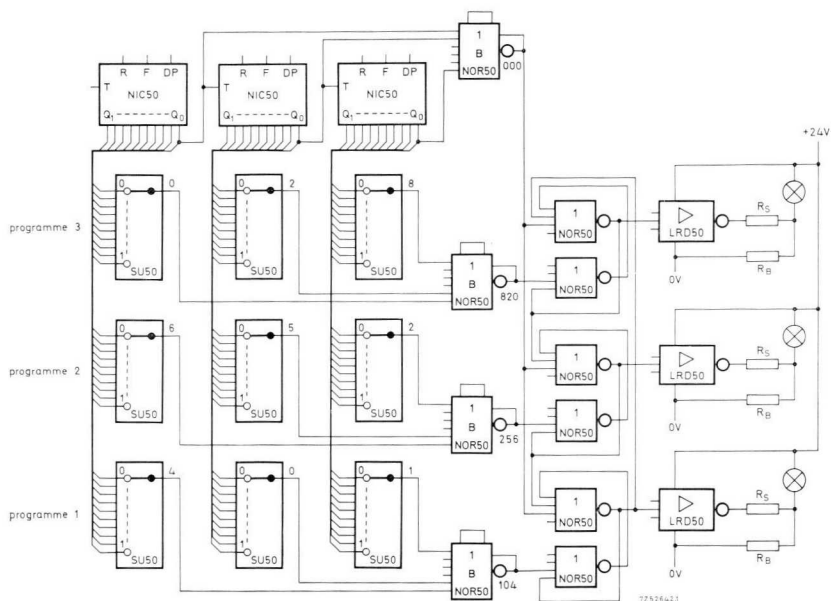


Fig. 15-1. Three-decade three-programme scheme.

and with a suitable capacitance between D_1 and D_2 :

$$\frac{10^6}{12 + 7 + 12} \text{ Hz} = 32.2 \text{ kHz.}$$

This calculation assumes worst case figures for all modules in the system but this is most unlikely to occur in practice. Typical values give the following operating speed:

$$\frac{10^6}{2n + 7 + Z} \text{ Hz} = \frac{10^6}{6 + 7 + 10} \text{ Hz} = 43.5 \text{ kHz.}$$

The addition of further logic as shown in Fig. 15-2 inhibits the spurious signals generated and hence the intentional delay of the Buffer NOR need not be used, i.e., D_1 not connected to D_2 , resulting in only a 4-9 μ s delay.

The operating speed in this case is typically:

$$\frac{10^6}{2n + 7 + Z} \text{ Hz} = \frac{10^6}{6 + 7 + 5} \text{ Hz} = 55.5 \text{ kHz.}$$

It is recommended however that D_1 and D_2 be always interconnected unless speeds in excess of 25 kHz are required.

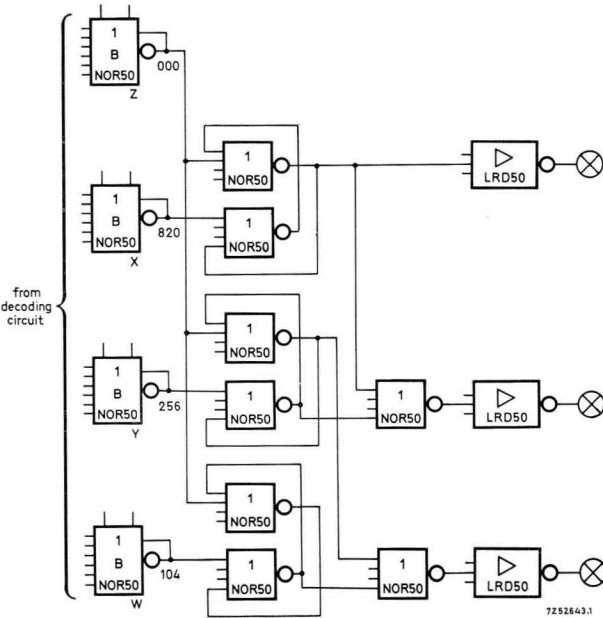
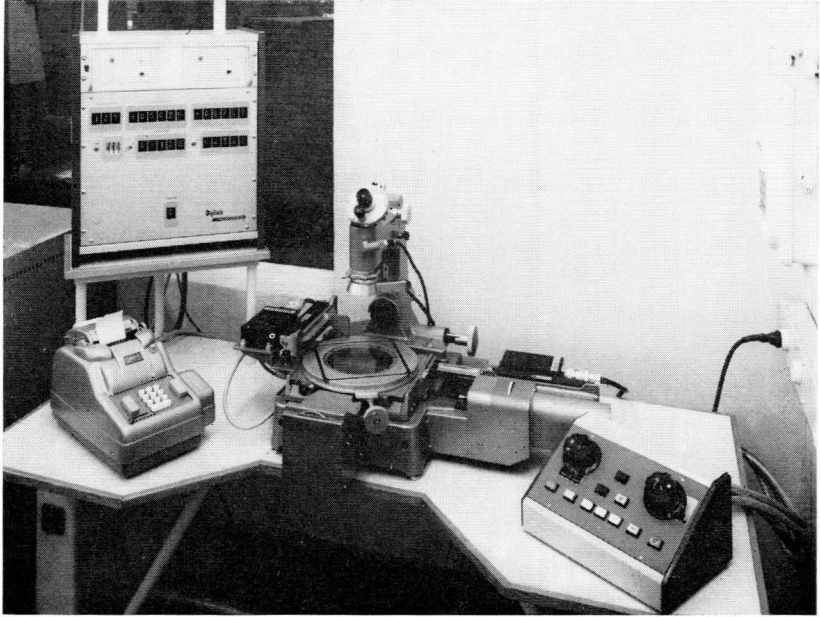


Fig. 15-2. Inhibiting the spurious signals in Fig. 15-1.



Industrial microscope

Automatic precision measuring system used in domestic appliance manufacture.

A counter/recorder with printer output linked to a microscope, form an automatic precision measuring system which carries out the following tasks more quickly and neatly than a team of operators and clerks could:

- measuring tool displacement accurately to 10 microns.*
- providing a direct display of the measured values.*
- printing-out these values.*

16 Loading Table

16.1 Rules governing Loading of the Modules

The loading table is actually a summary of the input and output data for the various modules of the 50-series.

By expressing the input requirements and output capabilities of most modules in "Drive Units" (D.U.), system design is greatly simplified.

The input requirements of all driven modules are additive. Therefore it is sufficient to examine whether the available output of a driving module can cover the input requirements of all driven modules.

The following rules should be followed when calculating loading.

- Add all input requirements;
- Follow the special input requirements which are mandatory for some modules;
- Where possible, input requirements and output capabilities are expressed in Drive Units (D.U.). A load requiring a certain number of D.U. can be driven by any module whose output has a greater or equal number of D.U. available.

Table 16-2

16.2 The Loading Table

type	function	input		output	
		terminal	required	terminal	available
NIC50	uni-directional direct display counter	R	to be driven from Q_R of PSR50	Q_0-Q_9	to drive $6 \times$ Buffer NOR's + $1 \times$ T-NIC50 + I_0-I_9 of $6 \times$ MID50 + PDU50
		T	to be driven from Q_T of PSR50 or Q_0-Q_9 of NIC50		
RIC50	bi-directional direct display counter	R	to be driven from Q_R of PSR50	Q_0-Q_9	to drive $6 \times$ Buffer NOR's + $1 \times$ T-RIC50 + I_0-I_9 of $6 \times$ MID50 + PDU50
		T_F/T_R	to be driven from Q_T of PSR50 or Q_0-Q_9 of RIC50	Q_0-Q_9	
		C_F/C_R	to be driven from Q of LRD50 or Q of NOR50/51 modules		
MID50	buffer memory with direct display	I_0-I_9	to be driven from Q_0-Q_9 of NIC50, RIC50 or MID50	Q_0-Q_9	to drive decimal input of PDU50 + I_0-I_9 of $3 \times$ MID50
		T_C	to be driven from Q_R or Q_T of PSR50		
SID50	driver plus and minus indicator tube	+ and - character	1 D.U.	none	not applicable
3.NOR50	6 input Buffer NOR dual 4 input NOR	G_1-G_6	to be driven from Q_0-Q_9 of NIC50 or RIC50	Q_1	2 D.U.
		G_7-G_{14}	1 D.U.	Q_2/Q_3	6 D.U.*
4.NOR51	quadruple input NOR	G_1-G_{16}	1 D.U.	Q_1-Q_4	6 D.U.*

PSR50	pulse shaper	B (via $R = 39 \text{ k}\Omega$)	2 D.U.	Q_T	$2 \times (T_R + T_F) - \text{RIC50} + 2 \text{ D.U.}$ or $4 \times \text{T-NIC50} + 2 \text{ D.U.}$ or $6 \times T_C\text{-MID50}$ or $6 \times \text{R-NIC50/RIC50}$ or $6 \times T_C\text{-MID50}$ 4 D.U.
	reset	T G	1 D.U. 1 D.U.	Q_R Q_L	
LRD50	lamp/relay driver	$G_1\text{-}G_3$	1 D.U.	Q	300 mA, 30 V (abs. max.) or $6 \times C_F/C_R\text{-RIC50}$
PDU50A	printer drive unit	$I_0\text{-}I_9$ L	to be driven from $Q_0\text{-}Q_9$ of NIC50, RIC50 or MID50 to be driven from $L_1\text{-}L_3$ of PDU50B	$Q_0\text{-}Q_9$	2 D.U.
PDU50B	printer drive unit	C $S_1\text{-}S_3$	to be driven from: — Q_T of PSR50 or — NOR module ** to be driven from: — $Q_0\text{-}Q_9$ of NIC50 or RIC50 — DCD50 — NOR module **	$L_1\text{-}L_3$	to drive input L of PDU50A
DCD50	decade counter and divider	$T_A/T_C/T_D$ T_{B1}/T_{B2} S C_S	0 D.U. 1 D.U. 1.5 D.U. 6 D.U.	$Q_A, \overline{Q}_A, \overline{Q}_B, \overline{Q}_C, \overline{Q}_D$ $Q_B, \overline{Q}_C, \overline{Q}_C, \overline{Q}_D$ Q_D, \overline{Q}_D $Q_A, \overline{Q}_B, \overline{Q}_B$ Q_C, \overline{Q}_C $\overline{Q}_A, \overline{Q}_D, \overline{Q}_D$	to drive $1 \times \text{T-NIC50/RIC50}$ } 6 D.U. + $1 \times \text{T-DCD50}$ or } 4 D.U. + $1 \times \text{B-PSR50}$ see data sheet

* also suitable to drive two times C_F or C_R of RIC50
 ** two inputs in parallel or one input always floating

16.3 Examples

16.3.1 NOR FUNCTION DRIVING $2 \times$ NOR50 PLUS $1 \times$ LRD50 (FIG. 16-1)

Available at terminal Q of NOR50:	6 D.U.
Required at terminal G , NOR50:	1 D.U.
G , NOR50:	1 D.U.
G , LRD50:	1 D.U.
Total required:	3 D.U.
Reserve :	+3 D.U.
This is allowed.	

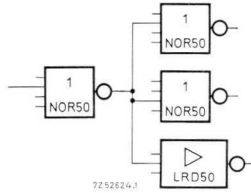


Fig. 16-1. Logic circuit.

16.3.2 PSR50 DRIVING $3 \times$ NOR51 PLUS $2 \times$ NIC50 (FIG. 16-2a)

Available at terminal Q_T of PSR50:	2 D.U. + $4 \times T$ of NIC50
Required at terminal G , NOR51:	1 D.U.
G , NOR51:	1 D.U.
G , NOR51:	1 D.U.
Total required:	3 D.U. + $2 \times T$ of NIC50
Reserve :	-1 D.U. + $2 \times T$ of NIC50
This is not allowed.	

Fig. 16-2b shows an allowable arrangement using two extra NOR functions.

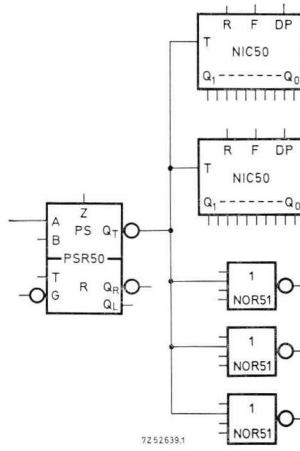


Fig. 16-2a. Counting and logic.

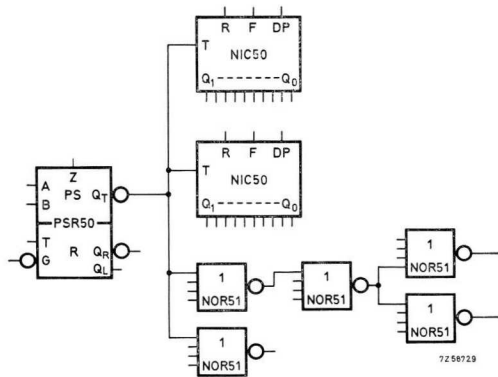


Fig. 16-2b.

16.3.3 PSR50 DRIVING $8 \times$ NIC50 PLUS $4 \times$ NOR51 (FIG. 16-3)

Available at terminal Q_R of PSR50: $6 \times R$ of NIC50

Required at 8 terminal R of NIC50: $8 \times R$ of NIC50

This is not allowed. A second PSR50 must be paralleled with the first in order to reset $8 \times$ NIC50 modules.

Available at terminal Q_L of PSR50: 4 D.U.

Required at 4 NOR INPUTS : 4 D.U.

This is allowed.

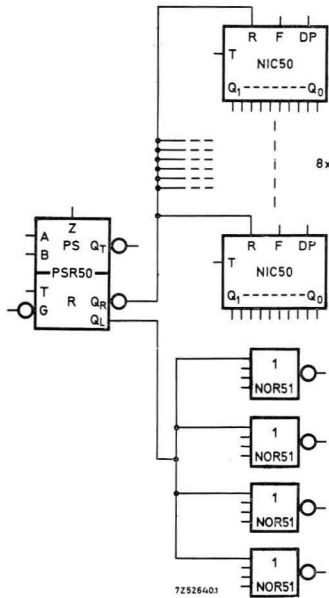


Fig. 16-3. Counting and logic.

16.3.4 LRD50 DRIVING THE RIC50 (FIG. 16-4)

Available at term. Q of each LRD50 : $6 \times C_F(C_R)$ inputs.

Required from terminal Q of each LRD50: $4 \times C_F(C_R)$ inputs.

This is allowed.

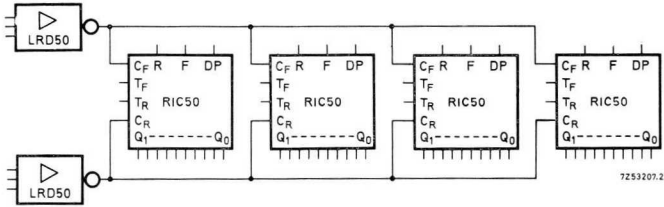


Fig. 16-4. Control of reversible counter.

16.3.5 NIC50 DRIVING 7 PROGRAMMES (FIG. 16-5)

- Available at Q_o of NIC50 : $6 \times B-NOR50 + 1 \times T-NIC50$
- Required for counter trigger drive: $1 \times T-NIC50$
- Required for Buffer NOR drive : $7 \times B-NOR50$

This is not allowed, therefore the number of preset programmes must be limited to six. For more than 6 programmes see chapter 13.6.3.

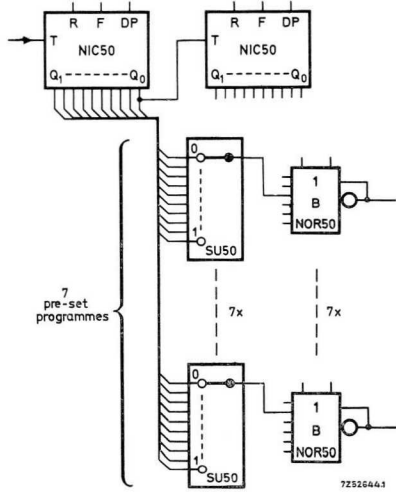


Fig. 16-5. Counting with preset outputs.

16.3.6 RIC50 DRIVING MID50 (FIG. 16-6)

Available from each RIC50 output: $6 \times$ Buffer NOR's + $1 \times$ T-RIC50
 + (I_0 to I_9) of $6 \times$ MID50 +
 $1 \times$ PDU50

Required from each RIC50 output: $6 \times$ Buffer NOR's + $1 \times$ T-RIC50
 + (I_0 to I_9) of $1 \times$ MID50

This is allowed.

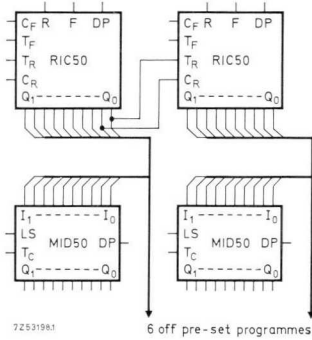


Fig. 16-6. Storage with MID50.

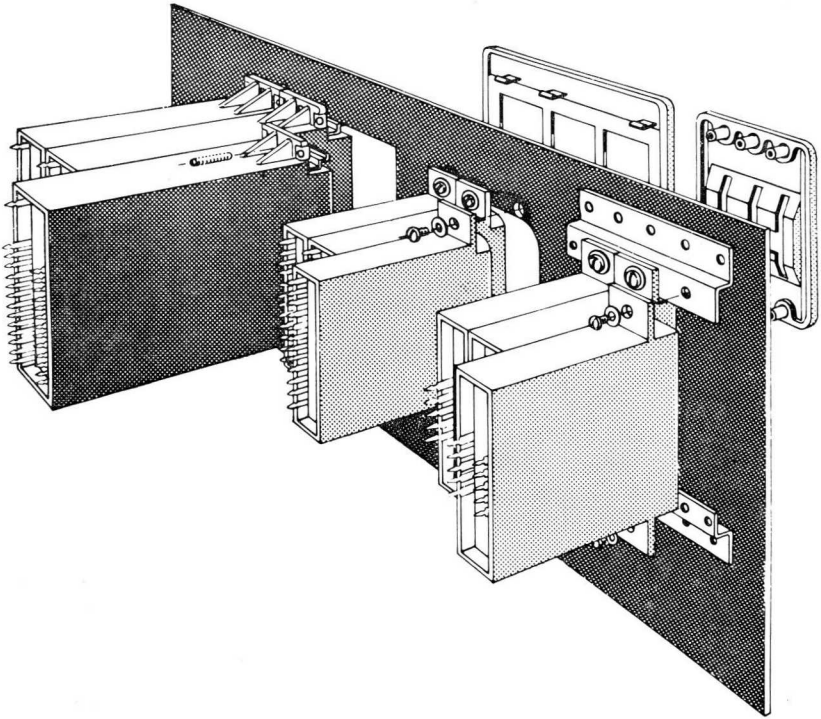


Fig. 17. Exploded view (from the rear) of a typical 3-decade/single-programme system. (Left) NIC50 display units. (Centre) preset switches. (Right) logic units.

17 General Installation Requirements

17.1 Mounting Details

17.1.1 THE INDICATOR MODULES NIC50, RIC50, MID50 AND SID50

The modules are housed in plastic cases, whose dimensions and terminal locations are shown in Fig. 17-1. The dimensions in Fig. 17-1 are given in mm; for inch values see the tables.

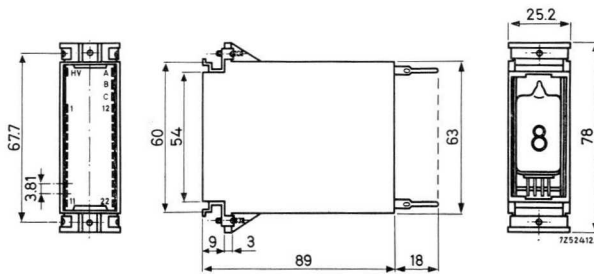


Fig. 17-1. Dimensions of indicator modules.

mm	inches
3	0.118
3.81	0.150
9	0.354
18	0.708
25.2	0.992
54	2.126

mm	inches
60	2.362
63	2.480
67.7	2.665
78	3.070
89	3.504

These modules are fixed to the panel by means of two screws butting against the rear face (see Fig. 17-2). A simple rectangular cut-out is required, whose dimensions in mm and inches are given in Table 17.1.

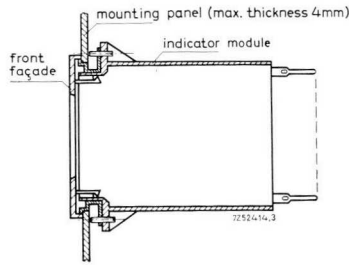
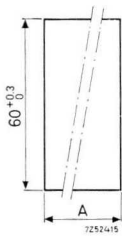


Fig. 17-2. Panel mounting.

Table 17.1 Panel cut-out.



number of modules	width <i>A</i>	
	mm	inches
1	25.4 + 0.5	1 + 0.02
2	50.8 + 0.5	2 + 0.02
3	76.2 + 0.5	3 + 0.02
4	101.6 + 0.5	4 + 0.02
5	127.0 + 0.5	5 + 0.02
6	152.4 + 0.5	6 + 0.02

The front façade clips into the main body. Front façades are available in single and multiple sizes up to a maximum of size 6 (see section 19.4). If the front façade is not required the modules may be mounted as shown in Fig. 17-3.

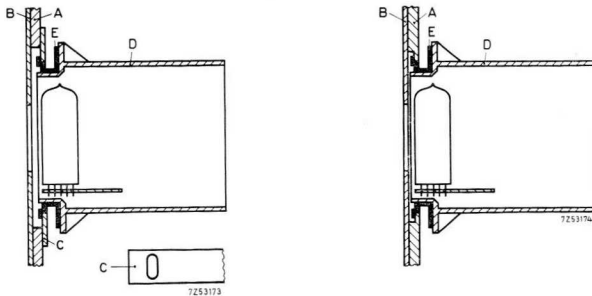


Fig. 17-3. Two methods of mounting the modules (if front façade is not required).
A — mounting panel; *B* — text panel; *C* — auxiliary mounting strips; *D* — housing;
E — metal mounting bracket.

The modules may be installed using the following procedure. They should firstly be secured with the clips provided, such that the screws are only finger-tight. The appropriate façade may then be fitted and the screws tightened without using force. If the façade is not now flush with the panel, the spacing between the modules may need to be increased. Finally, the façades should be checked for alignment. To make any adjustments the façade must be removed.

17.1.2 THE AUXILIARY MODULES 3NOR50, 4NOR51, PSR50, LRD50, PDU50 A AND B AND DCD50

Module dimensions and terminal locations are shown in Fig. 17-4. Dimensions are given in mm; for inch values see the tables.

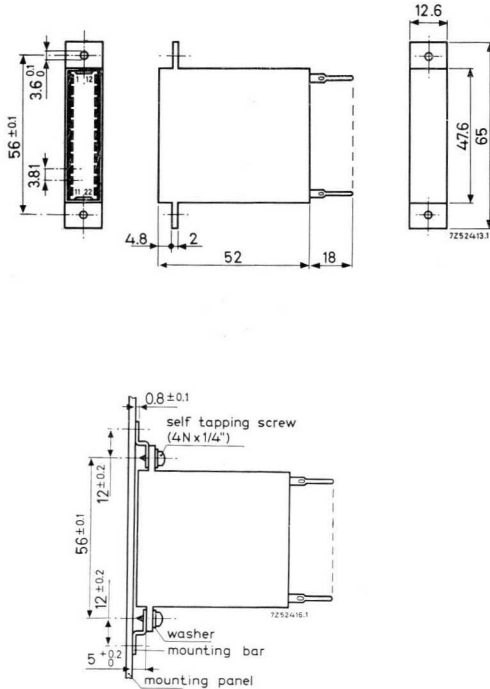


Fig. 17-4. Dimensions of auxiliary modules.

mm	inches
2	0.078
3.6 ^{0.1} ₀	0.142 ^{0.004} ₀
3.81	0.150
4.8	0.189
12.6	0.496
mm	inches
18	0.708
47.6	1.874
52	2.047
56 ± 0.1	2.205 ± 0.004
65	2.559

These modules may be fixed to the same panel as the other modules or remotely using Mounting Bar type MB50 (see Fig. 17-5, and section 19.3).

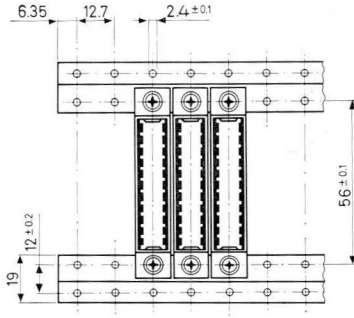


Fig. 17-5. Mounting Bar.

7252417

17.1.3 THE SWITCH UNIT SU50

Dimensions and terminal location of this unit are shown in Fig. 17-6. Dimensions are given in mm; for inch values see the tables.

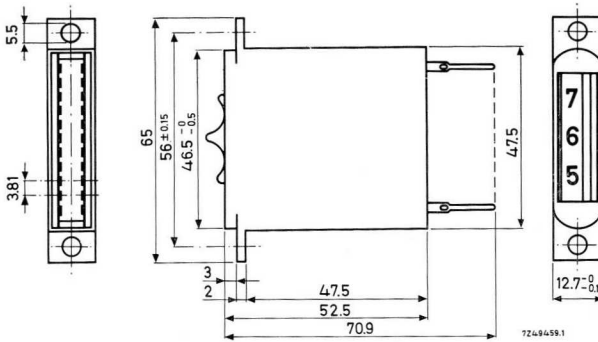


Fig. 17-6. Dimensions of thumbwheel switch.

mm	inches	mm	inches
2	0.078	46.5 ⁻⁰ ₋₀₅	1.831 ⁻⁰ _{-0.02}
3	0.118	47.5	1.870
3.81	0.150	52.5	2.067
5.5	0.216	56 ± 0.15	2.205 ± 0.006
12.7 ⁻⁰ _{-0.1}	0.5 ⁻⁰ _{-0.004}	65	2.559
		70.9	2.791

This module requires a panel cut-out as shown in Fig. 17-7. Dimensions are given in mm; for inch values see the table.

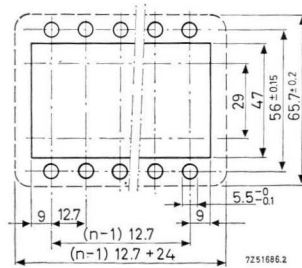


Fig. 17-7. Panel cut-out.

mm	inches
5.5 ⁻⁰ _{-0.1}	0.216 ⁻⁰ _{-0.004}
9	0.354
12.7	0.5
24	0.945
29	1.142
47	1.851
56 ± 0.15	2.205 ± 0.004
65.7 ± 0.2	2.587 ± 0.008

The main housing butts against the back of the panel. Self-tapping screws which are provided pass through the panel and screw into bosses on the rear of the façade, as shown in Fig. 17-8.

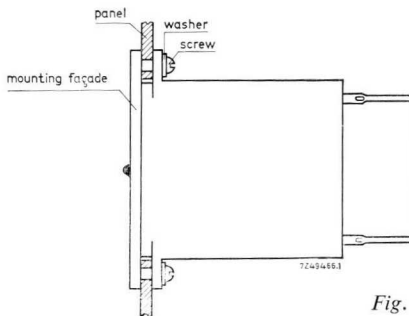
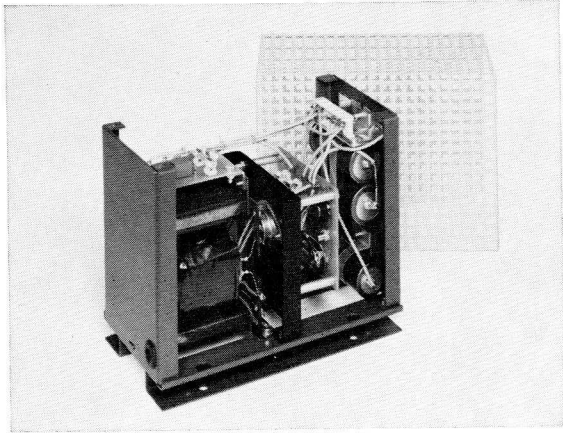


Fig. 17-8. Panel mounting.



Power supply unit.

17.1.4 THE POWER SUPPLY MODULE PSU50

Terminal locations and terminal spacing dimensions are shown in Fig. 17-9; mounting hole spacing and unit dimensions are shown in Fig. 17-10.

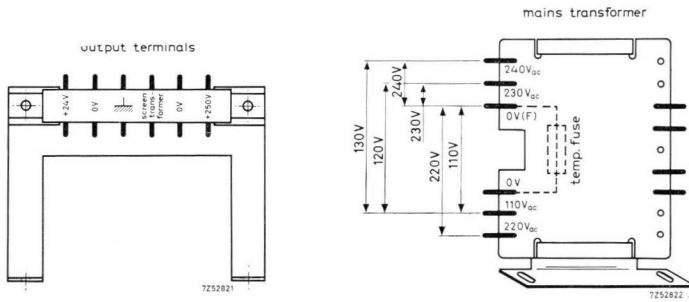


Fig. 17-9. Transformer connections and output terminal locations.

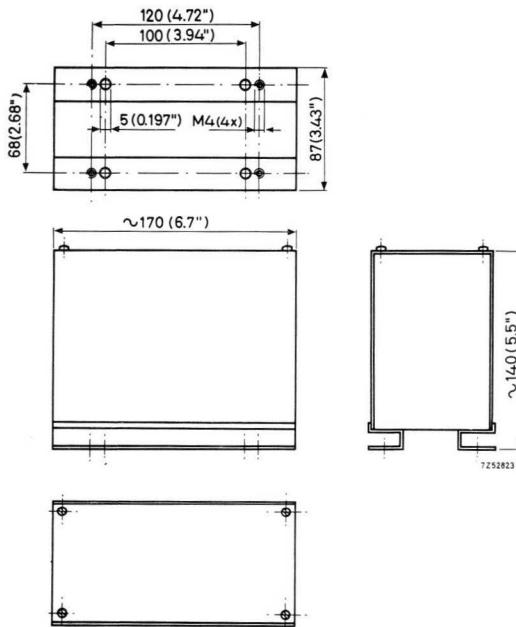


Fig. 17-10. Mounting details.

17.2 Interwiring Considerations

17.2.1 TYPICAL INTERWIRING PATTERNS

Consistency of pin function and careful pin layout makes interwiring between units straightforward. For example, logic supplies always use pins 1 and 2 (with the exception of the LRD50), allowing straight busbar connections, and logic interconnections are frequently between adjacent pins. Thus a Buffer NOR driving a memory would need interconnections as in Fig. 17-11.

Fig. 17-12 shows the interwiring pattern of a three decade counter with preceding PSR50.

Fig. 17-11. Typical interwiring pattern — Buffer NOR driving a memory.

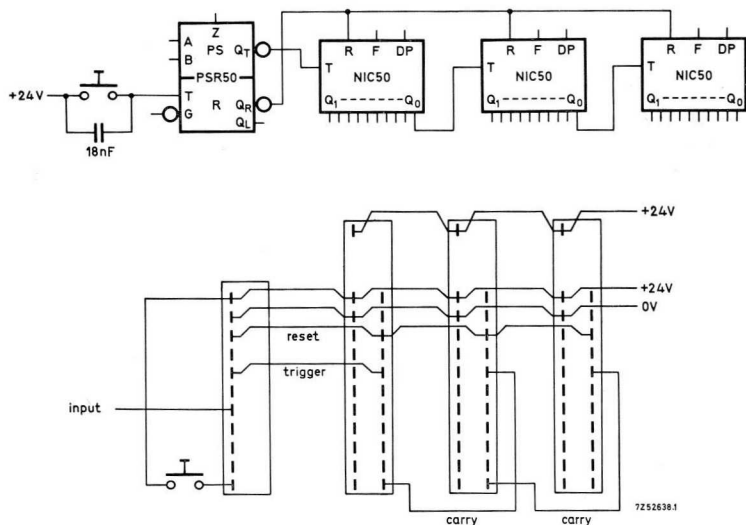
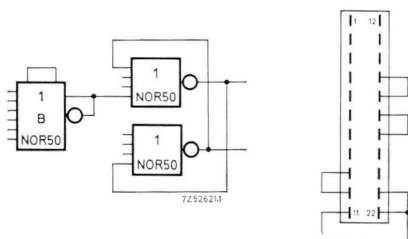


Fig. 17-12. Typical interwiring pattern — 3-decade counter plus PSR50.

Note that the display units have an additional 250 V connection (V_{P3}) placed well away from other pins. Care must be taken that this V_{P3} connection does not touch other pins as damage will inevitably result.

17.2.2 WIRE-WRAP DETAILS

All terminal connections in the 50-series can be made with the Wire-wrap* process. This section gives a description of the process, and tool types required for various wire gauges.

Pin dimensions are given in Fig. 17-13.

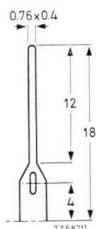


Fig. 17-13. Pin dimensions.

Wire-Wrap Connections

A wrapped joint consists of a sharp-edged usually rectangular terminal around which an electrical wire is secured by a number of close fitting turns. This number depends on the wire size which is used (minimum 8 turns for 30 gauge wire). The action of wrapping the wire round the terminal applies a hoop stress to the wire, the reaction to which is a torsional force on the terminal. This results in the sharp corners of the terminal biting into the wire producing gastight joints which withstand severe environmental conditions. Two versions are distinguished (see figure 17-14).

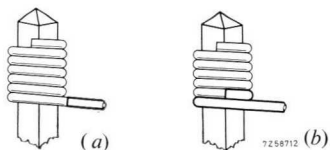


Fig. 17-14. Terminal types.

* Wire-wrap is a registered product of Gardner-Denver Pty.

- (a) The conventional type where the wrapping consists entirely of non-insulated wire.
- (b) The modified type where (min.) 1 turn is insulated and the remainder of the wrapping is non-insulated.

The size of the terminals varies as a rule with the thickness of the wire.

Advantages:

- The spacing of the terminals may be close
- The reliability of a wrapped connection is extremely high; the estimate is 10 times that of a soldered connection.
- The influence of human factors is small, provided adequate tools are used.
- The time and cost involved in making a wrapped connection is less than with a soldered connection.

Disadvantages:

- Automatic wrapping-machines are very costly.
- The wrapping method is not suitable for stranded wire.
- Mechanically testing a wrapped connection is destructive.

Necessary Equipment

Table 17-2 gives the type numbers of the Gardner-Denver tools required for various wire sizes.

Remarks:

- Each 50-series wire-wrap terminal can contain three wraps, consisting of 6 turns per wrap;
- The use of modified wraps is recommended for all types.

Table 17-2

pin dimensions		wire Ø			max. Ø isolation		type numbers of tools from Gradner-Denver		
mm	inches	A.W.G.	S.W.G.	mm	inches	mm	inches	modified wrap	standard wrap
0.76 ×	0.030 ×	30	33	0.25	0.0100	0.5842	0.023	507063	500353 ¹⁾
0.4	0.016	28	30	0.32	0.0126	0.9144	0.036	501389 ¹⁾	507100
		26	28	0.40	0.0159	0.8382	0.033	506445 ²⁾	508748
		24	25	0.508	0.0201	—	—	505415	505279
								502129	—

¹⁾ Special care is required with the wrapping tool in order to avoid overwrapping

²⁾ Bit 506445 only for PTFE/PVC wire to maximum isolation Ø 0.864 mm

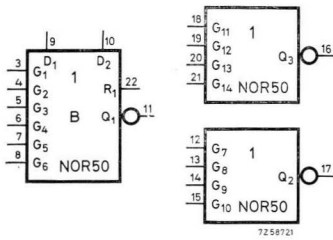
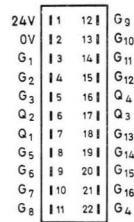
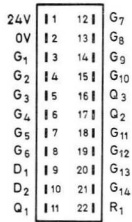


Fig. 17-19. 3NOR50.

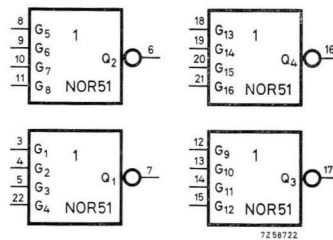


Fig. 17-20. 4NOR51.

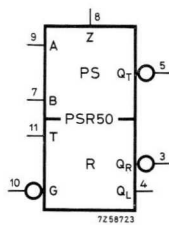
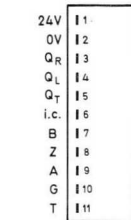


Fig. 17-21. PSR50.

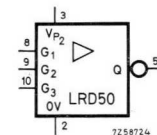
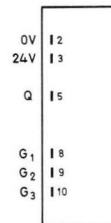


Fig. 17-22. LRD50.

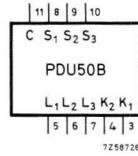
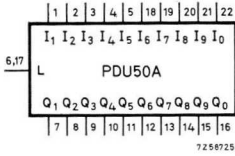
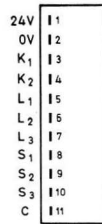
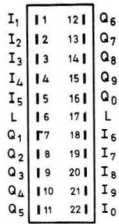


Fig. 17-23. PDU50A.

Fig. 17-24. PDU50B.

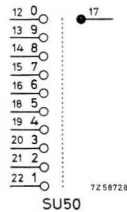
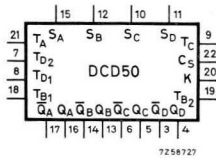
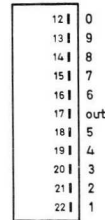
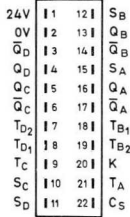


Fig. 17-25. DCD50.

Fig. 17-26. SU50.

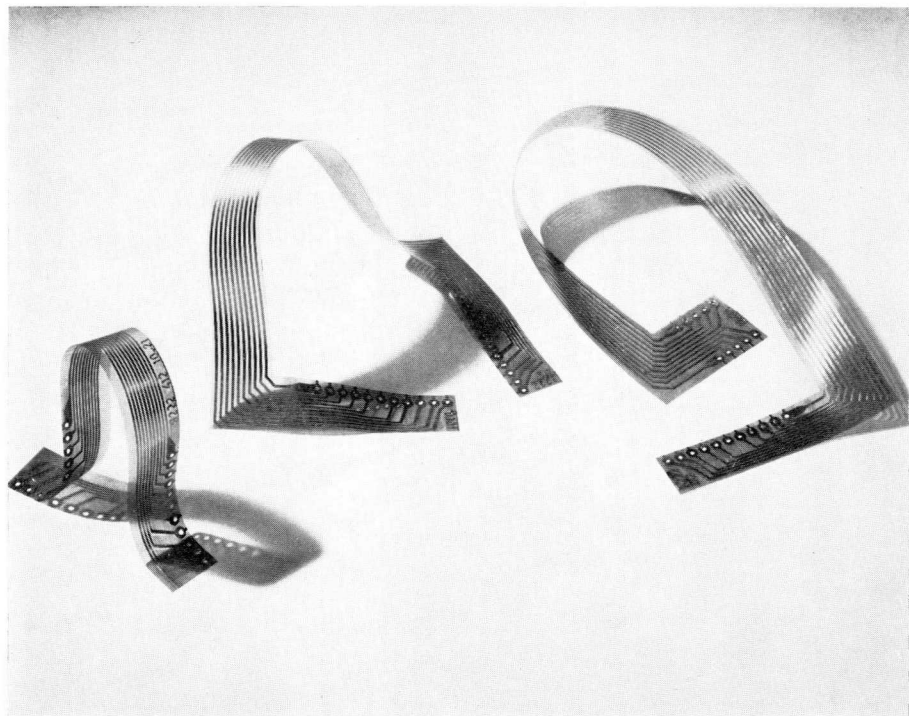


Fig. 17-27. Examples of flexible prints. The following types are available:

Type VSS50 — for interconnecting thumbwheel switches 10PIC in various programmes, when mounted vertically.

Type HCS50 — for interconnecting ten outputs of NIC50 or RIC50 to the ten inputs of thumbwheel switches 10PIC, when mounted horizontally.

Type HSS50 — for interconnecting thumbwheel switches 10PIC in various programmes, when mounted horizontally.

Type VCS50 — for interconnecting ten outputs of NIC50 or RIC50 to the ten inputs of thumbwheel switches, when mounted vertically.

18 General Electrical Considerations

18.1 Introduction

Two supply rails are needed, namely $+250\text{ V d.c.} \pm 18\%$ for indicator tubes and $+24\text{ V d.c.} \pm 10\%$ for logic units. PSU50, which supplies 40 and 250 mA respectively at these voltages, is adequate for many systems as it will supply twelve counting display units and supporting logic. It is advisable to provide a separate $+24\text{ V} \pm 25\%$ supply of suitable current rating for the output devices. Experience has shown that the use of a separate load supply minimises interference problems and avoids swings on the logic supply; this practice is therefore recommended. Interconnections between supplies are shown in Fig. 18-1.

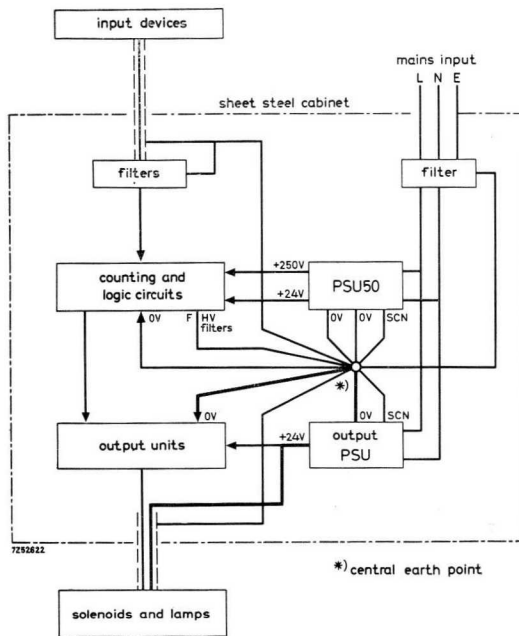


Fig. 18-1. Typical system supply and earthing connections.

18.2 Precautions against Interference

18.2.1 GENERAL

The 50-series direct display counters have been developed for application in the professional industrial field. This becomes evident after an appraisal is made of their main characteristics, such as supply voltages, counting rate, temperature range and the mechanical design of units and their mounting arrangements.

Most important, the 50-series design incorporates a high degree of protection against interference. Moreover, the 50-Series operates at the comparatively high supply voltage of 24 V, which has allowed extra protection against interference. These two qualities distinguish the 50-Series from other currently available counter ranges.

In spite of the precautions to assure trouble-free operation in environments with heavy interference, it should be realized that transistorized circuits are not completely immune. Noise pulses with amplitudes of 100 V, or even 1000 V, are by no means exceptional in industrial environments, and therefore additional protection measures might be necessary. If these measures are taken right at the start of design, they are neither costly nor time-consuming.

In general, interference signals enter a system by direct electro-magnetic radiation in the system, by induction in the cables between input devices and the system, and through the mains supply. Extensive testing and analysis has provided ways of eliminating interference from the above sources, and the knowledge thus gained is given in a number of recommendations, grouped according to the severity of the interference. (The numbers in the drawings Figs 18-2 and 18-3 refer to the recommendations listed.) The recommendations given in the first grouping ("Normal Precautions") should always be carried out, no matter what the situation may be. The user of the 50-Series, by considering his specific application and circumstances, can then easily find out what precautions are most applicable to his case. With these recommendations, we are convinced that the 50-series direct display counters will operate reliably under all circumstances of interference normally encountered in industry.

18.2.2 NORMAL INTERFERENCE PRECAUTIONS

- a. The equipment should be built into a closed metal cabinet. The cabinet must be connected to mains earth (E) at the point of cable entry.
- b. All 0 V points of the various system parts should be connected to a single Central Earth Point (CEP) by thick leads, which should be kept as short as possible. The CEP should be situated close to all units and be kept insulated, at that place, from the metal equipment cabinet.
- c. The CEP is to be connected by only one lead to the point where the metal equipment cabinet is interconnected with mains earth (E).
- d. Keep incoming and outgoing power leads inside the cabinet as short as possible.
- e. Leads with high voltages or switching currents must be separated from the logic lines.
- f. The constituent parts of the equipment must be mounted as close as possible to each other and interwiring should be kept as short as possible.
- g. Use a mains filter (see Sub-section 18.2.6). In Fig. 18-3 the mains filter case is electrically separated from the C_1 - C_2 interconnection and this interconnection is brought to the CEP. If, however, the filter is of a type having the case already internally connected to the C_1 - C_2 interconnection, then the case must be insulated from the metal equipment cabinet, and connected to the CEP instead.
- h. Mains switches, fuses, mains indication lamps, etc. must be inserted either in the filtered mains leads between mains filter and power supply unit, or housed in a separate metal case preceding the filter.

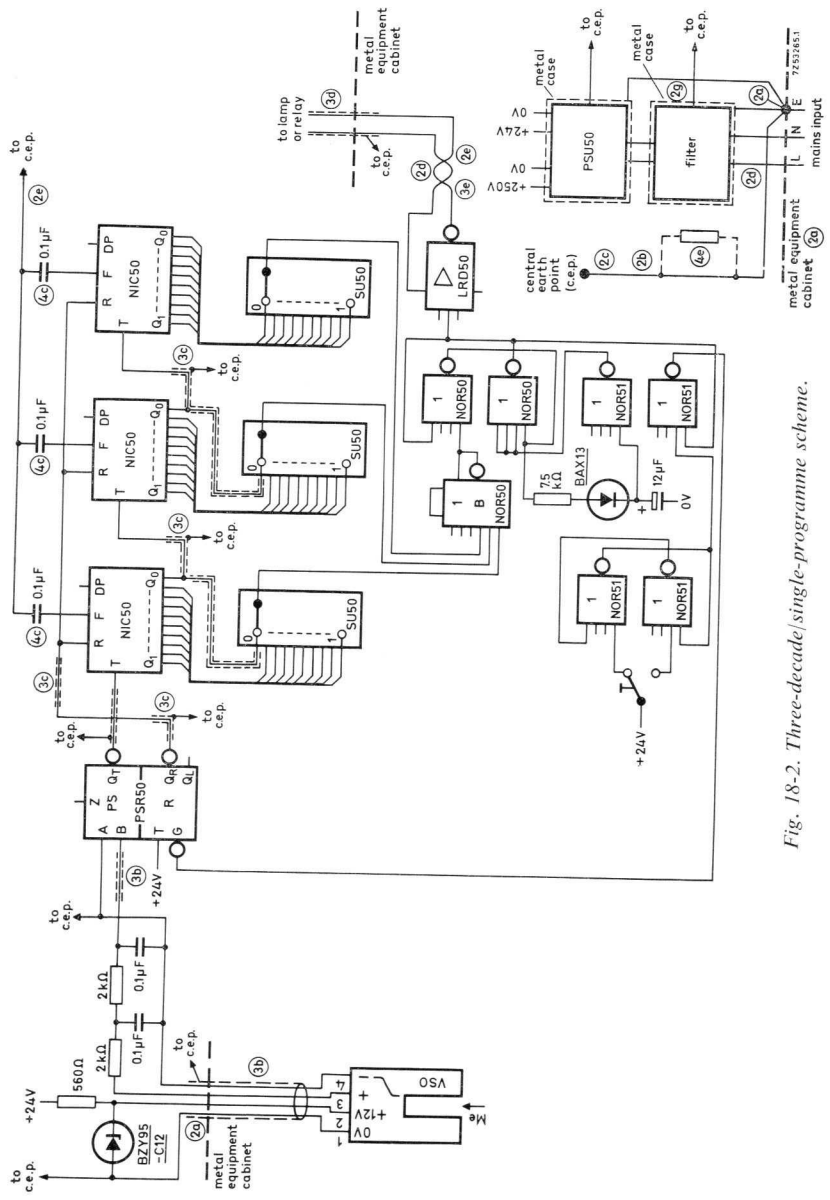


Fig. 18-2. Three-decade single-programme scheme.

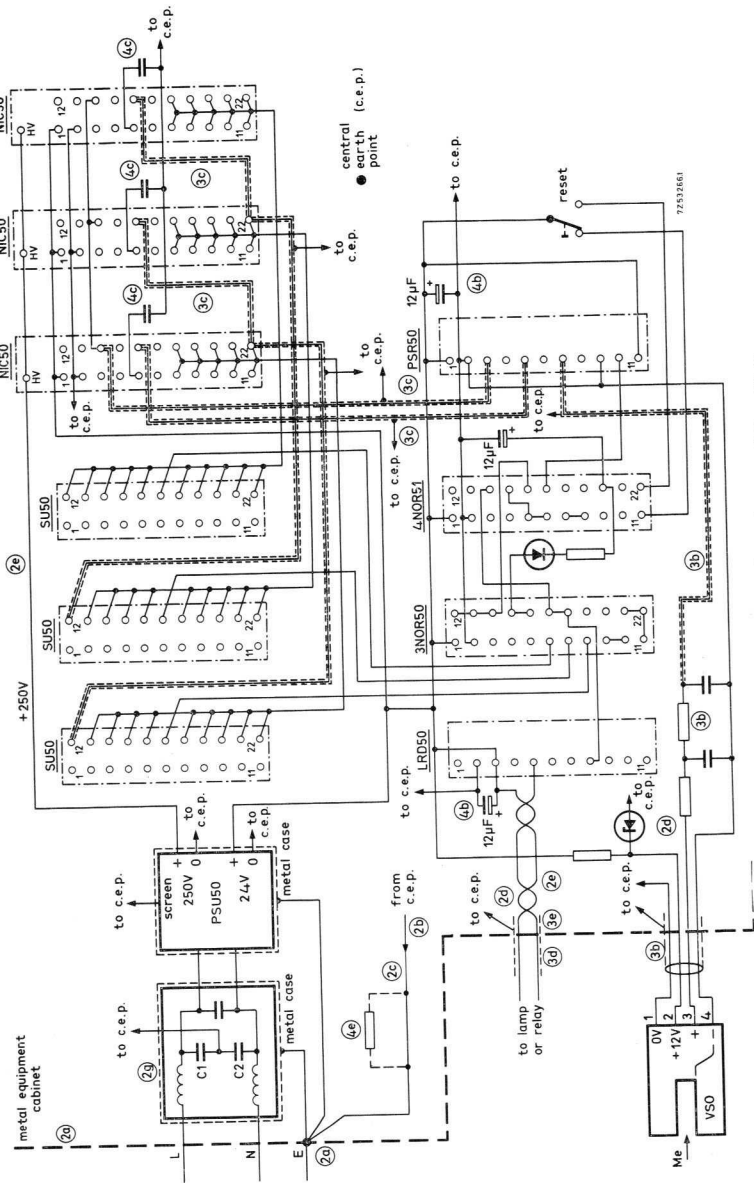


Fig. 18-3. Wiring details for scheme of Fig. 18-2.

18.2.3 HIGH INTERFERENCE PRECAUTIONS

- a. All recommendations stated under 18.2.2 should be observed.
- b. Leads from input transducers are to be screened outside the cabinet and filtered immediately after entering the cabinet. Only the signal line should also be screened after filtering inside the cabinet.
- c. The Trigger and Reset lines between PSR50 modules and counters must be screened.
- d. Outgoing leads from output power units should be screened outside the metal cabinet, particularly if:
 - no separate 24 V power supply is used for the output power units,
or
 - the output power units are mounted close to the logic circuits.
- e. Outgoing leads from output power units should be twisted inside the metal cabinet.

18.2.4 EXTREME INTERFERENCE PRECAUTIONS

- a. All recommendations stated under 18.2.2 and 18.2.3 should be observed.
- b. Connect small electrolytic capacitors between the +24 V and 0 V terminals of the PSR50. This should also be done with the LRD50, if a separate power supply unit is not used.
- c. Connect capacitors of 0.1 μF between terminal *F* of the counters and the CEP.
- d. A filter similar to the mains filter must be inserted in the outgoing leads of the power output units inside the equipment cabinet. See also 18.2.3b. Screening of the leads outside the cabinet is not necessary when the filter is used.
- e. Under certain circumstances, improvement may be realized by inserting a resistor, value between 1 and 10 $\text{k}\Omega$, between CEP and mains earth *E*, or even allowing CEP to float with respect to mains earth *E*.

18.2.5 TEST METHODS

To demonstrate the immunity of the 50-series counters to extreme interference, a simple counter has been built.

Figs 18-2 and 18-3 show the circuit diagram and associated interwiring diagram, respectively, of the equipment — a simple 3-digit, single preset programmed counter. With the precautions shown in the diagrams, this equipment operates reliably while being subjected to the high electric and magnetic fields produced by the tests described below. These test conditions are the severest to which electronic counters are normally exposed, even in heavy industry. Although the precautions taken were very simple and cheap, they were extremely effective.

WARNING: The brilliant fire-work display produced by the first three tests should be warning enough that high currents and voltages exist. This is dangerous —

TAKE THE APPROPRIATE PRECAUTIONS!

Very strong magnetic fields are produced in test 4, as you can see for yourself by placing a steel key in the coil. *Watches and sensitive instruments should be kept well away from the coil!*

Equipment used for the tests:

- a capacitor 50 μ F (min.) 250 V r.m.s.,
- a coil 120 turns, coil diam. 51.5 cm, wire diam. 1.6 mm, total coil resistance 0.5 Ω ,
- a push-button switch,
- two relays 36 A rating,
- a rough file,
- some hook-up wire.

Test 1 (Fig. 18-4)

Strike the end of wire *A* over the neutral lead, the earth terminal and the earth lead connected to the counter chassis.

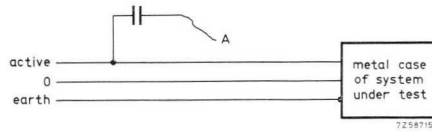


Fig. 18-4. Interference tests 1 and 2.

Test 2

As in test 1, but with the coil and capacitor in series.

Test 3 (Fig. 18-5)

Stroke the active terminal over a file as shown in Figs 18-5a and 18-5b.

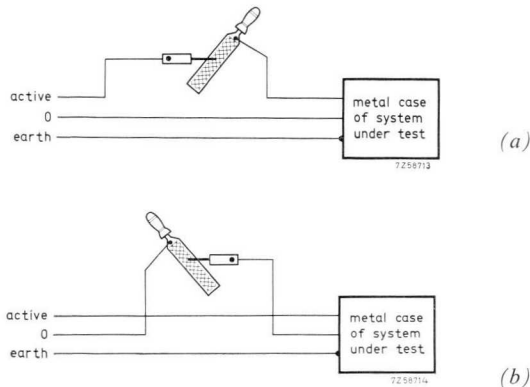


Fig. 18-5a, b. Interference test 3.

Test 4 (Fig. 18-6)

On closing contact *A*, relay *B* is activated and, after 10–20 ms, relay *C* is de-activated. During this period a current of $220/0.5 = 440$ A flows, giving a magnetic flux of $440 \times 120 = 50,000$ AT. Test both with the coil placed close to the equipment, and with the coil magnetically coupled with coiled input and output leads.

A slow-blow 10 A fuse is sufficient provided tests are made not more frequently than one every $\frac{1}{2}$ - 1 s.

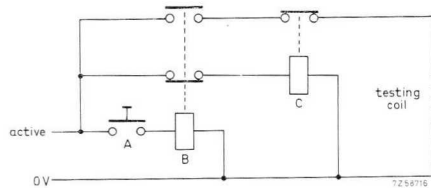


Fig. 18-6. Interference test 4.

18.2.6 MAINS FILTERS

Even away from high-interference environments, mains supplies are seldom free from transients and noise. This type of interference is effectively reduced by the use of a mains filter.

Mains Filter MF0.5A

The MF0.5A is rated at 0.5 A. It reduces the amplitude of interference voltages by more than 50 dB between 100 kHz and 10 MHz (see graph Fig. 18-7). The unit is shown in Fig. 18-8 and its dimensions given in Fig. 18-9.



Mains filter 0.5 A.

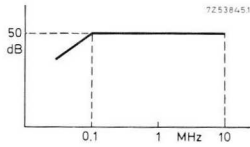


Fig. 18-7. Attenuation graph.

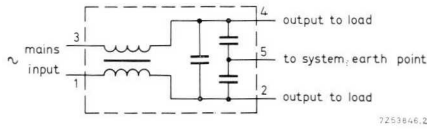


Fig. 18-8. Circuit diagram.

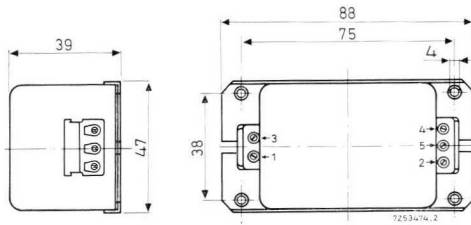


Fig. 18-9. Filter dimensions.

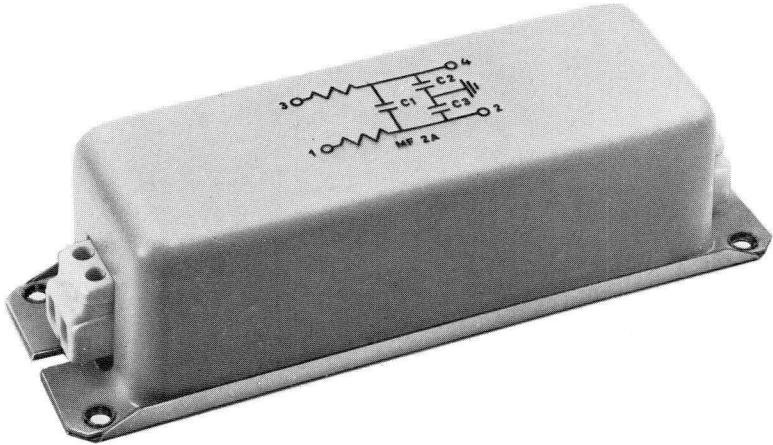
Technical Data

Maximum current	0.5 A
Maximum voltage	250 V
Test voltage	2 kV for 1 min.
Attenuation	
(for input frequencies between 100 kHz and 10 MHz)	> 50 dB
Temperature range	
operating	-25 to +70 °C
storage	-40 to +80 °C
Weight	250 g

Mains Filter MF 2.0 A

The MF 2.0 A is rated at 2 A. It reduces the amplitude of interference voltages by more than 50 dB between 300 kHz and 15 MHz (see graph of Fig. 18-10).

Dimensions of the unit are shown in Fig. 18-11.



Mains Filter 2.0 A

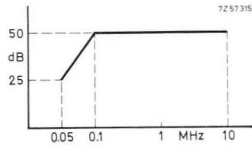


Fig. 18-10. Attenuation graph.

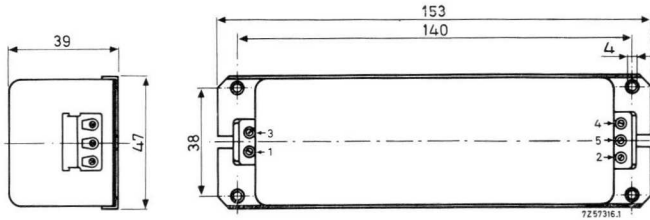
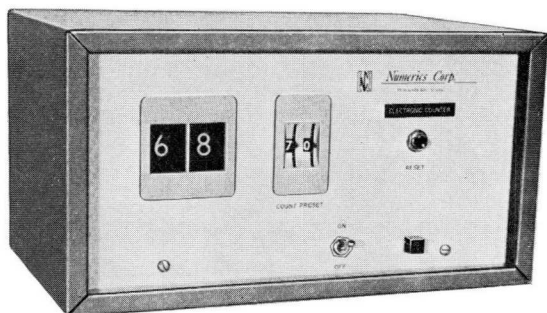


Fig. 18-11. Filter dimensions.

Technical Data

Attenuation

(for input frequencies between 300 kHz and 15 MHz)	> 50 dB
Maximum a.c. input voltage	250 V
Maximum a.c. input current	2 A
Test voltage for 1 min.	
a) across input terminals	2 kV
b) across input terminals and case	2 kV
Operating temperature range	-25 to +70 °C
Storage temperature range	-25 to +85 °C
Weight	570 g



I



II

General batch Counters

I. from Numerics Corp., Tewksbury, Mass. U.S.A.

Applications:

- batch counting on packaging machines
- carton counting on straight-line gluers and waxing machines
- length measuring — paper-steel-wire-aluminium
- corrugated box manufacture on printer-slotter.

II. from Darcon Controls, Westcliffe-on-Sea, England.

19 Accessories

19.1 The Empty Case Assembly ECA50

The ECA50 consists of the normal plastic housing for auxiliary units, a rear bar, and a general-purpose glass-epoxy printed-wiring board as shown in Fig. 19-1. The ECA50 may be used to mount special-purpose circuits of the user's own design.

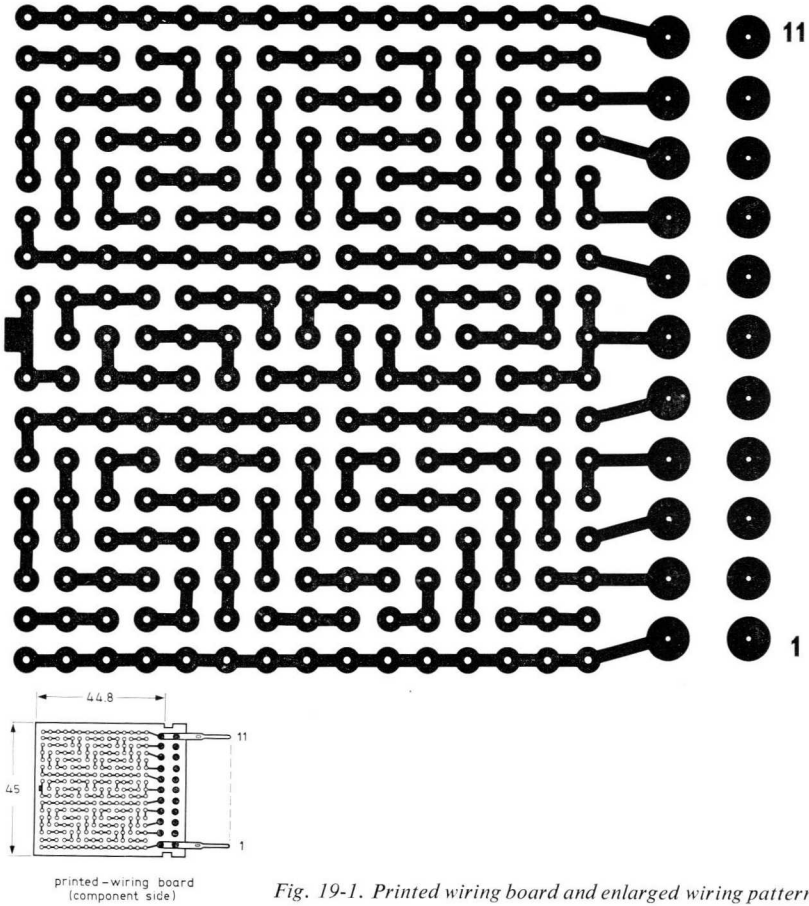


Fig. 19-1. Printed wiring board and enlarged wiring pattern.

19.2 Sticker Symbols

The drawing of a logic circuit often entails a large amount of repetitive work, as the same symbol may be used many times in a single circuit. To speed the drawing of such circuits, sheets of "stickers" are available, each sheet consisting of a stiff paper backing with a transparent adhesive sheet on which the 50-series module symbols are printed. Fig. 19-2 shows one of the sheets. Each symbol is readily detachable from the backing without cutting.

There are six different sheets, the type and number of symbols on each being given in the list below.

Sheet 1:	NIC50 (4 ×) + SU50 (8 ×),	cat.no. 4322 026 70260
Sheet 2:	LRD50 (3 ×) + PSR50 (2 ×) + 3NOR50 (3 ×) + 4NOR51 (2 ×),	cat.no. 4322 026 70270
Sheet 3:	RIC50 (4 ×) + SU50 (8 ×),	cat.no. 4322 026 70430
Sheet 4:	MID50 (8 ×) + SID50 (4 ×),	cat.no. 4322 026 70440
Sheet 5:	PDU50A (9 ×) + PDU50B (3 ×),	cat.no. 4322 026 71910
Sheet 6:	DCD50 (12 ×),	cat.no. 4322 026 71920

The catalogue numbers for sheets 1 to 6 are for 50 sheet packages.

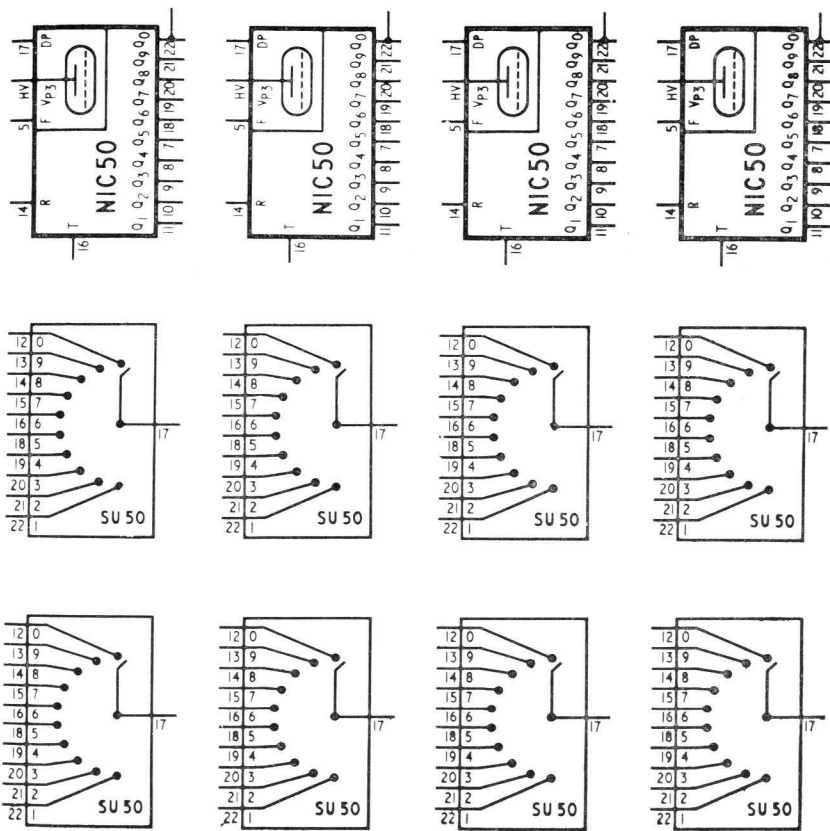


Fig. 19-2. Sticker sheet.

19.3 Mounting Bar MB50 (Cat. No. 4322 026 70170).

The MB50 is available in a standard 21-position length for mounting auxiliary modules. Two bars are required each unit being attached by two self tapping screws (4N x 1/4") and washers. Bar and mounting dimensions are shown (in mm) in Fig. 19-4, inch values being given in the table.

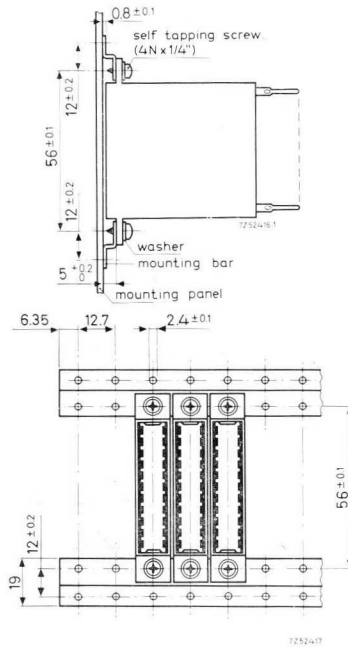


Fig. 19-3. Mounting Bar dimensions.

mm	inches	mm	inches
0.8 ± 0.1	0.032 ± 0.004	2.4 ± 0.1	0.094 ± 0.004
$5 +0.2/0$	$0.197 +0.008/0$	6.35	0.25
12 ± 0.2	0.472 ± 0.008	12 ± 0.2	0.472 ± 0.008
56 ± 0.1	2.205 ± 0.004	12.7	0.5
		19	0.748
		56 ± 0.1	2.205 ± 0.004

19.4 Front Façades

Front façades, type FIC, are available for one to six indicator modules type NIC50, RIC50, MID50 and SID50. The façades are provided with a coloured polarized screen. Façades, type FMF, for mounting from one to six switches are also available. The dimensions in mm of both types are shown in Fig. 19-4, varying dimensions being given in Table 19-1.

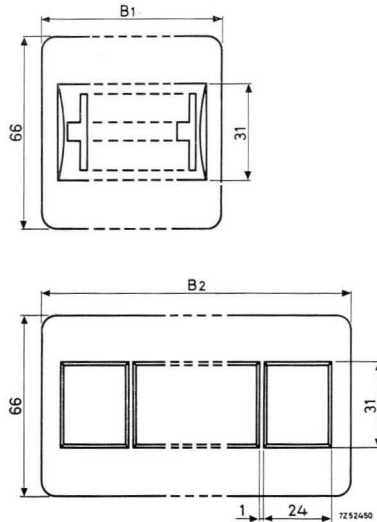


Fig. 19-4. Front façades.

Table 19-1

number of modules	indicator modules			thumbwheel switches		
	façade type	width B_2		façade type	width B_1	
		mm	inches		mm	inches
1	FIC1	35.4	1.394	FMF1	24	0.945
2	FIC2	60.8	2.394	FMF2	36.7	1.445
3	FIC3	86.2	3.394	FMF3	49.4	1.945
4	FIC4	111.6	4.394	FMF4	62.1	2.445
5	FIC5	137.0	5.394	FMF5	74.8	2.945
6	FIC6	162.4	6.394	FMF6	87.5	3.445

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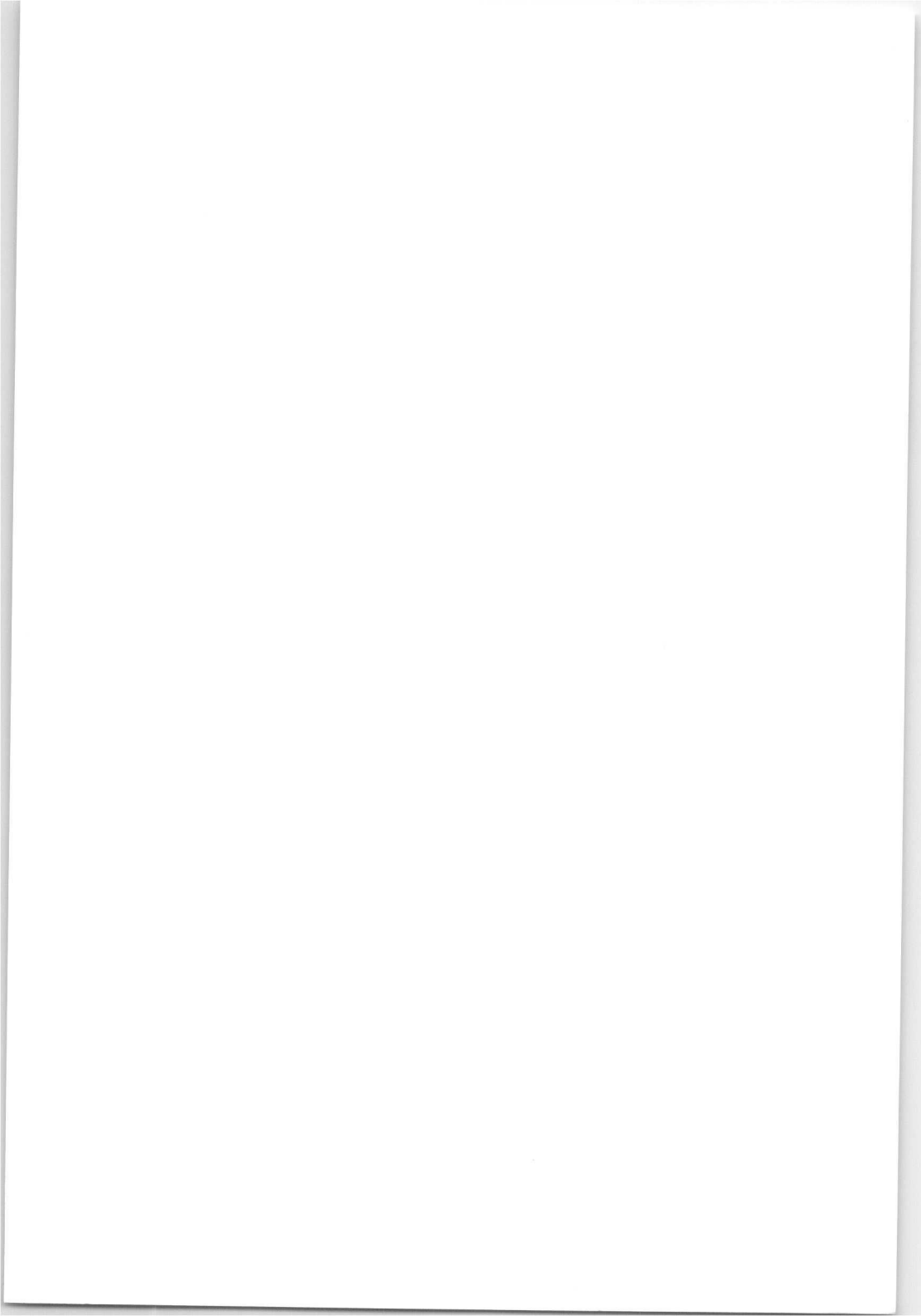
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