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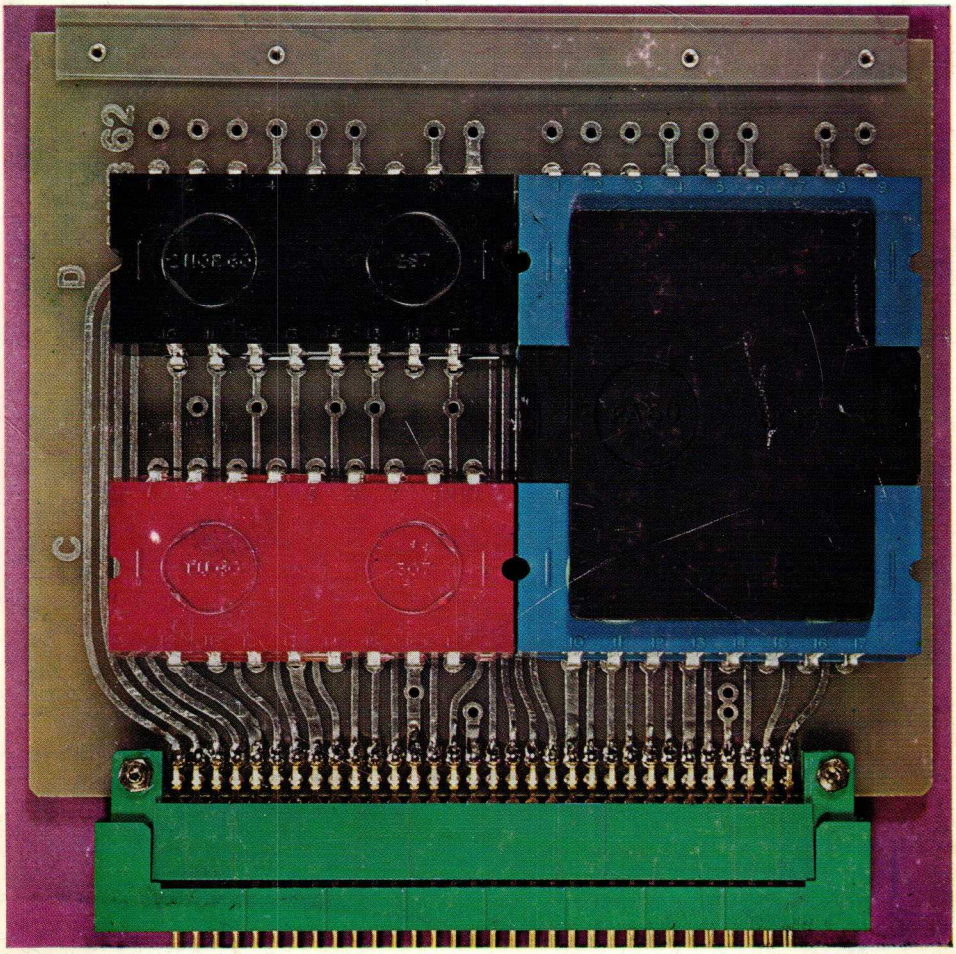
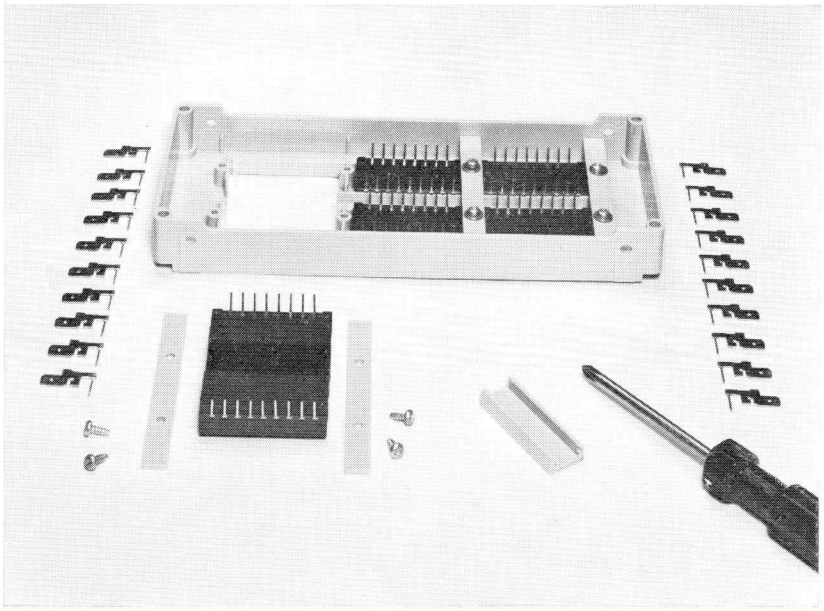
APPLICATION BOOK

ELECTRONIC COMPONENTS AND MATERIALS DIVISION

CONTROL SYSTEM DESIGN MANUAL FOR 60-SERIES NORBITS



Control System Design Manual for 60-Series Norbits



60-Series circuit blocks mounted in the Universal Mounting Chassis UMC60, catalogue number 4322 026 3833.

Control System Design Manual for 60-Series Norbits

A guide to the application of electronic logic circuits in industry

C. Rosielle

Edited by: J. Deerson

Technical Publications Department
Electronic Components and Materials Division

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Foreword

Bridging a gap . . .

Electronics is progressing at such a rate that today there are many developments which require the services of a specialist in order to adapt them to practice. Mechanical engineering has also made spectacular advances, both in technology and in production techniques.

It is well known, of course, that electronics can contribute in many ways to better machines and better products. The mechanical engineer, however, generally finds little time to delve into the intricacies of electronics. Becoming aware of the gap between the possibilities of electronics and the practical requirements from a mechanical engineer's point of view, the problem of bridging this gap was studied. The result of this study and the subsequent development is the 60-Series-electronic "circuit blocks", encapsulated for reliability and ease of handling, performing various commonly-required functions. The 60-Series can be considered as a number of standard building elements allowing the set up of a wide variety of control circuits.

After familiarization with the few simple design rules contained in this book, the mechanical engineer should have little difficulty in designing a system to take full advantage of this modern approach to electronic control.

Naturally, this book will not be able to answer every query that might arise regarding control system design; however, publications containing information on particular topics are constantly being produced. We invite you to send us a card

bearing your name and address so that it can be placed on our mailing list. Relevant publications will then be sent automatically.

We wish to thank the many persons from various countries who have contributed to this book with fresh ideas and information. A list of contributors is given opposite.

Since its introduction more than two years ago, response to the 60-Series has been very favourable. As a result, the units are now available as off-the-shelf items at sales outlets around the world.

Dr. W. K. Westmijze

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1 Principles

1.1 Fundamentals

"NORBIT" is the term given to a range of electronic circuit modules providing static switching and other functions for industrial control systems. The basic NORBIT module may be thought of simply as an electronic version of the conventional electromechanical relay, and to introduce the range, an explanation of the operation is given in terms of the relay. The term "NORBIT" is constructed from the words "NOR" and "BIT", hence the meaning of a "piece" or module of circuitry performing the logic function Neither . . . Nor.

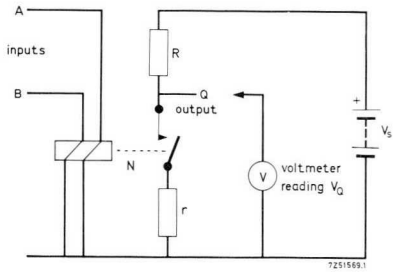


Fig. 1.1 Relay circuit.

In Fig. 1.1 the relay N is provided with a normally open contact and has two exactly similar coils A and B, connected together at one end. The relay contact N is connected through a resistor R to a d.c. voltage source, V_s. R limits the current drawn from the supply via the Q terminal or through the switch contacts in the closed position.

The resistance r represents the switch contact resistance. (The voltmeter is not an essential part of the circuit; its purpose is to make clear the meaning of "voltage" at point Q. The same voltmeter can serve for measuring the voltages at points A and B.) We shall regard Q as an output terminal, and A and B as input terminals, and establish relationships between voltages at these terminals.

Before attempting to do this it is worthwhile to consider the readings one would obtain on the voltmeter measuring V_Q in the two possible contact positions of switch N. With the contact N open as in Fig. 1.1 the voltmeter shows a "high" voltage; with the contact N closed the meter

would show a "low" voltage (nearly zero volts; across an ideal switch we would read 0 V).

Having observed this, one could express the output voltage at Q as being either "high" or "low". In other words, the output voltage at Q shows the characteristics of a binary variable i.e. the voltage at Q can have one of two possible values. The notation of the binary variable is further generalized by assigning the symbol "1" to the high level state and "0" to the low level state. The advantage of this notation is that it allows the input and output voltages to be treated as binary variables (i.e. as variables able to assume only two values) which enables switching algebra to be used, thus simplifying design (cf. Chapter 7).

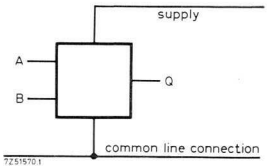


Fig. 1.2

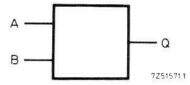


Fig. 1.3

For our purposes, the relay circuit of Fig. 1.1 can be just as well represented by a "black box" with a number of connections to it, and this is shown in Fig. 1.2. As a further simplification we can omit the supply connections — we are only interested in the relationship between output and inputs — as in Fig. 1.3.

Now, assuming that the coils A and B are such that when a "1" level ("high" level) is connected across any one of them the contact N will close, we find that four — and only four — situations can arise in practice. (An unconnected NOR input is equivalent to a "0" for that input.) The four possible input/output combinations are shown in Fig. 1.4).

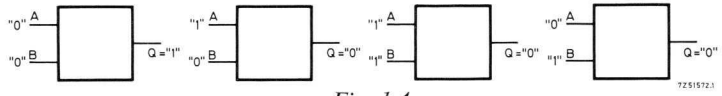


Fig. 1.4

These findings can be tabulated to show the possible combinations of inputs and the resulting outputs. Such a table is called a Truth Table. The dependent variable output Q is a function of the independent variable inputs. For what values of the input variable is the output Q a 1? When neither A NOR B is 1, i.e. when both are 0 (first row of Truth Table only).

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

It is customary to call a circuit which gives the relation between input and output as shown in the Truth Table above, a NOR operator. Another way to describe the performance of the NOR will be given later on.

1.2 "Static" Relay Performing the NOR Operation

"Static" means here that the "relay" does not have any moving parts. If we replace the relay and contact N by an element which is normally non-conducting we shall have an output situation which for the present considerations is identical to the one depicted in Fig. 1.1. If, by some suitable means, we can contrive that the application of a 1 to the input causes a current through R which, to all intents and purposes, is determined only by the value of R (or of $R + r$), the new circuit will behave in exactly the same way as the old and we can continue to regard it as a black box whose function is characterized by the Truth Table above.

An extremely suitable element to replace the relay contact is the transistor. In connection with resistors which act as the inputs, like coils A and B of Fig. 1.1, a circuit can be obtained which performs the NOR operation (cf. Chapter 2).

The functioning of the circuit in Fig. 1.1 can be elaborated, without any change in principle, by fitting the relay with more coils of the same type, all connected at one end to the zero supply line. Fig. 1.5 represents a NOR device with four inputs; the corresponding Truth Table is given below. The remaining 14 possible combinations all result in $Q = 0$.

We see from the Truth Table that Q cannot be 1 unless all the inputs are 0. This condition can alternatively be expressed as neither A NOR B NOR C NOR $D = 1$ will make $Q = 1$.

A	B	C	D	Q
0	0	0	0	1
0	0	0	1	0

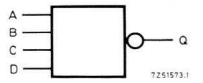


Fig. 1.5

The black box in Fig. 1.5 does not give any clue as to what the circuit does. With some additions we can give more information. The NOR operator from the NORbit 60-series is given by the symbol of Fig. 1.6.

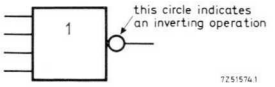


Fig. 1.6

This diagram depicts, symbolically, one of the two NOR operators built into each 2.NOR60 block. Each NOR has 4 input terminals and 1 output terminal. The circle at the output indicates that an inverting operation takes place. In practice, only the inputs actually being used are indicated.

1.3 The Basic Switching Operations

Other switching operations apart from the NOR operation are possible when the unit is connected in different ways, and we will now investigate some of these common configurations.

1.3.1 "NOT"

If only one input of a NOR operator is used, we have the two possibilities shown in Fig. 1.7. We see that if A is 1, Q is 0 and vice versa. This is often described as "Q is the inverse of A" or "Q is not A". The output of the circuits symbolized by Fig. 1.7 is not equal to the input. This leads to the concept of a NOT operator (or Negator as it is sometimes called).

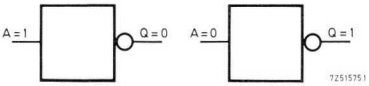


Fig. 1.7

A symbol commonly used to indicate the NOT operation is a bar over the corresponding variable, e.g. $Q = \bar{A}$ means "Q is NOT A" (hence if $A = 0$, $Q = 1$; and if $A = 1$, $Q = 0$).

1.3.2 "OR"

We know from the Truth Table (Sect. 1.1) that if A or B is 1, output Q_1 will be 0. If this output is connected to the input of a subsequent NOR, the output Q_2 will be at 1 level when, and only when, A OR B or both are at 1 level. We have found in this way that the arrangement performs

the OR operation. If A OR B (or both) are 1 the output will be 1.

It is customary and advantageous to use a "+" sign for the OR function, so we write $A + B = Q_2$, signifying that if a 1 is present on the left hand side, Q_2 will be 1.

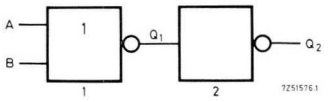


Fig. 1.8

Knowing that the second NOR operator performs the NOT operation, we can say that the input to the second operator in Fig. 1.8 must be:

$$Q_1 = \bar{Q}_2, \qquad \text{and} \qquad \overline{A + B} = \bar{Q}_2$$

so that

$$\overline{A + B} = Q_1.$$

Here we find a short-hand notation for the NOR operation. The case in which all four possible inputs to a NOR are used would be:

$$\overline{A + B + C + D} = Q.$$

(Note that the whole complex expression on the left hand side has been negated. From this the NOR operation could be defined as an "inverted OR".)

1.3.3 "AND"

We know from the first Truth Table that Q will be 1 only if A and B are 0. This implies that both A and B must be 1 to make Q_3 equal to 1 in the circuit of Fig. 1.9 which performs the AND operation. In algebraic notation the AND function for this circuit is given by:

$$A \cdot B = Q_3 \qquad \text{or, even more simply,} \qquad AB = Q_3.$$

The notation implies of course that if one of the factors on the left-hand side is 0, the "product", and therefore Q_3, will be 0.

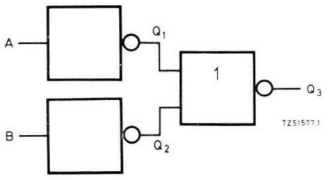


Fig. 1.9

It will be clear from the foregoing that a standard circuit performing the NOR function can be combined with other units of the same kind to make systems that perform functions other than NOR. Also, if only one input is used, the NOR function available from a single unit can be reduced to NOT.

1.3.4 "Memory"

The Memory function should be mentioned here, although it is not strictly in the same class as the previous four logic operations.

If a 1 signal is applied to the Set input of the circuit of Fig. 1.10, the output of NOR (2) will become a 1. By feeding back this 1 signal to another input of NOR (1), the output of NOR (2) will be kept at 1 even after the initiating 1 at the Set terminal is removed.

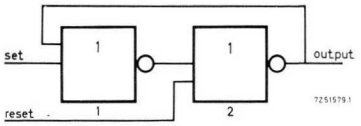


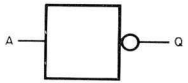
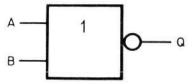
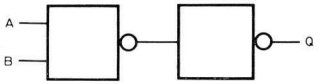
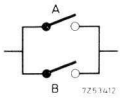
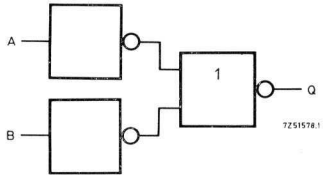
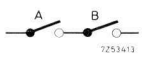
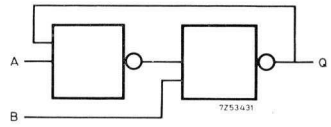
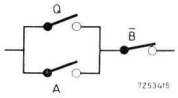
Fig. 1.10

By applying a 1 signal to the Reset terminal, the output of NOR (2) will return to 0 and remain 0 unless a 1 is again applied to the Set terminal after removal of the reset 1. (This assumes the Reset was initially at 0.)

The memory function is often used to store information for a certain time after the input conditions have disappeared. Useful applications are immediately apparent in alarm systems, which must often be capable of recording transient conditions, or in conjunction with timer devices, in order to establish a certain operating sequence.

The information given above will allow the solution of combinational logic problems. The Table on p. 7 gives a survey of the several basic logic functions in which NORbits are used and the equivalent relay functions.

1.3.5 Summary of Switching Operations

diagram	function	operation	symbolic description	relay contact equivalent
	NOT NEGATION INVERSION	output signal level is inverse of input signal level	$\bar{A} = Q$	
	NOR	if neither A NOR B is 1, $Q = 1$	$\overline{A + B} = Q$	
	OR	if either A OR B (or both) are 1, $Q = 1$	$A + B = Q$	
	AND	if both A AND B are 1, then $Q = 1$; inputs to the right-hand NOR are A, B, whence $\bar{A} + \bar{B} = A \cdot B$	$AB = Q$	
	MEMORY	if A is 1 AND B is 0, then $Q = 1$; if B is 1, then $Q = 0$ if both A AND B are 0, then $Q = 1$ or $Q = 0$, depending on previous input conditions	$(Q + A)\bar{B} = Q$	

1.4 Illustrative Problems and Solutions

Problem 1 — Design a NOR system that will make a lamp light up if one of the four doors of a car is opened.
Assign the letters A, B, C and D to the door contacts and let these also represent a 1 signal if the relevant door is open. Neglect power considerations. Calling the lamp L and assuming the lamp to light up at $L = 1$, we get: if A OR B OR C OR D is 1 then $L = 1$ (Fig. 1.11).

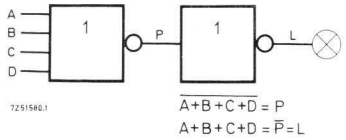


Fig. 1.11

Unlike conventional mathematics, the dependent variable (the output) is placed on the right-hand side. Another difference to be noted is that the equations are obviously "one-way", i.e., the output may be derived from the input, but not vice versa.

Problem 2 — As above, however lamp must only light up when A AND B AND C AND D are open.
We have $A \cdot B \cdot C \cdot D = L$ (Fig. 1.12).

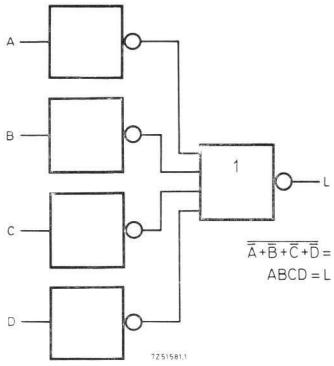


Fig. 1.12

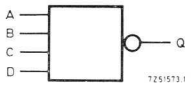


Fig. 1.13

This could be done more simply by making an open door provide a 0 signal (Fig. 1.13).

Problem 3 — An alarm signal must be obtained if fans *A* AND *B* OR fan *C* stop AND motor *D* is running.
First step: set up circuit for *A* AND *B* (Fig. 1.14). Assume a stopped fan gives a 1 signal.

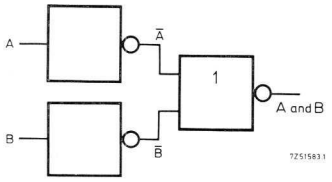


Fig. 1.14

Second step: (*A* AND *B*) OR *C* (Fig. 1.15).

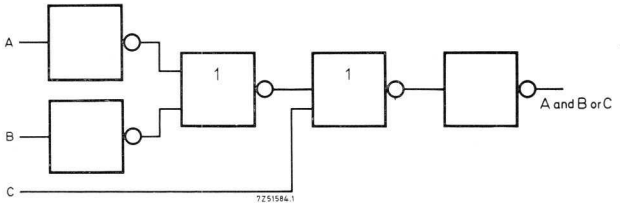


Fig. 1.15

Here it is advantageous to mention the importance of *sequence* in switching algebra. Briefly, it may be stated that an AND operation should be worked out before an OR operation, except where the OR is enclosed in a priority bracket (as in step 3 below).
Third step: [(*A* AND *B*) OR *C*] AND *D* (Fig. 1.16).

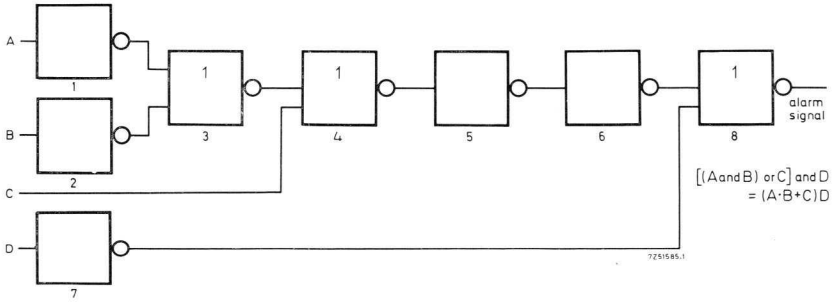


Fig. 1.16

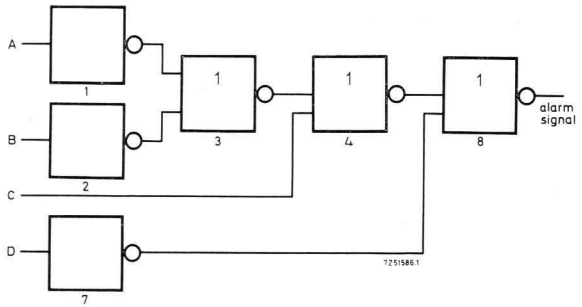


Fig. 1.17

Fourth step: simplifications. Observe that NOR (5) and NOR (6) represent two inversions; they can therefore be omitted, giving the circuit of Fig. 1.17. We also observe that NORs (1), (2) and (7) have one signal input only. They, too, can be omitted if 0 signals are used as alarm signals for A, B and D; see Fig. 1.18. $\bar{A}$, $\bar{B}$ and $\bar{D}$ are 0 and C is 1 for alarm condition.

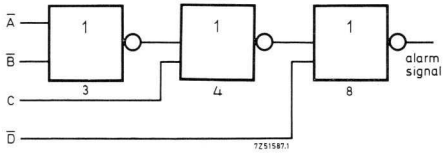


Fig. 1.18

1.5 General Rules for Simplification of Diagrams

— Any arrangement of two single-input signal-inverting NOR operators in tandem can be omitted (Fig. 1.19).

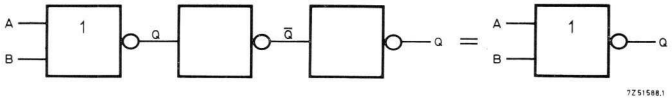


Fig. 1.19

— A NOR operator having one input only can be left out if an inverse input signal can be made available instead.

— Any NOR operator having one input only, connected between two other NOR operators can be omitted, together with the following operator.

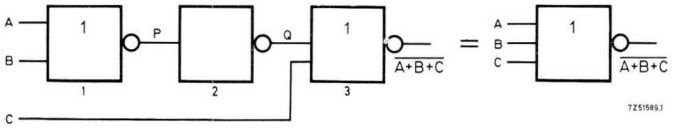


Fig. 1.20

In the first arrangement of Fig. 1.20, $P = \overline{A + B}$, and $Q = \overline{\overline{A + B}} = A + B$. So the input to NOR (3) equals $A + B + C$.

1.6 Design Procedure

In designing a system for NORbits it is wise to adopt the following sequence:

(a) Define the problem in clear English using the logical concepts of AND, OR, NOT, NOR and the memory function.
(b) Split the problem, where necessary, into parts that can be recognized as basic functions.
(c) Set up a tentative schematic diagram for the parts; switching algebra, as described in Chapter 7, is often of value here.
(d) Interconnect the parts in accordance with the functional relations that exist between them as described in (a).
(e) Simplify the results obtained under (c) and (d).
(f) Check performance of resulting circuit by assuming the binary variables to be available in all possible combinations. The best way of doing this is to prepare a Truth Table or set up the circuit on a Simulator, such as "SIM60" described in Chapter 2.
(g) Check the fan-out of each unit with the Loading Table to ensure that no unit is overloaded. This is explained more fully in Chapter 2.

2 Brief Description of the 60-Series

2.1 Introduction

In Chapter 1 we found that the NOR unit is simply a present-day version of the long established relay. But what actually does this small encapsulated unit contain?

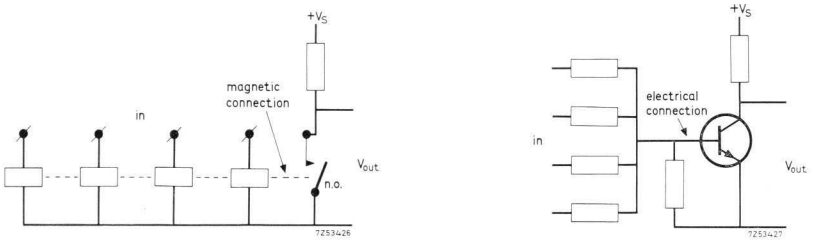


Fig. 2.1. The NORBIT-relay equivalent.

At the left of Fig. 2.1 is a simple relay circuit and at the right is a NOR circuit (each unit contains two such circuits), consisting of 6 resistors and a transistor. If a current is present in any input coil of the relay, the normally-open contact will close and $V_{out} = 0$; if a sufficiently high positive potential (1 level) is present at any input of the NOR circuit, the transistor becomes fully conducting and $V_{out} = 0$. The output is the inverse of the input. The actual output voltage denoted by 0 may range from 0 to $+0.3$ V.

The transistor being made of crystalline material acts as a very good insulator (open switch) when zero or a small positive biasing voltage is applied to the base. On the other hand, if a positive voltage of a certain magnitude is applied to the base the transistor will be fully conducting; i.e. current through the transistor is determined only by supply voltage and resistor R. The transition from fully-conducting to non-conducting or vice-versa takes place very quickly, thus making an excellent fast-acting switch.

Simplicity is just one advantage of the NOR unit; others are extreme reliability *, small power consumption, wide tolerance on supply voltage, small size, high speed, and low cost.

* Independent of the number of operations.

The minimum 1 level voltage required at an input resistor of a NOR unit to make the transistor fully-conducting is +11.4 V, which is thus the minimum loaded output voltage required if the NOR is to drive further units (Fig. 2.2).

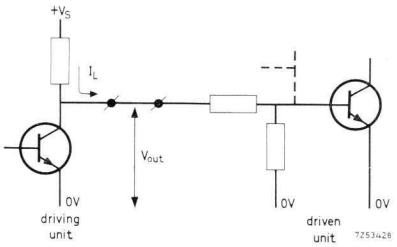


Fig. 2.2. Coupling of NORs.

If this is to be so, the output load resistance must be a minimum of 15 kΩ, equivalent to six NOR inputs. If the load current I_L is made greater than that corresponding to this load resistance, V_{out} may drop below 11.4 V which would be insufficient to switch subsequent NORs. From this we derive the Drive Unit (DU), equal to the drive requirement of one NOR input. The Loading Table (section 2.3) gives the input requirements and output capability ("Fan-out") in DUs for the other units in the range, and the table must be obeyed when putting a design into practice.
The following section gives general information on the units. These are:

2.NOR60	—	Dual NOR Unit
2.IA60	—	Dual Inverter Amplifier
TU60	—	Timer Unit
2.SF60	—	Dual Switch Filter
PA60	—	Power Amplifier
PSU60/61	—	Power Supply Units (see chapter 3)

2.2 Functions of the Various Units

2.2.1 Dual Four Input NOR gate, 2.NOR60

The 2.NOR60 unit contains two identical independent transistor-resistor NOR circuits. Each circuit has four inputs (pins 1, 2, 3, 4, or 5, 6, 7, 8). If any input of a NOR is at 1 level, the output (pin 5 or 14) of that NOR will be at 0 (Fig. 2.3).

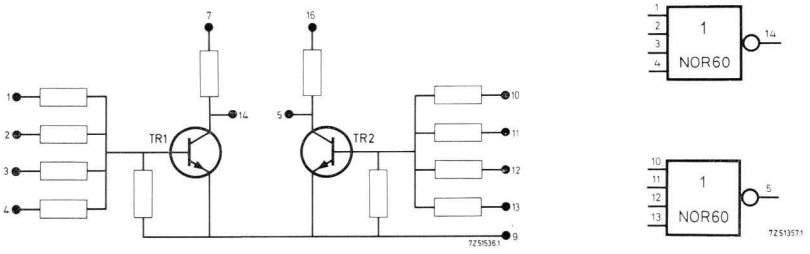


Fig. 2.3. The 2.NOR60, its circuit and symbol.

*Collector-*OR *function:* The outputs (transistor collectors) of several NORs (up to 5) can be connected directly together to extend the number of inputs. Thus, linking pins 5 and 14 on a 2.NOR60 block will give a NOR with a capacity of eight inputs (Fig. 2.4*a*).

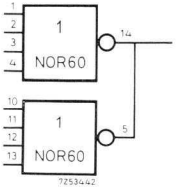
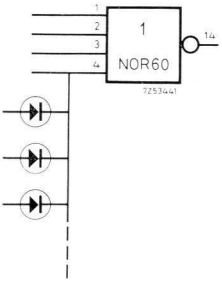


Fig. 2.4a. Collector-OR configuration.

Fig. 2.4b. Extra inputs with diodes.



Supply voltage is to be connected to one unit only, e.g. pin 7 *or* pin 16, not both, in the above example.

More inputs can be added, to a maximum of 24, by connecting diodes (6 per input) (Fig. 2.4*b*); type BAX 13 diodes should be used.

2.2.2 Dual Inverter Amplifier, 2.IA60 (Fig. 2.5)

The 2.IA60 unit comprises two inverter amplifiers IA60. Use as a single amplifier is feasible, in which case the denomination LPA60 is used. The 2.IA60 has a similar circuit to the NOR60, but much higher loadability is possible. To obtain the 2.IA60, the emitter of TR_1 (pin 17) should be connected to 0 V common (pin 9), and collector resistor of TR_2 (pin 6) to output of IA2 (pin 5). A 1 level input (pin 4 or 13) will cause a 0 level

output (pin 14 or 5-6 respectively). The output capability is 20DU. Diode input extension, as shown for the NOR60 in Fig. 2.4(b), can also be applied.

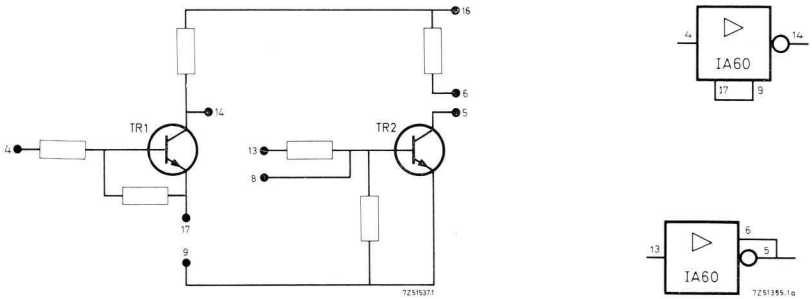


Fig. 2.5. Circuit and drawing symbols, 2.IA60.

To obtain the LPA60 (Fig. 2.6), pin 17 should be connected to the base of TR_2 (pin 8) and the load connected between pins 5 and 16. When pin 4 is at 1 level, pin 5 will be at 0 level, current thus flowing through the load. Pin 8 must not be connected directly to a voltage source. A low value of the collector resistance of 300 Ω allows an output of 140DU with this configuration.

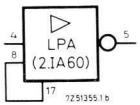


Fig. 2.6

With 1 and 0 signals applied to the input, the LPA60 will function as a switch. The minimum load resistance is 300 Ω.

Special measures should be taken to protect the LPA60 against overloading when it is used to switch tungsten filament lamps or inductive loads, such as relays. The maximum current rating of 100 mA must always be

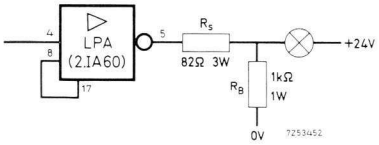


Fig. 2.7

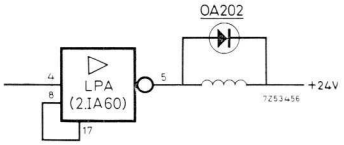
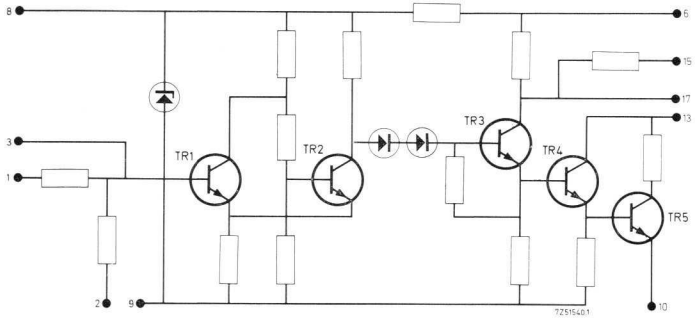


Fig. 2.8

respected. For such lamps, a filament preheating current should be drawn through the bleeder resistor R_B (Fig. 2.7). The series resistor R_s should be a minimum of 82 Ω, with a lamp Cat.No. 9234 640 21700. A relay or contactor coil forms an inductive load and it is necessary to connect a diode across the load as shown in Fig. 2.8 to protect the transistor of the unit against the high back e.m.f. when switching off. Release of the relay or contactor is then delayed somewhat, as current will continue to flow until the energy stored in the coil inductance is dissipated.

2.2.3 Power Amplifier PA60 (Fig. 2.9)

The power amplifier PA60 comprises a *Schmitt* trigger followed by a buffer and driver stage, which provides adequate drive to the power transistor under all conditions of permissible supply voltage and input



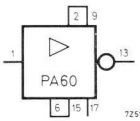


Fig. 2.9. Circuit and drawing symbol, PA60.

signal. It is mounted in a size B case (cf. Chapter 14). The load should be connected between pin 13 and + of a power supply. A 1 input will switch on the load current.

The PA60 has a much higher loadability than the 2.IA60, the minimum

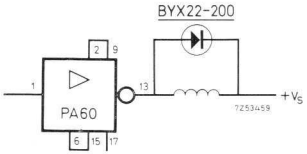


Fig. 2.10

load resistance being 30 Ω. When used as a medium power switch, precautions against overloading must be taken if driving inductive loads, etc., as in Fig. 2.10.

2.2.4 Timer Unit TU60

The TU60 unit gives an inverted output; a delayed 1 output is obtained, following a 0 input. No delay occurs when the input returns to 1.

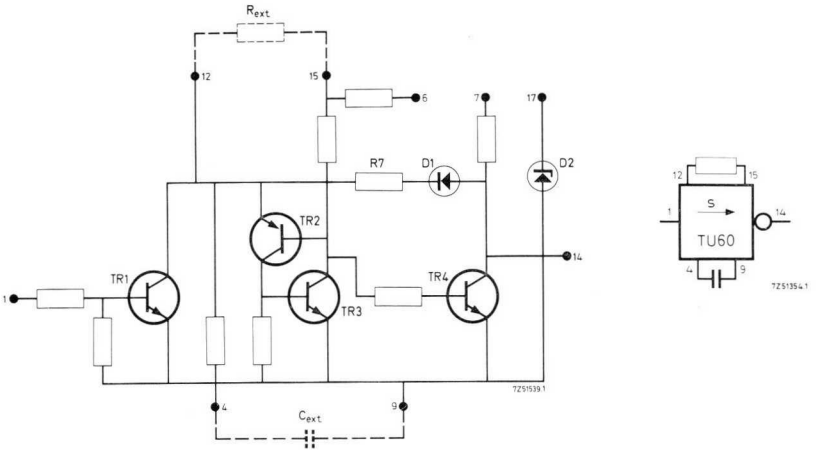


Fig. 2.11. Circuit and drawing symbol, TU60.

With the input at 1 the capacitor (C_{ext}) in Fig. 2.11 is discharged. When the input goes to 0, TR_1 ceases to conduct so that the capacitor is allowed to slowly charge until the base potential of TR_2 is exceeded. TR_2 starts to conduct and provides base current for TR_3, which speeds the turn-on of TR_2. TR_4 ceases to conduct and the output level at pin 14 changes from 0 to 1. Positive feedback is provided via D_1 and R_7. The operation of the circuit is shown in Fig. 2.12.

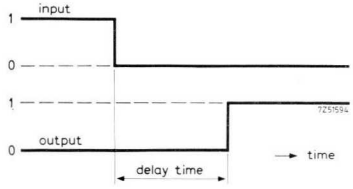


Fig. 2.12. Time diagram.

At switch-on, a delay is always present even if the input is at 1. If memories are involved in a circuit together with the TU60, a reset signal of longer duration than the timer delay should be given at switch-on.

R_{ext} and C_{ext} are external components which can be chosen to give a required delay, equal to $R_{ext}C_{ext}$ seconds. (See Chapter 14.)

2.2.5 Dual Switch Filter 2.SF60 (Fig. 2.13)

The function of the 2.SF60 unit is to eliminate the effects of contact bounce of mechanical switches, and interference on long input lines.

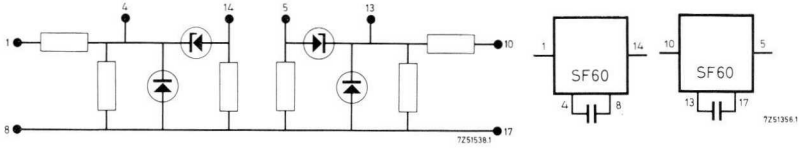
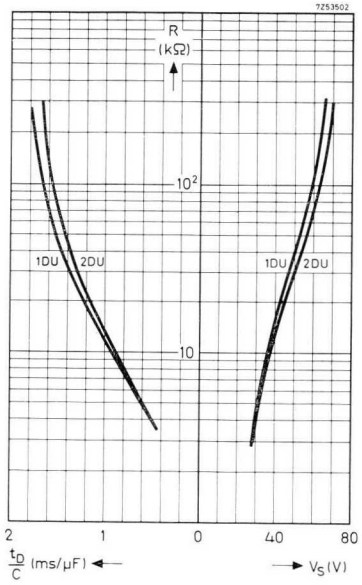


Fig. 2.13. Circuit and drawing symbol.



The circuit consists of two identical filters for minimizing the effects of contact bounce and spurious interference on long lines between switch and system input. The switch filter is designed for a switch contact voltage of 100 V, to ensure reliable switching. The voltage divider enables the input to be presented with a high impedance load whilst the internal circuitry is presented with a lower impedance source. The time for which contact bounce is eliminated t_D is determined by an external capacitor (connected between pins 4 and 8, or 13 and 14).

Fig. 2.14. Maximum value of R and resulting value of t_D/C for switch supply voltages of 30 to 70 V. R to be connected between pins 1 and 4, or 10 and 13.

The zener diode provides a threshold voltage. *D* protects any driven NORBIT against excessive base current which could result from a large negative voltage appearing at the filter input. It also prevents reverse voltages occurring at the capacitor, which thus may be of a polarized type. The output capability is 2DU per unit.

See Chapter 14 (Specifications) for details on switching speed possible, and further information. See Figs 2.14, 2.15 for operation at switch voltages other than +100 V.

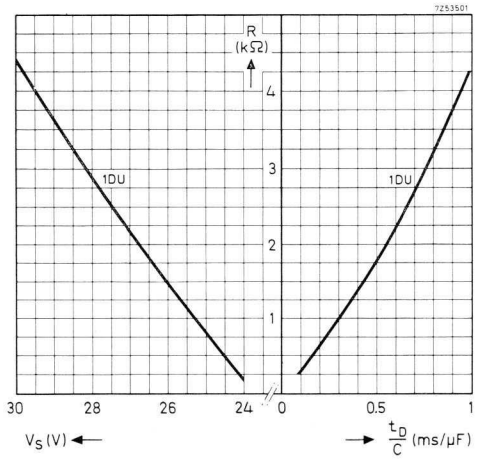


Fig. 2.15. As for Fig. 2.14, but supply voltages of 24-30 V.

2.3 Practical Design Considerations

After designing the logic system, the loading on each circuit block output must be checked. This is done with the aid of the Loading Table below (1 DU is required to drive one input of a NORBIT). If the number of DUs required exceeds the DUs available at an output, then an IA60 or LPA must be used, it being remembered that these are inverters.

Before designing the power supply for a system, the total current demand for the greatest number of units in the 0-state at any one time must be ascertained. The maximum supply current for the conducting state is given in the last column.

Table 2 — Loading Table

unit	input	output (supply voltage 24 V ± 25 %)	I_{max} (mA)
2.NOR60, per function	1 DU	6 DU	4.2
2.IA60, per function	2 DU	20 DU	14.0
2.IA60 (connected as LPA60)	2 DU	$R_{load} \geqslant 300\ \Omega$; with $R_{load} = 300\ \Omega$, output = 140 DU	114
PA60	1 DU	$R_{load} \geqslant 30\ \Omega$	26.2 + I_{load}
TU60	1 DU	5 DU	10.1
2.SF60, per filter	+100 V	2 DU	3.3

2.4 SIM60

The SIM60 is a self-contained portable logic simulator, housed in a small light-weight suitcase as shown in Fig. 2.16.

There are three important applications for the simulator.

(1) *Verification of circuit performance in the design stage*

Before "bread-boarding" the prototype of a control circuit it will often be desirable to make sure that the proposed circuit will behave as intended. The capacity of the SIM60 will generally allow build-up of the lay-out of a 60-Series printed wiring board. If the control circuit comprises several panels, the lay-out and interconnection for each panel should be checked before the actual assembly is made.

The plug and cord connections allow fast hook-up, which will often eliminate the time-consuming question "what went wrong and where?"

(2) *Verification of circuit drawings*

After realization of the prototype, the circuit will usually have to be documentated by drawings — either for maintenance and/or production information. It is an unfortunate fact that designs are often altered during the prototype construction — the drawing room must often work with bits and scraps of information. The drawing produced will have to be

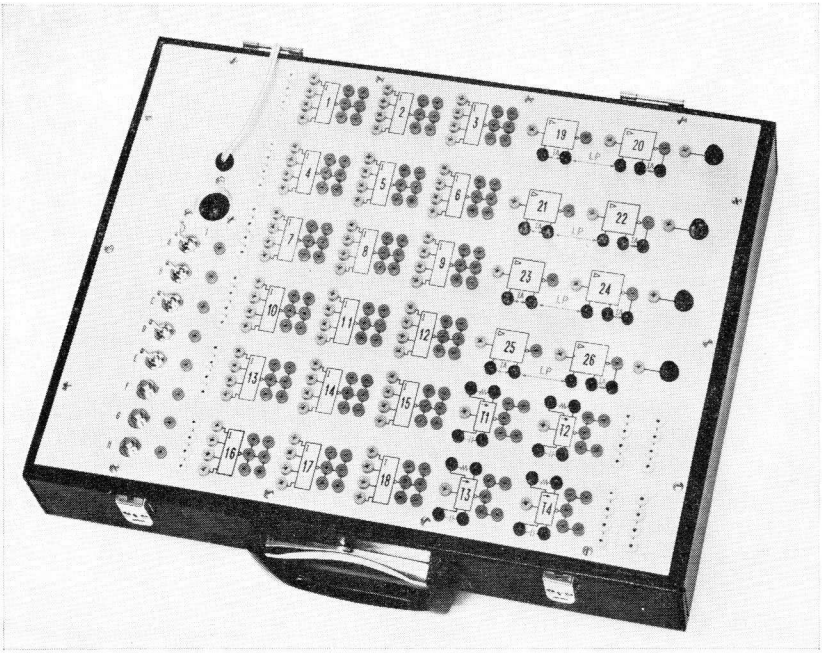


Fig. 2.16. The "SIM60" tester.

checked, and preferably this check should be done by building the scheme on the SIM60.

(3) *Logic trainer*

Apart from being a useful engineering tool, the SIM60 can serve as a logic trainer. It will be found that working with the trainer while learning about the theoretical concepts deepens the student's insight into control logic. By using the simulator he will gain experience in hours which otherwise can take weeks or months of time and costly materials.

This Application Manual gives the SIM60 instruction material under various headings. As a guide, it is suggested that the student attempt to realize the following functions and circuits on the simulator, in the order indicated:

NOR, NOT, AND and OR functions (Section 1.3.1 etc.), various-memory circuits (Section 8.1.3), EXOR and Coincidence circuits (Section 8.1.1 and

8.1.2), circuits with the TU60 (Section 8.2), and sequential circuits Section 8.3).

Table 2.2 Contents of the SIM60

description	quantity	remarks
2.NOR60	9	18 NOR functions
2.IA60	4	8 inverting amplifiers; each 2.IA60 may be connected as an LPA60
TU 60	4	without external resistor and capacitor
indicator lamps	4	1 red, 1 yellow, 1 white, 1 green — can be used as output indicators by connecting the lamp as a load to an LPA60
power supply	1	suitable for operation on 127-220-240 V, 50/60 Hz mains; provided with cable and socket
toggle switches	5	to simulate 1 or 0 input conditions
push buttons	3	to simulate temporary 1 input signals
sockets	308	(in various colours) gives access to inputs and outputs of the functions
patch cords		
long (50 cm) :	10	
medium (30 cm) :	20	
short (20 cm) :	10	
dimensions (cm) :	42×32×9.5	closed
weight (kg) :	5.5	approximately

The functions are indicated by a graphical symbol engraved in the simulator panel. The output of each unit is multiplied to provide the fan-out capability of the unit. Alongside the switches, groups of sockets are multipled (indicated by line between sockets) to allow signals from the switches to be connected to various control inputs simultaneously.

2.5 Stickers for the 60-series NORbits

Drawing symbols of NORbits printed on self-adhesive, transparent material are available. They can be used for faster preparation of system drawings. The stickers are supplied in sheets, each containing the arrangement of drawing symbols. Each sticker can be separately detached from the sheet, without cutting. A sheet is shown in Fig. 2.17, approximately three quarters full size. The sheets may be ordered in packets of 50.

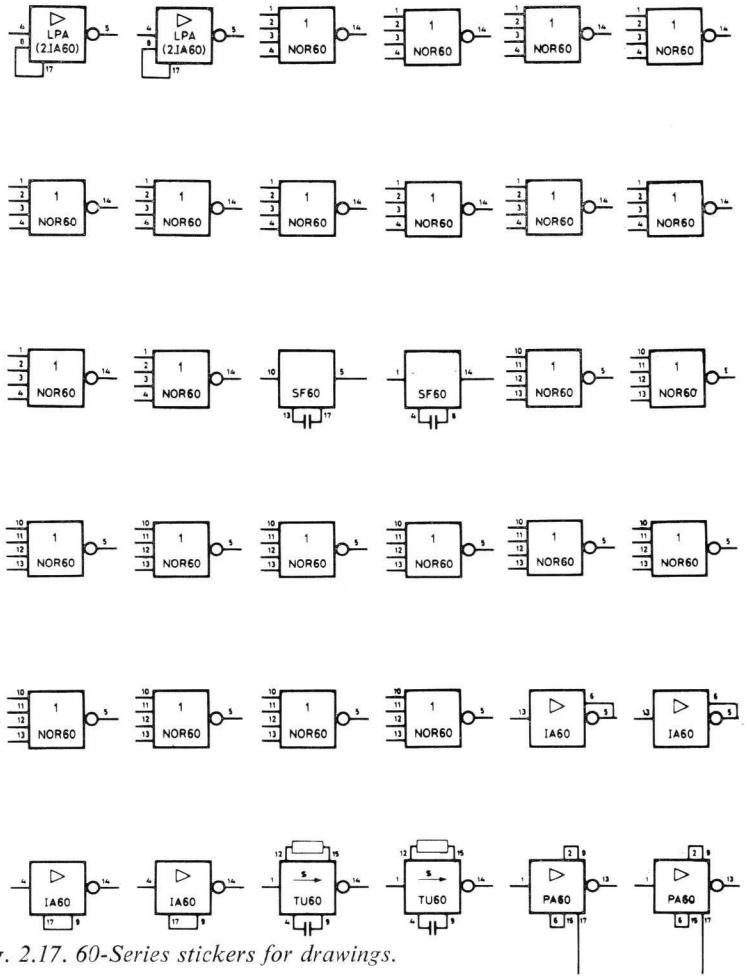


Fig. 2.17. 60-Series stickers for drawings.

3 Power Supplies

The power supply for a NORBIT-60 control system is a simple matter, as current requirements are small and only one large-tolerance voltage is required for the logic. Normal operation is +24 V, ± 25% but operation on 12 V for portable or alarm systems is possible. (Input devices sometimes require other voltages — e.g. usually +100 V for mechanical switches, +12 V for electronic transducers.)

Special power supply units, PSU60 and PSU61 are available (Section 3.1). Alternatively, supply may be obtained from 3-phase a.c. or batteries (sections 3.2 and 3.3). Following sections cover turn-on of supply, and loss of supply.

3.1 Power Supply Units PSU60 and PSU61

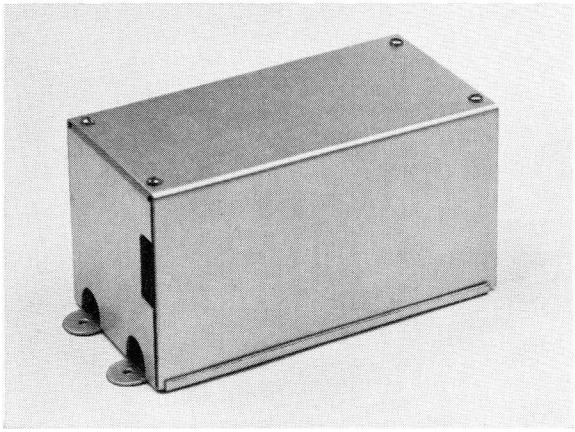


Fig. 3.1. Power Supply Unit.

The units PSU60 and PSU61 cover the supply requirements for the 60-Series in the majority of cases. Both units deliver +24 V ± 25% at 0.5 A, but the PSU61 has an extra output of +100 V at 25 mA. The terminal arrangement is given in Fig. 3.2.

Input to the units is 110-120 V a.c. or 220-240 V a.c. +10% to −15%, 47 to 440 Hz. Full specifications on regulation, ratings and part numbers

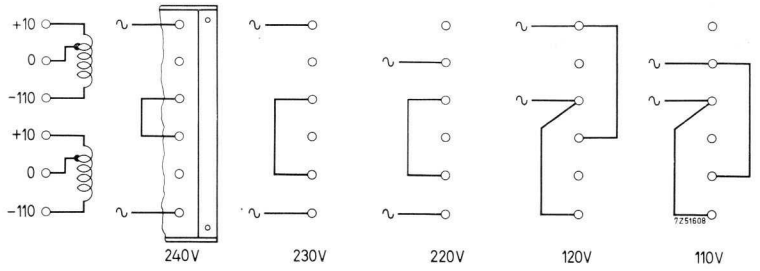


Fig. 3.2. Terminal arrangement.

etc. are given in Chapter 14. The units may be disassembled for maintenance. The housing for both units is the same.

3.2 Supply from 3-Phase Mains

This method of supply has an advantage over single-phase supply in that no electrolytic smoothing capacitor is needed, because of the small ripple produced. Data on the transformer required for 3 A, 5 A and 10 A units giving a nominal voltage of 24 V are presented below. A typical arrangement (Fig. 3.3) is a 3-phase bridge rectifier. The transformer (primary in delta, secondary in star) should preferably have an electrostatic screen between primary and secondary windings. The transformer data are summarized overleaf.

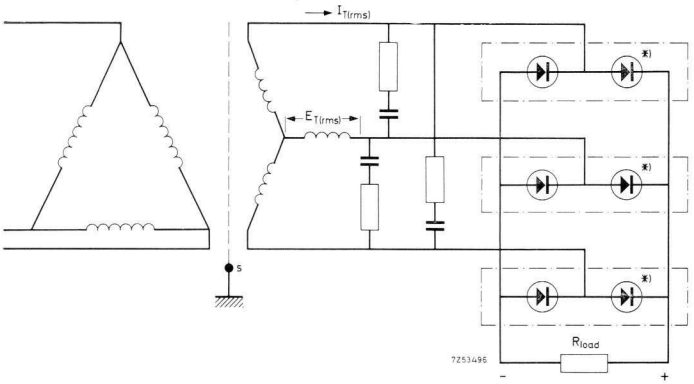


*Fig. 3.3. D.C. from 3-phase supply. Screen S should be connected to system ground; diodes marked *) are reverse-polarity types.*

output current	3 A	5 A	10 A
T_T (r.m.s.)	10.4 V	10.4 V	10.4 V
I_T (r.m.s.)	2.9 A	4.9 A	9.8 A
Secondary VA (total)	107 VA	178 VA	357 VA

Suitable diodes are the BYX20/200 and BYX20/200 R, for all the current requirement. These diodes can be mounted two by two with adaptors Type 56232 on a common vertical 3 mm blackened aluminium heat sink * having a surface area (one side) of

100 cm² for the 10 A unit ($R_{th\ h-a} <$ 5 deg C/W),
40 cm² for the 5 A unit ($R_{th\ h-a} <$ 12 deg C/W),

for ambient temperatures up to 75 °C. The 3 A unit requires no heat sink if equipped with these diodes.

3.3 Obtaining a Supply for Input Devices

Electronic input transducers normally require a lower voltage than the logic circuitry. It may be obtained from the 24 V d.c. logic supply V_s by using a dropping resistor R and voltage regulator diode D_z as shown in Figs 3.4, 3.5 and 3.6. Where several transducers must be supplied, or if the Light Interruption Probe (LIP1) is to be used, the circuit of Fig. 3.7 should be employed.

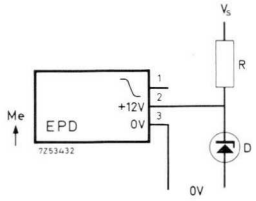


Fig. 3.4. 12 V d.c. supply for the EPD.
D = BZY95-C12; R = 220 Ω ± 10%, 2 W.

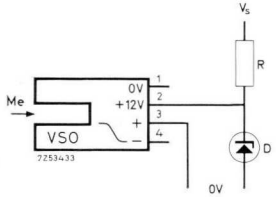
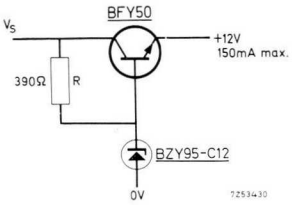


Fig. 3.5. 12 V d.c. supply for the VSO.
D = BZY95-C12; R = 270 Ω ± 10%, 2 W.

* Allow for air flow. For small heat sinks on printed wiring boards, see Sect. 4.4.

Fig. 3.6. 15 V d.c. supply for the CSPD. D = BZY95-C15; R = 220 Ω, 2 W.



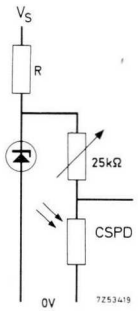
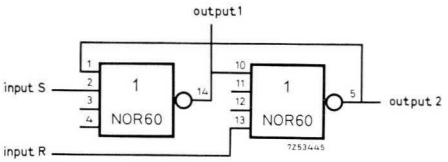


Fig. 3.7. 12 V d.c. supply. The output can deliver 150 mA_{max} for supplying up to 16 VSOs, 12 EPDs, or a single LIP1. R = 390 Ω ± 10%, 1 W; the BFY50 should be fitted to a blackened aluminium heat sink 75 mm × 75 mm × 2 mm with mounting accessory 56218 (non-insulated).

3.4 Turning-on of the Power Supply

When energizing the system there is a need for a general reset of memories. A memory circuit consists essentially of two cross-coupled NORs (Fig. 3.8). The nature of this circuit is such that, if supply voltage is available and there are no other input signals, only one output can be high, determined by the previous input conditions on the set terminal *S* and reset terminal *R*.

Fig. 3.8. Memory circuit.



However, turning-on the supply voltage initially gives an ambiguous situation. With the power supply off, both outputs will be at 0 V, and the transistors in the NORs will be non-conducting. If now the supply voltage is applied, the state the memory takes will depend upon the small differences that exist between the individual NOR circuits. Which of the two NORs will become conducting depends on the current gain of the respective transistors, the one having the highest gain needing a smaller input (thereby bringing its output at "0" level first). Automatically the other one will have "0" input and exhibit the "1" level. This phenomenon takes place during the interval that the supply voltage rises from 0 to its final value. Which output will be "1" and which output "0" depends further-

more upon the loading of the outputs of the two inverters by the associated circuitry and upon the wiring capacitance. Thus, it is essential to have firmly established initial conditions.

To establish such conditions it is necessary to ensure that the memories will take a definite state by means of a reset signal during the time that the power supply voltage rises to its final value. The duration of this signal should be long enough to eliminate erroneous memory states.

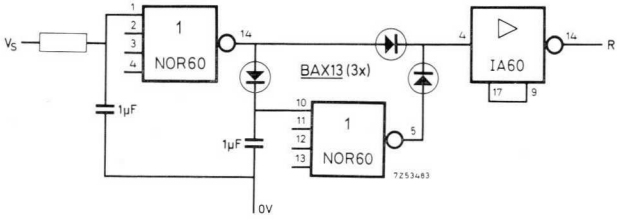


Fig. 3.9. Memory reset circuit.

Fig. 3.9 shows a circuit that will produce this signal. Output "*R*" should be applied to the reset terminals of the memories. The Inverting Amplifier used here has enough driving capability to reset 19 memories. Further details are given in Section 8.6.

3.5 The Consequence of Loss of Mains Supply

For many industrial processes and particularly those operating on a "real-time" basis the consequence of loss of mains supply is an important consideration. A typical example is an automatic packing plant; if supply voltage is lost then any units in the machine may be faulty. The faulty units must be extracted from the production line before continuing. Processes employing electrical synchronization are also affected; the

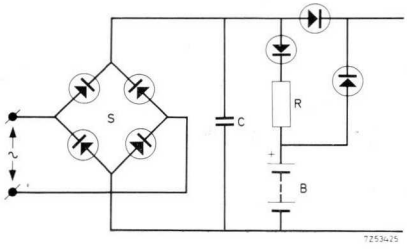


Fig. 3.10. Stand-by battery B paralleled with logic supply bridge network S. Resistor R should be chosen to allow a small trickle charge to flow through B.

machines must usually be re-synchronized before production can continue.

We discuss here two methods of dealing with loss of supply, (*a*) ensuring that supply failure is very rare, and (*b*) minimizing the consequences.

(a) This is achieved by connecting a high-reliability battery in parallel with supply voltage. It should require no maintenance and be capable of being continuously trickle-charged (see Fig. 3.10). An alarm system should be installed to warn of battery discharge current.

(b) To minimize the consequences of supply failure, the production process should not re-start automatically at the return of supply voltage but be dependent on closing of a switch, to enable the production line to be cleared of faulty units and re-synchronized if necessary. A circuit could be employed similar to the one in Fig. 3.11 (*C*, output; *X*, *Y*, *R*, reset signals).

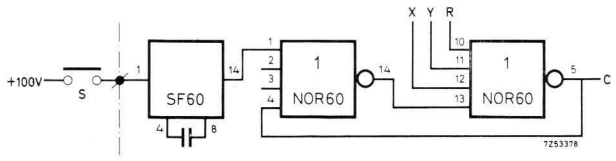


Fig. 3.11. Switch S must first be closed before an output is obtained.

Where more than one supply is used, extra precautions should be taken to minimize the consequences of failure of one of the supplies.

4 Interconnection Methods and Hardware Accessories

To allow the blocks to perform their functions correctly and reliably, proper interconnections must be made between them. The 60-Series is so designed that a variety of interconnection methods is possible, and the following sections give these, together with some brief data on the hardware accessories available, such as mounting chassis and heat sinks.

4.1 Connection of Individual Blocks

The blocks may be bolted to metal strips as in Fig. 4.1 or to other surfaces. Connections between the blocks may then be made with insulated wire by point-to-point soldering or by wire-wrapping, as given in Section 4.3.

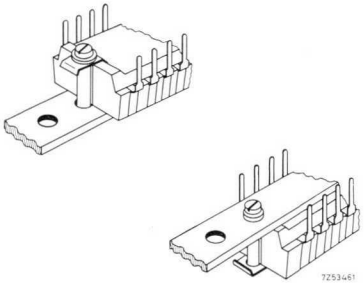


Fig. 4.1. Individual assembly.

A more convenient method is to use the Universal Mounting Chassis, UMC60 (shown in the frontispiece).

The connection of individual blocks — while having the advantage of being flexible in layout — is, however, not the easiest system to service, due to the time which can be lost when trying to locate a faulty unit. This method is therefore mainly of interest to the designer as a good way of bread-boarding a prototype circuit, or for systems which are to be used in an area where service is readily available, and down time is not going to be too expensive. If the method were to be used in series production, then it is essential that full documentation be made of the system to aid in servicing. It is advisable also to provide a few extra units, to cater for future expansion or to serve as spares.

Compatible boards, chassis and connectors

board			chassis	connector		
type abbr.	cat. no.	circuit block accommodation	cat. no.	number of contacts per connector	type abbr.	cat. no.
PWB60 or PWB60/P	4322 026 39920 4322 026 39930	10, size A	4322 026 38230 standard	2×22 0,156″ pitch	FO47 or FO50 or FO53 *	2422 037 62212 2422 037 12212 2422 039 12212
PWB61 or PWB61/P	4322 026 39940 4322 026 39950	10, size A	. . . 38240 standard	2×23 (0.2″ pitch)	FO45 or FO45 *	2422 020 52591 2422 035 52312
GPB60 or GPB60/P general purpose	4322 026 38600	size A size B 10 0 8 1 5 2 3 3 0 4				2422 020 52591
	4322 026 38610	as for . . . 38600				
SRB60 shift register	4322 026 39640		. . . 38240			
PWB62 or PWB62/P miniature	4322 026 39651	4, size A 2, size B	. . . 38250 miniature	2×32 (0.1″ pitch)	female connector provided with panel	

* modified wrap

4.2 Printed Wiring Board Assembly

Assembly of the circuit blocks on a printed wiring board (PWB) can offer benefits over individual assembly in many cases. Three types of board are available:

standard types (PWB60 and PWB61 and General Purpose Boards);
special types;
miniature boards for "terminal logic" (PWB62).

PWB Assembly has the great advantage for quantity production that all circuit block connections on a board are made in one go, compared to the one-terminal-at-a-time method of individual assembly. This process makes use of dip-soldering and is described in detail in Section 4.3.

A second advantage of PWB assembly is that servicing is greatly simplified. If each board is designed to perform a single function, then it is usually an easy matter to pinpoint a faulty board and replace it by another in the case of a fault. In this way, replacement stocks can be reduced, and servicing and down-time greatly cut.

Special connectors are available by which the boards may be connected into the complete system. Where a number of boards are to be stacked together, a chassis should be used. The Table on p. 31 gives the compatible chassis, connector and board combinations.

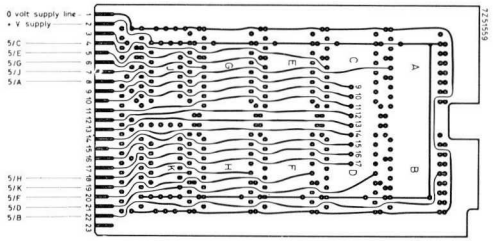
4.2.1 The Standard Types

The boards are pre-drilled to accept the standard blocks, the holes being plated through to pads on both sides of the board. Additional, undrilled tinned pads are provided on one side of the board, the other side having a pattern of conductors.

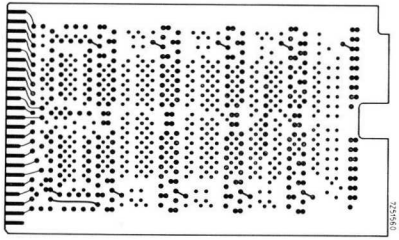
PWB60; PWB60/P; PWB/61; PWB61/P

It will be found convenient to allocate identifying letters (say *A* to *K*) to the 10 block positions. It facilitates the identification of the terminals of individual circuit blocks, as illustrated in Fig. 4.2. PWB60 has 2×22 terminals, and PWB61 has 2×23. Figs 4.3 and 4.4 show the dimensions of the PWB60 and PWB61.

One output of a 2.NOR60 or 2.IA60 (or the output of an IA60 used as a Low Power Amplifier) is brought out by tracks connecting point number 5 of each location to an edge contact. It is important to note that in the case of a switch filter this point would be the 100 V input, which



a



b

Fig. 4.2. The PWB61. (a) track side; (b) pad side,

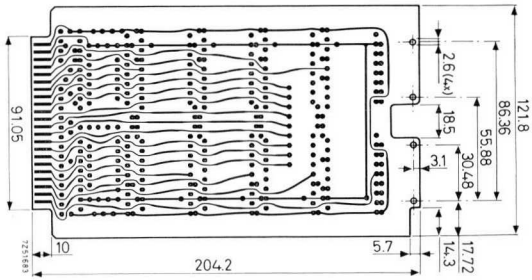


Fig. 4.3. Dimensions, PWB60

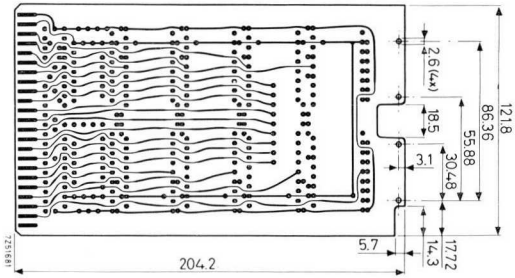


Fig. 4.4. Dimensions, PWB61

emphasises the need for polarizing keys to prevent inadvertant reversal of a board and consequent damage to the circuits.

Pad No. 7 of each position is bridged to the positive track so that both units of a 2.NOR60 are provided with a supply. In the event of a 2.NOR60 being wired for collector-OR operation, this track should be cut. The pads for the circuit block wires are so arranged that they may be interconnected by bare copper wire 0.2 mm diameter. Insulation is necessary, of course, where pads or wires must be crossed (see Fig. 4.5).

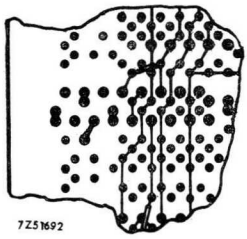


Fig. 4.5. Printed pad connections

Additional double pads are provided at positions *A* and *B*, which facilitate the connection of external resistor-capacitor networks for timers if they are mounted in these positions.

Edge contacts 9 to 17 inclusive are connected by tracks to pads adjacent to positions *A B C D*, which obviates the need for long connecting wires from these positions.

Separate components can be mounted in the holes between circuit block positions, supply voltage being taken from holes in the positive and negative tracks. Positions *J* and *K*, nearest the edge connector, are provided with a number of holes for separate components in the event of these positions not being used for circuit blocks.

PWB60 and PWB61 are of glass-epoxy material, PWB60/P and PWB61/P of phenol paper.

General Purpose Boards GPB60, GPB60/P

These boards provide mounting facilities for up to 10 standard 60-series blocks as well as for PA60 units. If used for PA60s alone they will accommodate up to 4. Alternatively, combined assemblies can be made, as shown in the Table on p. 31. Fig. 4.6 shows the GPB60.

It is essential that the blocks be mounted on the track side of the board and in such a way that terminal 9 (0 V terminal) of the blocks is inserted in the innermost of the tracks that run along the three sides of the board. It is recommended that the two inner tracks be paralleled to reduce line impedance.

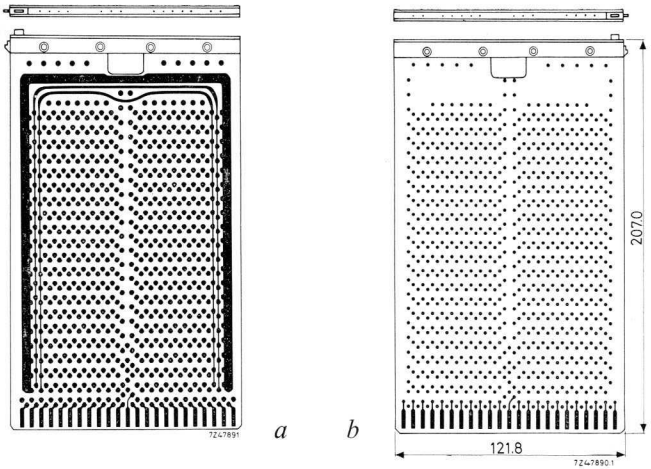


Fig. 4.6. The GPB60 with extractor. (a) track side; (b) pad side

Apart from their main purpose these boards may also be used for miscellaneous components, thus enabling a whole system to employ compatible racks and connectors.

GPB60 is glass-epoxy and GPB60/P of phenol paper.

4.2.2 Special Boards

If a large quantity of a particular function is to be made, it may be well worthwhile to consider manufacturing a special board for the purpose. One advantage is that if the prototype has proved to work correctly then all the production models will have a very high chance of doing likewise. Moreover, above a certain quantity the cost drops below that for individual assembly. Once knowing the assembly cost of the standard PWB, it is easy to calculate whether a function should be standardized to give the lower production cost and shorter assembly times of the special PWB. Cost quotations may be obtained from the manufacturer.

4.2.3 Miniature Board PWB62 and Terminal Logic

Terminal logic is a technique which, when properly applied, can combine the advantages of all the other methods. The miniature board (termed PWB62) can accomodate four Size A blocks (e.g. 2.NOR60) or two

Size B blocks (PA60). All terminals of each block are brought to the female connector 4332 026 10920 on the board according to the diagram (Fig. 4.7), which shows both sides of the board with connector numbering. The Table opposite relates the connector numbering with the terminal numbers of the circuit blocks.

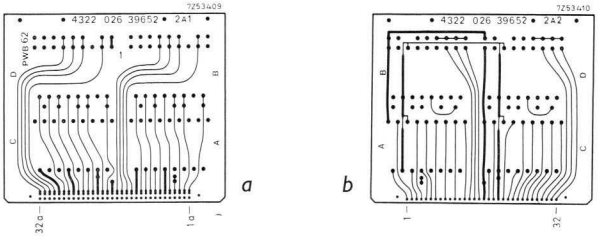


Fig. 4.7. The PWB62. (a) track side, (b) pad side

The units are mounted on the boards so as to give as many similar boards as possible. Units are then interconnected (by wire wrapping) at the connector terminals, hence the term "terminal logic". Advantages are:

— very little detailing of panel lay-out required;
— systems can be built from a few standard panels, reducing reserve stock quantity necessary;
— interconnection wiring can be done by unskilled labour using wire-wrap techniques. (Use male connector Cat.No. 2422 025 89082.) For large quantities, back panel inter-wiring may be advantageous; here, the male connector Cat.No. 2422 025 89083 should then be used with a special mounting strip;
— system documentation can be greatly simplified.

4.3 Soldering and Wire-wrapping Procedures

4.3.1 Point-to-point Soldering

Never use soldering paste or liquid flux. They contain an acid that is apt to damage the components and the printed circuit irreparably. Use only resin-cored solder containing 60% tin and 40% lead.

Use a small soldering iron consuming about 30 W, fitted with a pointed bit. A heavy, hot iron will char the resin-bonded paper assembly board. Using an iron for an excessively long time is not only pointless but harmful. Apply the hot iron and the cored solder to the joint simultaneously.

block in position	terminal number of block	connector number component side	connector number solder side	block in position	terminal number of block	connector number component side	connector number solder side
A	1		13	C	1		29
	2		11		2		28
	3		9		3		26
	4		7		4		24
	5		6		5		23
	6		4		6		21
	7		20		7		20
	8		2		8		19
	9		17		9		17
	10	12a			10	28a	
	11	10a			11		27
	12	8a			12		25
	13	6a			13	25a	
	14		5		14		22
	15		3		15	22a	
	16		20		16	20a	20
	17		1		17		18
B	1		16	D	1		32
	2		15		2		31
	3		14		3		30
	4	16a			4	32a	
	5	15a			5	31a	
	6	14a			6	30a	
	7		20		7		20
	8	13a			8	29a	
	9		17		9		17
	10				10	27a	
	11	11a			11	26a	
	12	9a			12	24a	
	13	7a			13	23a	
	14	5a			14	21a	
	15	3a			15	19a	
	16	2a	20		16		20
	17	1a			17	18a	

The solder will start to run, and after about three seconds there will be ample liquid solder on the joint. Now take the solder away and, as soon as the joint is properly covered, remove the iron. Do not allow any of the soldered parts to move for at least five seconds after the iron has been removed; a good idea is to blow on the hot joint to cool it more quickly. The solder is not settled until its shiny surface becomes dull. The joint is then finished.

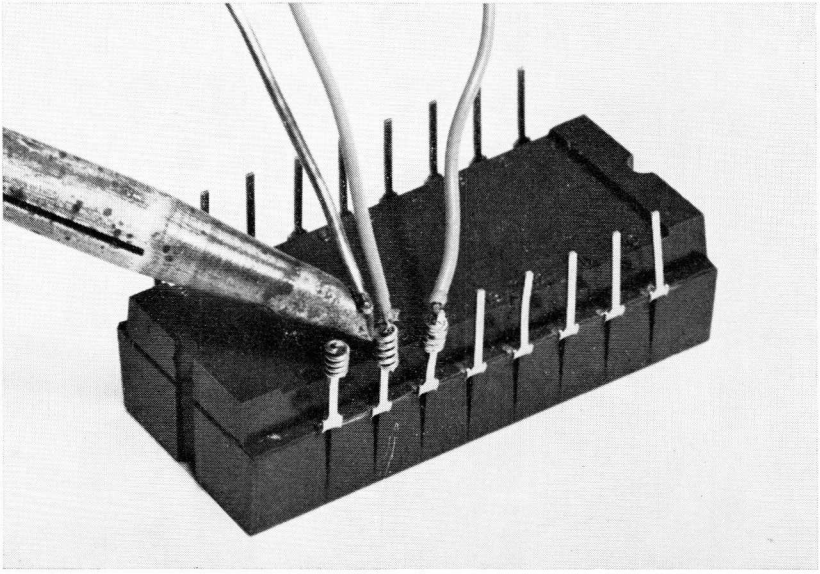


Fig. 4.8. A method of supporting the joint for soldering, using a small spiral of wire. At left, the spiral is placed on a pin. Centre, the connecting wire end is placed inside the spiral. Right, solder is applied to fill the spiral.

It is impossible to make good soldered joints with a dirty bit. Remove soiling and any surplus solder from the hot bit by brushing it quickly with a clean cloth. Never touch any surfaces to be soldered with your fingers.

The connector wires on components should be clean and ready for soldering. Occassionally, however, piece of insulating material adhere to the wires and these should be carefully scraped off. Fig. 4.8 shows a way in which the joint can be supported while soldering.

4.3.2 Wire Wrapping

Wire wrapping, a solderless method of making connections, has proved very successful. The joint is made by wrapping a number of turns of wire around the pin with a special tool. The wire must be bare or PVC-insulated single strand copper. The best general purpose gauge is 0.4 mm (0.0159 in.). This diameter is the maximum permissible. This may safely

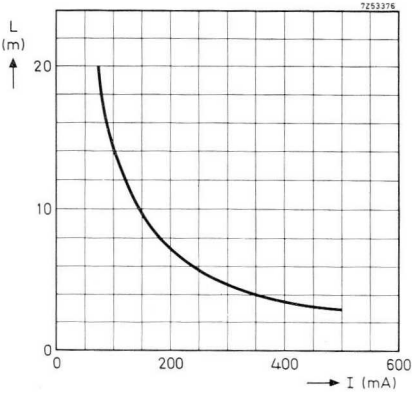


Fig. 4.9. Relationship between length L of 0.4 mm diameter wire and safe working current I (maximum 500 mA).

be used for all logic wiring with the exception of PA60 output and pin 10 connections. Care must be exercised, when commoning 0 V and +24 V pins, that the voltage drop due to wire resistance does not exceed 0.2 V. The graph shown in Fig. 4.9 gives safe working currents for lengths up to 20 m. Two wrap joints per pin may be made. The PA60 output (terminal 13) and 0 V (terminal 10) connections may be made by connecting two 0.4 mm diameter wires in parallel.

Hand, electric (battery or mains) and pneumatic tools are available. The power tools are generally better in that the wrapping speed and hence wire tension are controlled automatically. For reliable joints at least six complete turns of wire must be wrapped onto the pin. This entails stripping off insulation to a minimum of 2 cm with 0.4 mm wire.

Two types of simple wrap joint are in use. A "standard bit" wraps only the bare wire round the pin, whilst a "modified bit", besides wrapping the bare wire, provides a wrapped insulation turn. Note that six turns of

bare wire are still required for the modified wrap. The latter technique is preferable as it gives much better resistance to vibration. It incurs no price penalty, and the pin will still accomodate two wraps*. (Fig. 4.10)

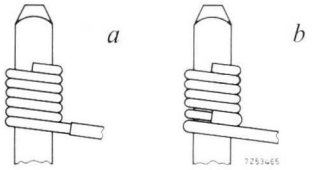


Fig. 4.10. Wire wraps. (a) standard; (b) modified.

4.3.3 Dip Soldering

Dip soldering is the term given to the operation in which all the components on a printed wiring board are connected simultaneously by dipping it in a bath of liquid solder.

Prior to soldering, the boards should be dried in order to make sure that the plated-through holes will be filled with solder and that the solder fillet will not show blow-holes or open cracks. Drying should be done in two stages: (1) Prior to mounting components, allow the boards to dry for at least 12 hours at a temperature of 105 °C. Subsequently mount the components on the boards and prepare for soldering within 3 days. If this is not feasible, store the boards immediately after drying at 65 °C. (2) After having mounted the components, dry the assembly for at least 15 hours at 65 °C.

The next stage is to spray the boards evenly with flux. Place the boards edge to edge in racks so that, when spraying the pattern side, no flux can settle on the components mounted on the opposite side of the board. Connect the gun to compressed air of 1.5 atmosphere and at a regular speed of approximately 50 cm/s move the gun from left to right and back again at a distance of approximately 40 cm from the boards. Start and finish spraying beyond the board so that it is evenly sprayed up to the edge. Allow the sprayed boards to dry in air for at least 45 minutes to (but preferably not more than 3 hours) to prevent evolution of gases during dip soldering.

The final stage is the soldering operation itself. Cover the connector

* A complete wrapping assembly consists of a tool, bit and sleeve. The *Gardner-Denver Company* make a suitable tool. The bit and sleeve size vary according to the wire size in use and method but will all fit into any tool. For a wire size of 0.4 mm, use bit numbers 505 279 (standard wrap) or 506 445 (modified wrap).

contact area with Teflon strip, to prevent soldering of the contacts, and place Teflon wire in holes which are not to be soldered. Clamp the boards in a non-solderable holder (e.g. of stainless steel) and dip in solder for 5 seconds as shown in Fig. 4.11 (temperature of the solder bath should be 240 °C) to allow the solder to flow up through the plated-through holes. Since Teflon gives off dangerous fumes when heated, adequate precautions must be taken.

At regular intervals clean the dross from the bath, using a flux-wetted spatula. Just before dipping deposit a few drops of flux on the solder.

After the soldering process has been completed, clean the board carefully with a cleaning agent such as Teepol and rinse with pure water. Dry the board for three hours at 65 °C. Handle the board only by the sides.

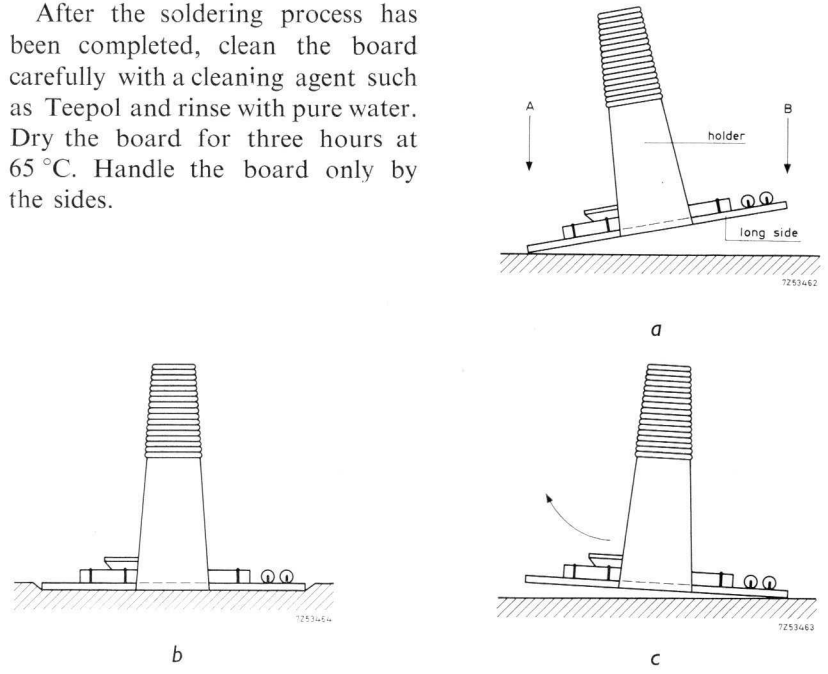


Fig. 4.11. (a) When placing the board onto the solder surface, be careful not to make a sliding movement but to lower the board at B as soon as it touches the surface at A. The gold-plated terminals must always touch first. (b) The board will tend to warp while heating up, therefore apply some pressure on the board so that it touches the surface completely and the top side is flush with the solder surface. Solder in this position for 5 seconds. (c) The soldering operation being finished, withdraw the board from the bath with a sliding movement to remove excess solder.

4.4 Hardware Accessories

4.4.1 Chassis

The chassis mentioned in Section 4.2 are supplied in kit form. All are assembled similarly to the Type 4322 026 38240 which is described in detail below. Fig. 4.12 shows the three chassis types.
For correct assembly the following aids are recommended:
aligning kit, catalogue number 4322 026 38440, including: 4 aligning pins, 1 aligning plate and a dummy printed-wiring board;
polarizing key for aligning of the connectors;
screw driver for pan-head screws;
spanner with 7 mm jaw.

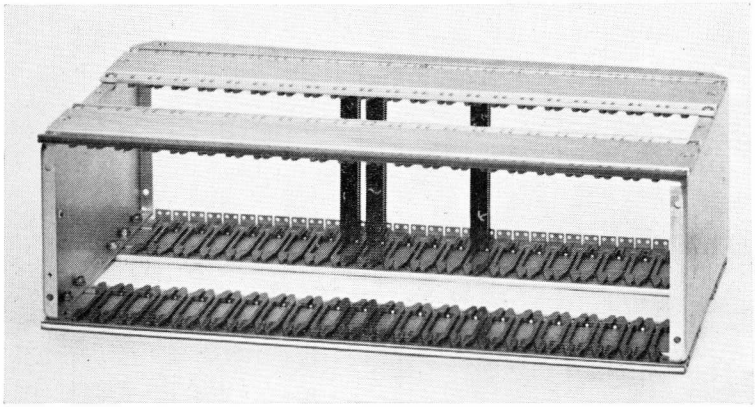


Fig. 4.12a. Chassis Type 4322 026 38240.

Attach a connector rail to a profile strip by means of 2.6 mm bolt (5 mm long) and a washer, see Fig. 4.13. Use the middle one of the mounting holes.

In the same way attach the other connector rail to a profile strip. Attach both side plates to the profile strip by means of four 4 mm bolts (10 mm long) and twelve 4 mm bolts (8 mm long), see Figs 4.13 and 4.14. Do not tighten these screws and do not yet insert the countersunk screws, as the profile strips have to be aligned first.

If the chassis is intended to be used for printed-wiring boards with a length of 207 mm, mounting has to be done as in Fig. 4.14; for printed-

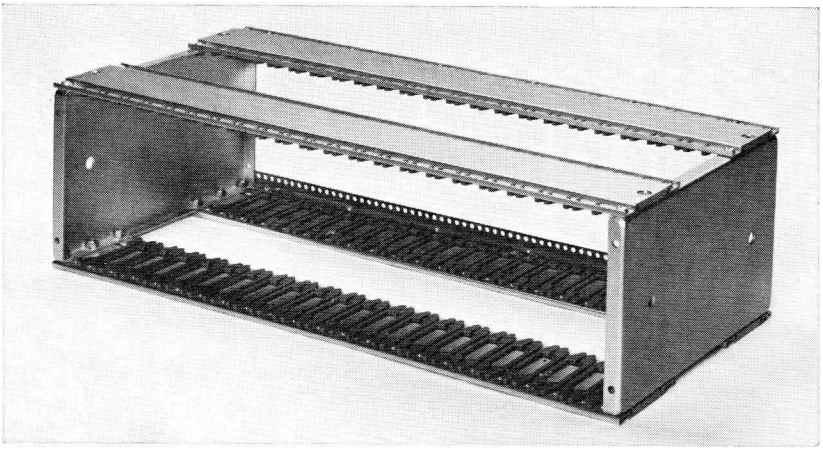


Fig. 4.12b. Chassis Type 4322 026 38230.

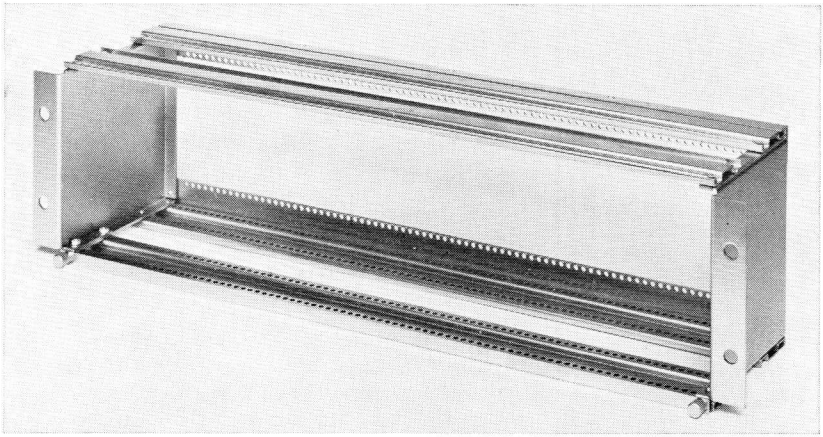
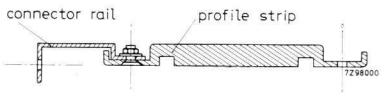


Fig. 4.12c. Chassis Type 4322 026 38250 (miniature).

wiring boards of 180 mm length the chassis has to be mounted as shown in Fig. 4.15.

Fig. 4.13



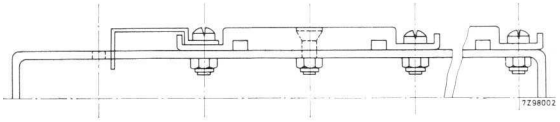


Fig. 4.14

Insert the four aligning pins in the holes which are to take the countersunk screws later on. Slip the aligning plate on the pins and tighten the eight screws on one side of the chassis. Take care that the connector rails remain aligned. Remove the plate, slip it on the pins at the other side of the chassis and tighten the eight screws on that side.

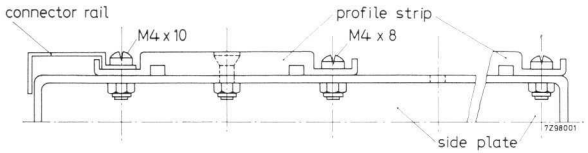


Fig. 4.15.

Remove the aligning plate and the aligning pins and insert the countersunk screws.

The pairs of profile strips should now be equidistant at 122.6 mm for easy accomodation of the printed-wiring boards. Snap the board guides into the desired holes of the profile strips in such a way that the round recesses face the outside of the chassis. If necessary the recesses can be colour coded.

For a symmetrical disposition of the printed wiring boards, do not use the first hole in the mounting strip.

Place the printed-wiring connector in the slots formed by profile strip and connector rails. Fit it by means of two 2.6 mm cylindrical screws (6 mm long) and washers. Do not tighten these screws either, as the connector has to be aligned first. Apply the polarizing key in the appropriate position in the connector (see the slots in the dummy printed-wiring board). Insert the dummy printed-wiring board in the connector and tighten the screws. Remove the board and the polarizing key.

The chassis can be fitted in a 19″ rack by means of two brackets, catalogue number 4322 026 38450. These brackets must be fastened to the chassis with two screws with self-locking hexagonal nuts. For mounting a stack of chassis in a rack, special brackets must be used, the length of the brackets depending on the number of chassis. If several chassis are to be mounted on top of each other, the profile strips of adjacent chassis should be bolted together, and the bottom strips of the lowest

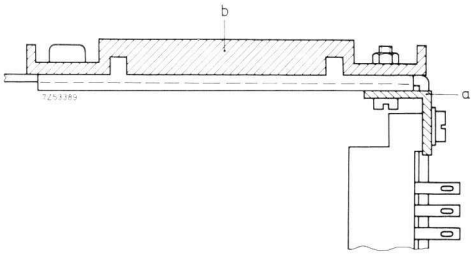


Fig. 4.16. Chassis 4322 026 38230 detail, (a) connector rail, (b) profile strip

chassis must be supported in the middle.

Construction details of the chassis differ slightly, the main difference being in the connector rails. The chassis Type 4322 026 38230 has the connector rail mounted as shown in Fig. 4.16.

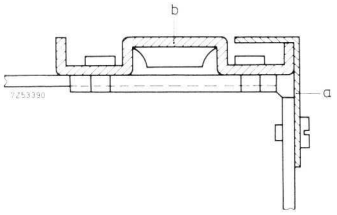


Fig. 4.17. Chassis 4322 026 38250 detail. (a) connector rail, (b) profile strip (not to scale)

The miniature chassis Type 4322 026 38250 has its connector rail mounted as in Fig. 4.17.

4.4.2 Heat sinks

The heat sinks shown in Figs 4.18 and 4.19 contain a central hole for the cable bundle and a smaller hole for mounting a semiconductor device. A third hole allows the pins of a device on a nearby heat sink to be accommodated, thus saving space. The dimensions of the heat sinks are such as to allow mounting on a printed wiring board, as shown in Fig. 4.20. The heat sinks can be mounted on both sides of the board, if adequately insulated.

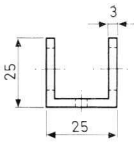
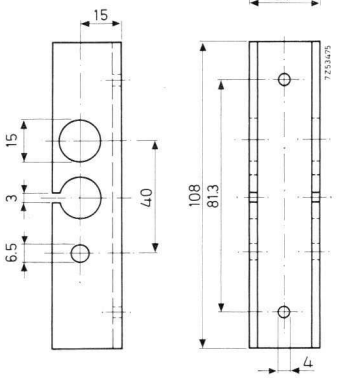


Fig. 4.18. Heat sink, Cat.No. 8222 290 7105.



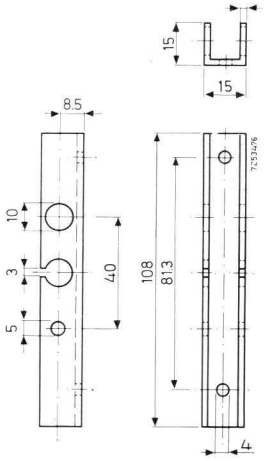


Fig. 4.19. Heat sink, Cat.No. 8222 290 7112.

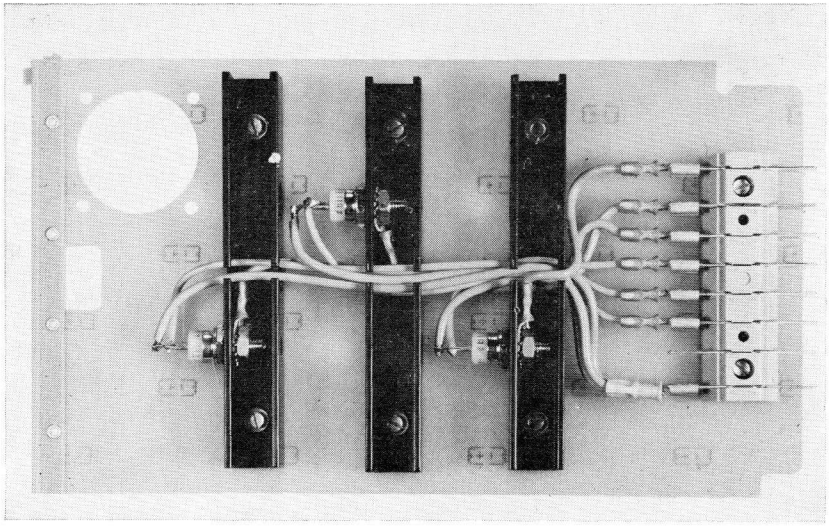


Fig. 4.20. Small heat sinks mounted on a PWB.

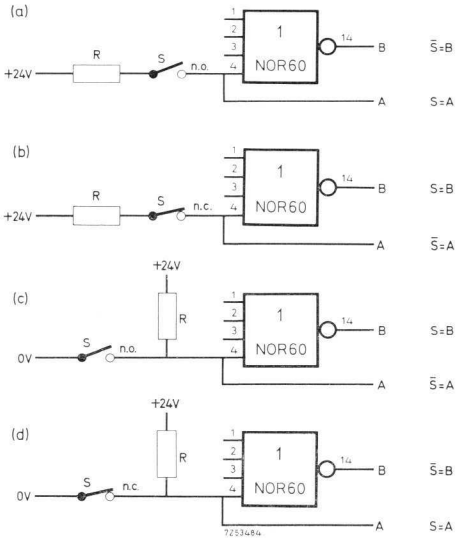
The larger heat sink (Cat.No. 8222 290 7105) has a thermal resistance of not greater than 4.5 deg C/W at 7 W dissipation, and will accept for example, Type BTY91 thyristors. The smaller (Cat.No. 8222 290 7112) has a thermal resistance not greater than 8 deg C/W at 4 W dissipation, and accepts, among others, Type BTY79 thyristors or BYX38 diodes.

5 Input Devices

An "input device" is needed to convert information about a situation into usable signals. Two main categories, electromechanical and electronic input devices, may be distinguished.
All electromechanical input devices have in common that a change in input condition is signaled by the opening or closing of a mechanical switch.

5.1 Electromechanical Input Devices

Four ways of connecting a switch to the logic circuitry are given in Fig. 5.1. S denotes operation, either opening or closing, of the switch. $\bar{S}$ means that the switch remains in the position shown.



The value of resistor R determines the current available to drive the logic (given here in Drive Units). If R is made 0 Ω (not possible in cases *c* and *d*) the loadability depends only on the capacity of the power supply.

Fig. 5.1. Mechanical switch arrangements.

R	available DU
7.5 kΩ (0.25 W)	6
2.2 kΩ (0.5 W)	20
1.1 kΩ (1 W)	40

It will be noticed that, logically speaking, cases *a* and *d*, and cases *b* and *c*, are identical. However, in cases *a* and *c* the switch contact is normally open, and in *b* and *d* it is normally closed. The configuration to be used will depend on the application. As contact surfaces become dirty after a while, *a* or *c* should not be used in an alarm circuit, but they are recommended to ensure continuity of service, as a dirty contact will then have no effect.

Thumbwheel switches, giving the possibility of logic programming are available (see Chapter 14).

No measures have been taken in these circuits to eliminate contact-bounce or reduce "noise" which can interfere with the logic system if long input wires are used. Terminating the line at the logic input with a small capacitance of 10 to 100 nF will often be sufficient. If these effects are a problem (discussed more fully in Chapter 6) the dual switch filter 2SF60 should be used. Each switch filter normally requires 100 V d.c. input, and delivers 2 DU. (For operation at other voltages, see Chapter 2.)

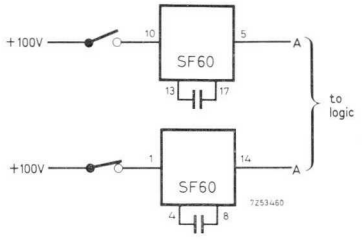


Fig. 5.2. Use of switch filter.

Various methods are available for operating a mechanical switch automatically or remotely. The common relay, too well known to need comment, is one; two others are given below.

The Iron Vane Switched Reed (IVSR, Fig. 5.3) contains a magnet and a reed switch with normally closed contacts. If an iron vane of suitable dimensions is passed through the gap in the sealed IVSR housing, the magnetic field through the reed is reduced to such an extent that the switch opens.

The IVSR has application as a limit switch, position indicator, or signal source (low speed). It is free of most of the difficulties encountered with conventional switches and can successfully replace micro-switches. Input voltages up to 32 V d.c. (0.1 A) may be used. It is obvious that the IVSR should not be used in environments where iron dust or scraps might impair its operation.

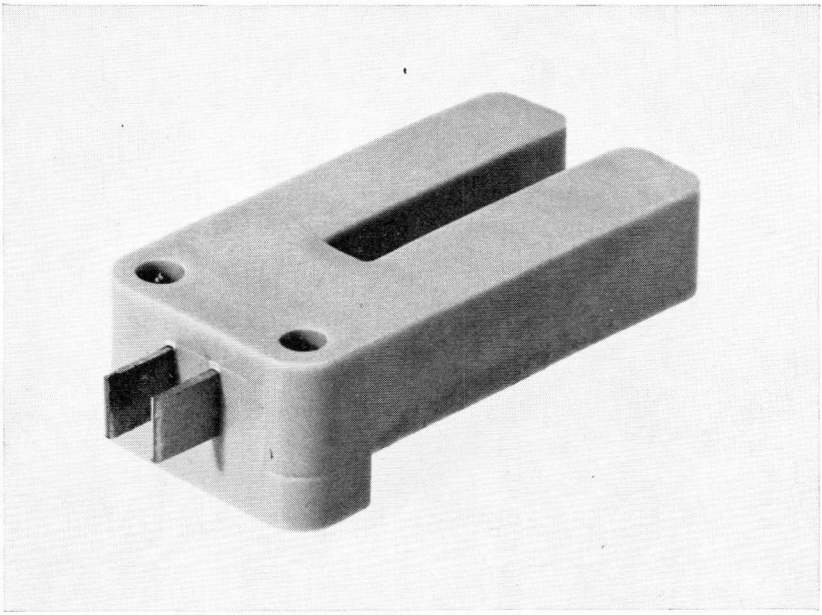


Fig. 5.3. The IVSR and drawing symbol.

The Magnetic Proximity Detector (MPD, Fig. 5.4) contains a reed switch placed in the balanced magnetic field of two magnets. When the field is disturbed by the presence of ferromagnetic material, the contacts close. Applications are as a detector for the presence, passage, or positioning of ferrous objects such as levers, tool holders on machines and elevator cabins. Detection range of 17 mm from the sensitive face of the MPD allows ease of mounting. The maximum input voltage is 100 V d.c. (25 VA max.).

It should be realized that capacitance directly across the contacts of any switch can be the cause of excessive currents through the switch at the moment of closing the contacts. This should be avoided by placing a resistor (Fig. 5.5) in series with the switch contacts and close to it (i.e. not at the power supply end of the line). A typical value is $R = 7.5\ \text{k}\Omega$.

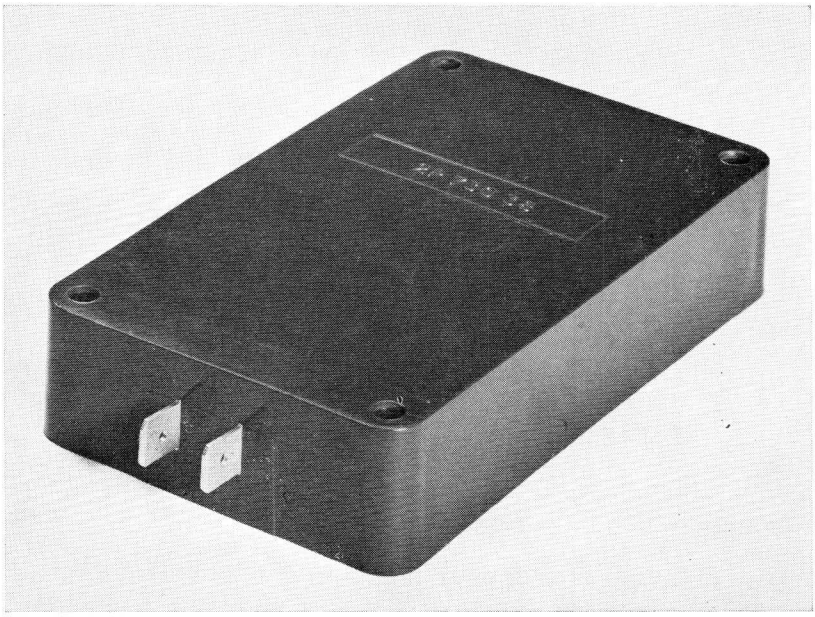


Fig. 5.4. The MPD and drawing symbol.

Switch contacts can be connected to give either output voltage or no output voltage, as illustrated in Figs. 5.5*a* and *b* respectively, at contact closure.

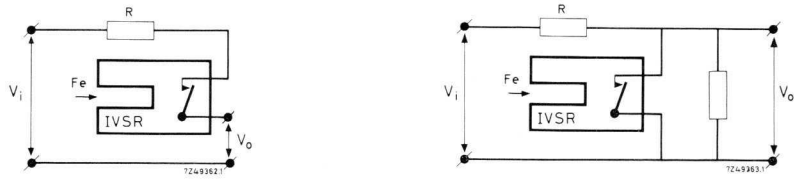


Fig. 5.5. Contact connection methods.

5.2 Electronic Input Devices

Electronic input devices have great advantages Contact-bounce problems are eliminated; hardly any maintenance is required and reliability is excellent. Four types are described below. For specifications, see Chapter 14.

Input cables should be shielded (shield connected to ground of the logic at the cabinet) and terminated with an *RC* filter at the cabinet. The *RC* product should be made as large as possible, consistent with system speed requirements.

The Vane Switched Oscillator (VSO, Fig. 5.6) has the circuit shown in Fig. 5.7. The left-hand part of the circuit is an oscillator. The coils L_1 and L_2 are physically separated by the gap in the VSO. A piece of metal between L_1 and L_2 will reduce the feedback from L_2 to L_1 and consequently the voltage over L_3. This voltage is rectified and filtered. The positive voltage at terminal 3 will then be reduced with respect to that at terminal 4.

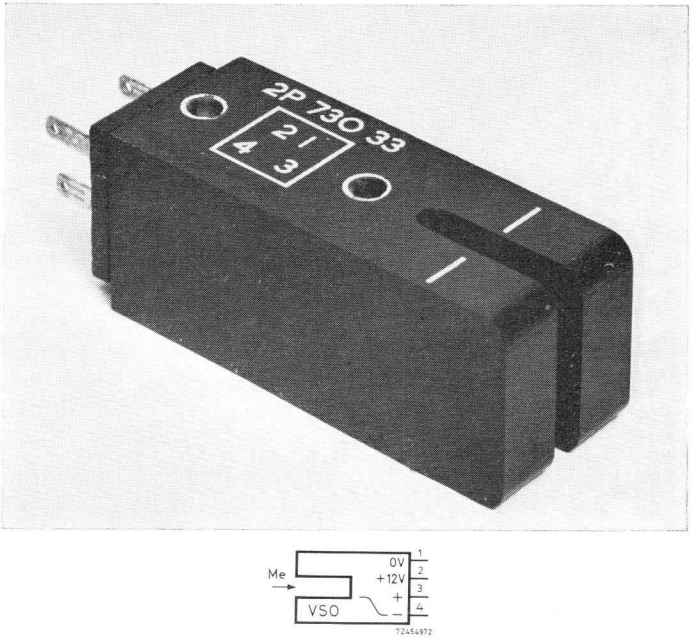


Fig. 5.6. The VSO and its drawing symbol.

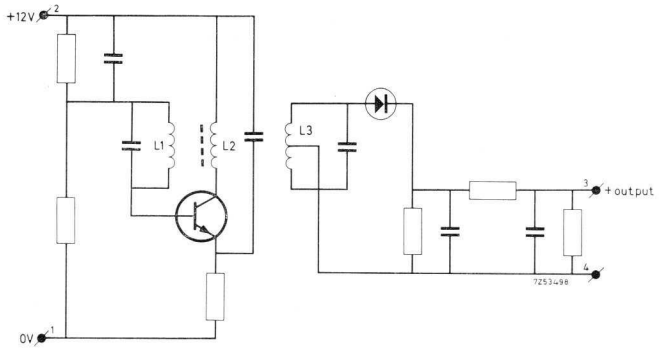


Fig. 5.7. Circuit diagram of the VSO.

The supply voltage of $+12$ V $\pm$ 10% may be obtained from the logic supply (current drain: 12 mA). Fig. 5.8 shows the method of connection to a NORBIT: four inputs must be paralleled. The output can drive 6 DU.

The unit is capable of detecting objects passing at a frequency of 1 kHz. Any metal can be used for the activating vane. These characteristics open up a wide field of application: revolution counting, angular position control, counting of small objects, foil continuity checking and so on.

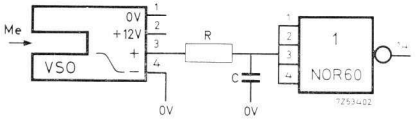


Fig. 5.8. Connection method for the VSO. $R \leqslant 2200\ \Omega$. Maxtmum working frequency 100 Hz for $R = 2200\ \Omega$ and $C = 0.47\ \mu F$.

The Electronic Proximity Detector (EPD, Fig. 5.9) has the circuit shown in Fig. 5.10. TR_1 and L_1 and L_2 form an oscillator which is coupled to the detector stage TR_2. Normally TR_2 rectifies the oscillator voltage, thereby making the base voltage of TR_3 negative with respect to its emitter (TR_3 conducting). This brings the output voltage to about $+12$ V. Reducing the oscillation by inserting a metal object (its shape is irrelevant) into the field of the sensing coil reduces the output voltage.

The supply voltage is 12 V $\pm$ 5% (current drain 16 mA), the operating frequency is 1 kHz. Fig. 5.11 shows the method of connection to a NORBIT, two inputs should be paralleled. The EPD is well suited to detect the presence (e.g. of containers, workpieces, metal parts) or the passage (for counting or programming) of electricially conductive objects.

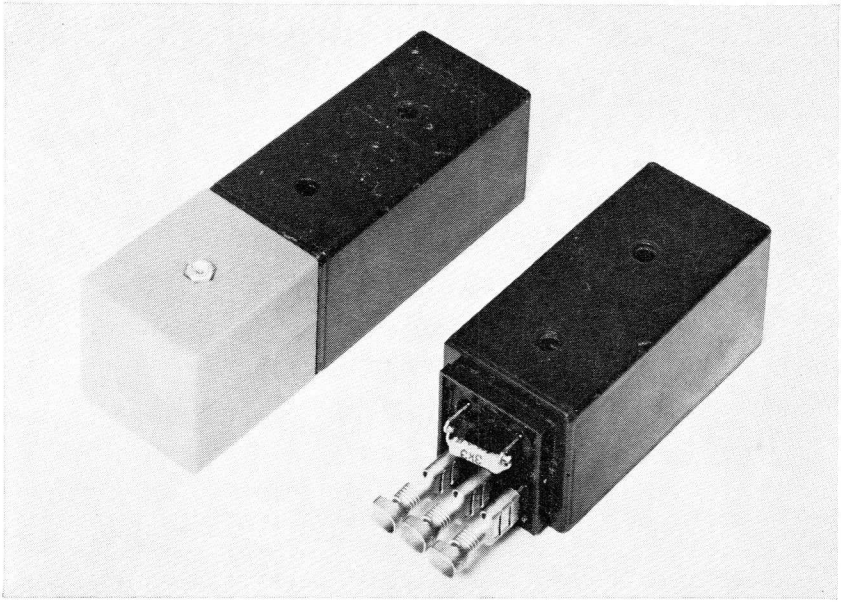


Fig. 5.9. The EPD and its drawing symbol.

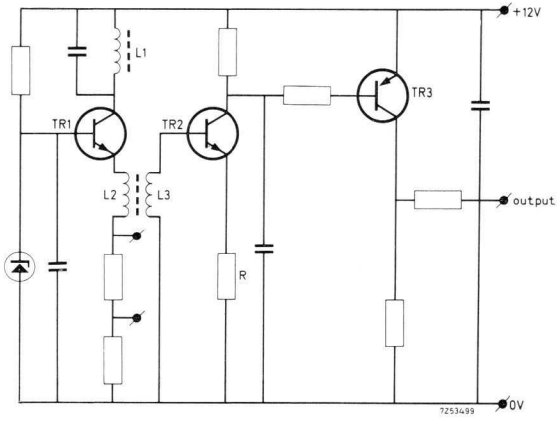


Fig. 5.10. Circuit diagram of the EPD.

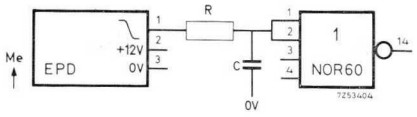


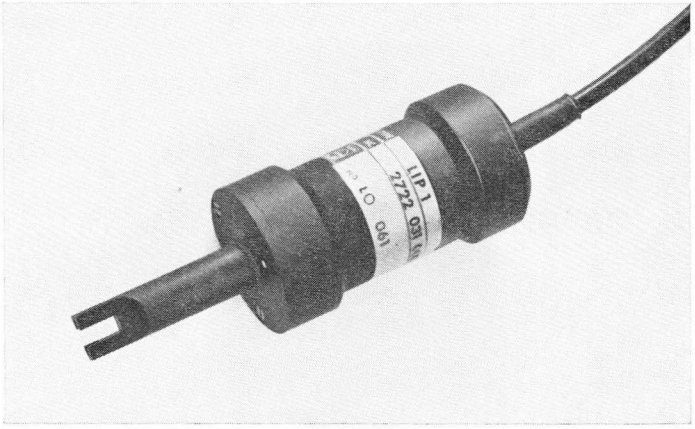
Fig. 5.11. Connection method for the EPD $R \leqslant 3300\ \Omega$

R	*C*	f_{max}
3300 Ω	*470 nF*	*66 Hz*
3300 Ω	*47 nF*	*660 Hz*
1000 Ω	*100 nF*	*1000 Hz*

The Light Interruption Probe (LIP1, Fig. 5.12) consists of a lamp and photosensitive element using a novel optical system, and an emitter follower output stage, all contained in a brass housing. If a small object intercepts the light beam across the gap at the end of the LIP1, the output voltage (which is normally low) will go high.

The supply voltage is 12 V $\pm$ 5% (current drain: 180 mA), the maximum detection frequency exceeds 10 kHz.

The LIP1 will find wide applicability in the fields of accurate position control and revolution counting owing to its fast response and sensitivity to small objects.



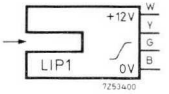


Fig. 5.12. The LIP1 and its symbol.

Fig. 5.13 shows the circuit connections. When connecting to NORBITS all the latter's inputs should be paralleled.

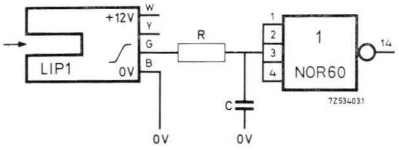


Fig. 5.13. Connection method for the LIP1. The RC product should be made as large as possible

The Photo Electric Detector (CSPD, Fig. 5.14) has an acryl-butyl-styrene housing and contains a cadmium-sulphide cell with a lens at one end. The maximum permissible voltage across the cell is 150 V, the maximum detection frequency is 6 Hz.

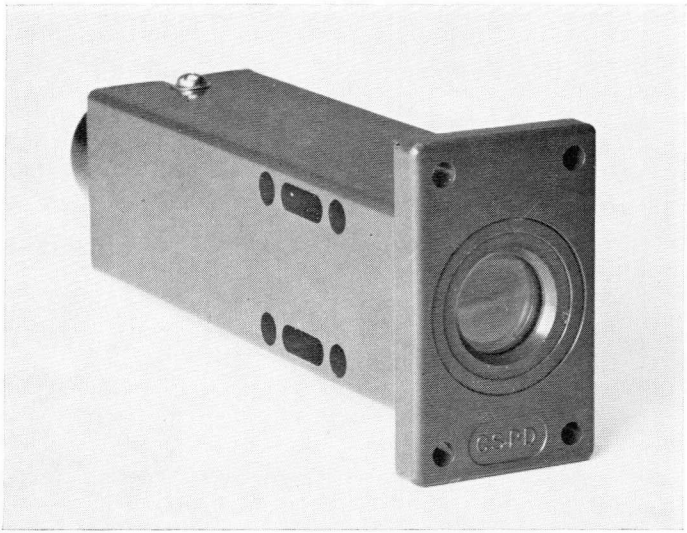


Fig. 5.14. The CSPD.

The CSPD is intended to be used with the lamp unit, 1MLU. With an ambient illumination level of 500 lux a resistance ratio of 10 to 1 or more can be obtained.

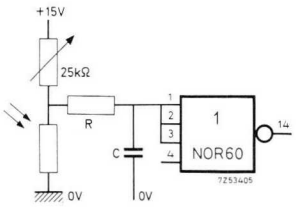


Fig. 5.15. Connection method for the CSPD. $R < 3300\ \Omega$, RC should be as large as possible.

The connection method for the CSPD is given in Fig. 5.15; NORbit connection is made by paralleling 3 inputs. Resistor R must have a value such that the voltage drop across the CSPD is less than 0.3 V in the non-conducting state of the subsequent NOR.

6 Noise Considerations

Noise is usually defined in this context as interference consisting of spurious and unwanted electrical signals of arbitrary magnitude and character. Incorrect working of the equipment may result if the "signal-to-noise" ratio is not high enough. Noise can originate from a number of sources, but usually it can be reduced to acceptable levels simply by correct positioning of the system and its components. Although the 60-Series is relatively insensitive to interference when compared with other types of control, care must nevertheless be taken to guard against it.

Noise can enter the logic system in two ways: conduction through input, output and supply wires (Section 6.1), and induction directly from strong external magnetic and electric fields, caused for example by neighbouring power lines (Section 6.2). Section 6.3 discusses internally generated noise and Section 6.4 deals with grounding methods.

6.1 Noise Entry through Connecting Wires

6.1.1 Noise from Input Devices

An electromechanical switch can always be expected to produce a lot of noise, especially when it is operating. Here the switch filter 2.SF60 should be used, with an RC time of 0.01 s to 0.1 s. The switching speed of mechanical input switches is normally so low that a suitable low-pass filter can be incorporated in the input line. The filter must have an RC product of 0.01 s to 0.1 s to integrate noise at the input lines sufficiently (see Fig. 6.1). Here, the sum of $R_1 + R_2$ is the equivalent of R in the input device connection circuits of Chapter 5).

The filter can be mounted near the logic circuit where the input signal is fed-in (ground of filter connected to ground of logic, or preferably to ground of system), but a better solution is to mount all the input filters on printed wiring boards in a separate corner of the rack. The latter solution prevents noisy wires coming into the neighbourhood of the logic circuitry. In very severe cases the filters must be mounted inside the cabinet just where the input wires enter. The 0 V return wire from the switch must be connected to the System Ground Point (SGP) in order to transport noise energy picked up by this wire directly to ground. If the plus of the logic supply is to be connected to the switch as in Fig. 6.1*b*, this wire must be connected to the plus output terminal of the supply. This applies also to terminals 8 and 17 of the Switch Filter. (For safety

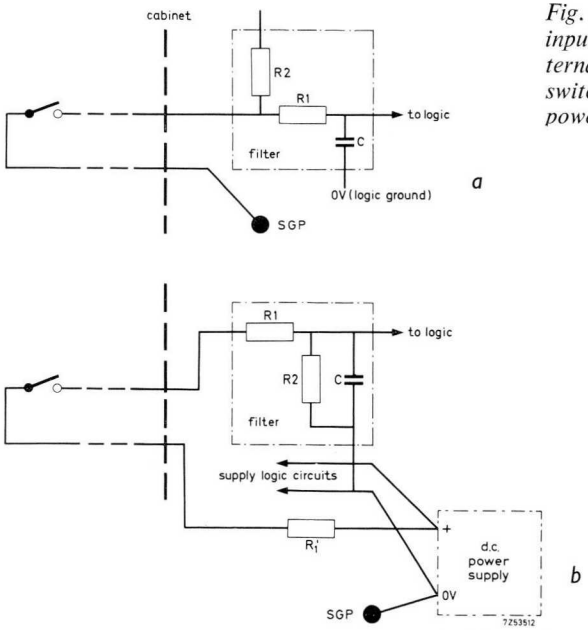


Fig. 6.1. Elimination of input device noise. (a) External switch supply, (b) switch supplied from logic power supply.

reasons, i.e. short--circuiting, it is advisable to insert a resistor R_1' between plus and the wire to switch.)

Electronic types of input device such as the EPD do not produce significant amounts of noise.

6.1.2 Noise Entry from the Mains Supply

Large current surges in the external power distribution system are apt to disturbances at the logic Power Supply Unit output. The PSU must thus be preceded by a filter, such as the MF 0.5A, as shown in Fig. 6.2. (For specifications see Chapter 14.) An attenuation of about 50 dB can be achieved for frequencies of 100 kHz up to 10 MHz. Both "common mode" noise (noise signals between the two lines and ground and "asymmetrical noise" (noise between the two lines) are attenuated. The two input terminals of the filter are to be connected to the mains supply lines. It is advisable to mount the filter at the place where these lines enter the cabinet (Fig. 6.6), thus preventing the noisy lines from influencing the circuitry inside the cabinet. The output terminals are to be connected to the d.c. power supplies in the cabinet. *The ground point of the filter must be connected to the SGP.*

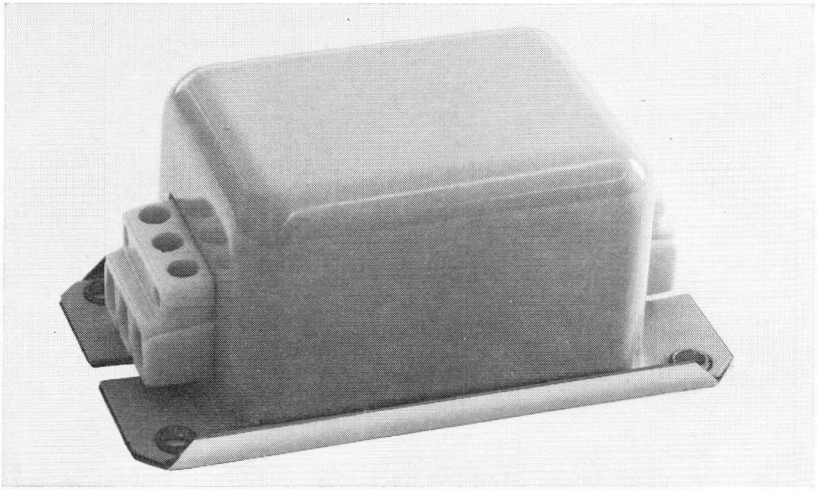


Fig. 6.2. Mains filter, MF 0.5A.

The a.c. ground should be separated from the SGP because the former is very noisy. If only relatively little mains noise is to be expected, the filter of Fig. 6.3 can be used.

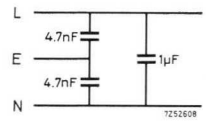


Fig. 6.3. Alternative mains filter.

In addition, mains transformers should be provided with a primary screen earthed at the SGP.

6.1.3 Noise induced in Incoming Wires

Strong electric or magnetic fields in the vicinity of the input cables can induce noise in the wires; this can often be corrected with a switch filter. However, when input signals have a relatively high frequency, for instance in the region 100 Hz-10 kHz, it is not possible in general to obtain enough attenuation of noise with a low-pass filter. In that case it is necessary to shield the input wires. A shielded cable with twisted pairs is very suitable for this purpose; the grounded electrostatic shield greatly reduces the capacitance to noisy surroundings, while the twisted pair has a low mutual inductance with the surroundings. *The shield of the cable must be connected to the SGP.* (If cables enter the cabinet via a plug, the shield should be fed

into the cabinet via one of the terminals of the plug.) *The shield at the other end of the cable must be left floating.*

Fig. 6.4 gives an example of the method of connecting electronic input devices to the system. Particular values of R and C for each device are given in Chapter 5.

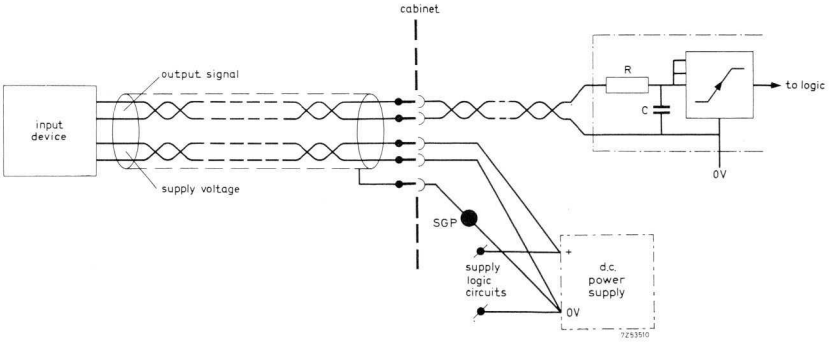


Fig. 6.4. Connection of input devices to a control system. The RC product should be made as large as possible, consistent with maximum system speed.

6.2 Direct Interference by Electro-Magnetic Fields

The control system should always be enclosed in a sheet metal cabinet which is properly grounded, noting however that it is not good practice to enclose both logic and a.c. equipment such as contactors in the same cabinet. If this is unavoidable the a.c. and d.c. equipment should be segregated and magnetically screened from each other.

Any a.c. wiring on the d.c. side should be segregated from d.c. cabling and preferably run in steel conduit or trunking.

High voltages near the control system may induce secondary voltages in the system through mutual capacitance between the high voltage line, the system, and ground. The induced voltage is proportional to inducing voltage and to the ratio C_{m1}/C_{m2} (see Fig. 6.5). The remedy here is to ensure that the system is well removed from power bus-bars and other high-voltage equipment, and to ensure that proper grounding is used.

6.3 Internally Generated Noise

The mutual inductance and capacitance between wires and parts inside the cabinet can give rise to "crosstalk", i.e. transfer of signals from one

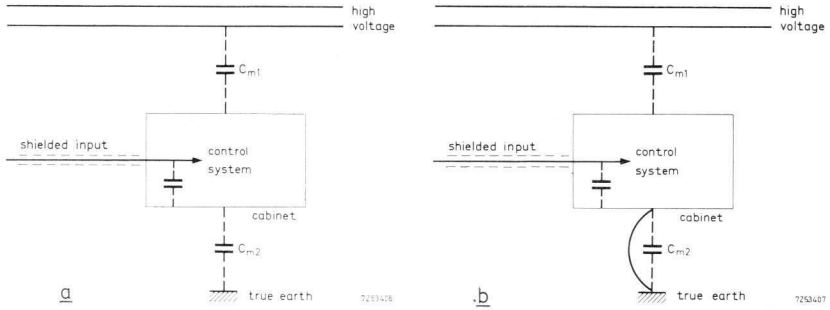


Fig. 6.5. Influence of neighbouring power lines. (a) Control system input and cabinet disconnected from ground, or connected to ground via high-impedance line (the control system input may sense a voltage level); (b) C_{m2} and C_{m3} short-circuited by a low-impedance line to true ground (the influence of neighbouring power lines is greatly reduced).
C_{m1} — mutual capacitance between high-voltage source and control system input;
C_{m2} — mutual capacitance between input and true earth.

wire to an adjacent one. Reduction of this mutual capacitance and inductance may be achieved by:

(1) Point-to-point wiring, giving less crosstalk than wiring in cable harnesses (larger distance between wires).
(2) Keeping "noisy" interconnections away from noise-sensitive interconnections (for instance excluding high current output wires from a cable harness containing wires transmitting logic signals).
(3) Using a twisted pair when large current signals have to be transmitted to another part of the system. A twisted pair (current return wire around signal wire) has a low di/dt and reduces inductive crosstalk;
(4) Using a shielded wire when capacitive crosstalk is important. The shield is connected to the SGP and thus gives electrostatic shielding from other interconnections (moreover, shielding reduces inductive crosstalk).
(5) Using shielded twisted pairs to give protection against capacitive and inductive crosstalk.
(6) Avoiding routing of *high currents* through *logic circuit ground.* High current peaks may give high voltage peaks across the ground impedance (ground self-inductance is more important than ground resistance). If a free wire of 1 m length has a self-inductance of about 1.6 μH, a current change of 1 A in 1 μs gives a voltage peak of 1.6 V.

To avoid this, separate the ground return for high currents from the ground return for logic circuits, and use a low-impedance ground (thick wire).

It is recommended that the inputs of all logic systems always be fitted with a filter capacitor of such a value that system speed requirements are just maintained.

6.4 System grounding considerations

Use *one* system ground point (SGP). All shields etc. should be grounded at this point via separate wires. If the cabinet is used as a shield, the

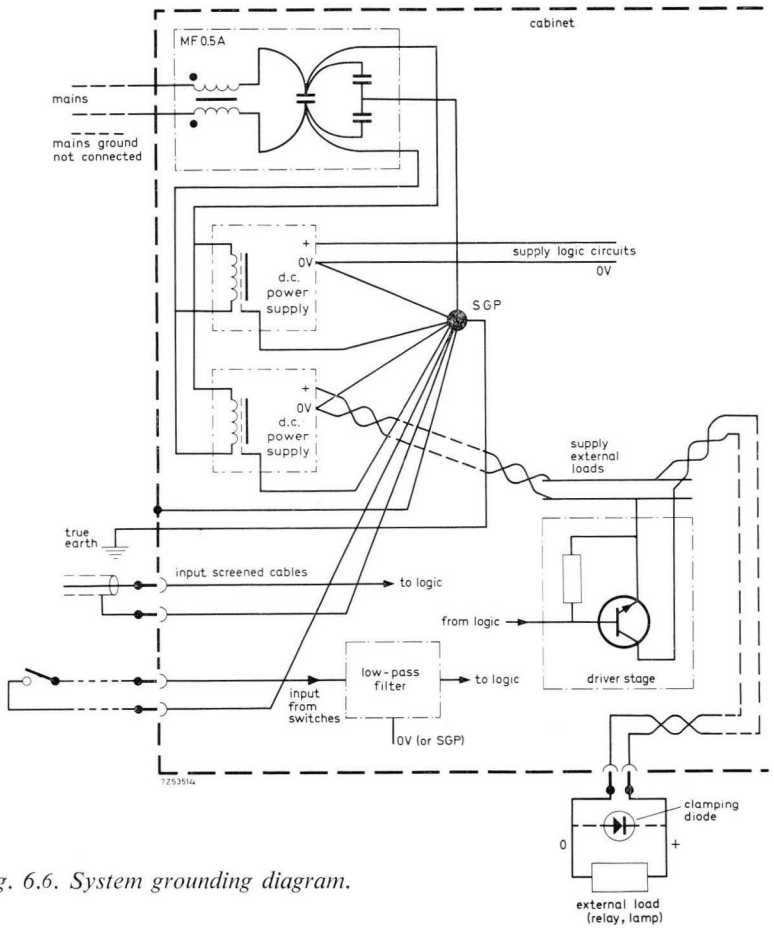


Fig. 6.6. System grounding diagram.

cabinet must be grounded at the SGP. Never use the cabinet or the framework inside the cabinet as ground return conductor, as it then nullifies the shielding effects. The system ground point should be connected to a true earth. Never use a.c. ground for this purpose, because it is very "noisy". If the cabinet is used as a shield, make sure that all metal parts of the cabinet and the frame make good contact, otherwise the shielding properties are lost. Sharp edges of small holes in the cabinet are particularly good radiators of high-frequency interference.

Fig. 6.6 depicts a typical layout.

If there is not a true earth point available, special precautions must be taken:

(1) Do not connect the cabinet to the SGP. (Keep the system grounding point floating with respect to all metal parts of frame work and cabinet.)

(2) Never connect the a.c. ground to the cabinet unless this is necessary for safety reasons, for example. Site the cabinet out of "noisy" areas.

7 Switching Algebra for Norbit System Design

Although it is possible to design control circuits on a "cut and try" basis, the use of switching algebra with its few, simple principles enables faster solution and provides an explicit and powerful shorthand to describe the system. This chapter explains the principles (introduced briefly in Chapter 1) in sufficient detail to allow their use in most practical situations.

7.1. Switching Functions

7.1.1. Concepts

Logic

Originally used by the ancient Greeks in such phrases as "Epistimè Logikè", meaning "knowledge of reasoning", logic was concerned with the evaluation of propositions in terms of "True" or "Not True". Often this branch of logics is called "logic of propositions", or — because only two values are used — bivalent logic.

Switching Algebra

The algebraic notation used here was described by *G. Boole* about 120 years ago in analysing propositional logic problems and the principles of bivalent logic in an analysis of relay switching circuits was applied by *Shannon* in 1938.

Switching algebra is the engineering application of bivalent logic principles. It will be realized that a switch (conventional or static) exhibits bivalent characteristics (closed / open, conducting / not conducting). Algebraic discipline not only forces the user to define a problem accurately, but switching algebra moreover offers a number of working rules by which analysis and synthesis can be simplified.

Binary Variable

A binary variable is a variable that has one of two possible values. For example, the logic of propositions given above uses "True" and "Not True" (or False, which is less well defined). Furthermore it excludes the possibility of the binary variable having both values simultaneously (i.e. True and simultaneously Not True), and having neither value.

Similarly, the two possible contact positions of a switch can be interpreted as a binary variable e.g. "closed / open" or "operated / not operated". Although here one value is the negation of the other, as a pair of values the symbols 1 and 0 will be substituted for True / Not

True or Closed / Open, as this permits a more general treatment of logic problems on an algebraic base.

Postulates

A "postulate" is a fundamental condition. Assigning the letter "*a*" to the binary variable and using the sign "=" as a symbol expressing identity, the pair of postulates 1*a* and 1*b* (Fig. 7.1) may be formed. Using the signs $= \cdot + ( )$ as connectives (not necessarily having the same meaning as in ordinary arithmetic) the postulates 2, 3 and 4 are introduced. The relevant switch condition is shown for each postulate; here, a closed switch indicates that the output is equal to the 1 level.

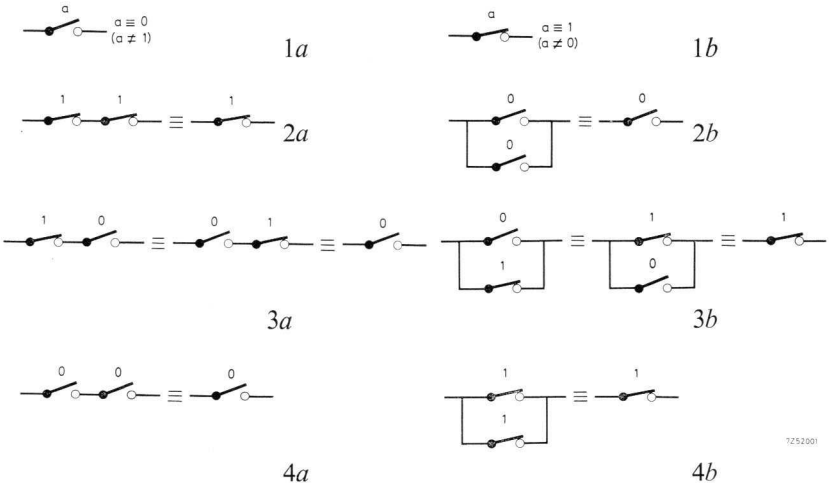


Fig. 7.1. Postulates and their switch representations.

Apart from postulate 4*b*, all could be interpreted as simple examples of ordinary arithmetic if the signs had the conventional meaning. Though this seems attractive, the actual meaning is different in the present context.

postulate 1*a*: $a = 0$ if "*a*" is not 1
postulate 2*a*: $1 \cdot 1 = 1$
postulate 3*a*: $1 \cdot 0 = 0 \cdot 1 = 0$
postulate 4*a*: $0 \cdot 0 = 0$

postulate 1*b*: $a = 1$ if "*a*" is not 0
postulate 2*b*: $0 + 0 = 0$
postulate 3*b*: $0 + 1 = 1 + 0 = 1$
postulate 4*b*: $1 + 1 = 1$

Introducing one more sign, a bar over a symbol (or group of symbols) and defining this bar to mean the negation of the value represented by the symbol itself, we can write:

postulate 5*a* $\bar{1} = 0$ postulate 5*b* $\bar{0} = 1$

Expressed in words, $\bar{1}$ and $\bar{0}$ are termed "one bar" and "zero bar" or, alternatively "not one" and "not zero".

7.1.2. The Logic of Switching Networks

In control circuits, binary devices are used to establish the function between input and output. It is convenient to picture these as switches, the contact network being of any degree of complexity. Using "operated" and "not operated" for the two possible states of a switch instead of "closed" or "open" is of advantage, assigning "1" to the condition that operates the switch and "0" to the condition that does not operate it. This allows for two initial contact conditions, i.e. normally open or normally closed contacts.

The expression $a = F$ in which a is an independent variable and F is the associated dependent variable can be depicted as in Fig. 7.2.
For the two possible values of a we get:

a	F
1	1
0	0

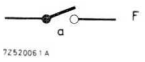


Fig. 7.2. Representation of $a = F$.

which means that if a is operated ($a = 1$) F will be 1. Basic logic functions are NOT, AND, OR, and complex negation.

The "NOT" Function

The logic function NOT can be depicted as a normally closed switch, so that non-operation of the switch ($\bar{a} = 1$) results in $F = 1$ (Fig. 7.3):

a	F
1	0
0	1

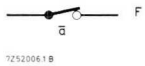


Fig. 7.3. Representation of $\bar{a} = F$.

The "=" sign should be taken to mean "results in F". This meaning is different from that in ordinary arithmetic; it implies that no displacement of terms is allowed from the left-hand side to the right-hand side of the

"=" sign or vice versa as this would interchange cause and effect.

The tables above which were used to find the value of the dependent variable F for the two possible values of the binary variable a are called "Truth Tables". As will be seen later, a truth table is a useful aid in the investigation of switch networks.

The "AND" Function

In Fig. 7.4, F will be 1 only if both a AND b are 1; this function is known as the AND function.

Table 7.1

a	b	c	$F = (a \cdot b \cdot c)$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

It is obvious that the AND can be extended to any number of binary variables, and is not limited to switches; it can be applied to any situation in which all of the binary variables have to be 1 to result in a value of 1 for the dependent variable.

By way of example the truth table for a three-variable AND is given in Table 7.1; it will be seen that only if all independent variables are 1, will F be 1. From this it follows that the $\cdot$ sign can be used as in arithmetic (a single 0 makes $F = 0$).

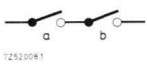


Fig. 7.4. Representation of $a \cdot b = F$.

The "OR" Function

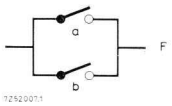
In Fig. 7.5 it is clear that F will be 1 if a OR b (or both) are 1. Therefore the expression $a + b + c = F$ is called an OR function. With an OR function it is sufficient that one independent binary variable has the value 1, for F to be 1. As F is also 1 when several independent variables are 1, this function is often referred to as "inclusive OR". Table 7.2 shows F as an OR function of three independent binary variables a, b and c.

Table 7.2

a	b	c	$F = (a + b + c)$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Note that the usual way to set up the independent variables in a truth table is to make the first row all zeroes, then alternate 1s and 0s in the last column

Fig. 7.5. Representation of $a + b = F$.



(column c). Preceding column b alternates at half this frequency, and column a at half this again. This method accounts for every possible combination, eliminating omissions and repetitions.

Negation (inversion)

The bar over a binary variable indicates that it is to be taken as the complement of the value given to the symbol proper i.e. $\bar{a} = 0$ if $a = 1$. This interpretation is not limited to the case where a is a single binary variable; compound terms or functions can also be negated.

This gives rise to some interesting theorems for the AND and the OR functions of two binary variables, demonstrated by Tables 7.3 and 7.4.

Table 7.3

a	b	$(a + b)$	$\overline{(a + b)}$	$\bar{a} \cdot \bar{b}$
0	0	0	1	1
0	1	1	0	0
1	0	1	0	0
1	1	1	0	0

Table 7.4

a	b	$a \cdot b$	$\overline{a \cdot b}$	$\bar{a} + \bar{b}$
0	0	0	1	1
0	1	0	1	1
1	0	0	1	1
1	1	1	0	0

Table 7.3, giving $\overline{a+b}$ (column4) has been formed by negating the values for $(a + b)$ from the third column, with a fifth column, $\bar{a} \cdot \bar{b}$, added. Comparing columns 4 and 5 we see that $\overline{a + b} = \bar{a} \cdot \bar{b}$ for every possible value of the binary variable. This means, of course, that $\overline{a + b}$ is identical to $\bar{a} \cdot \bar{b}$ (or, briefly, to $\bar{a}\bar{b}$). In more general form

$$\overline{a + b + c + \ldots + n} = \bar{a}\,\bar{b}\,\bar{c} \ldots \bar{n}.$$

The function

$$\overline{a + b + c \ldots + n} = F$$

is known as the NOR function and it is the one performed by NORbits. Comparing the 4th and 5th columns of Table 7.4, giving $\overline{a\,b}$, we find:

$$\overline{a\,b} = \bar{a} + \bar{b},$$

or in general:

$$\overline{a\,b\,c \ldots n} = \bar{a} + \bar{b} + \bar{c} \ldots + \bar{n}.$$

These two theorems, due to *De Morgan*, are extremely useful in the practical manipulation of switching functions.

7.1.3 Theorems

In addition to the two theorems derived above, there are several others which are dealt with below.

A number of theorems can be derived in dual form for a single binary variable from the postulates given previously (Sect. 7.1.1). No formal proof is offered, but switch arrangements are used to support interpretation in Figs 7.6 to 7.9.

The visualisation of postulates and theorems for a single binary variable by switches shows that any arrangement representing the left-hand side of the symbolic notation can be reduced to a single switch, provided that:

— the · sign is interpreted as a series connection of switches represented on each side of this sign (observe that the dot is often omitted in equations);

— the + sign is interpreted as a parallel connection of the switches represented on each side of this sign.

Some of the more important theorems for one, two and three independent variables are brought together for quick reference in Table 7.5. They

Table 7.5

1*a*	$a \cdot 1 \equiv a$	1*b*	$a + 0 \equiv a$
2*a*	$a \cdot 0 \equiv 0$	2*b*	$a + 1 \equiv 1$
3*a*	$a \cdot a \equiv a$	3*b*	$a + a \equiv a$
4*a*	$a \cdot \bar{a} \equiv 0$	4*b*	$a + \bar{a} \equiv 1$
5*a*	$(\bar{a}) \equiv \bar{a}$	5*b*	$\overline{(\bar{a})} \equiv \bar{\bar{a}} \equiv a$
6*a*	$a \cdot b \equiv b \cdot a$	6*b*	$a + b \equiv b + a$
7*a*	$a \cdot b \cdot c \equiv (a \cdot b)c \equiv a(b \cdot c) \equiv \equiv b(a\,c)$	7*b*	$a + b + c \equiv a + (b + c) \equiv \equiv (a + b) + c \equiv b + (a + c)$
8*a*	$a(a + b) \equiv a + ab \equiv \equiv a(1 + b) \equiv a$	8*b*	$a + ab \equiv a(1 + b) \equiv a$
9*a*	$(a + b)(a + c) \equiv a + bc$	9*b*	$ab + ac \equiv a(b + c)$
10*a*	$(a + \bar{b})b \equiv ab$	10*b*	$a\bar{b} + b \equiv a + b$
11*a*	$(a + b)(\bar{a} + c)(b + c) \equiv \equiv (a + b)(\bar{a} + c)$	11*b*	$ab + \bar{a}c + bc \equiv ab + \bar{a}c$
12*a*	$(a + b)(\bar{a} + c) \equiv \bar{a}b + ac$	12*b*	$ab + \bar{a}c \equiv (\bar{a} + b)(a + c)$
13*a**	$\overline{a \cdot b \cdot c} \equiv \bar{a} + \bar{b} + \bar{c}$	13*b**	$\overline{a + b + c} \equiv \bar{a} \cdot \bar{b} \cdot \bar{c}$

*) theorem of De Morgan

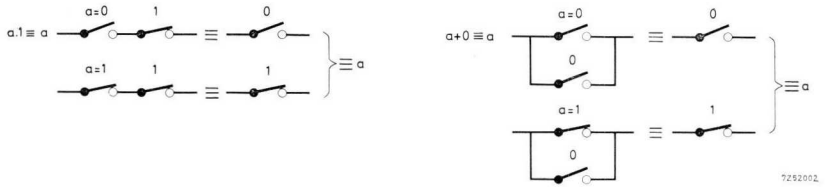


Fig. 7.6. Theorem 1 and switch representations. Left, theorem 1a; right, theorem 1b.

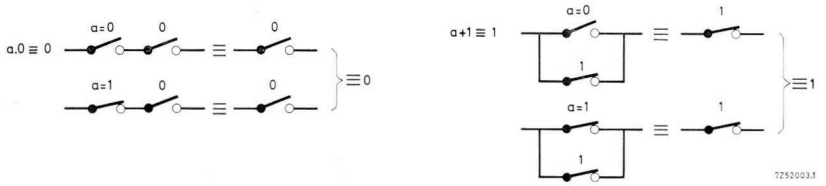


Fig. 7.7. Theorem 2 and switch representations. Left, theorem 2a; right, theorem 2b.

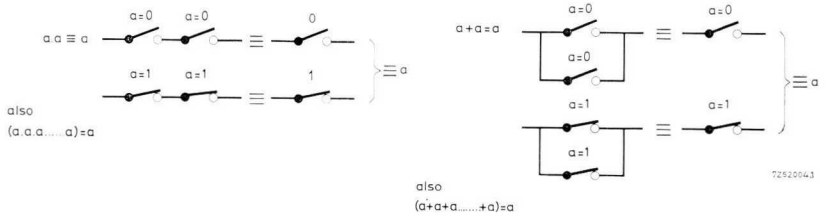


Fig. 7.8. Theorem 3 and switch representations. Left, theorem 3a; right, theorem 3b.

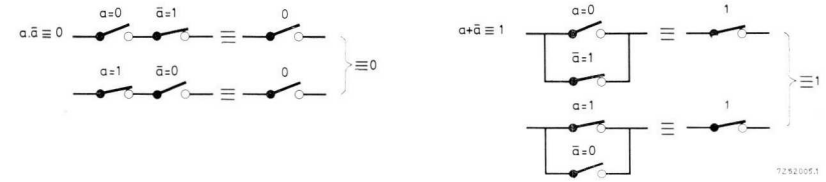


Fig. 7.9. Theorem 4 and switch representations. Left, theorem 4a; right, theorem 4b.

may be verified by a truth table or by using the theorems presented earlier. It should be mentioned that AND takes precedence over OR (just as multiplication takes precedence over addition). Brackets have the same function as in conventional arithmetic.

That logic theorems come in pairs has been demonstrated above. It can be stated that: if in a theorem the · sign is replaced by + (or + by ·), and 1 by 0 (or 0 by 1), the result is the dual of the original; for example theorem 4*a*, $a \cdot \bar{a} \equiv 0$, becomes $\bar{a} + a \equiv \bar{0} = 1$ (theorem 4*b*).

Most theorems can be proved by direct reference either to those for a single binary variable or to the postulates. In some instances an indirect approach, using the implications of theorems 3*a*, 3*b*, 4*a* and 4*b* can be very useful. As the theorems express true identity, they can be read from right to left, as well as from left to right. A few simple rules which will help in the solution of problems are given below.

Rule 1 — "Multiplying" a binary variable by 1 does not change its value (theorem 1*a*). Simplification is often possible if 1 takes the form $(q + \bar{q})$ (theorem 4*b*) and the correct variable is chosen for q.

Rule 2 — "Adding" 0 to a binary variable does not change its value (theorem 1*b*). Simplification is often possible if $q \cdot \bar{q}$ (theorem 4*a*) is used, q being suitably chosen.

Rule 3 — "Addition" of two identical terms, gives the original term (theorem 3*b*).

Rule 4 — "Multiplication" of identical terms (theorem 3*a*) does not change the term.

Rule 5 — If both values of a variable (or combination of variables) appear in a sum of products, then the product of this variable and the variables associated with it, can be omitted from the expression.

Rule 6 — Similarly, if both values of a variable (or a combination of variables) appear in a product of sums, the sum of this variable and the variables that are associated with it, can be omitted.

Section 7.4.1 gives some examples illustrating the use of the rules.

As a further remark on simplification of equations, it should be recognized that some theorems exhibit "absorption" of variables or combinations of variables. This is well illustrated by theorem 8*a*, in which b is absorbed. This effect can be of value when rearranging logic functions.

Switching algebra provides many other theorems as well as rules for simplifying switching functions; as such, these are beyond the scope of this publication. There is extensive literature on the subject.

7.1.4 The Memory Function

In practical control circuits it is often necessary to have a persisting value for a binary variable if the duration of that variable is short. Take a switching circuit of the form shown in Fig. 7.10. Here M_a is the output that results from $a = 1$. If a now becomes 0, M_a will stay 1, because M_a became 1 at the moment a became 1. Now M_a could be called a memory indicating that a had been 1 (a sets memory at 1).

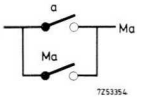


Fig. 7.10. The basic memory configuration.

It is necessary to provide means to bring M_a to 0 at a desired moment. This can be done by a reset signal r. Two basic forms are possible.

$$a + M_a\bar{r} = M_a.$$

With this memory (Fig. 7.11), setting takes precedence over resetting. If $r = 1$, $\bar{r} = 0$, thus $a = 1$ gives $M_a = 1$ (as long as $a = 1$).

$$(a + M_a)\,\bar{r} = M_a.$$

With this memory (Fig. 7.12), resetting overrules setting, since $r = 1$, $\bar{r} = 0$ makes the left-hand term 0.

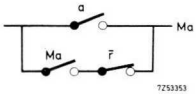


Fig. 7.11.

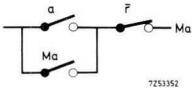


Fig. 7.12.

Clearly, a switching function having a binary variable on both sides of the = sign contains a memory function for that variable.

7.1.5 Instability and Racing

It is important that the designer recognize and correct instability or racing if these occur in a system design, as the consequences can be an output which is either meaningless or incorrect.

Instability is caused by connecting units in an "impossible situation", such as True = Not True, expressed algebraically as $a = \bar{a}$. The output F in Fig. 7.13 will alternate between 1 and 0 (at a frequency approximately one third the switching frequency of a NOR unit), when input a is 0.

Other expressions which cause instability are of the types:

$$a + b = \bar{b} \quad \text{or} \quad a \cdot b = \bar{b}.$$

These expressions have no practical meaning and can result only from

incorrect statement of the problem or incorrect manipulation of the switching algebra.

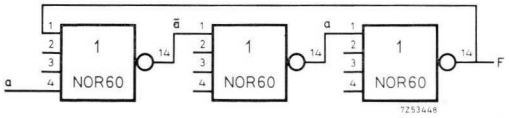


Fig. 7.13. Configuration giving instability.

Racing is the term given to the situation drawn in Fig. 7.14, where output F is either 1 or 0, depending on whether NOR (A) or NOR (B) is the faster when the input a changes from 1 to 0.

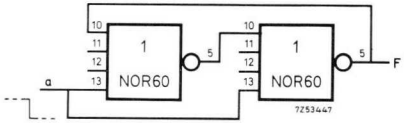


Fig. 7.14. Illustration of a "racing" situation.

7.1.8 Limitation of Switching Algebra

Although the Boolean or Switching Algebra technique of logic circuit design is well worthwhile in a good number of cases, it is difficult to use in the description of systems containing time delays. In other words, it is limited to description of "instantaneous logic" systems. Where time delays are involved, it is best to proceed as follows:

— Make an absolutely clear and unambiguous statement of the problem.
— Then simply reason out the configuration required, stage by stage if possible.
— Finally make a truth table, including *all possible* input combinations and time delays.

Note also that Switching Algebra gives a purely theoretical description of the results to be expected from a circuit. In some cases the time required to operate a relay may have to be accounted for.

7.2 Synthesis of Switching Functions

The conversion of a logic expression (either of combinational or sequential type) into a practical circuit may be approached in several ways, as described below. It is important to realise that, in any one problem, the logic level to which reference is made be clearly understood and remain unchanged throughout. With the 60-Series, for example, this is the 1 level (positive "high" voltage); for instance, although the NOR 60 unit could

be considered as an AND operator for 0 level signals, this is — strictly speaking — inconsistent, because all functions are defined in terms of 1 level independent variables.

7.2.1 Combination Logic

In combination logic the value of the dependent output variable(s) is determined only by the value of the independent binary input variables. Timing or sequence play no part in the result.

The initial approach is to write down the algebraic notation for a given switching network. Taking for example the network of Fig. 7.15 and using the notation AND, OR, NOT, all combinations can be ascertained that result in $F = 1$. So: a AND $\bar{b}$ OR a AND $c = F$, which can be written as:

$$a \cdot \bar{b} + ac = a(\bar{b} + c) = F.$$

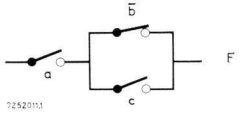


Fig. 7.15. Example of a switching network.

More complex networks can be treated similarly.

Where there are several dependent binary variable outputs, each must be established along the same lines. In Fig. 7.16, for example, for F_1 we obtain:

$$a(\bar{b} + c) + \bar{a}(\bar{c}d + b)d = F_1,$$

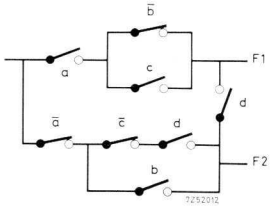


Fig. 7.16. Example of a switching network with two outputs.

which can be written as:

$$a(\bar{b} + c) + \bar{a}\bar{c}d + \bar{a}bd = a(\bar{b} + c) + \bar{a}d(\bar{c} + b) = F_1.$$

For F_2 we obtain:

$$a(\bar{b} + c)d + \bar{a}(b + \bar{c}d) = F_2.$$

From the above, two observations can be made:

— Any contact network can be written as a sum of products, i.e. the

network can be presented as a number of parallel paths each of which is a series arrangement that makes $F = 1$.

— Apart from depicting $F = 1$, a contact network can be described by the complementary function $F = 0$, which is sometimes an advantage. As 0 is the negation of 1, the function $F = 0$ can be obtained from the function $F = 1$ by negation. This may be helpful when the function $F = 0$ has less terms, or the terms are such that they allow simpler realization with a particular type of logic operator.

However, in a number of practical situations, the inverse of a function has a significance in its own right. In any case it is recommended that the inverse notation of a switching problem be examined as so to detect unwanted combinations. The synthesis of a switching function from a verbal or written specification can best be achieved by following a logical sequence of steps such as that given below:

(*a*) Write down the specification in terms of AND, OR and NOT.

(*b*) List the independent binary variables.

(*c*) Assign to them the letters *a*, *b*, *c* . . . .

(*d*) Define the condition of the independent binary variables to which the value 1 is assigned.

(*e*) List the dependent binary variables.

(*f*) Assign letters to these (*P*, *Q*, *R* . . .).

(*g*) Define the condition of the dependent binary variables to which the value 1 is assigned.

(*h*) Set up a truth table, providing columns for *a*, *b*, *c* . . . and *P*, *Q*, *R* . . . . Each row of the truth table must give one combination for the independent variables. For each combination of independent variables write the corresponding vaules of *P*, *Q*, *R* . . . .

(*j*) Set up the switching functions for (*P*, *Q*, *R* and . . .) and quote the outputs as a sum of products for *P*, *Q*, *R*, . . ., in accordance with (h).

(*k*) Simplify switching functions, if possible, using theorems and rules given in previous sections.

To illustrate the method, an example is worked out in Sect. 7.4.2.

Apart from the procedure outlined above, a mixture of reasoning and algebra can sometimes yield a solution. The example below gives such an approach.

Often a circuit is required to control an oscillating motion of a tool (grinding, milling, etc.) or of a container. The tool is to move from *l*eft to *r*ight and vice versa between two limit switches. Apart from the limit switches (*l* and *r*), three push-buttons (*stop*, *k* and *p*) are provided for

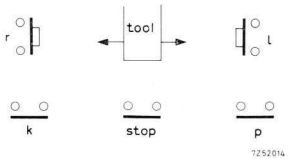


Fig. 7.17. Diagrammatic representation of a machine tool and control switches.

stop, left-hand start and right-hand start. Pressing any two switches should also stop the movement. The tool in an end position gives r, $l = 1$. A push-button pressed gives 1. See Fig. 7.17.

Movement is controlled by solenoids (valves, contactors, etc.), R and L. The independent variables and their definitions are listed below.

r = left-hand limit switch; $r = 1$ initiates right-hand movement.
p = push button; $p = 1$ initiates right-hand movement.
l = right-hand limit switch; $l = 1$ initiates left-hand movement.
k = push-button; $k = 1$ initiates left-hand movement.
s = stop button; $s = 1$ stops movement.
The dependent variables and their definitions are:
R = solenoid for right hand movement; $R = 1$ gives right-hand movement.
L = solenoid for left hand movement; $L = 1$ gives left-hand movement.

In setting up switching functions for L and R, it should be noted that they have to appear as memory functions, because the push buttons and limit switches give only short-duration signals.

Although a truth table may be used to obtain a solution to the problem on the lines shown earlier, reasoning may provide a quicker answer. This type of problem can usually be solved in the following way by starting from the dependent variable.

We know that R is to be 1 if $p + r + R$ are 1; furthermore R can be 1 and stay 1 only if l is NOT 1 (initiating left-hand movement by the right-hand limit switch), AND push button k is NOT pressed (k pressed would initiate left hand movement also), AND stop button s is NOT pressed, AND L is NOT 1 (excluding simultaneous right- and left-hand movement). So:

$$(p + r + R)\bar{l}\bar{k}\bar{s}\bar{L} = R.$$

Applying similar reasoning for L:

$$(l + k + L)\bar{p}\bar{r}\bar{s}\bar{R} = L.$$

Various methods have been described to facilitate the reduction of switch-

ing functions to their simplest form. One method, contributed by *Karnaugh*, is described in a former publication *).

7.2.2 Sequential Logic

Sequential logic requires memory functions to distinguish between past and present input conditions, usually in conjunction with combination logic. As the sequence of both the independent variables and of the dependent variables may change, the straightforward approach using a truth table is unlikely to yield the easiest solution. In practice, therefore, a reasoning approach is usually preferred.

Various types of sequential circuits can be distinguished:

(*a*) control systems with a prescribed sequence for the input variables;
(*b*) control systems with a prescribed sequence for the output variables;
(*c*) control systems employing combinations of (*a*) and (*b*).

These three types will be illustrated by a few typical examples.

Example of Type (a): Simple Alarm System

It often arises in industry that a condition (or conditions) must be monitored, and an attendant's attention be drawn to or correcting action be initiated at the presence or absence of a certain binary variable. Such control systems are usually termed alarm systems.

The following specification is assumed for such a system. If an alarm condition a ($a = 1$ for alarm) is present, even transiently, a lamp L must flash and a buzzer B sound ($B = 1$). After acknowledging the alarm by pressing a push button p momentarily ($p = 1$ for pressed button) the buzzer must stop and the lamp be lit steadily for as long as the alarm condition persists. As soon as the alarm condition disappears (after acknowledgement) the lamp L must extinguish.

The memory sections of the system will be dealt with first. As a may be available transiently but should nevertheless be acknowledged, a memory will be required for $a = 1$; let this memory output be designated by M_a. We must therefore have $a + M_a = M_a$.

Obviously $M_a = 1$ is the condition for which the buzzer must sound, so by assigning $B = 1$ to the buzzer, $M_a = B$.

The other input variable p (the push button for acknowledgement) may be available only for a moment. Another memory is thus needed to remember that p was pressed. Indicating this memory by M_p, gives $p + M_p = M_p$.

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* "Logic elements in digital equipment" order No. 32/048/BE.

M_p must stop the buzzer B by resetting M_a, so the expression for M_a is completed by adding the reset condition, giving:

$$(a + M_a)\overline{M_p} = M_a.$$

Similarly M_p must stay 1 after p has been made 1 for as long as the alarm signal a remains 1. If a becomes 0 after M_p has been made 1, M_p must become 0, so the complete expression for M_p is:

$$p + M_p \cdot a = M_p.$$

We shall now consider the combination logic sections. As the lamp may operate in either steady or flashing modes, some combination logic is necessary, as well as a source of alternating 1 and 0 values. This alternating 1 and 0 can be assumed to be an output f from an oscillator. Taking M_a, M_p and f as independent variables and assigning $L = 1$ to the lit lamp, the lamp must flash when $M_a = 1$ or it must light steadily when $M_p = 1$ and M_a is not 1, so we get:

$$f \cdot M_a + aM_p = L.$$

Example of Type (b): Machine Control

Very often control systems are required to produce a sequence of outputs. Such a system can be represented by a number of simultaneous functions.

When F_n is completed, a delay must elapse after which the cycle is restarted at F_1 and so on. For such a control system a time sequence diagram can be drawn, as shown in Fig. 7.18. From this diagram one can derive the necessary switching functions for each step, these being initiated

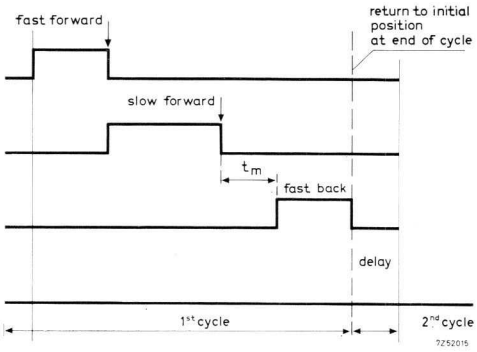


Fig. 7.18. Time sequence diagram.

at the end of the preceding step. The initiating signal may be obtained from various sources: timers, position indicators, sensors, limit switches, etc. In the figure t_m denotes the machining time.

Example of Type (c): Automatic Pipe Cutter

Fig. 7.19 shows, by way of example, a pipe cutter. Pipe is fed to the cutting position by a motor which is stopped when the end of the pipe closes limit switch *S*. The cutter and its drive motor are mounted on a table driven by the transport motor *T*. The cutter motor *C* runs continuously, but *T* is started by *S* closing, and the table is driven forward to cut the pipe. When the table is fully forward, switch *f* is closed. *T* is reversed, and the table is retracted until switch *b* is closed. Switch *b* restarts *M* and the cycle is repeated.

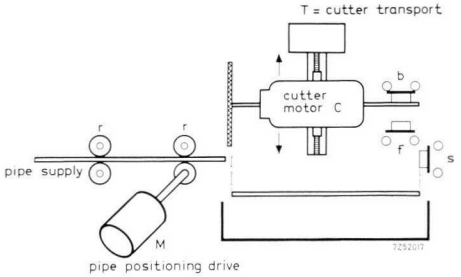


Fig. 7.19. Automatic pipe cutter.

7.3 Realization of Switching Functions with NOR units

7.3.1 Basic Logic Functions

Earlier the NOR operation was defined as

$$\overline{a + b + c + \ldots + n} = F.$$

The symbol adopted for the NOR units is given in Fig. 7.20 With all inputs at 0, $F = 1$. With one or more inputs at 1, $F = 0$. Hence

$$\overline{a + b + c + d} = F \quad \text{or} \quad \bar{a}\bar{b}\bar{c}\bar{d} = F.$$

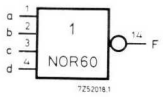


Fig. 7.20. The NOR *function.*

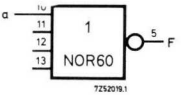


Fig. 7.21. The NOT *function* $\bar{a} = F$.

The functions possible with the NOR unit are illustrated in Figs 7.21 to 7.24.

Using these arrangements, equal to AND, OR, NOT and Memory functions, one can follow a "graphical" procedure to achieve a given switching function.

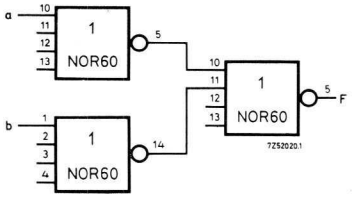


Fig. 7.22. The AND *function: a.b = F.*

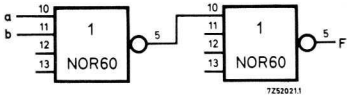


Fig. 7.23. The OR *function: a+b = F.*

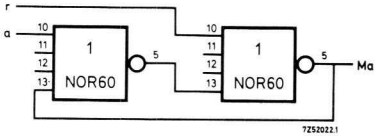


Fig. 7.24a. The memory function: $(a + M_a)\bar{r} = M_a$.

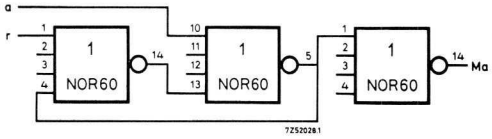


Fig. 7.24b. The memory function: $a + M_a \cdot \bar{r} = M_a$

7.3.2 Graphical Method of Designing Systems

Let us take for example the realization of $a(b + \bar{c}) = F$ with NOR units.

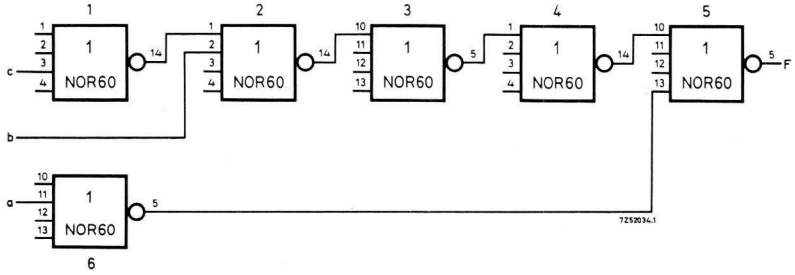


Fig. 7.25. Realization of $a(b + \bar{c}) = F$.

From the graphical presentation (Fig. 7.25) of the complete switch function a number of simplifications become apparent: for example, NOR(3) and NOR(4) are two single-input inverters in series and can be omitted (Fig. 7.26).

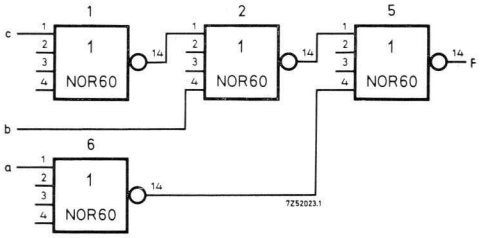


Fig. 7.26. Simplification of Fig. 7.25.

In an actual circuit there is often an initial choice between 0 and 1 conditions for any input. If the variables a and c could be obtained as 0s instead of 1s, to obtain $F = 1$, the whole problem could be solved with two NOR units (Fig. 7.27).

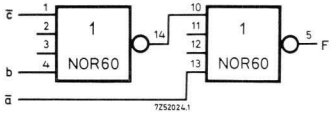


Fig. 7.27. Further simplification of Fig. 7.25.

Another possibility for simplification exists when a single-input NOR inverter is connected between two NOR units (Fig. 7.28). NOR(1) and NOR(2) perform the OR operation, so the output of NOR(2) is $a + b + c$; together with d we obtain from NOR(3): $\overline{(a + b + c) + d} = F$ which is identical to $\overline{a + b + c + d}$. The same situation can be obtained if a, b and c are brought straight to NOR(3) together with d; in this way NOR(1) and NOR(2) can be eliminated.

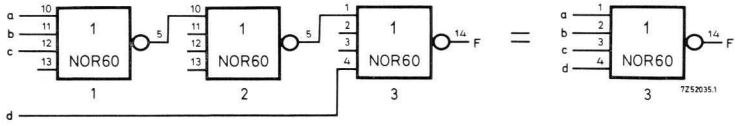


Fig. 7.28. Illustration of elimination of two NORs.

If the total number of inputs required exceeds the four provided on a standard NOR unit, up to 8 inputs can be obtained by using the two

NOR units of each 2.NOR60 block in a "collector OR" configuration as shown in Fig. 7.29. Supply voltage should be applied only to one plus supply terminal (preferably to terminal 7 on standard printed wiring boards PWB 60 and PWB 61, a track being interrupted). Outputs No. 5 and No. 14 should be interconnected.

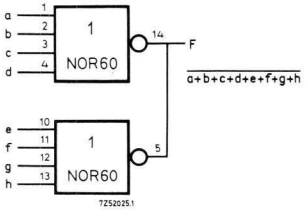


Fig. 7.29. The "collector-OR" configuration

As a second example of the graphical method let us realize

$$(a + \bar{b}\bar{c})\,\overline{(d + e)} = F.$$

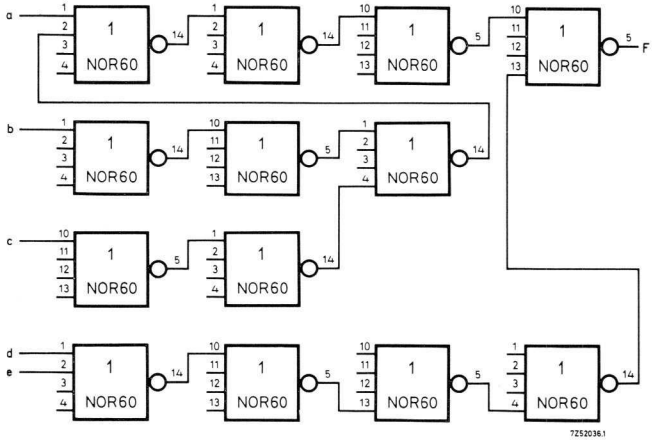


Fig. 7.30.

Fig. 7.30 depicts this expression. As in the previous example, the various subsections are obtained separately, the aggregate being subsequently simplified.

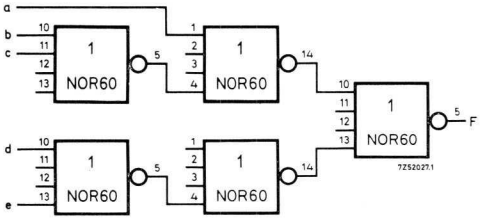


Fig. 7.31. Simplification of Fig. 7.30.

Eliminating double inversions we get the circuit of Fig. 7.31. Recognizing that d and e are brought to a NOR unit followed by an inverter, both steps can be eliminated as shown in Fig. 7.32. From the above it will be clear that the graphical method has the advantage of being straightforward, requiring no special manipulation of the switch functions; a disadvantage is the need to arrive at the final diagram by a number of drawings. A more direct solution can usually be obtained by using the algebraic method.

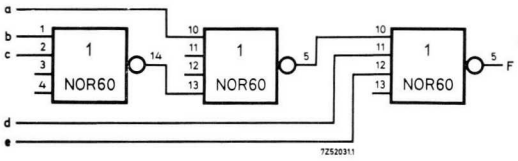


Fig. 7.32. Further simplification of Fig. 7.30.

7.3.3 Algebraic Method of Designing Systems

From a switching function using AND, OR and NOT as basic functions, an equivalent function using NOR units can be obtained by proceeding as follows:

(1) Replace all AND operations by NOR operations performed on the negated variables, e.g. write $a \cdot b \cdot c$ as $\overline{\bar{a} + \bar{b} + \bar{c}}$.

(2) Replace all ORs by double NOR operations, e.g. write $a + b + c$ as $\overline{\overline{a + b + c}}$.

Applying these procedures to the previous example (Section 7.3.2), we have again: $(a + \bar{b}\bar{c})\,\overline{(d + e)} = F$ (Fig. 7.30).

Observing procedure (2) we write

$$(a + \overline{b + c})\,\overline{(d + e)} = F,$$

because $\bar{b}\bar{c} = \overline{b + c}$. Now taking the two expressions between brackets and again applying procedure (1):

$$\overline{\overline{(a + \overline{b + c})} + \overline{(d + e)}} = F,$$

for which we get:

$$\overline{\overline{(a + \overline{b + c})} + (d + e)} = F,$$

since $\overline{\overline{(d + e)}} = d + e$. This can be written (the brackets no longer serve any purpose) as:

$$\overline{\overline{a + \overline{b + c}} + d + e}.$$

Each bar represents a NOR unit, so in total 3 units are needed.

7.3.4 Memory Functions

The use of the NOR operator notation can be applied also to expressions containing memory functions.

The equation for a memory in which "set" takes precedence over "reset" is:

$$a + M_a\bar{r} = M_a,$$

which according to rule (1) can be written as:

$$a + \overline{\overline{M_a} + r} = M_a.$$

Now applying rule (2):

$$a + \overline{\overline{M_a} + r} = M_a,$$

which requires three NORs (Fig. 7.33); the two top bars indicate $\overline{Ma}$ is already available.

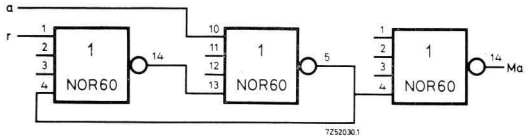


Fig. 7.33. Memory where setting takes precedence over resetting.

For the memory in which reset takes precedence over set:

$$(a + M_a)\bar{r} = M_a,$$

we write, according to rule (1):

$$\overline{\overline{(a + M_a)} + r} = M_a,$$

which gives the diagram of Fig. 7.34.

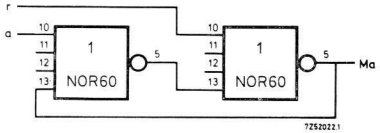


Fig. 7.34. Memory where resetting takes precedence over setting.

7.4 Examples in Switching Algebra

This section gives a few examples of the manipulation of switching algebra, to illustrate the methods described in the previous sections.

Example 1 (*Section 7.1.3*)

Proof of Thm. 10*b*.

This example illustrates the application of rules 1 and 3. Using rule 1 gives:

$$\begin{aligned} a\bar{b} + b &= a\bar{b} + (a + \bar{a})b \\ &= a\bar{b} + ab + \bar{a}b. \end{aligned}$$

Applying rule 3, adding ab we get:

$$a\bar{b} + ab + ab + \bar{a}b = a(b + \bar{b}) + b(a + \bar{a}) = a + b \text{ (thm. 10b.)}$$

Example 2 (*Section 7.1.3*)

The following example shows the use of rule 5:

$$abc + \bar{a}bd + bcd = abc + \bar{a}bd.$$

As "a" appears in abc and $\bar{a}$ appears in $\bar{a}bd$, their product bcd can be omitted. To prove this, multiply bcd by $(a + \bar{a})$ which gives

$$\begin{aligned} abc + \bar{a}bd + bcd(a + \bar{a}) &= abc + \bar{a}bd + abcd + \bar{a}bcd \\ &= abc(1 + d) + \bar{a}bd(1 + c) \\ &= abc + \bar{a}bd. \end{aligned}$$

Example 3 (*Section 7.1.3*)

Rule 6 is illustrated by the following example:

$$\begin{aligned} &(a + b + c + d)(a + \bar{b} + d + e)\,(a + c + d + e) \\ &\qquad = (a + b + c + d)\,(a + \bar{b} + d + e). \end{aligned}$$

Since b is present in both values, the variables associated with b, being $(a + c + d) + (a + d + e) = (a + c + d + e)$ can be omitted. This can be proved by inverting the original product of sums:

$$\bar{a}\bar{b}\bar{c}\bar{d} + \bar{a}b\bar{d}\bar{e} + \bar{a}\bar{c}\bar{d}\bar{e}.$$

According to rule 1 $\bar{a}\bar{c}\bar{d}\bar{e}$ can be omitted; now inverting once more results in:

$$(a + b + c + d)\,(a + \bar{b} + d + e).$$

Example 4 (*Section 7.1.3*)

Another example of rule 6 is as follows:

$$(a + b)cd + \bar{a}\bar{b}ce + cde = (a + b)cd + \bar{a}\bar{b}ce.$$

Here both values of a combination of variables (a, b) appear, for we have: $(a + b)$ and $\bar{a}\bar{b}$, which is $\overline{a + b}$ (De Morgan). By writing $(a + b) = p$ and $\bar{a}\bar{b} = \bar{p}$ we get

$$pcd + \bar{p}ce + cde,$$

which is similar to Example 2 and can be treated in the same way.

Example 5 (*Section 7.2.1*)
A lamp should light up if any one, but only one, of three push buttons is pressed.

(a) The lamp should light up if one OR other of the push buttons is pressed, but NOT if two or more are pressed.
(b) The independent variables are the 3 push buttons.
(c) Let the push buttons be indicated by a, b and c.
(d) Let a be "1" if push button a is pressed,
let b be "1" if push button b is pressed, and
let c be "1" if push button c is pressed.
(e) The dependent variable is the lamp.
(f) Assign the letter L to the lamp.
(g) $L = 1$ if the lamp lights up.
(h) The truth table is as follows:

combination	a	b	c	L
1	0	0	0	0
2	0	0	1	1
3	0	1	0	1
4	0	1	1	0
5	1	0	0	1
6	1	0	1	0
7	1	1	0	0
8	1	1	1	0

(j) Combinations No. 2 ($\bar{a}\bar{b}c$), No. 3 ($\bar{a}b\bar{c}$) and No. 5 ($a\bar{b}\bar{c}$) give $L = 1$, so we get:

$$\bar{a}\bar{b}c + \bar{a}b\bar{c} + a\bar{b}\bar{c} = L.$$

8 Practical Circuits

This chapter contains a number of circuits of a fairly basic nature that have been found to be of particular value when setting up control circuitry, including sequential control. A knowledge of these "higher order" functions will allow the circuit designer to recognise the requirements of a layout. Going through the circuits presented here will provide many ready-made answers to design problems and give an insight into the way in which the functions could be linked to achieve more complex ones.

We shall consider in succession circuits for general combinational logic functions; time delays; the squaring of input signals; sequential circuits; counters; shift registers; and square wave generators.

All switching theories are based on the assumption that the input is either true 1 or 0 level. A slowly changing input may cause high frequency parasitic oscillations to appear at the output, due to feedback effects via stray capacitance between output and input. Where a slowly changing input could be expected, for example the signal from an integrating network, it is good practice to decouple the output by means of a small capacitor; typically, a value of 10 nF is sufficient.

8.1 General Combinational Logic Functions

By using various combinations of the basic logic circuits introduced in Chapter 1, the following functions can be made.

8.1.1 Coincidence

The circuit of Fig. 8.1 gives coincidence, that is, all inputs must be the same (*all* 1s or *all* 0s) to give an output. The function is $ab + \bar{a}\bar{b} = F$, for two inputs.

This circuit is sometimes used as a safety circuit, by using two input devices and checking that both devices give the same output.

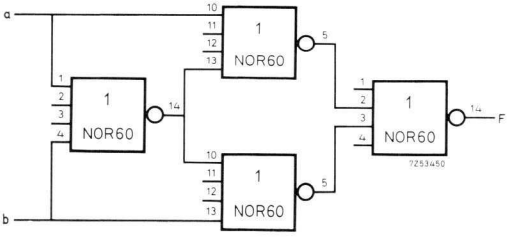


Fig. 8.1.
"Coincidence" circuit.

8.1.2 The EXOR

The OR function described in Chapter 1 is more accurately described as an "inclusive OR" because one or more inputs cause an output. The exclusive OR, known also as EXOR, performs the function wherein any one input, but not more than one, will give an output, as shown in Fig. 8.2. The function is $a\bar{b} + \bar{a}b = F$, for two inputs. This is the inverse of the coincidence function. An application for this circuit is in remote control, where conflicting commands from two or more separated stations must not occur coincidentally.

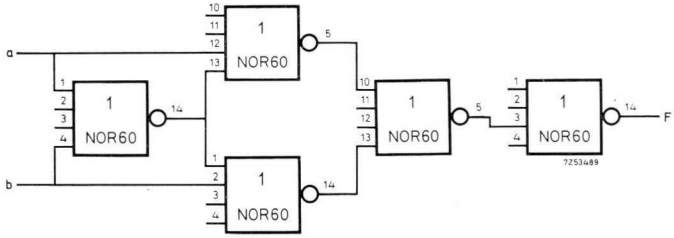


Fig. 8.2. "EXOR" circuit.

8.1.3 Memory functions

This section gives some further ideas on application of the memory principle discussed briefly in Chapters 1 and 7.

Cross-coupled memories. Only one of the outputs F_1 and F_2 in Fig. 8.3 can be at 1 level at any one time (both can be 0). An application here is in elevator control systems, to ensure that the cabin is not commanded to move in two directions simultaneously.

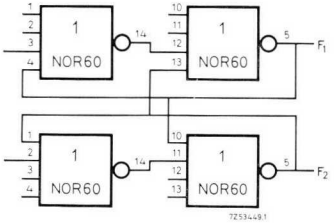


Fig. 8.3. Cross-coupled memory.

Attainment of speed. Industrial processes often require that the speed of a shaft does not either drop below or exceed a certain limit or that objects pass a point with a repetition frequency either below or above a certain limit. The circuit of Fig. 8.4 signals these conditions. It

is basically a memory which is reset automatically after a certain time (see also section 8.2.3).

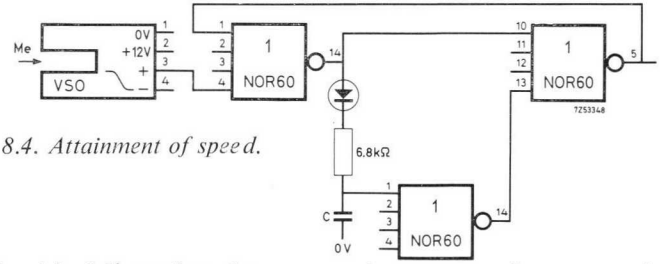


Fig. 8.4. Attainment of speed.

A 1 level is delivered to the memory input every time a vane is not in the VSO slot. Capacitor C discharges slowly to 0 level voltage, at which the memory output eventually becomes. The circuit produces a fixed duration pulse output. By feeding the output to a TU60 having a suitable delay (see Fig. 14.8), the TU60 output will stay 0 until the input reaches a certain frequency.

Detection of direction. Direction of an object, e.g. a clockwise or anticlockwise movement, can be detected using two cross-coupled memories in the configuration shown in Fig. 8.5*a*.

The input devices here are VSOs; a vane on the shaft should be long enough to enter both VSO slots, as indicated. If the vane now enters the VSO(1) slot from above, the NOR(1) output becomes 1 and sets the following memory ($M_a = 1$). The vane now enters VSO(2), but the NOR(2) output remains at 0 due to cross-coupling with NOR(1). M_a therefore stays set until the vane passes beyond VSO(2), at which point both inputs to NOR(3) are 0 and M_a is reset to 0. Thus, M_b remains at 0 and M_a delivers a pulse at every passage of the vane. The reverse occurs if the vane travels in the opposite direction, that is VSO(2) to VSO(1). Memory outputs M_a and M_b could be used as inputs to an adder/subtractor device giving the total number of shaft revolutions (forward minus reverse). If steady M_a and M_b signals are required, the NOR(3) resetting circuit could be removed and two reset connections made as shown in Fig. 8.5*b*.

8.2 Time Delay Circuits

Time delay of signal levels must often be introduced in control circuits. Delays can be produced by use of *RC*-elements or the TU60. Circuits to produce a pulse of specified duration using these methods are given in Section 8.2.3.

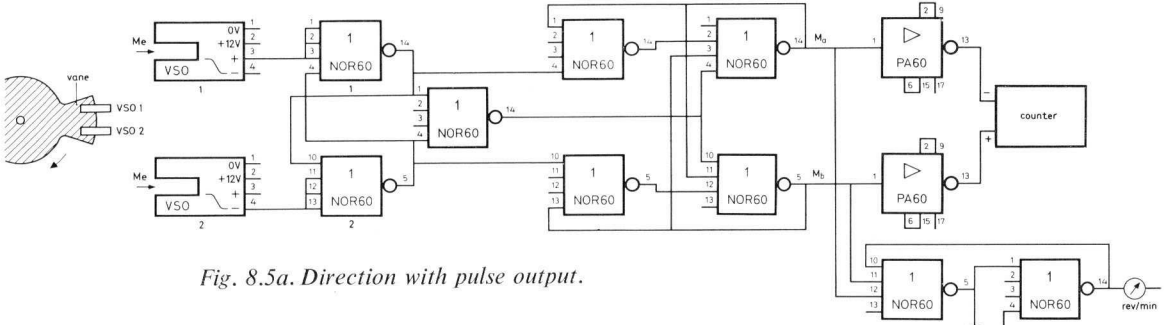


Fig. 8.5a. Direction with pulse output.

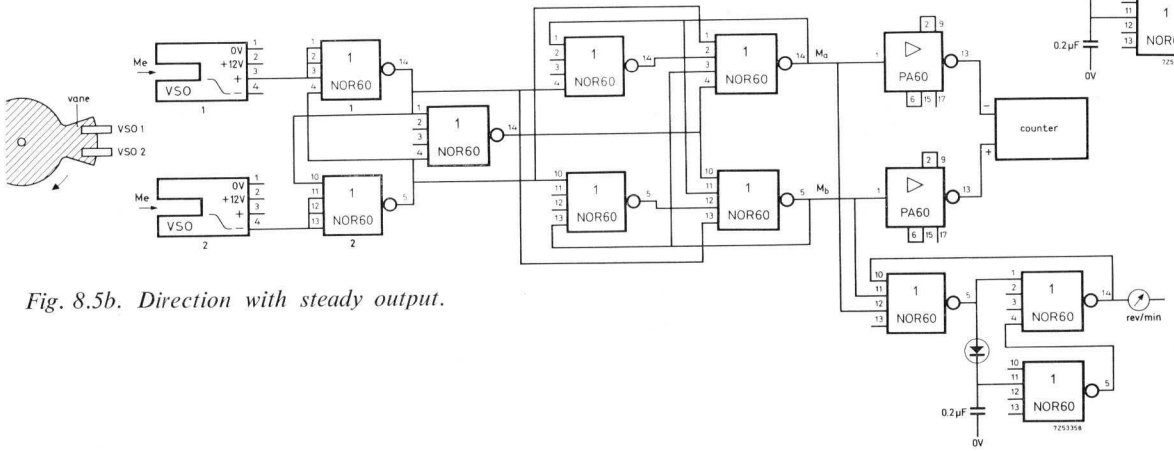


Fig. 8.5b. Direction with steady output.

8.2.1 Delays with RC Elements

It may be desirable to delay the result of a level change for some time, e.g. to make sure that a level is changed before or after a change of level at another point in the system is effected. Various simple methods using the delay introduced by *RC*-combinations are available.

If a 0 to 1 level step is applied to the network of Fig. 8.6 the output voltage will increase and decrease exponentially (after the input has gone from 1 to 0) at a rate determined by the values of *R* and *C* (Fig. 8.7).

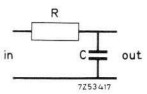


Fig. 8.6. RC-network.

Fig. 8.7. Effect of the RC-network (a - input, b - output).

Now, if this network is connected to a square-wave source and the output is loaded by a NOR input the NOR output is delayed with respect to the input level change (Fig. 8.8). It will be seen that the insertion of the *RC*-element causes two discrete delays. The one at the left is determined by the maximum low level output. The actual value of this level will depend largely upon the current gain of the transistor in that particular NOR, but all we know is the data from the specifications saying that this level will be at least 1 V, all other NOR inputs floating. With one or more inputs returned to the zero volt line (either directly or via the output of other NORs in the 0 output state) this level will be higher than 1 V. A further complication is brought about by the fact that the rate of rise of the voltage across *C* will also be governed by the load (i.e. the input impedance of a number of units connected in parallel with *C*).

A similar reasoning applies to the minimum high level which causes the NOR to be fully conducting (output 0 level). As the rate of rise and

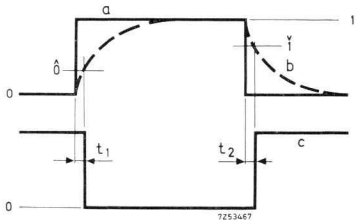


Fig. 8.8. (a) Input to RC-network, (b) input to NOR, (c) output from NOR.

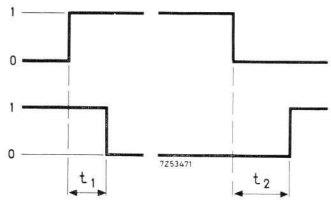


Fig. 8.9. Effect of RC-network.

decay of voltage across C is proportional to the actual value of the supply voltage, time delays will become shorter for maximum low level conditions (t_1) and longer for minimum high level conditions (t_2).

Fig. 8.9 summarizes the effects of the RC-network on the output of the NOR; here t_1 denotes the delay of a positive-going input, and t_2 that of a negative-going input.

Delay of both positive- and negative-going steps is not always required or desirable. The following circuits give typical delays to be expected with various configurations.

Delay of a negative-going step only. In Fig. 8.10, C starts charging via R

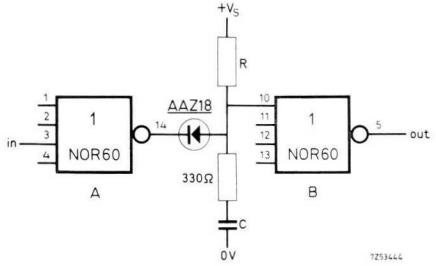


Fig. 8.10.(a). Negative-going delay circuit.

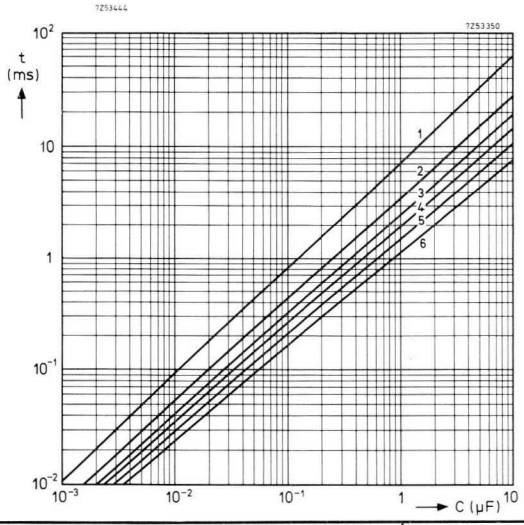


Fig. 8.10. (b). Dependence of t on C and R. The value of R depends on the loading on NOR B output, as follows:

loading	*1*	*2*	*3*	*4*	*5*	*6*	*DU*
max. value of R	*47*	*22*	*15*	*13*	*9*	*7·5*	*kΩ*
curve	*1*	*2*	*3*	*4*	*5*	*6*	

after NOR *A* output goes to 1 (input goes to 0). After a certain time *t*, the input of NOR *B* becomes sufficiently positive to switch its output to 0. When the input to *A* becomes 1, NOR *B* output becomes 1 immediately.

Delay of positive-going step only. If NOR *A* input becomes 1 the capacitor discharges slowly through the input resistor(s) of NOR *B* until its output goes to 1 (Fig. 8.11).

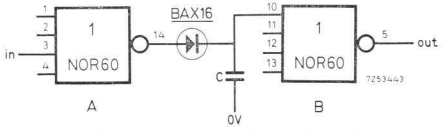


Fig. 8.11a. Positive-going delay circuit.

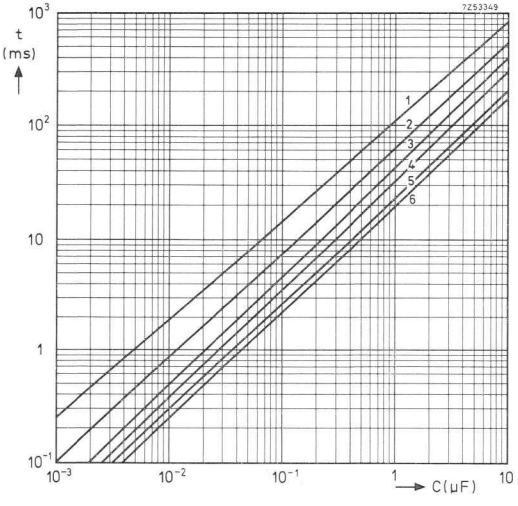


Fig. 8.11b. Dependence of t on C and loading (1 to 6 DU).

Unequal delay of positive- and negative-going steps. Circuits which give both positive- and negative-going step delays, but of appreciably differing times, are given in Fig. 8.12. If the two resistors in Fig. 8.12*a* have the same value, twice as much current will flow into the capacitor at a positive-going step as will flow out at a negative-going step. Thus positive-going delays will be halved. In Fig. 8.12*b*, negative-going steps are delayed less than positive-going ones. As had been pointed out, this circuit produces a delay that is not well-defined and of relatively short duration. If more

accurate or longer time delays are required the TU60 should be used.

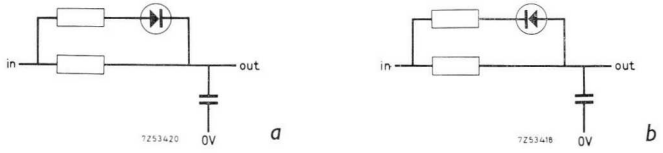


Fig. 8.12. Circuits providing unequal delays; (a) positive-going delay exceeds negative-going delay; (b) negative-going delay exceeds positive-going delay.

8.2.2 Delays with the TU60

The symbol for the timer unit is given in Fig. 8.13. The resistor and capacitor are external and should be selected and added by the user to provide the delay he requires in his particular circuit. By making the resistor adjustable a wide range of time delays can be obtained (see Chapter 14).

Essentially, the unit performs an inverting operation which is delayed when the input signal is negative-going but not otherwise.

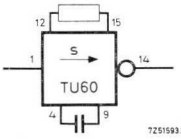


Fig. 8.13. Timer unit TU60.

Fig. 8.14 gives an example of the delay of the output after the input has gone to 0. The delay time t is approximately RC seconds. A positive-going input signal will result in an undelayed 0 at the output (Fig. 8.15).

The precautions to be observed if this timer is to be used in arrangements where short time delays are needed in rapid sequence are given in Chapter 14.

An important phenomenon should be mentioned here. If, after having started a time delay period, the timer input goes 1 and stays 1 for at least 18.9 ms per μF of C before the delay time as determined by the external R and C has elapsed, the delay will restart after the input has

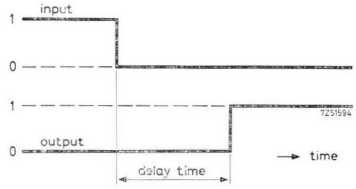


Fig. 8.14. Delay of negative-going step.

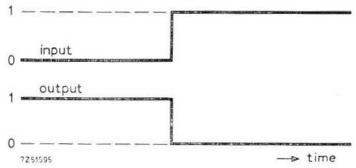


Fig. 8.15. Effect of positive-going step.

gone to 0 (Fig. 8.16). If during the delay time the input is brought to and kept at 1 level, the output will stay 0.

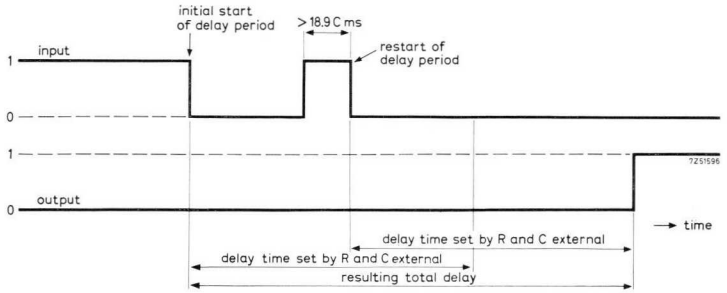


Fig. 8.16. Re-start of delay period.

8.2.3 Generation of a Fixed-Duration Pulse

In order to exploit the possibilities of level logic more fully and to obtain a predictable condition from a source that may have characteristics which might cause ambiguous situations, circuits which produce a pulse of specified duration are available.

The two NORs in Fig. 8.17*a* form a memory which will be reset after a certain delay governed by C. The circuit can be triggered either by a pulse or by a rising voltage. Fig. 8.17*b* gives the relationship between C and pulse duration t_p. At the output 5 DU is available; delays up to 100 ms are possible.

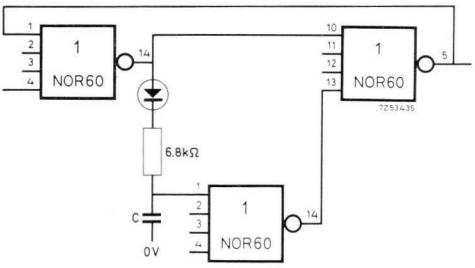


Fig. 8.17a. Pulse output circuit.

The circuit can be used for standardizing input signals to a control system, e.g.:

— to reduce the output duration with respect to the input duration;
— to stretch an input signal for producing an output of longer duration;
— to change a slowly varying input voltage into a steep pulse;
— to give an initial reset pulse to memories at power turn-on (Fig. 8.18).

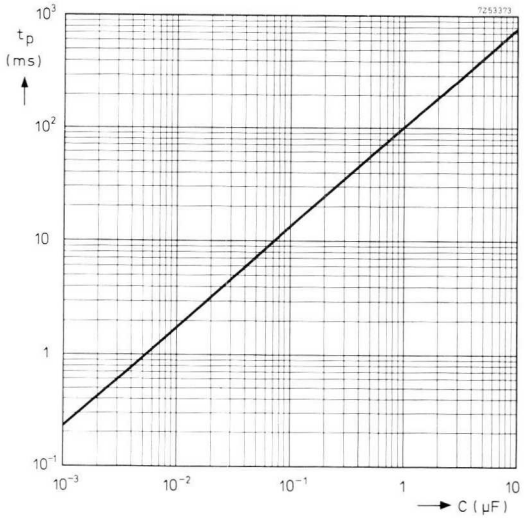


Fig. 8.17 b.
Pulse duration t_p as a function of C.

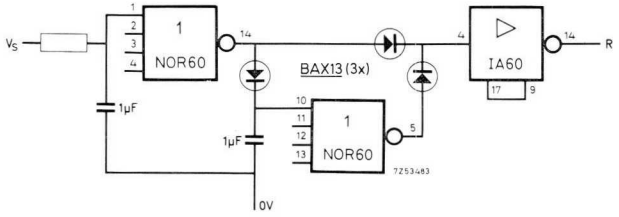
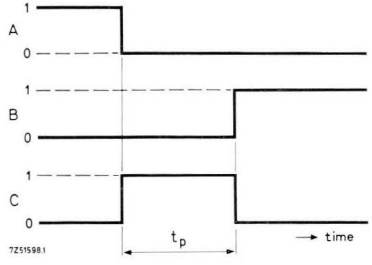


Fig. 8.18. "Automatic reset" pulse output.

Two circuits which produce a 1 signal of a longer duration are given in Figs 8.19 and 8.20. The circuit of Fig. 8.19 converts a zero-going step



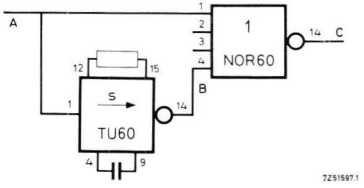


Fig. 8.19.
Pulse output with the TU60.

into a 1 level pulse, that of Fig. 8.20 may be used when it is desired to stretch a 1 input signal of short duration. They give an output of 6 DU and 5 DU respectively.

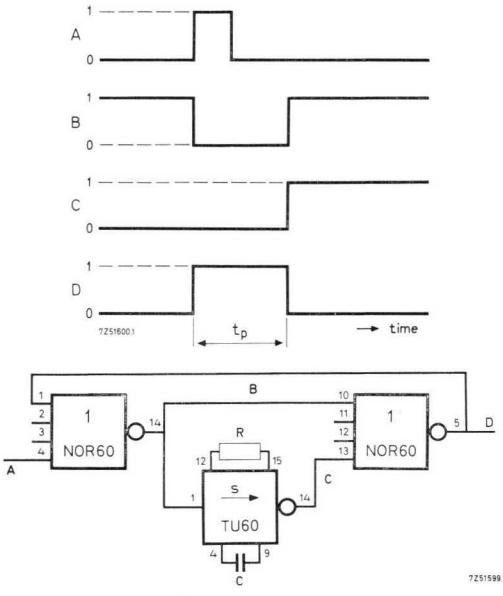


Fig. 8.20. Stretching an input pulse using the TU60. $t_p = RC$, if the time during which the output is 0 between pulses exceeds 6.4 ms per μF of C, if the pulse time exceeds 3.3ms per μF of C and, moreover, if 0.1 $M\Omega < R < 1$ $M\Omega$.

8.3 Squaring of Input Signals

In order to improve the accuracy obtainable from sensors with an analogue type of output voltage (e.g. a VSO), use can be made of the circuit of Fig. 8.21 and 8.22. This results in a large amplification of the input

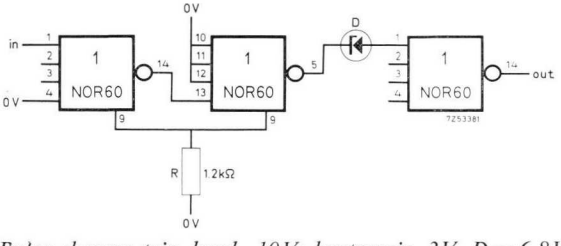


Fig. 8.21. Pulse shaper: trip level, 10V; hysteresis, 3V .D = 6,8V VRD.

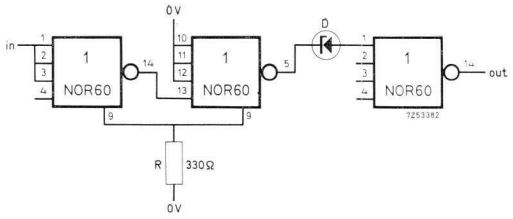


Fig. 8.22. Pulse shaper: trip level, 3V; hysteresis, 0.6V. D=6,8V VRD.

voltage. Here by the logic levels are much better defined because the time for which the output is within the indefinite region, is greatly reduced.

The circuit of Fig. 8.23*a* is another form of the Schmitt Trigger type of squarer. The circuit produces an output having very short rise and fall times, independent of the input wave shape. The output capability is 20 DU. Fig. 8.23*b* shows output level F vs. V_{in} for diode type BA114.

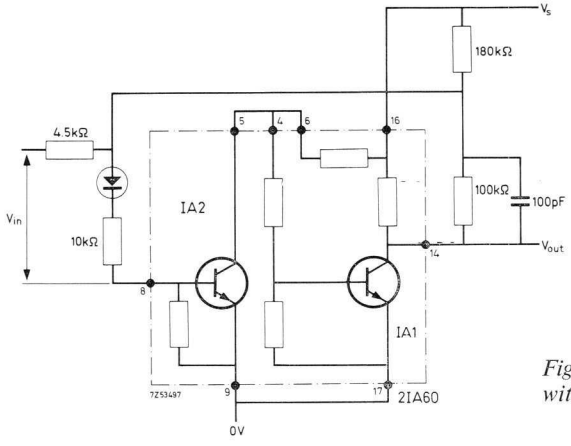


Fig. 8.23a. Pulse shaping with the 2.IA60.

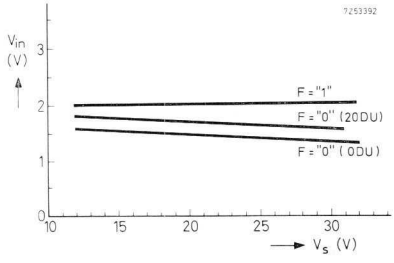


Fig. 8.23b.

8.4 Sequential Logic Circuits

These types of circuit are frequently encountered in industrial control in various degrees of complexity. The following circuits give some typical configurations. Counters, a particular form of sequential logic, are dealt with in section 8.5.

8.4.1 Sequential Circuit for an Industrial Process

A typical example of sequence control is given by the following description of a metal cleaning process. A number of operations must take place in the order given below:

operation	initiated by	controlling
1: Soak clean	push-button or *LS* 4	timer and *S* 1
2: Cold rinse	timer output	*S* 2
3: Cathodic clean	*LS* 2	*S* 3
4: Anodic clean	*LS* 3	*S* 4
1: Soak clean	*LS* 4	timer and *S* 2
...	...	...

Automatic recycling is to take place at the end of operation 4. In this example *S* denotes the solenoid to switch on the driving motor, the pump, etc.; *LS* is the limit switch.

Fig. 8.24 shows the lay-out of the basic circuit. On pushing the press-button, memory *1* for operation 1 is set, giving a 0 signal to the timer unit and energizing S_1. The timer output eventually goes to 1, setting memory *2* for operation 2 (energizing S_2) and resetting memory *1*. When operation 2 is complete LS_2 will be closed and memory *3* set by the two 0 level inputs at NOR *A*. A similar action occurs for subsequent operations. If automatic recycling is required, switch *SR* must be closed, so that memory *1* is set again, independently of the start button.

Basically, the circuit consists therefore of a number of memories, AND functions and time delays. The AND functions are necessary to ensure that an operation will start only if the appropriate limit switch AND previous operation signals are present.

8.4.2 Queueing Problem

It is often desirable in control problems to acknowledge input signals in the order in which they arrive. For example, when the raw material used by a machine in a manufacturing process is running low, the machine communicates back to the central store that it requires replenishing, but

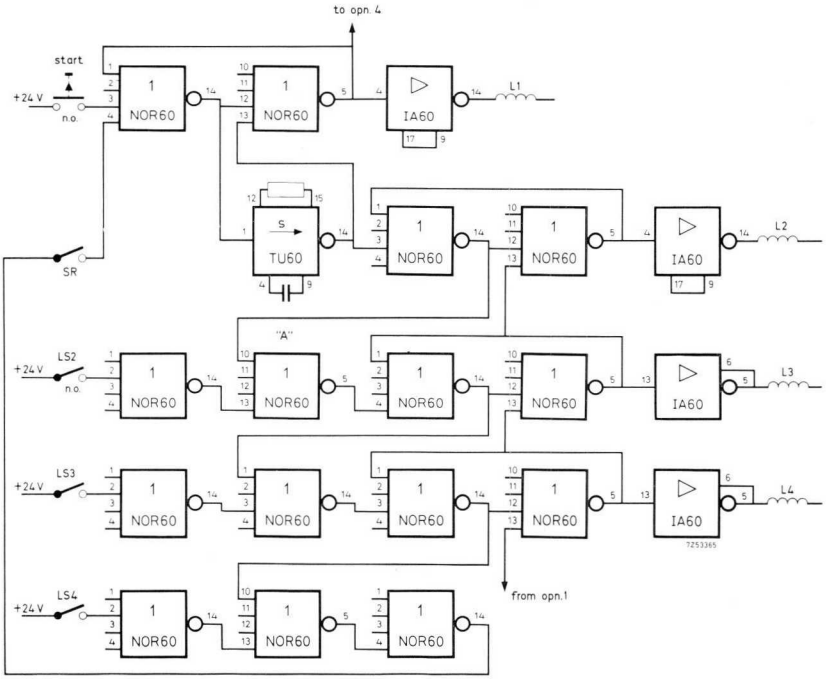


Fig. 8.24. Basic logic circuit for a metal-cleaning process.

perhaps other machines are also waiting to be served by the central store. It is therefore imperative that the machines are dealt with in the order in which the requests for more raw material were made. Obviously there are many other instances where it is desirable to form a queue. We will examine this problem in terms of NORS.

In the "bi-stable" circuit of Fig. 8.25, if A and B are both 1, then X and Y are both 0. If A changes to 0, Y will be 0 and X will be 1. But if B changes to 0 and A stays at 1, Y will be 1 and X will be 0. Therefore, we can state that if A operates before B, then Y is 0. Now, given four

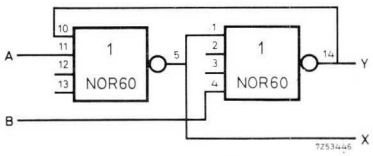


Fig. 8.25. Bi-stable circuit.

variables A, B, C and D, by comparing each pair we obtain a complete description of the queue. This would be as shown below.

A	AB	AC	AD
BA	B	BC	BD
CA	CB	C	CD
DA	DB	DC	D

The order in which the letters are written indicates their priority. For example, in the top row we have A, then AB, AC and AD, indicating that A is first in the queue. The same applies to the other rows. If we feed a group in one of the rectangles in the top row into the circuit of Fig. 8.25, a 1 output will appear if A becomes 0 first. The same will apply to rows B, C and D. If we now substitute the circuit of Fig. 8.25 for each of the rectangles excluding rectangles A, B, C and D, and connect the output Y of each circuit on the same row to a NORBIT acting as an AND gate, then a 1 signal will appear at the output of the NOR corresponding to the variable first in the queue.

This will be illustrated by the following example (Fig. 8.26). Suppose C to be first in the queue and B second. As soon as C changes from 1 to 0, all inputs to the C AND gate are now a 0, because the Y-outputs of the rectangles CA, CB and CD were already 0. So the C AND gate delivers a 1.

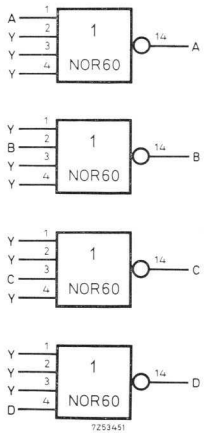


Fig. 8.26. Basic queueing circuit.

The Y outputs from the rectangles AC, BC and DC, however, have become a 1, thus blocking the A, B and D AND gates.

Since B was second in the queue, all inputs of the B AND gate are all 0, except the one from rectangle BC. However, as soon as C returns to 1, the Y output from rectangle BC changes from 1 to 0, by which the B AND gate is opened, now delivering a 1 and in its turn becoming first in the queue.

The circuit can be simplified by reducing the number of NORBITS. If we look again at the table we can

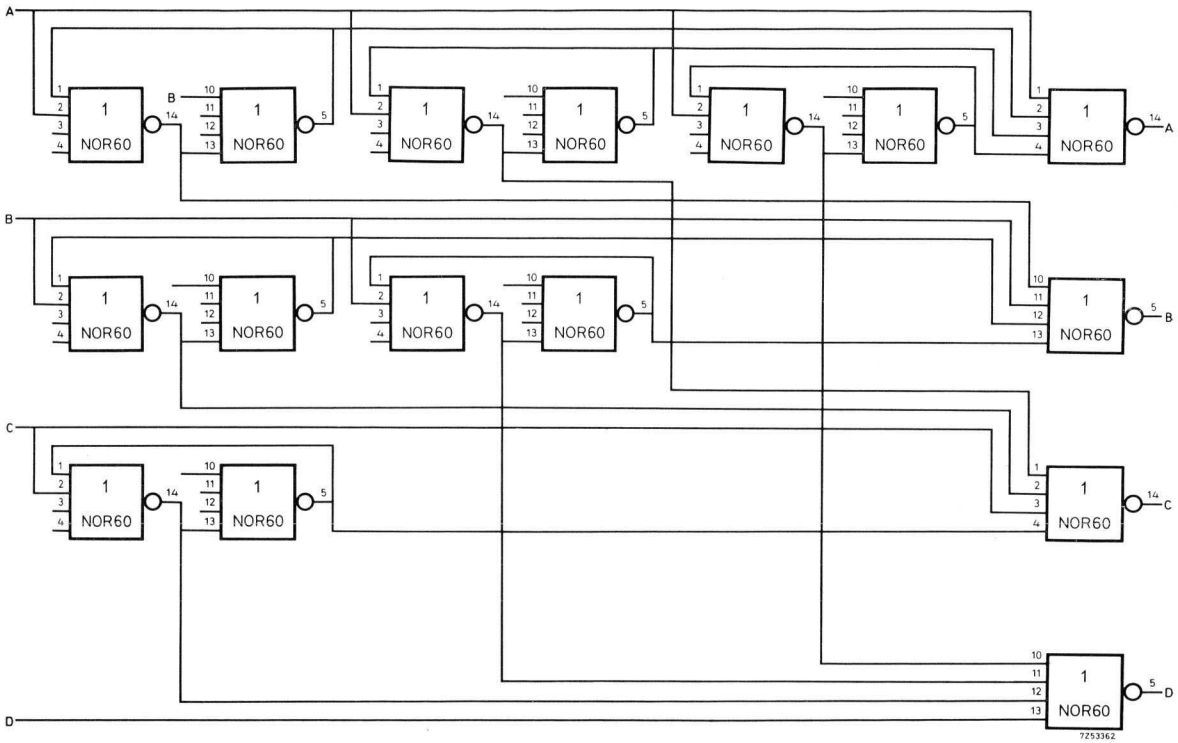


Fig. 8.27. Queue-of-4 circuit. At the left: inputs; at the right: outputs.

see that in many cases the function in one rectangle is the complement of another. Therefore, instead of taking the signal from output Y it could be taken from the complementary output X. All the functions below the bold lines thus become redundant. The complete queue of 4 is shown in Fig. 8.27.

8.5 Counting Circuits

Control circuits sometimes require a counting facility as part of the combinational or sequential logic. In most cases the number to be counted is related to a number of steps in the control operation. The number of steps will usually be a fixed low number; moreover very seldom will there be need for display, or variation of the count. In such instances one of the following circuits may serve the purpose.

The signal that constitutes the counting information may be derived from various input devices, either electromechanical or electronic. Level logic is used throughout. In order to be independent of the actual form of the count information, the input signal is shaped. Long lines should be terminated with an SF60 unit or a capacitor to avoid trouble from interference.

8.5.1 Simple Column-type Counter

In the column-type counter of Fig. 8.28 each count is registered and stays registered as shown below.

P_1	0	1	1	1
P_2	0	0	1	1
P_3	0	0	0	1
P_4	0	0	0	0
count	zero	one	two	three

The input count signal should be a positive-going voltage, shaped to a square pulse of fixed duration (by means of the circuit of Fig. 8.17*a* if necessary).

Initially all memories (P_1 to P_n) are reset to zero. The diode and capacitor network is connected to the output of the left-hand NOR, now at 1 level, thus all the memories except P_1 are kept at zero output. If now the sount signal a is applied to all memories, only the P_1 memory will change state if the time for the voltage across C to decay to zero is longer than the duration of the a signal. The next count signal, provided it comes after

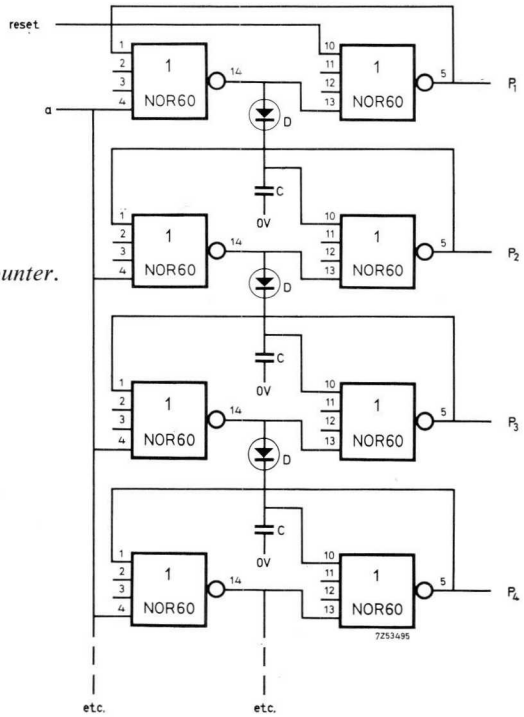


Fig. 8.28. Simple column counter.

the time needed for the capacitor to be discharged has elapsed, will set P_2, and so forth (Fig. 8.29). If no further additions are made the circuit shown will count up to 4, and remain in this condition.

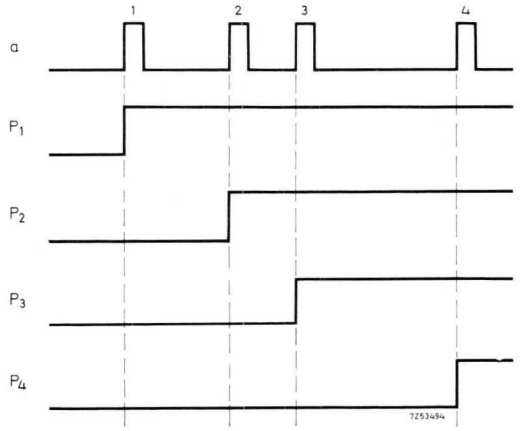


Fig. 8.29. Timing diagram.

Outputs P_1-P_n can be used in any desired way; as there is only 3 DU available, LPAs might be used as output amplifiers. By making the $n + 1$ count produce a reset and a set (count) signal, the counter may be emptied without loss of the $n + 1$ count. The signal-shaping circuit should produce the required number of DUs for the number of stages used (1 DU required per stage).

8.5.2 Counter having only one output at 1 level

The P outputs of the above counter may be made to give, through subsequent logic, only one active output at a time. A typical application of such a circuit, described below, is in programme generation (cf. Section 11.1).

In Fig. 8.30, the pulse a is inverted. At reset or start of counting P_0 is 1, and outputs P_1-P_n are 0. The first pulse a sets P_1 at 1 level but does not affect subsequent stages if capacitors C create a longer delay than the

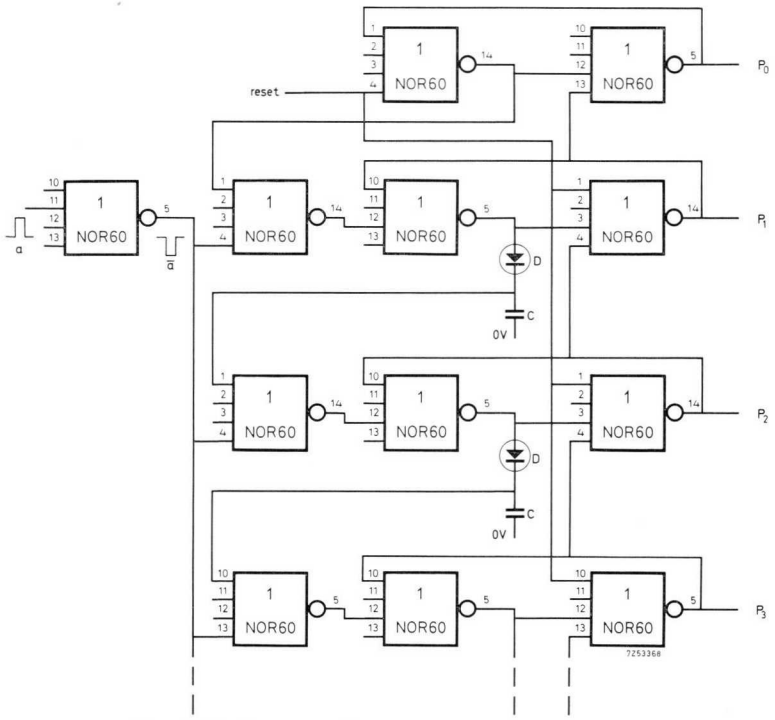


Fig. 8.30. Counter with only one output at 1 level.

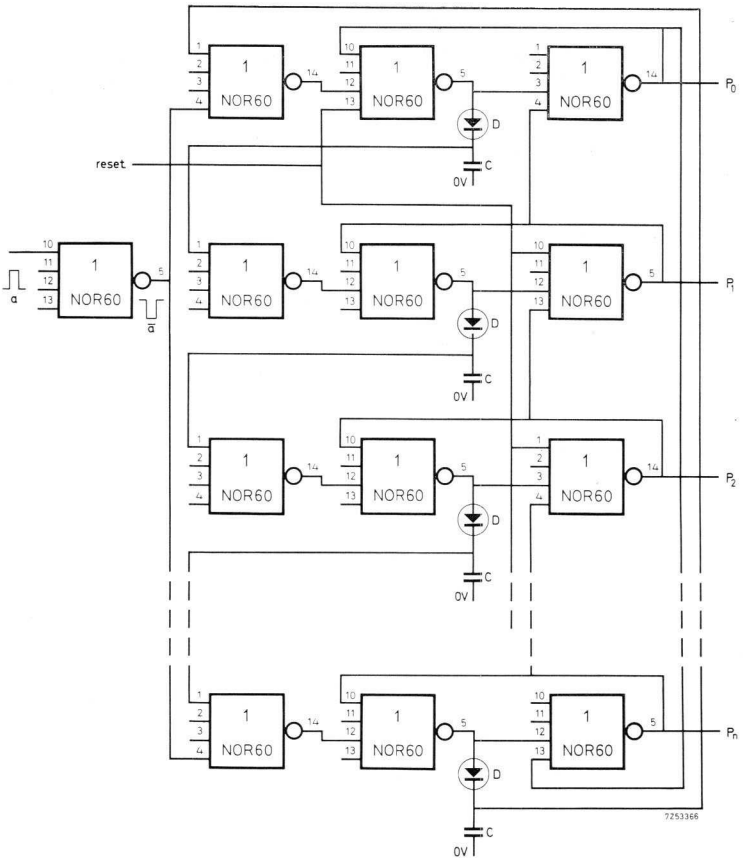


Fig. 8.31. Ring counter.

duration of pulse a, because their left-hand NORs are then blocked by 1 levels from preceding stages. A second pulse a will set P_2, which then resets P_1.

8.5.3 Ring Counter

A ring counter resumes counting at zero after having reached the full count The ring counter shown in Fig. 8.31 operates on the same principle as the circuit of Fig. 8.30, i.e. only one output P is at 1 level at any moment. At the count of $n + 1$, however, P_0 is set and counting is resumed without loss of input pulses. The general reset line extends only to the last-but-one stage; P_n is reset only by P_0.

8.5.4 Reversible Counter (columm type)

The circuit of Fig. 8.32*a* can be made to count forwards (P_1 to P_n) or backwards (P_n to P_1), by applying the pulses to be counted to one of two inputs, as (*b*) or by using a single input for all count pulses, and secondary inputs "Backward" and "Forward" to one of which zero level is applied, as *(c)*. Power turn-on reset should make all *P* outputs zero. The maximum number of stages is 19. For component values, see p. 129.

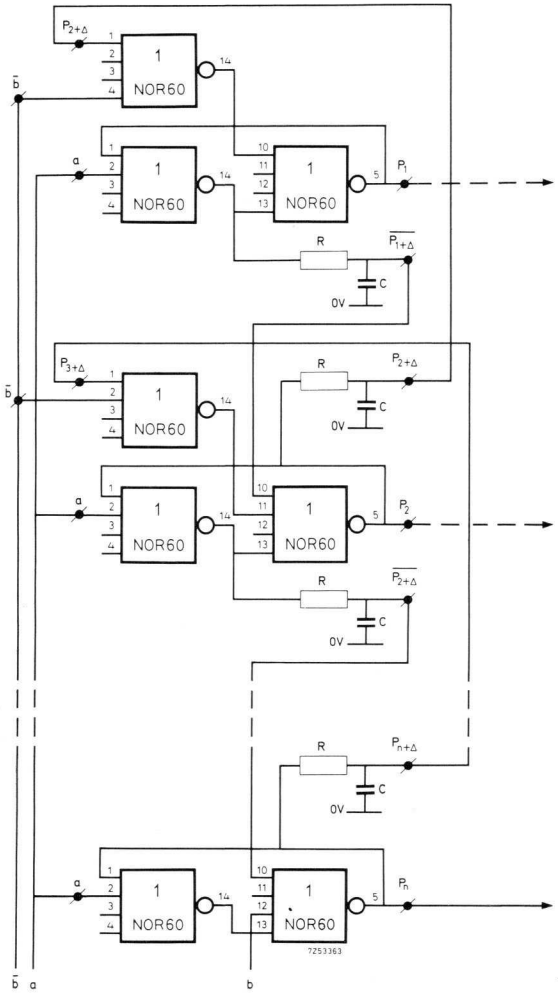


Fig. 8.32a.

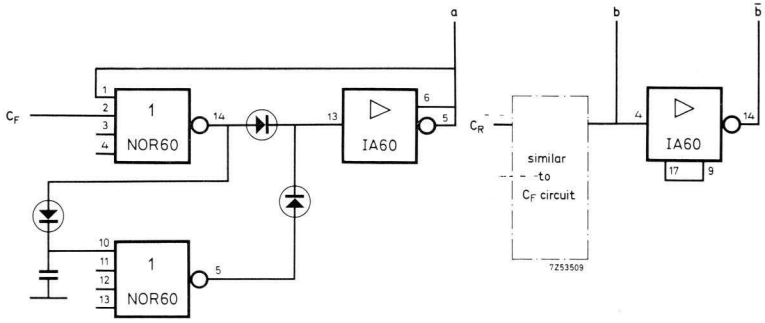


Fig. 8.32b. Separate forward (C_F) and reverse (C_R) counting signals.

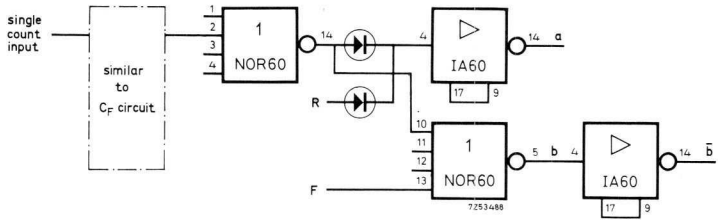


Fig. 8.32c. Single counting signal, with counting direction determined by $F = 0$ (forward) or $R = 0$ (reverse.)

8.5.5 Fast Counter

All counting circuits described above have a somewhat limited speed because of the capacitors between stages. Much faster counting is possible, however, by using direct coupling.

Two counters are described, identical except that one is equipped with NORs, the other with simple diode gates. The latter essentially much cheaper version is likely to prove more attractive for most applications, although the upper temperature limit of the counter is 60 °C with the AAZ18 diodes specified. This circuit has also the advantage of requiring less space, and a single decade can in fact be built on one printed wiring board. Prototype counters have been operated satisfactorily up to 50 kHz; as far as supply dependence is concerned, it is well within the 60-Series voltage tolerance of $\pm$ 25%.

As the operation of the two counters is identical, the same description will suffice for both. The block diagrams are shown together to facilitate

comparison. In each case drawing (*a*) refers to the NOR gates and drawing (*b*) to the diode gate circuit.

The counters are based on the "double rank" system for inherent safety and because no auxiliary memories are then required. This makes a pulse divider necessary which, together with the counter proper and a coupling unit (to interconnect decades), brings the number of sub-units to three.

It will be noted that the diode gated version counts 1 level pulses whereas the NOR version counts 0 level pulses, which leads to the inverted pulse diagrams shown in Fig. 8.33.

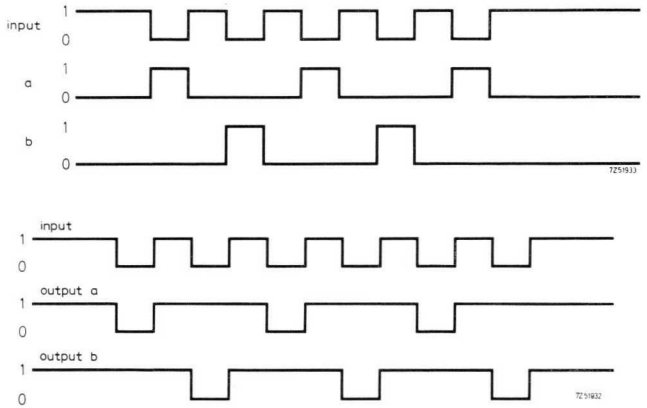


Fig. 8.33. Relationship between divider input and output signals.

The block diagrams of the divider are shown in Fig. 8.34 and the relevant pulse diagram in Fig. 8.35. Resistor R is included to ensure that A_{10} and A_{11} are switched before A_7. *RESET* switches all memories to the start condition.

Assume a train of pulses on the input; A_{10} has a 0 on its second input, so that the first 0 pulse will switch A_{10}, which will reset memory A_{3-4}, and output a will go 0. When the input returns to 1, gate A_8 will open, reset memory A_{1-2}, which in turn will set A_{3-4}, restoring output a to 1 level.

The next 0 input pulse will open gate A_{11} to reset memory A_{5-6} so that output b becomes 0. Restoration of the input to 1 will open A_9 so that memory A_{1-2} is set and output b returns 1.

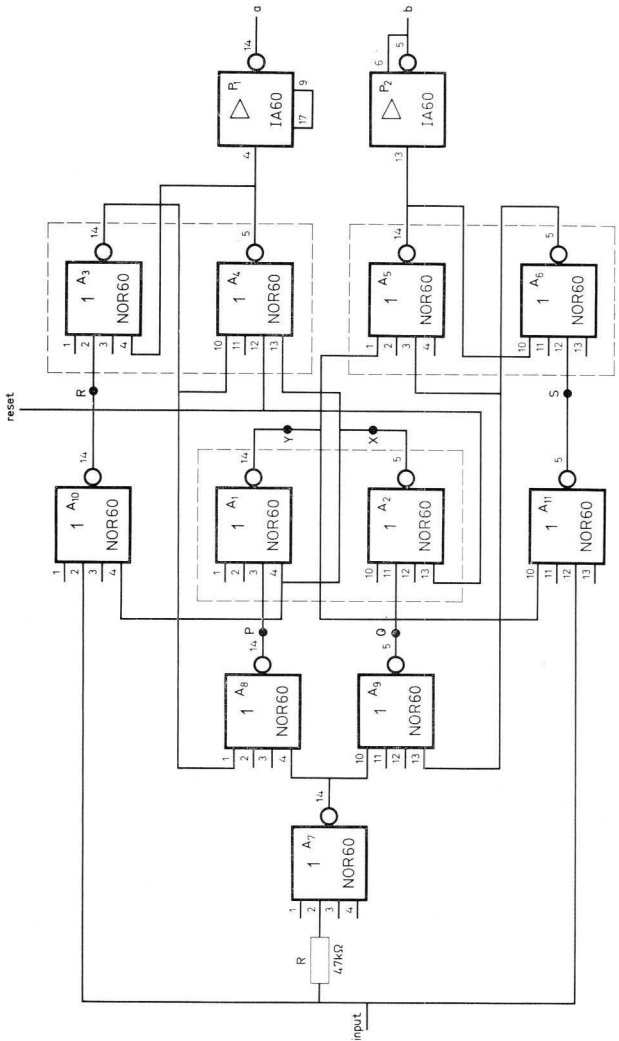


Fig. 8.34a. NOR gate pulse divider.

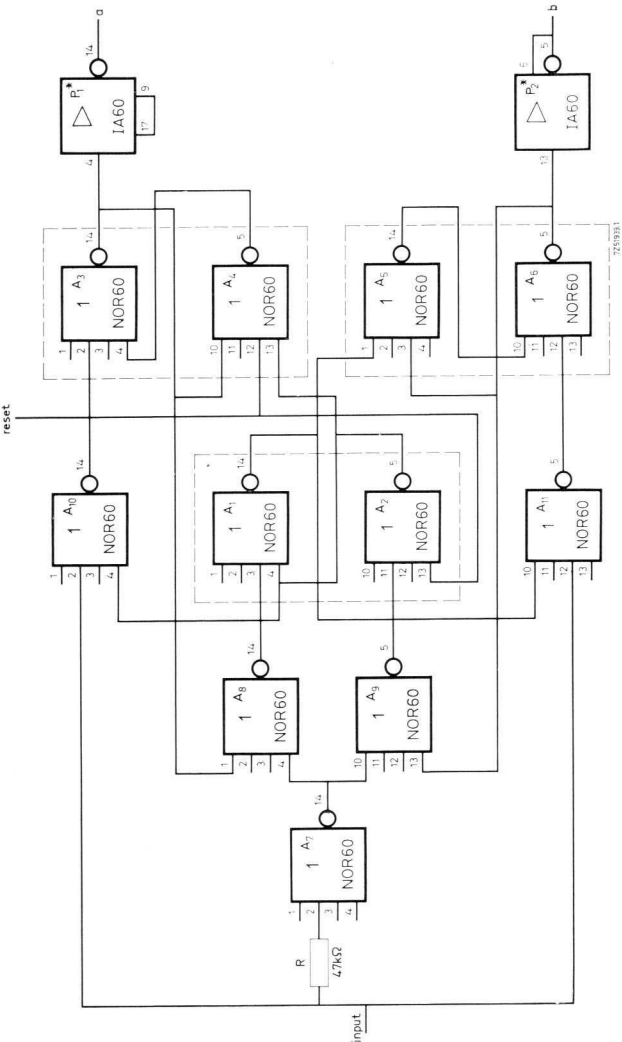


*Fig. 8.34b. Diode gate pulse divider. The NORs marked * must not be connected to supply voltage.*

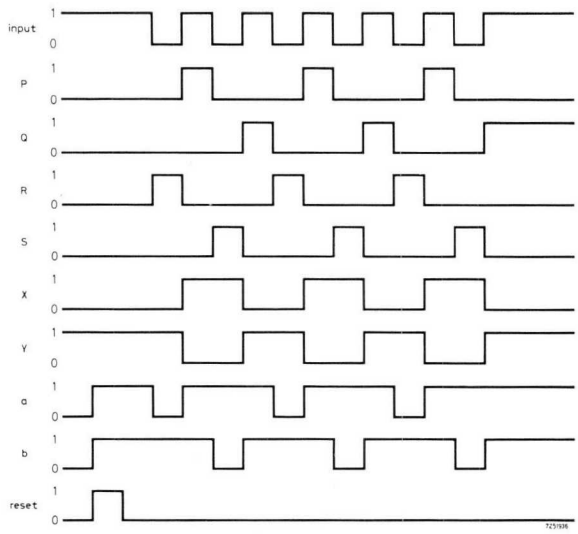


Fig. 8.35. Pulse diagram for Figs 8.34(a) and (b).

The two versions of the counter are shown in Fig. 8.36 and Fig. 8.37; their truth table is given below.

position	A	B	C	D	E
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1
10	0	0	0	0	0

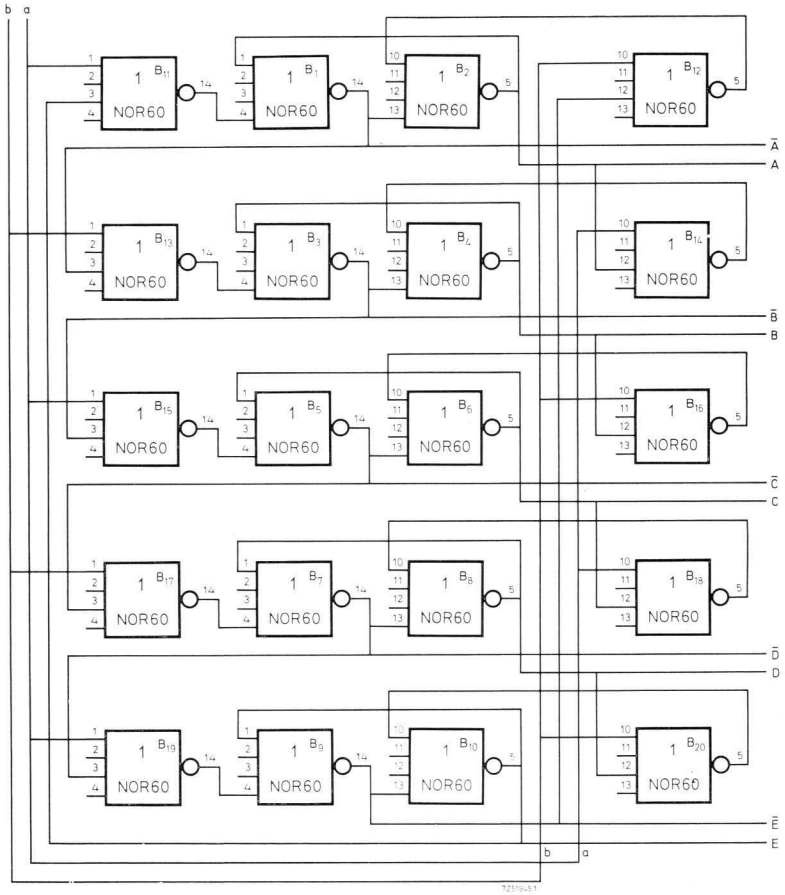


Fig. 8.36. NOR gate counter.

In the start condition all outputs are at 0, the associated inverse outputs being 1. Each input gate, B_{13}, B_{15}, B_{17} and B_{19} has one input taken from the inverse output of the preceding stage. So that the first input pulse on a will switch B_{11} and set memory B_{1-2} (changing the output on A to 1 level) B_{11} is prepared by the fifth stage output.

The next pulse will be on b and will set the memory of the second stage, and so on, down to the fifth stage. When the fifth stage has been set, the next pulse on b will reset the first stage. Similarly, the next pulse on

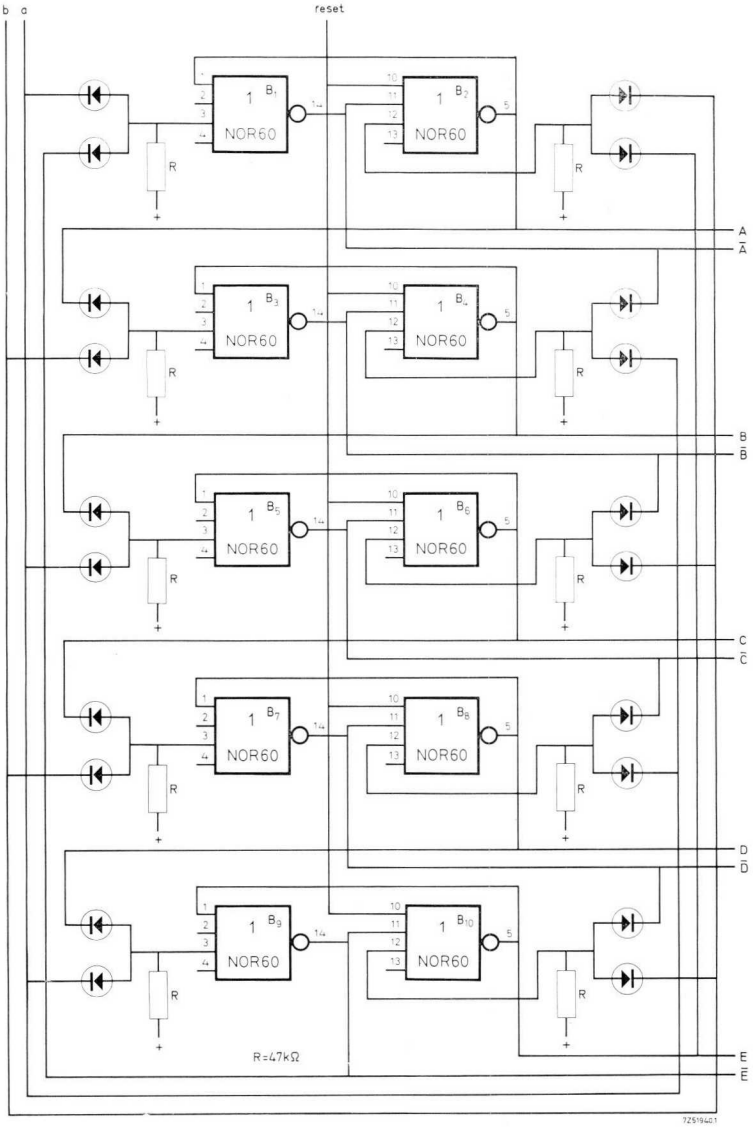


Fig. 8.37. Diode gate counter.

a will reset the second stage, and so on, until the fifth stage has been reset. The action then recommences.

Although it would be simple to use a pulse divider to couple two decades, a more economical way is shown in Fig. 8.38 (the associated pulse diagram is shown in Fig. 8.39). A *b* pulse, in conjunction with *A* and *E* being 0, will set memory C_{1-2} to agree with the condition of C_{3-4}. The next *a* pulse will then set to the C_{3-4} opposite condition, ready for memory C_{1-2} to be switched again as soon as *A*, *E* and *b* are all zero. This will occur only on a change from count 9 to count 0.

For the interval between the *b* pulse and the succeeding *a* pulse, on the first occasion that C_{1-2} is set, C_5 has 0 on all inputs, so that an output pulse will be produced on *a'* via P_3. On the next occasion the output pulse will be on *b'* via C_6 and P_4.

Fig. 8.40 shows four decoding systems. The first (*a*) is suitable for decoding the 1 outputs of the diode gate counter; (*b*) is suitable for the 0 outputs of the NOR gate counter; (*c*) is for the diode gate counter in

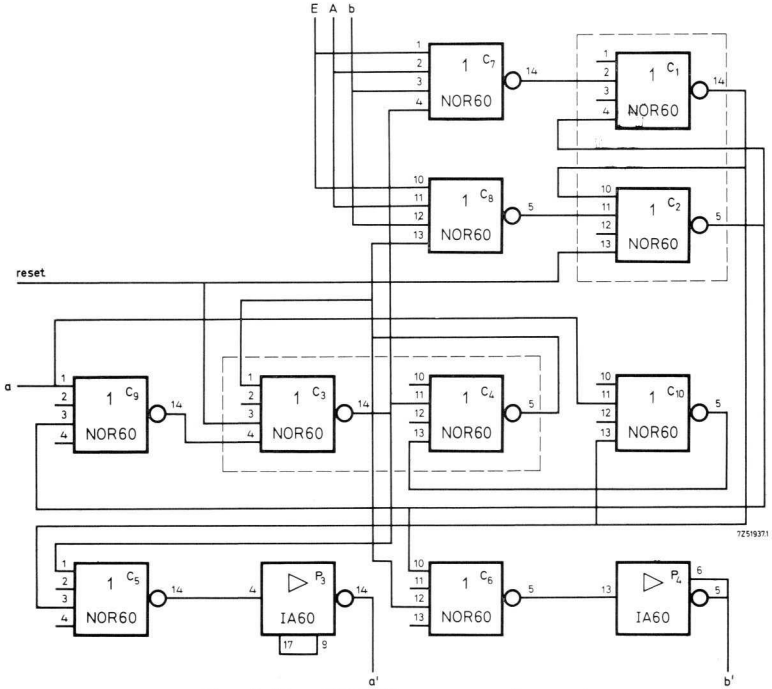


Fig. 8.38a. NOR60 gate coupling unit.

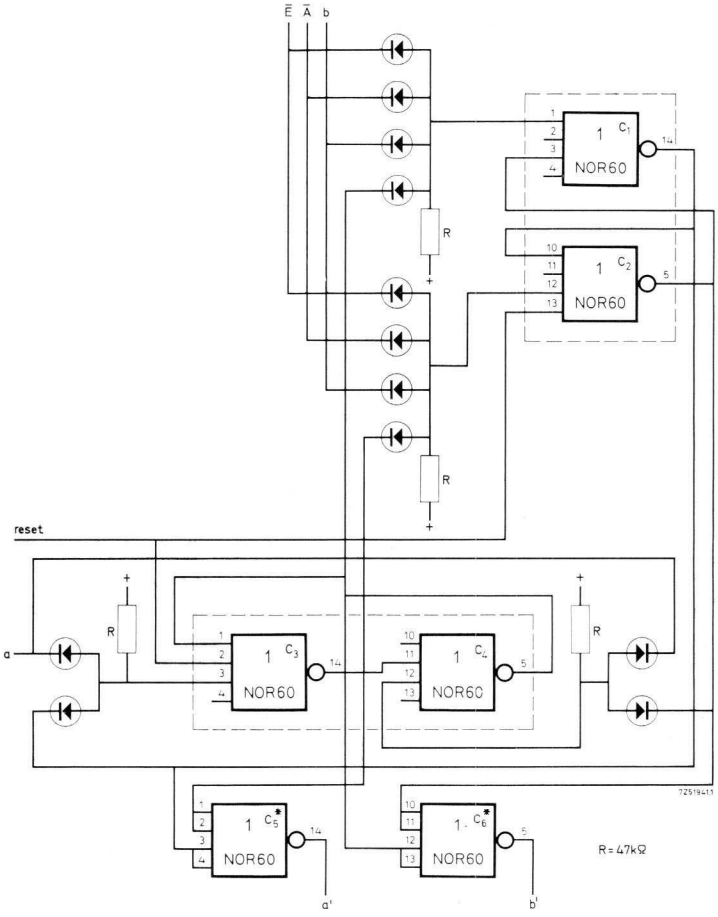


*Fig. 8.38b. Diode gate coupling unit. NORs marked * must not be connected to supply voltage.*

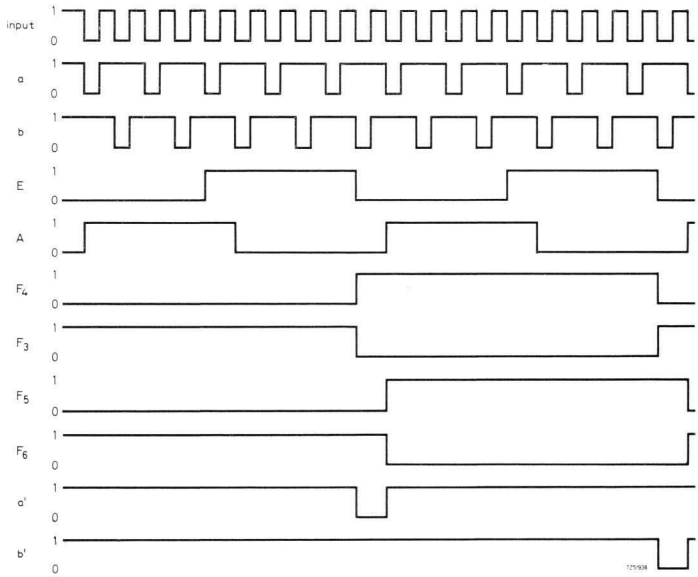


Fig. 8.39. Pulse diagram for Figs 8.38 (a) and (b).

conjunction with a decoding thumbwheel switch (10-position 2-pole switch, catalogue number 4311 027 82201); and (*d*) shows how a numerical indicator tube can be driven via BSX21 silicon transistors from the diode counter. The decoding sequence is shown in the table below.

1 level at terminals:	and 0 level at terminals:	indicates a count of:
$\bar{A},\bar{E}$	A,E	0
$A,\bar{B}$	$\bar{A},B$	1
$B,\bar{C}$	$\bar{B},C$	2
$C,\bar{D}$	$\bar{C},D$	3
$D,\bar{E}$	$\bar{D},E$	4
E,A	$\bar{E},\bar{A}$	5
$\bar{A},B$	$A,\bar{B}$	6
$\bar{B},C$	$B,\bar{C}$	7
$\bar{C},D$	$C,\bar{D}$	8
$\bar{D},E$	$D,\bar{E}$	9

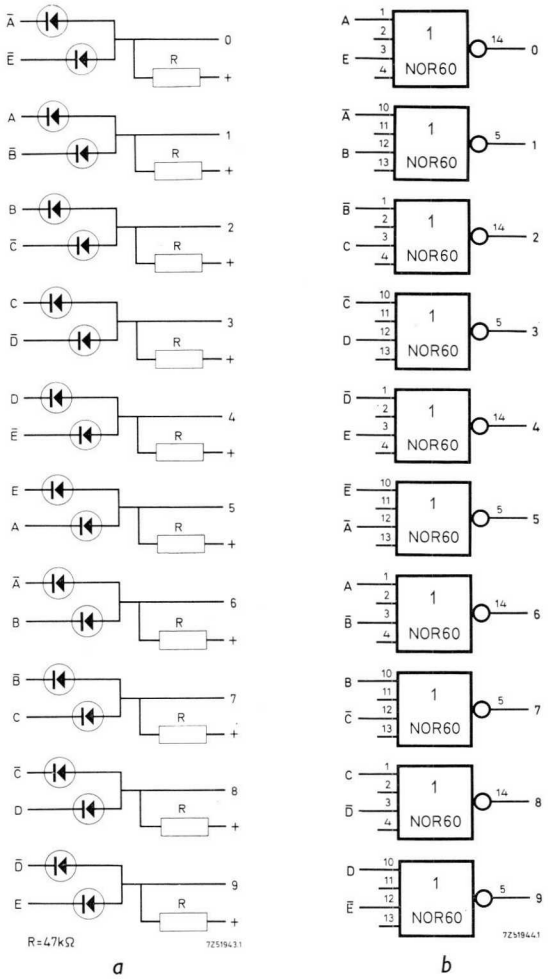


Fig. 8.40. (a) Diode gate output decoder; (b) NOR60 gate output decoder.

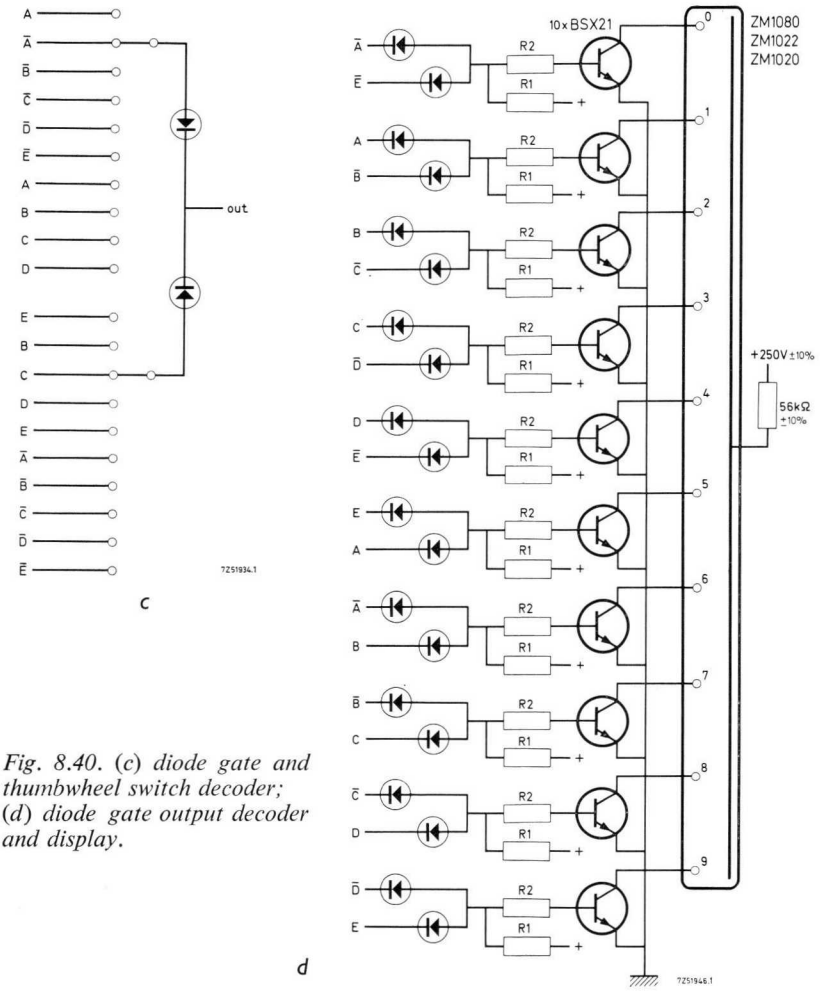


Fig. 8.40. (*c*) *diode gate and thumbwheel switch decoder;* (*d*) *diode gate output decoder and display.*

The counter can be used to provide a programme sequence; Fig. 8.41 shows an interesting programme generator in which NOR gates are used to decode the output of the counter. In the example shown, programme 1 is initiated when memory 1 is set and is switched off when memory 2 is set. Naturally any other sequence can be used.

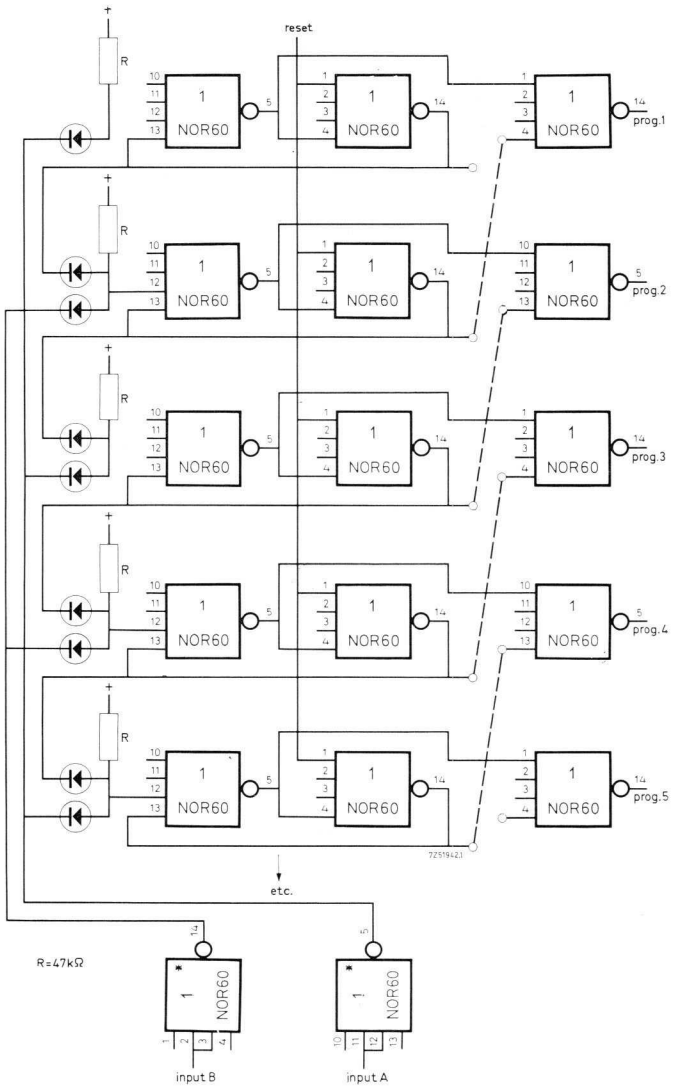


Fig. 8.41. Programme generator using NOR-gates to decode the counter output thus providing a programme sequence.

Another type of direct coupling, using master-slave stages (described in detail for the shift register circuit, Section 8.6) can be employed in counter

circuits. Such a circuit, consisting of five stages, is shown in Fig. 8.42. Input pulses are applied at T, and a reset signal at R. The outputs are exactly in accordance with the outputs of the decoder circuits (Table, p. 118) for any number of input pulses.

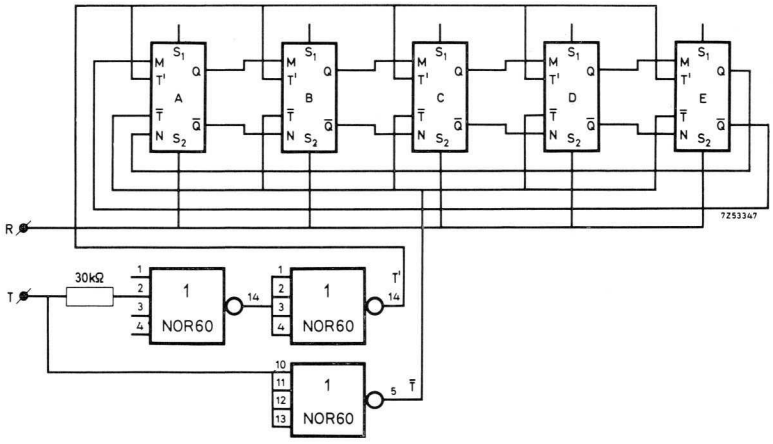


Fig. 8.42. Decade counter.

Experiments have been carried out on the direct-coupled counter to establish its degree of immunity to interference signals at the input. The results are given in Fig. 8.43; the shaded area represents the "safe" interference signals, that is, those whose combined effect of duration and size is not sufficient to cause malfunctioning of the counter. (Fig. 8.36).

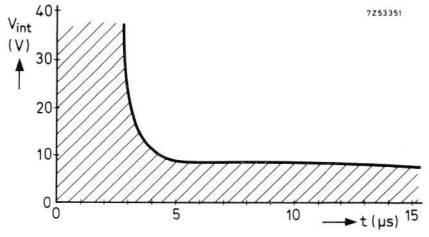


Fig. 8.43.

8.5.6 Decade Counter

Any counter having complementary outputs, for instance the one using the flip-flops mentioned above, can be operated as a decade counter with binary output, with the addition of a logic circuit such as that given in Fig. 8.44.

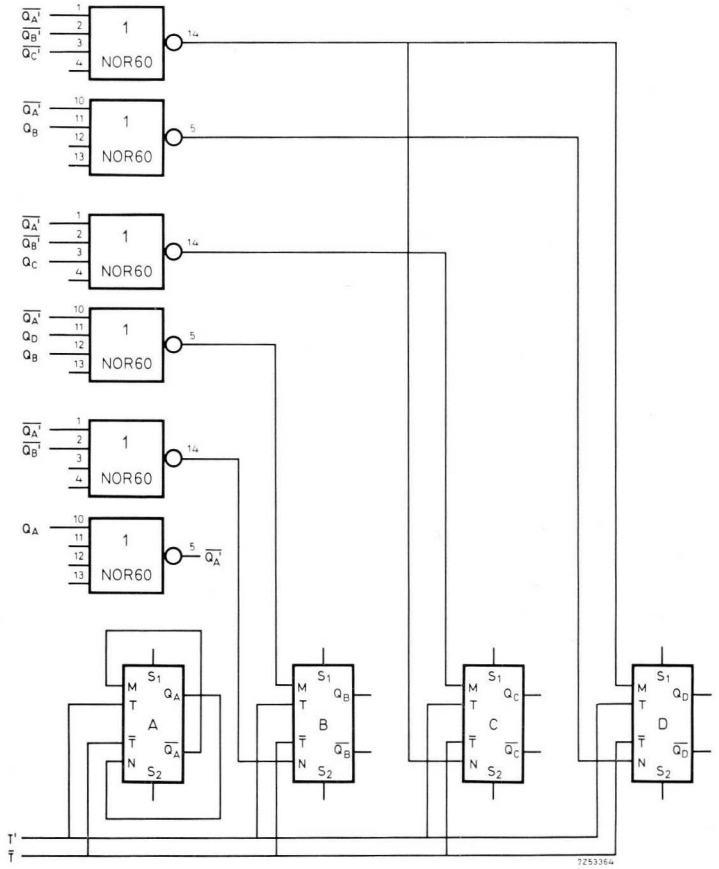


Fig. 8.44. Connections for the decade counter.

The counter requires four stages. The binary code, which is to appear at the counter outputs, is given in the table overleaf for a count up to ten.

number of input pulses	counter outputs			
	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	0	0	0

The characteristics of each flip-flop stage are as follows:

if $M = 1$ and $N = 0$, then after triggering $Q = 1$ and $\bar{Q} = 0$,
if $M = 0$ and $N = 1$, then after triggering $Q = 0$ and $\bar{Q} = 1$,
if $M = 0$ and $N = 0$, then after triggering Q is unchanged.
$M = 1$ and $N = 1$ is not permissible.

With this information, the logic circuit can be designed. From the table, it is apparent that the flip-flop A must change state each time a trigger pulse appears. This can be achieved by connecting $\bar{Q}_A$ to M_A and Q_A to N_A; in this case the flip-flop works to a scale of two. Flip-flop B must change from 0 to 1 after input pulses 1 and 5 (but not 9). Thus, M_B should be 1, and this is obtained from a NOR, the inputs of which are $\bar{Q}_A$, Q_B and Q_D. Flip-flop B must change, 1 to 0 after pulses 3 and 7; thus N_B must be 1, obtained from the output of a NOR whose inputs are $\bar{Q}_A$ and $\bar{Q}_B$. Similarly, NORs are used for the M and N inputs of flip-flops C and D. The condition for M_C is the same as that for N_D, thus one NOR is enough; another NOR is used to invert Q_A, making $\bar{Q}_A'$, which supplies the other NORs.

8.5.7 Display of the Count

The output from a counter is sometimes required to be displayed immediately, instead of (or in addition to) being used to control further operations. Although this can be done with the 60-Series, another series of circuit blocks, the 50-Series, has been developed specifically to meet this

need. Thus it is recommended that the 50-Series blocks be used when direct display is required. The logic levels of the two series are compatible.

8.6 Serial Shift Registers

Process data are generally given in time sequence. In such cases the data, in ones and zeros, may be needed in the same sequence at a later stage of the process. Circuits which will store and move out the data in this way are termed shift registers.

An example of the application of a shift register is in the detection of rejects on a production line (Fig. 8.45).

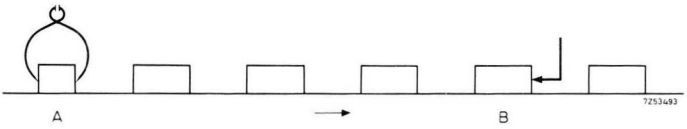


Fig. 8.45. Application of a shift-register.

At *A* a test is performed on an article travelling on the belt, for instance a measurement or weight test. At *B* an operation is to be performed on the article, such as machining; however, this must not be done if the test result was poor. There is a spacing of three articles between positions *A* and *B*, so a 5-stage register is necessary.

If all articles tested are good, each output of the shift register will be at 1 level. Assume now that a faulty article is submitted to the test: the extreme left output will turn to 0. This 0 is made to shift one place to the right every time an article is tested, until finally it arrives at the extreme right position, where it blocks the operation at *B*. In other words, the position of the 0 in the shift register represents the actual position of the faulty article on the belt. The shift register action could be shown as tabulated below.

position →	*A*				*B*
no faults	1	1	1	1	1
faulty article	0	1	1	1	1
no faults	1	0	1	1	1
no faults	1	1	0	1	1
no faults	1	1	1	0	1
no faults	1	1	1	1	0

It will be observed that the shift register requires two inputs: the information input, and an input to shift the information in the register from stage to stage. The following sections give circuits suitable for converting these inputs into signals for driving an *RC*-coupled and a direct-coupled register, together with the register circuits themselves.

8.6.1 RC-Coupled Shift Register

Fig. 8.46 shows the basic circuit of an *RC*-coupled shift register, capable of working at a speed of 500 shifts/s. The inputs *a*, *b* and *c*, obtained from the special "information" and "shift" circuits, are as follows:

a - input information: $a = 0$ at a faulty article; *b* - "transport part" of shift pulse and will write 0 if previous memory contained 0; *c* - "erase part" of shift pulse, which will erase 0.

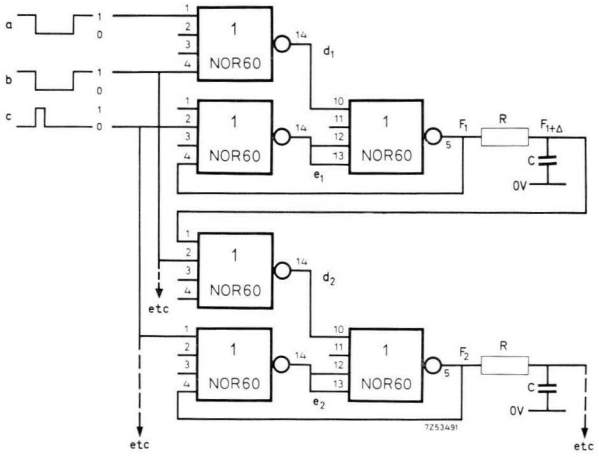


Fig. 8.46. Basic capacitively-coupled shift register.

The requirements for the circuit are:

a - 0 should persist preferably at least as long as $b = 0$; *b* - 0 should be longer than $c = 1$; Δ (delay time) should be longer than $b = 0$. The input signal to next stage $F_1 + \Delta = a$.

Observe that fault information is presented here in 0 level signals. At power supply turn-on all memories should be set to the 1 state by a positive pulse. Section 8.2.3 gives a suitable circuit.

The time diagram (Fig. 8.47) depicts writing-in of a 0 in F_1 with a_1 and writing-in of a 0 in F_1 and F_2 with a_2. Subsequently two shift signals (b_3, c_3) and (b_4, c_4) shift 0 out due to absence of a_3, a_4. Outputs F_1 to F_n can be fed individualy via an inverting NOR (single input) and LPA60 to a display or activating device. By using several outputs, programming or "coded" display is possible. The e signal is fed to two paralleled NOR inputs to provide adequate drive for accommodating the discharge current from C.

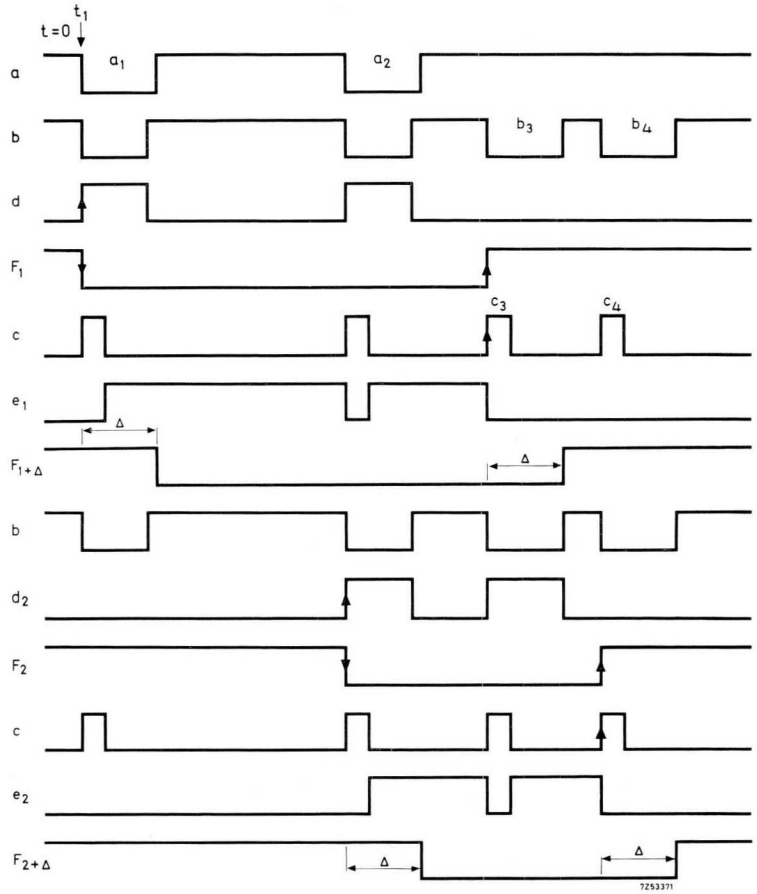


Fig. 8.47. Timing diagram.

The circuits required to produce the "*b*" and "*c*" shift pulses are basically the same (Figs 8.48, 8.49), but the one for *b* has an extra inverter. Looking at the *b* circuit preceding the IA60, it will be noted that it consists of a memory circuit which is turned off after an interval determined by the discharge of C_2. This type of shift pulse generation produces an output which is largely independent of the way in which the input is changed.

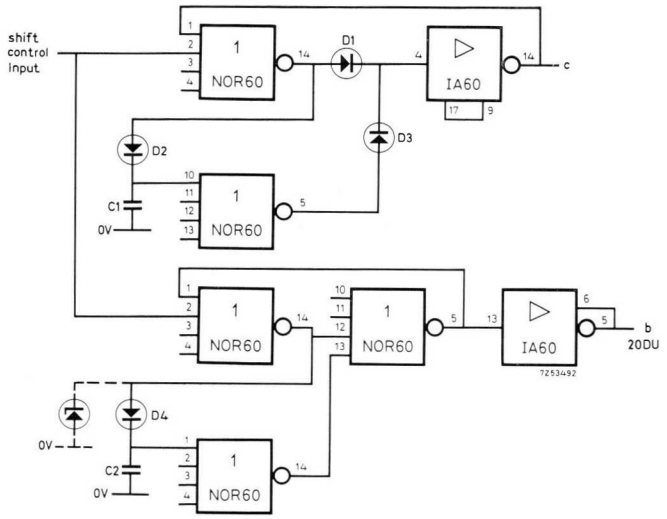


Fig. 8.48. Generation of the b and c signals.

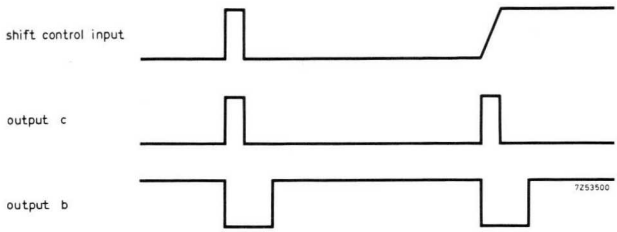


Fig. 8.49. Timing diagram.

As there is a requirement for the *a* information pulse as regards the duration of the zero time of *b* as well as the delay Δ, it is sometimes useful to standardize arbitrary *a* signals with a circuit similar to that for *b*, as in Figs 8.50, 8.51. A NOR can be used instead of an IA output stage, as there is no particular drive requirement.

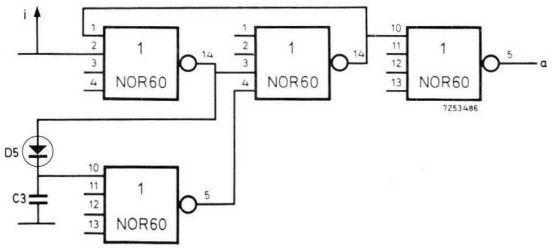


Fig. 8.50. Generation of the a signal.

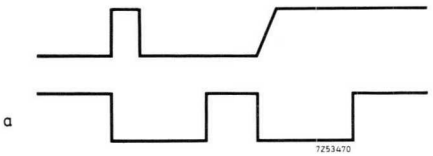


Fig. 8.51. Timing diagram.

It is further of importance to consider the quoted time requirements for a, b and c as the delay Δ must be longer than a. The actual value of Δ will vary with the spread in values of individual capacitors and in NOR characteristics, as well as on the loading at outputs F. The shortest duration in this system is the time for c. The time required is that needed to set a memory in the 1-state, which is about 10 μs, and the table below gives values of R and C for various output capabilities to accommodate this minimum time. (The values given will make Δ a minimum of 100 μs).

output capability	R	C
0 DU	24 kΩ ± 2%	22 nF ± 10%
1 DU	13 kΩ ± 2%	33 nF ± 10%
2 DU	7.5 kΩ ± 2%	47 nF ± 10%

Fig. 8.52 is a block diagram of the complete shift register with auxiliary circuits. The i and s signals may be obtained from EPDs or VSOs. The maximum number of stages is 19. The output capability can be increased by adding NOR and IA60 units.

Parallel insertion of information can be effected by applying a 1 to the p inputs (terminals 11 in Fig. 8.46).

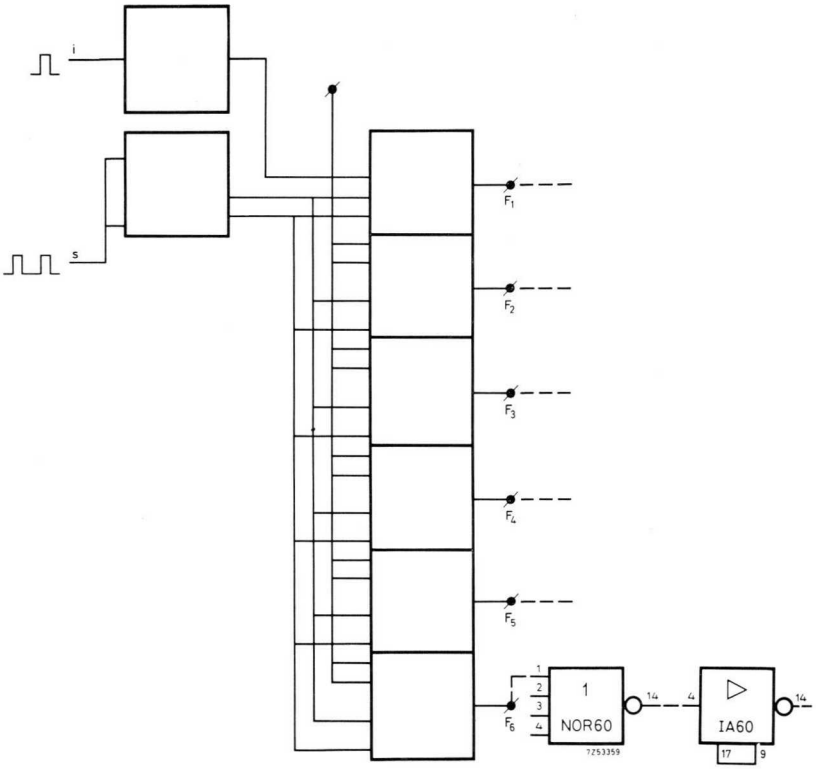


Fig. 8.52. Complete shift register.

8.6.2 Direct-coupled Shift Register

The shift register described below operates on a principle different to the one just given. Since no capacitive coupling is used, maximum operating speed is greatly increased; speeds of 25 kHz are entirely practical.

Fig. 8.53 shows one stage of the register. In the preceding example, decoupling between stages was achieved by using a level signal derived from a capacitor; here, decoupling is obtained by the diode gates D. If signals T' and $\bar{T}$ are 0, the inputs to "master" and "slave" are clamped at 0, and the output from the preceding stage (terminals M,N) has no effect. In this type of flip-flop, terminals M and N are complementary outputs.

Shifting of information from M,N to Q, $\bar{Q}$ is achieved by applying

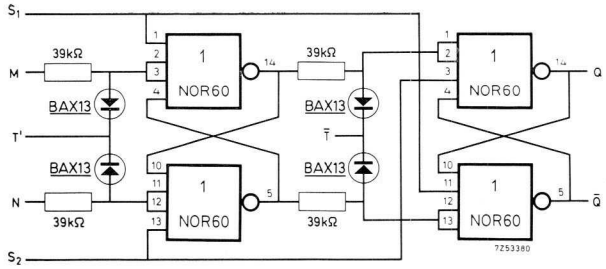


Fig. 8.53. One stage of the d.c. shift register.

signal T to the circuit of Fig. 8.54. NORs B, C and D have all four inputs paralleled; this results in short rise and fall times of their outputs. As T rises from 0 to 1 , $\bar{T}$ falls from 1 at 2 V to 0 at 3 V. NOR A has a higher threshold voltage, due to the 30 kΩ resistor; T' rises from 0 at 6 V to a at 8 V. The fraction t/t_1 (Fig. 8.55) remains almost constant, independent of the rise and fall time of T. In this way, the circuit operates on level logic rather than on trigger logic, both as regards the input and the T signals.

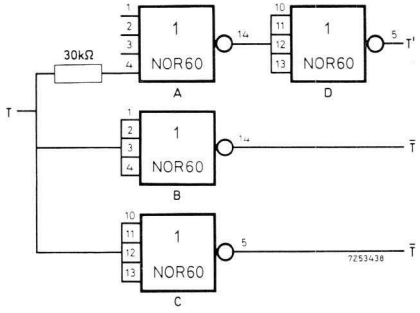


Fig. 8.54. Generation of $\bar{T}$ and T' pulses.

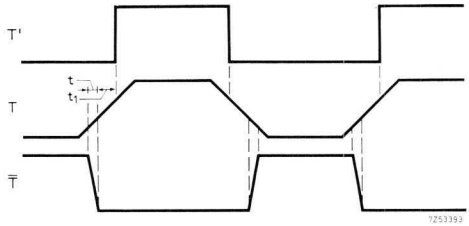


Fig. 8.55. Timing diagram.

The following sequence will thus occur (Fig. 8.55):

(1) slave inputs clamped;
(2) master inputs unclamped and outputs UV assume the inverse levels of the M-N signals;
(3) master inputs clamped;
(4) slave inputs unclamped and outputs Q, $\bar{Q}$ assume the inverse levels of the master outputs, i.e., the same levels the *M-N signals* had.

Input signals to the stage from the preceding Q-$\bar{Q}$ outputs must be present before the T pulse is applied. The outputs Q and $\bar{Q}$ can be set at either level by appropriate signals applied to S_1 and S_2. Parallel insertion of information is thus also possible.

The T pulse may be obtained from a circuit as shown in Fig. 8.17. Fig. 8.56 shows the set-up of a 4-stage shift register. Parallel extraction of information is possible from any Q and $\bar{Q}$ output, provided the loading on the Q terminal does not exceed 3 DU for intermediate stages or 5 DU for the final stage outputs. If the register is to consist of more than 24 stages (but not more than 36), the circuit of Fig. 8.57 should be used to generate the $\bar{T}$ and T' pulses.

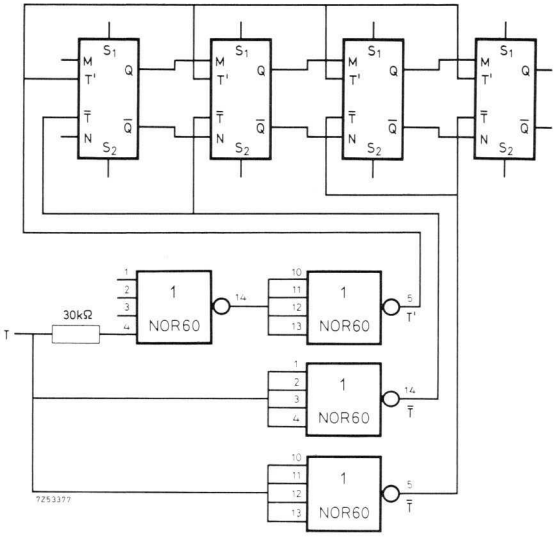


Fig. 8.56. Four-stage shift register.

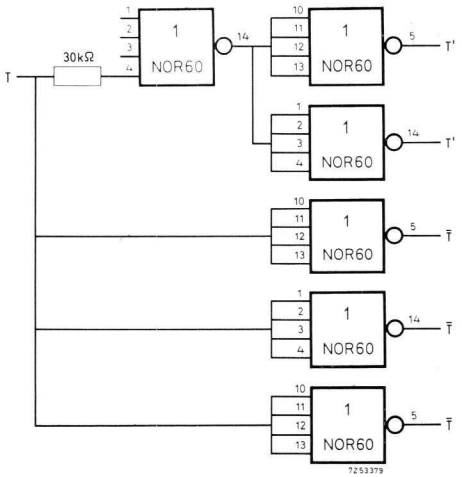


Fig. 8.57.

8.7 Generation of Repetitive Square-Wave Signals

Formation of square-wave signals with NORbits is a simple matter, as the output of the unit can be made to have only one of two values (high or low). Square-wave signals find application, for example

— as a clock pulse source for synchronizing switching operations,
— as a time reference for counting operations,
— as a gate signal for controlling thyristors, and
— for operating buzzers in alarm systems.

8.7.1 50 Hz Pulse Source

Each time the voltage at one end of the transformer secondary exceeds the 1-level ($V_{F(D1)} + V_{Z(D2)}$), the respective NOR output will go to zero. Alternating zero pulses will be generated at the outputs A and B; either output can drive 6 DU.

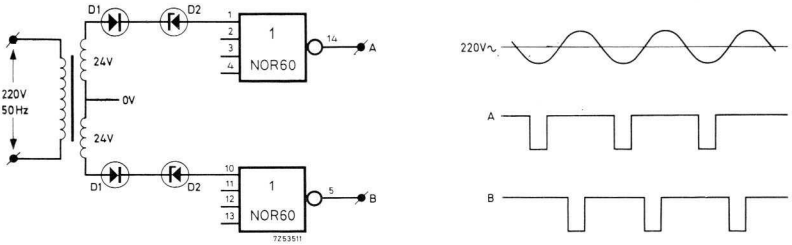


Fig. 8.58. Circuit giving 50 Hz square-wave pulses.

Synchronizing circuits using the mains supply as a reference automatically acquire the highly accurate time-keeping of the mains, and the circuit described is an ideal one where long term synchronism is required.

8.7.2 Square-Wave Generator

The circuit of Fig. 8.59 is termed a free-running multivibrator, that is, an oscillator whose frequency is controlled by an internal source. The frequency range is approximately 2 Hz to 10 kHz, depending on the value of capacitors C (see Fig. 8.60). The circuit may be used as a general-purpose square-wave source.

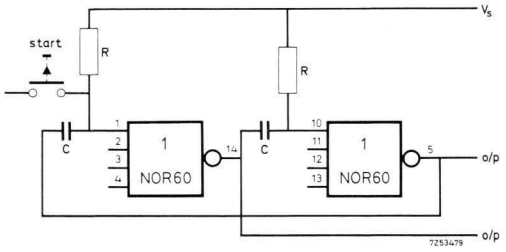


Fig. 8.59. Square-wave generator with NOR60.

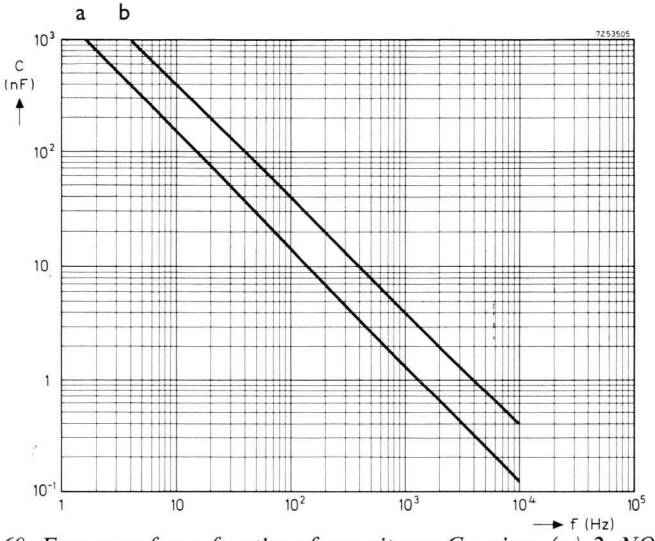


Fig. 8.60. Frequency f as a function of capacitance C, using: (a) 2. NOR60, (b) 2.IA60.

For optimum results, R should be 820 kΩ. Either output can drive 5 DU. If a higher output capability is required, the 2.IA60 may be used instead of the 2.NOR60, as shown in Fig. 8.61; the output capability is then 19 DU for each output. For optimum results, R should be 300 kΩ. See Fig. 8.60 for the frequency dependence on C.

In these circuits the supply voltage should rise quickly to full value at switch-on, otherwise starting difficulties may occur (both outputs may remain at 0). Starting may be ensured by using a push-button as shown or by applying a positive-going (1 level) step from other logic.

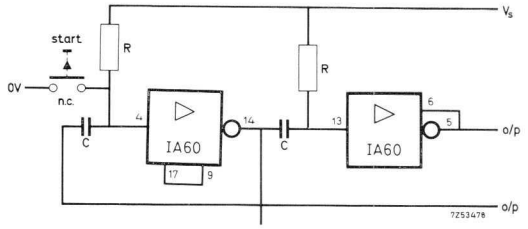


Fig. 8.61. Square-wave generator with IA60.

8.7.3 Self-starting Square-Wave Generator

In this circuit two NOR units are cross-connected to form a free-running oscillator; their outputs are taken to the AND gate formed by the two lower NORs (Fig. 8.62).

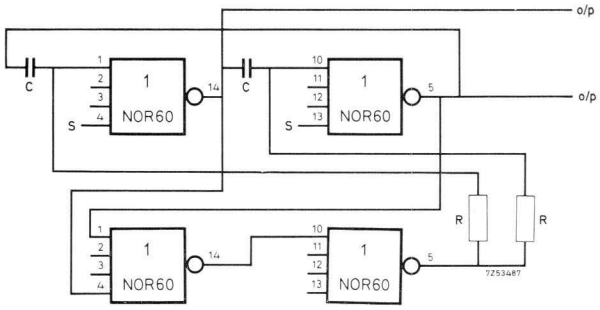


Fig. 8.62. Self-starting generator.

Should both oscillator outputs lock at 0 level at switch-on, a 0 signal from the OR gate will cause one output to become 1 and oscillation starts.

Oscillation can be stopped by applying a 1 level at either input *S*. Fig. 8.63 shows the dependence of the oscillation frequency on the value of *C*.

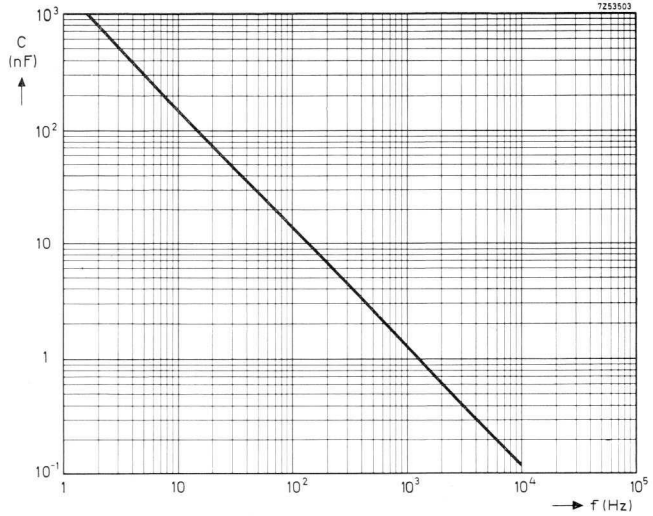


Fig. 8.63. Frequency f as a function of capacitance C.

The circuit finds use where it is essential that oscillation starts immediately upon switch-on. For optimum results, *R* should be 510 kΩ. The output capability is 4 DU per output.

8.7.4 Relaxation Oscillator

In Fig. 8.64, the two NORs form a pulse shaper. The voltage regulator diode BZY60 causes the IA60 to have a high tripping level. *C* is charged

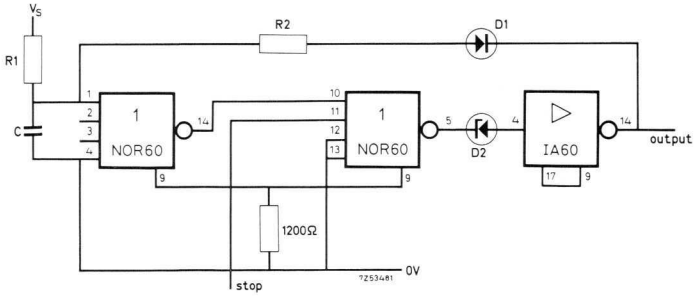


Fig. 8.64. Relaxation oscillator.

via R_1 until this level is reached; the output of the IA60 then becomes zero, and the capacitor is discharged via R_2. When C is almost discharged, the output of the IA becomes high, and the capacitor will be charged again via R_1. The frequency f depends on the value of C and on the combination of R_1 and R_2 (see Fig. 8.65). The output can drive 20 DU.

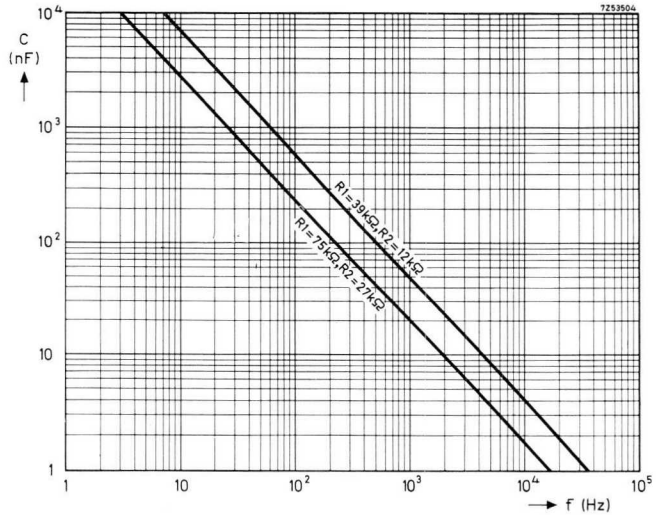


Fig. 8.65. Frequency f as a function of capacitance C.

8.7.5 Low-Frequency Pulse Generator

The circuit of Fig. 8.66 generates square-wave pulses. The timer unit TU60 controls the repetition time t_r of the pulses, and C_2 and R_2 the pulse duration t_p. Fig. 8.67 shows the dependence of t_r on R_1 and C_1. The pulse duration t_p varies in the following way:

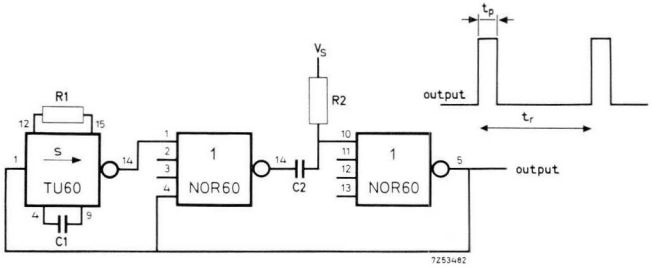


Fig. 8.66. L.F. pulse generator.

for $C_1 = 0.1\ \mu F$, $t_p \geqslant 7.2$ ms ($t_p \cong 10$ ms if $R_2 = 30\ k\Omega$, $C_2 = 1.0\ \mu F$); for $C_1 = 10\ \mu F$, $t_p \geqslant 72$ ms ($t_p \cong 200$ ms if $R_2 = 47\ k\Omega$, $C_2 = 10\ \mu F$). The output capability is 4 DU. The output of the TU60 can drive up to 3 DU with pulses of a few microseconds duration.

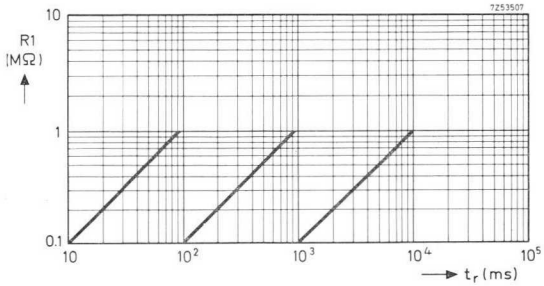


Fig. 8.67. Pulse repetition time t_r as a function of resistance R1. C = 0.1μF, 1μF and 10μF (left to right)

8.7.6 Low-Frequency Square-Wave Generator

The circuit shown in Fig. 8.68 is formed by cross-coupling two pulse generator circuits similar to the one in Fig. 8.66. The *X*, *Y* outputs produce square waves as shown in Fig. 8.69, with a t_1/t_1' ratio of 1 if the

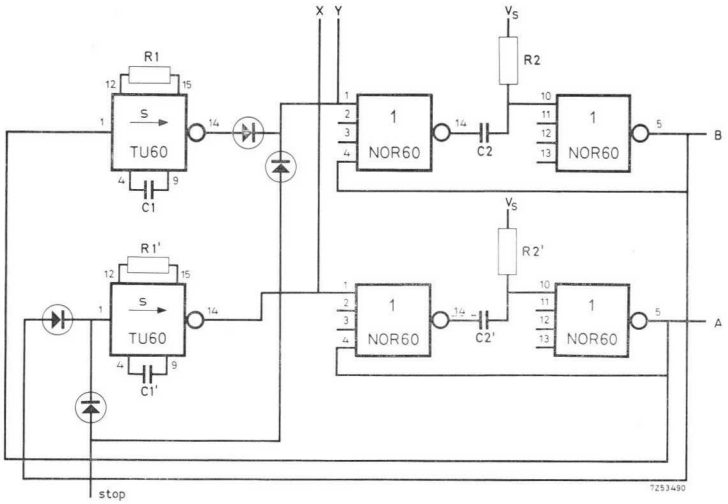


Fig. 8.68. L.F. square-wave oscillator.

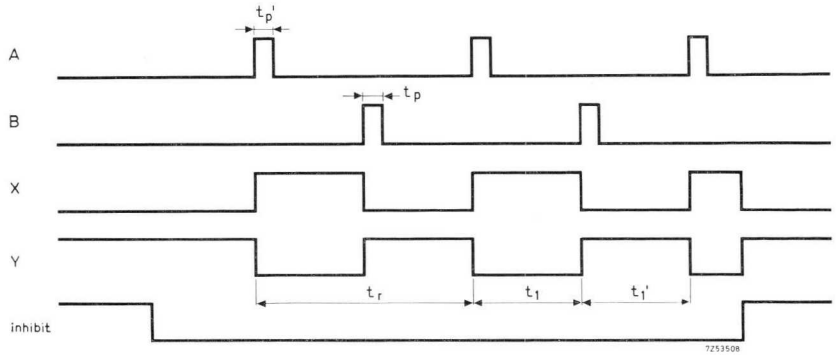


Fig. 8.69. Wave shapes at different points.

component values in the top circuit are the same as the corresponding values in the lower circuit. The output capability is 3 DU at each output. Fig. 8.70 gives the dependence of t_1 on the value of R_1 for three combinations of $C_1 = C_1'$, $R_2 = R_2'$ and $C_2 = C_2'$, namely:

combination	C_1	R_2	C_2
A	0.1 μF	47 kΩ	3.2 μF
B	1 μF	30 kΩ	1 μF
C	10 μF	47 kΩ	10 μF

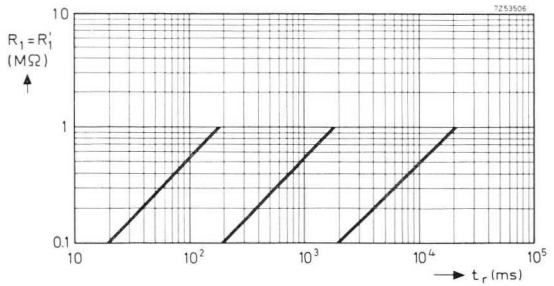
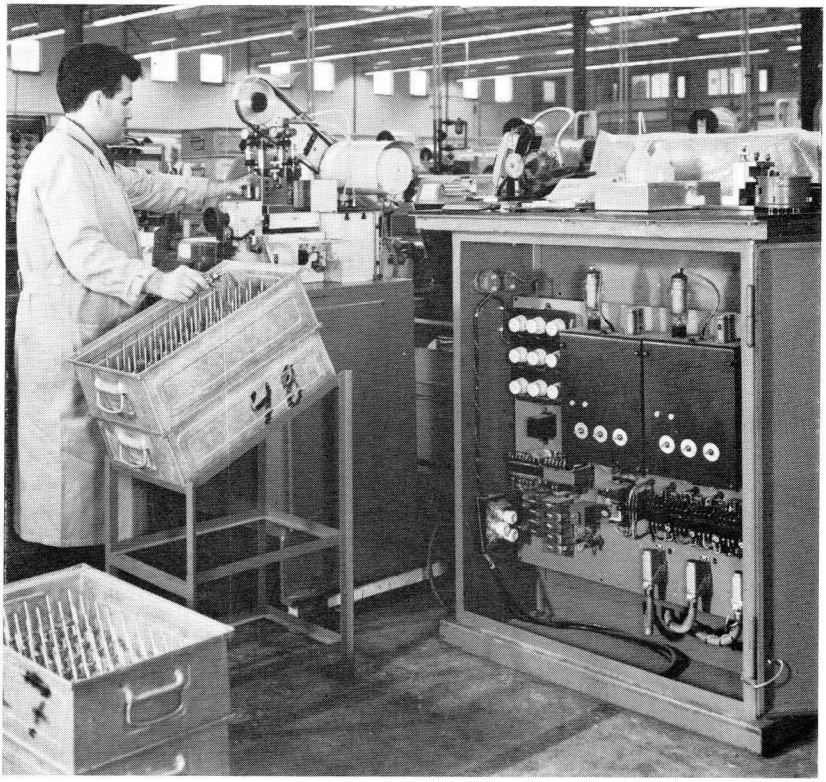
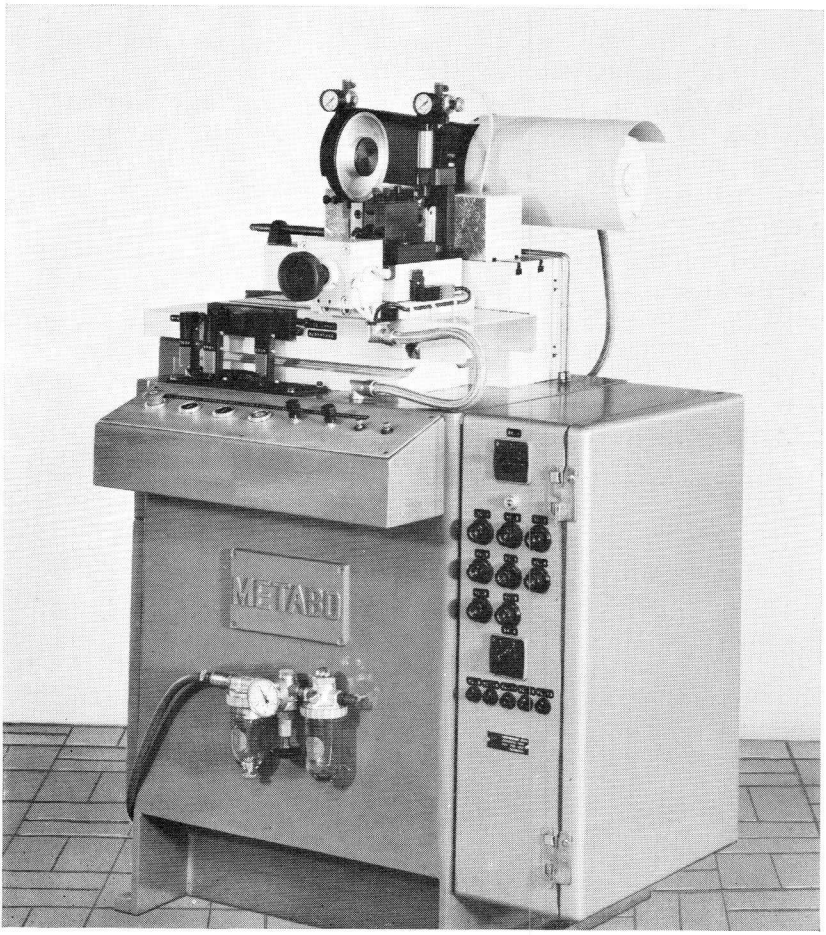


Fig. 8.70. Pulse repetition time t_r as a function of $CR_1 = R_1'$. Combinations A, B and C (left to right)



Above: An automatic machine used for finishing the commutators of small motors. Here, the control functions are performed by relais contained in the large cabinet at the right of the photo.

Opposite: The same machine, but with the control relays replaced by NORbit modules. The entire control system is now contained in the box at the right-hand side of the machine.


METABO

9 Static Switching of High Power

9.1 Introduction

Static switching — switching of current without the use of moving (mechanical) contacts — can most conveniently be achieved with the thyristor, a solid-state semiconductor device. This chapter gives some general information on its application in the output, or high-power stages of control systems. This part of the system is often not as simple to design as the logic sections because of the widely differing requirements of current and voltage which occur in every new situation, and the care which must be taken to avoid undesirable effects such as interference.

The thyristor — in contrast to the diode — has a control electrode, the "gate". Normally, the thyristor blocks current in both directions. If a small positive trigger signal is applied to the gate, however, it goes into conduction, provided the anode is more positive than the cathode. It remains in conduction even if the trigger signal is removed, until the thyristor current is reduced below a minimum "holding current" value. The thyristor then blocks all current until another trigger signal is applied.

The trigger signals should conform to voltage and duration requirements stated in the data sheets of the thyristor. The following paragraphs discuss this and other requirements, and how these may be satisfied.

9.1.1 Triggering

A special unit is available for supplying a trigger signal to a pair of thyristors from the logic; this is the Thyristor Trigger Module, TTM (Cat.no. 2722 032 00001). The TTM consists of a blocking oscillator providing trigger signals via a transformer capable of triggering a pair of thyristors.

The output pulses of the TTM have a duration of over 20 μs — long enough to trigger thyristors with resistive or slightly inductive load. An inductive load will limit the rate at which the current through the thyristor rises. If the current at the end of the trigger pulse has not attained the latching current value the thyristor will not stay in conduction.

A method of overcoming this consists of shunting an RC network across the load (Fig. 9.1). The effect of this network is depicted in Fig. 9.2; the thyristor current rises sharply before falling to normal. Taking $R = 100\ \Omega$, C values between 0.33 and 2.2 μF will be found to accommodate most loads.

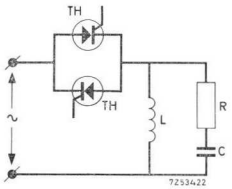


Fig. 9.1. Resistor R and capacitor C shunted across the inductive load L to attain holding current of thyristors TH.

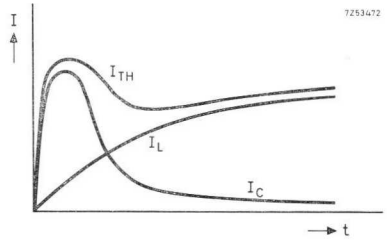


Fig. 9.2. Effect of the configuration of Fig. 9.1. Thyristor current I_{TH} is the sum of load and capacitor currents (I_L and I_C respectively).

An alternative triggering circuit is the one given in Fig. 9.3, which uses auxiliary thyristors TH_3 and TH_4 to give a continuous trigger signal. They can be low-current types, but should have the same voltage rating as TH_1 and TH_2. Resistors R should have a value that prevents the gate dissipation of TH_1 and TH_2 from exceeding the limits specified for these thyristors. This indicates a value of R of 2.2 kΩ for 220 V operation and 3.9 kΩ for 380 V (a.c.) operation, assuming the average permissible gate dissipation to be 500 mW at a gate current of 100 mA. The disadvantage of the dissipation associated with this circuit can partly be overcome by applying to the auxiliary thyristors a lower voltage in phase with the anode voltage of the thyristor to be triggered.

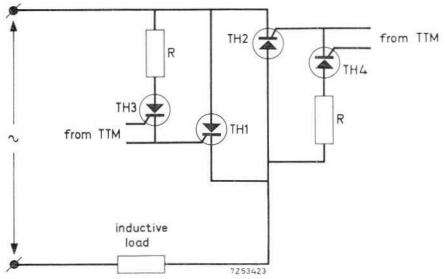


Fig. 9.3. Triggering circuit using auxiliary thyristors TH_3 and TH_4.

9.1.2 Isolation from the Logic

If the loads are operated from the a.c. mains the logic circuit must be isolated from the mains. The conventional method of obtaining this isolation is to use a transformer between the logic and the gate-cathode

circuit of the thyristors; this technique is employed in the TTM (Thyristor Trigger Module).

Another circuit that could be used to obtain isolation makes use of an incandescent lamp and two photo-sensitive cells (Fig. 9.4). This circuit is suitable for operation on normal mains voltages of 220 V a.c. The requirement is of course that the lamp and cells are housed in such a way that the dark resistance of the cell is high enough to prevent a triggering current from being produced inadvertently. This requirement, together with cell dissipation, will limit the operation of this circuit to an ambient temperature of 40 °C.

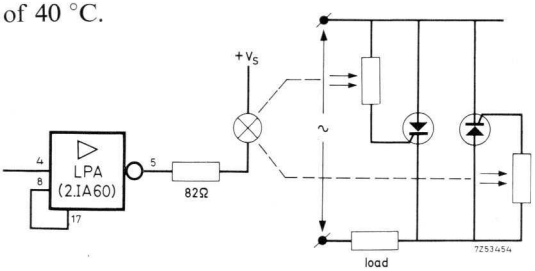


Fig. 9.4. One method of obtaining isolation of the logic from the a.c. load supply.

9.1.3 Transients and Commutation

Reliable operation with thyristors must take account of voltage transients which may be superimposed on the mains. The magnitude of the permissible peaks partly depends upon the voltage ratings of the thyristors to be used and will, in general, require the addition of *RC* damping circuits across the thyristor mains connections. The thyristor data sheets should be consulted to obtain the recommended values of *R* and *C*.

RC networks are also necessary between the cathode and anode to limit the rate of rise of voltage applied to the thyristor. Here again the details depend upon the thyristor characteristics as well as on the load. Furthermore, the *RC* combination should be such, that at turn-on of the thyristor the current from the capacitor is limited, so that the maximum permissible peak current and rate of change of the current are not exceeded. The list below gives some typical *RC* values.

$$I_{TAV} \leqslant 16A: R_1 = 33\,\Omega\ (2W),\ C_1 = 0{,}33\ \mu F.$$
$$I_{TAV} \leqslant 70A: R_1 = 22\,\Omega\ (4W),\ C_1 = 0{,}75\ \mu F.$$

It will be clear that the determination of the *RC* element is related strongly to the thyristor used, and the manufacturer's data for the actual

application should be obtained. It should therefore be kept in mind that the examples given in this chapter can merely be of a typical nature.

9.2 Switching A.C. Loads

9.2.1 Switching with an Inverse-Connected Thyristor Pair

In the circuit under discussion (Fig. 9.5) the 2.IA60 is connected as an LPA, switching the power supply voltage (12 V) to the TTM. The 12 V

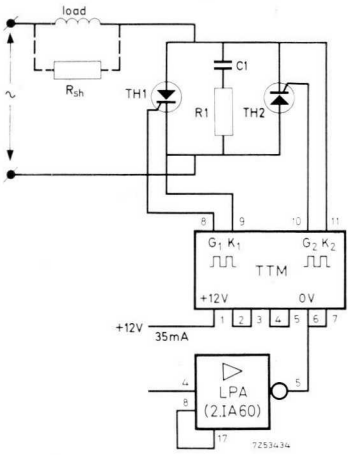


Fig. 9.5. The inverse-connected thyristor pair configuration. Current will flow in the load (shown here as being inductive) on application of a 1 level signal to the LPA input.

supply may be obtained as shown in Chapter 3. A series *RC* network should be shunted across each thyristor. For values of R_1 and C_1 see the list on p. 144.

The circuit could give difficulties with highly inductive loads having a low operating current, as this may lead to uncertain triggering of the thyristors, the holding current possibly being of the same order as the load current. Certain low-power 220 V a.c. coils will have this characteristic. In this case thyristors with low holding current could be used. However, by shunting the load with a resistor (R_{sh}) or series resistor-capacitor combination capable of handling the holding current of the thyristor, the circuit can usually be operated satisfactorily.

Resistive loads exhibiting a very low "OFF" resistance value should preferably be switched on at approximately zero mains supply voltage. This can be done by making the low voltage a logic condition for the switch-on moment.

9.2.2 Switching an A.C. Circuit with a single Thyristor

The switching of single-phase a.c. loads can also be obtained with a single thyristor by the circuit depicted in Fig. 9.6. The connection of the thyristor across the bridge is such that, although the load carries a.c. current, the current through the thyristor is uni-directional.

The load may be resistive or inductive. In case of inductive load, the holding current and trigger pulse requirements apply as indicated above. Attention must also be paid to the requirement of allowing time for thyristor turn-off, compensating for the phase shift due to inductance by shunting the load with a suitable *RC* combination.

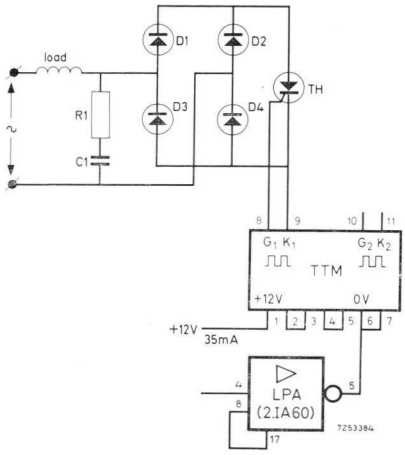


Fig. 9.6. Switching of alternating currents with a single thyristor.

9.2.3 Switching a 3-Phase Motor

The circuit of Fig. 9.7 below will switch on the motor *M* if a 1 level pulse is applied at *A*, and off if a 1 is applied at *B*. Overload protection is provided by the temperature-sensitive PTC resistor. The two thyristor bridges are similar.

It is advisable to make the gate and cathode connections to each thyristor as a separate twisted pair, and provide that the TTM units are adequately ventilated, to ensure reliable operation. The R_1C_1 networks should be placed directly across the thyristors concerned.

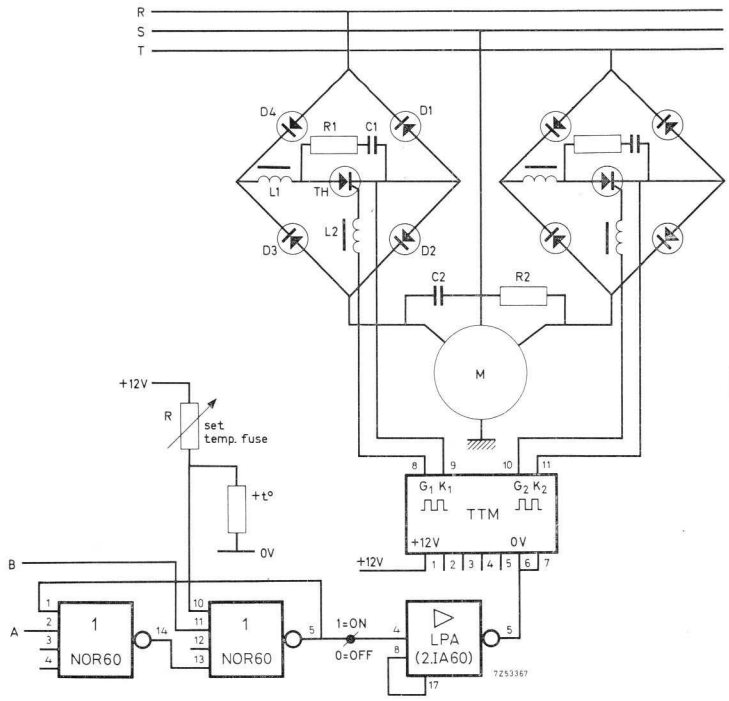


Fig. 9.7. Switching of a 3-phase motor. A typical 3 h.p. motor would require the following component values: $R_1 = 22\ \Omega$, $R_2 = 10\ \Omega$, $C_1 = C_2 = 1\ \mu F$ *(1000 V),* $L_1 = 9$ *turns and* $L_2 = 15$ *turns (both wound on core cat.no. 4322 020 36620),* D_1 *to* D_4 = *BYX25/800 R, TH = BTX12/600 R.*

9.2.4 Reversal of a 3-Phase Motor

Fig. 9.8 shows the circuit for reversal of a 3-phase motor. Two control networks, each consisting of a logic circuit, TTM and two bridges with thyristors, are necessary: one for forward and one for reverse. A 1 level at *F* makes the two outside bridges operable for forward motion, and a 1 level at *R* gives reverse motion via the two inner bridges. To avoid short-circuiting the 3-phase lines a delay is introduced of a minimum of 20 ms between each input (e.g. from a memory) and the logic. Temperature protection can be incorporated as described in Section 9.2.3. The general recommendations given in that section should also be followed here.

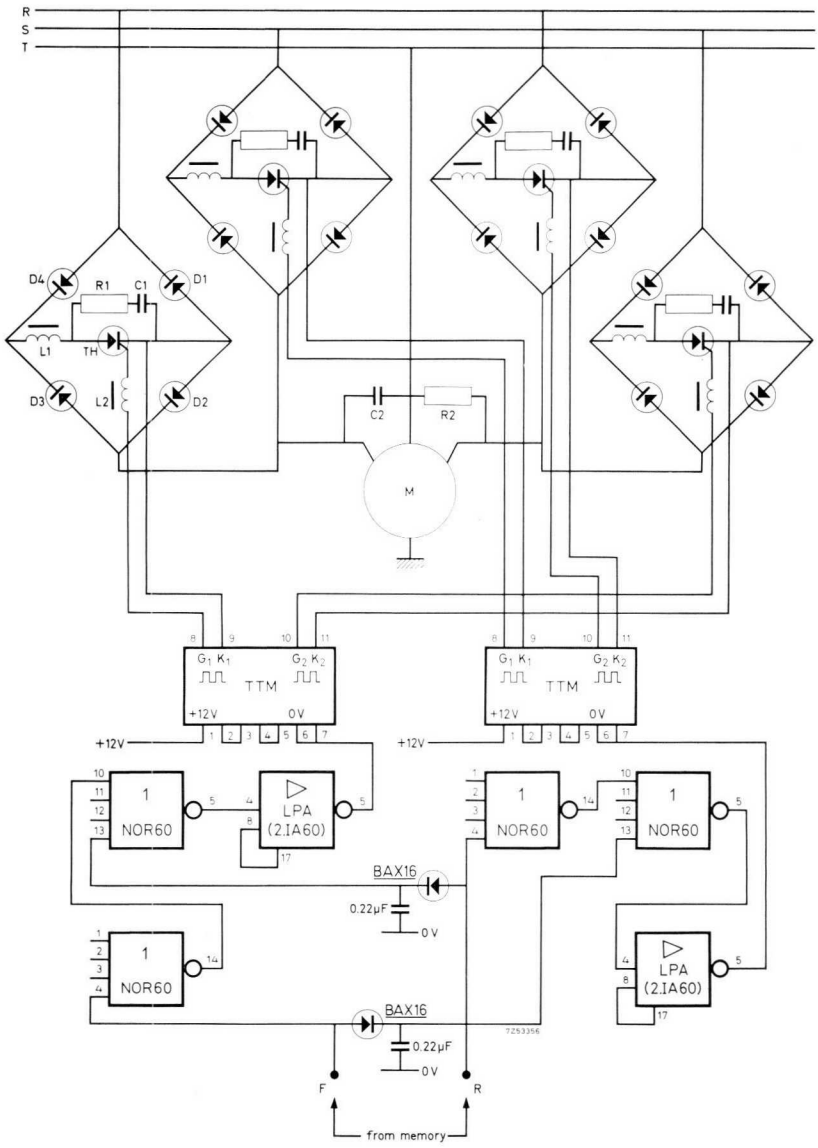


Fig. 9.8. Reversal of a 3-phase motor. For typical component values, see Fig. 9.7.

9.3 Switching D.C. Loads

The following diagrams illustrate methods of switching d.c. loads operated from various types of ac. and d.c. supply. The general notes regarding triggering and protection of the thyristors if the load is inductive apply here also (Fig. 9.9 to 9.14).

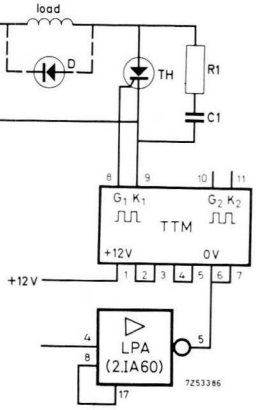


Fig. 9.9. Switching half-wave unidirectional current with a single thyristor. Flywheel diode D dissipates the inductive load energy at switch-off and helps protect the thyristor against over voltage. A second circuit can also be switched simultaneously by the TTM.

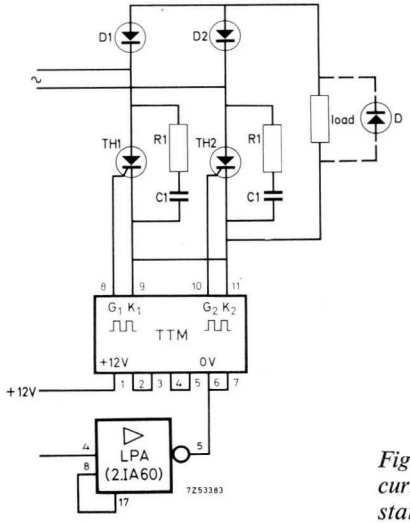


Fig. 9.10. Switching full-wave unidirectional current with two thyristors. The precautions stated in Fig. 9.9 should be followed here also.

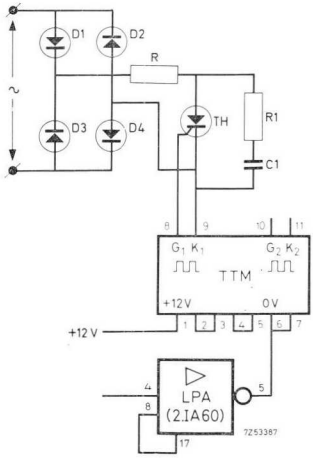


Fig. 9.11. Switching full-wave unidirectional current with a single thyristor for resistive loads. The TTM could switch another such circuit simultaneously.

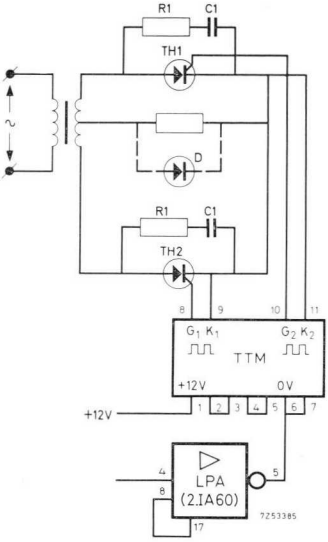


Fig. 9.12. Switching full-wave unidirectional current from centre-tapped transformer secondary; resistive or inductive load.

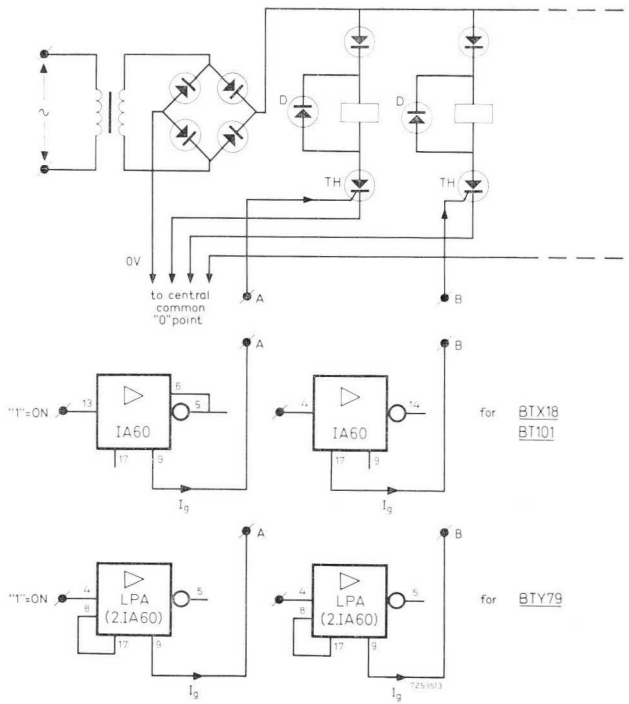


Fig. 9.13. Switching of small loads with a common zero connection. The thyristor for each load could be triggered directly by an IA60 giving a triggering current I_g of 10 mA (e.g. thyristor types BTX18 and BT101), or by an LPA giving I_g = 100 mA (e.g. thyristor type BTY79). Relay coils often form a load of the type described. Shunting the inductive loads with flywheeling diodes D is advisable.

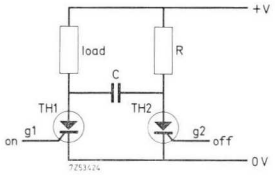


Fig. 9.14. Method of obtaining both switch-on and switch-off control over a steady unidirectional current. In the diagram, the current through the load is switched on with TH_1 by means of a pulse at g_1. To switch off, a pulse is applied to g_2 causing TH_2 to conduct and momentarily short-circuit C. The current through TH_1 will thus drop below its holding current value and TH_1 will cease to conduct further, as does TH_2 after C has recharged. C and R should be chosen according to the thyristor ratings.

In those circuits where a TTM unit is employed to trigger the thyristors, it should be remembered that a 1 level at the associated LPA input will cause current to flow in the load.

9.4 Full Control of D.C. Motors

Use of a thyristor bridge is one of the most satisfactory ways of achieving full control over a d.c. motor supplied from the 3-phase mains. A scheme for the control of speed, torque, and direction of a d.c. motor using circuit blocks from the 60-Series and 40-Series is described briefly below. Further information is available in a separate publication.*

The circuitry necessary to supply the thyristor gates with the correct signals can be divided into the following five basic functions:

(1) Central Control Unit (CCU)
(2) Logic Control Unit (LCU)
(3) Phase Limit Unit (PLU)
(4) Phase Shift Trigger Unit (PTU)
(5) Twin Trigger Unit (TTU).

These five functions may be used in various combinations to give virtually any type of control. They have been built experimentally on printed-wiring boards with very satisfactory results. The following types of circuit blocks are used: 2.NOR60, 2.IA60, PA60, DOA40 and PSM40 (circuit blocks from the 40-Series).

The block diagram of Fig. 9.15 shows by way of illustration the layout of such a system. The motor is fitted with a tachometer whose output V_{tacho} is proportional to the motor speed. This is fed back to the CCU, together with a current I proportional to the motor armature current, and a reference voltage V_{ref} whose polarity is used to control motor direction.

Signals from the CCU go to the LCU, which controls reversal of direction, and to the PTUs, which control the phase angle at which triggering of the thyristors takes place. Two thyristor bridges are used, one for the forward and one for the reverse motor currents. The trigger phase angle for bridge 2 is controlled by the TTUs. The way in which the thyristor bridges are connected to the motor is shown in Fig. 9.16. The trigger pulse timing is given in Fig. 9.17.

The functions mentioned above require supply voltages of $+12$ V and -12 V, $\pm 5\%$; in addition the PTU and TTU require $+24$ V $\pm 25\%$. The permissible temperature range for the units is -10 to $+70$ °C.

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* D.C. Motor Control with 60-Series and 40-Series Circuit Blocks.

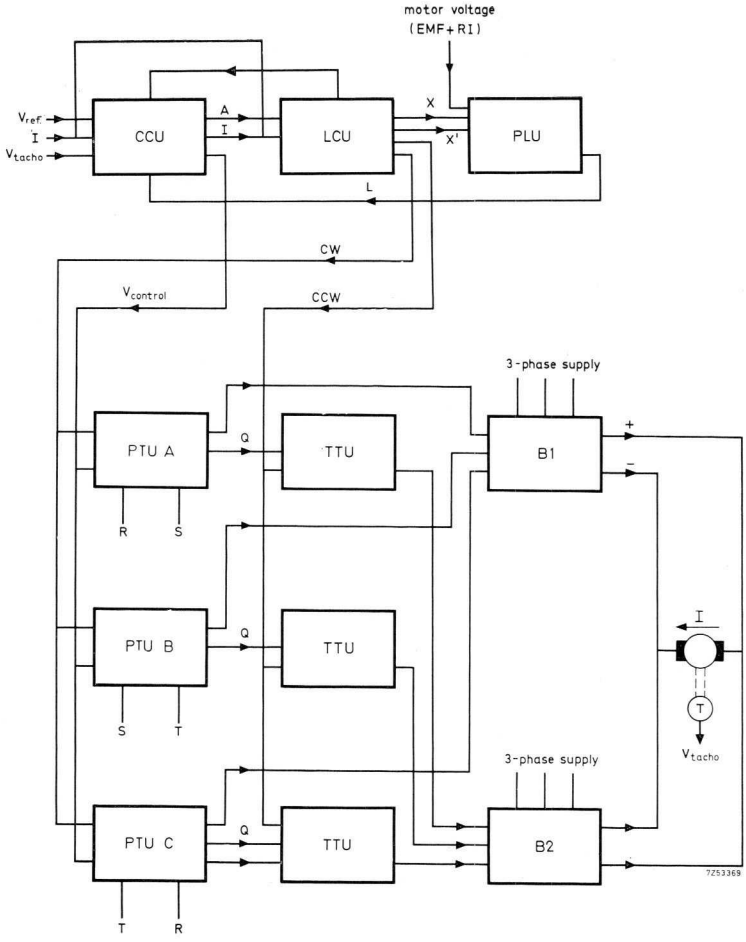


Fig. 9.15. Block diagram of the typical motor control system described in the text.

Various other motor control systems can be easily realized. To facilitate the design of a particular system, the functions the various units can perform and their input requirements and output signals are summarized in the following sections.

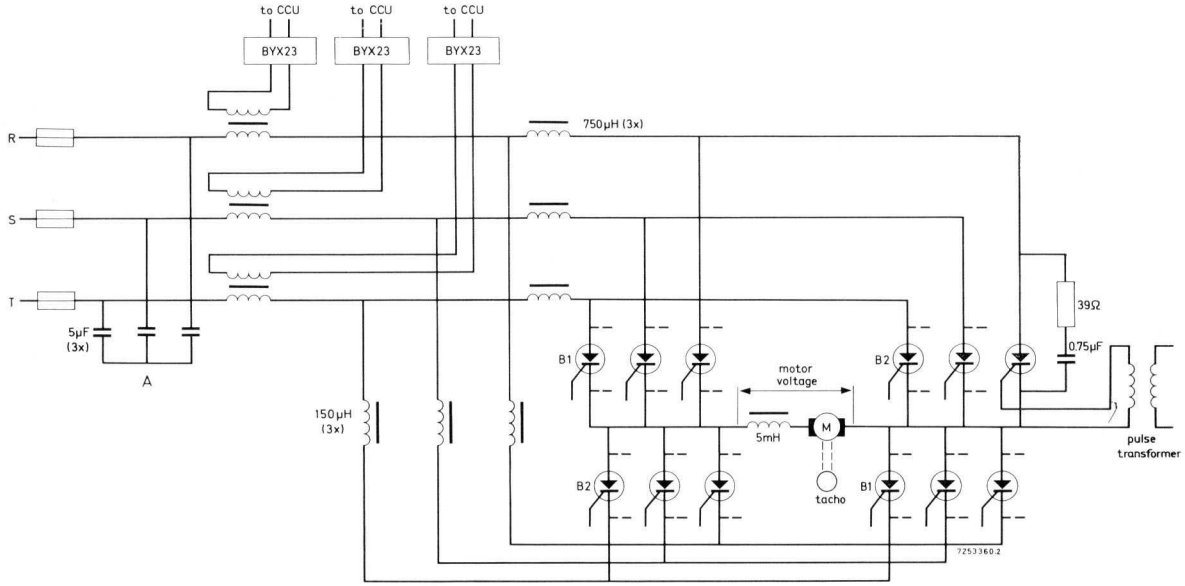


Fig. 9.16. Connection of the thyristor bridges B_1 and B_2 to the 3-phase supply and motor. For additional filtering, the motor terminals could be connected to point A via 10 µF capacitors.

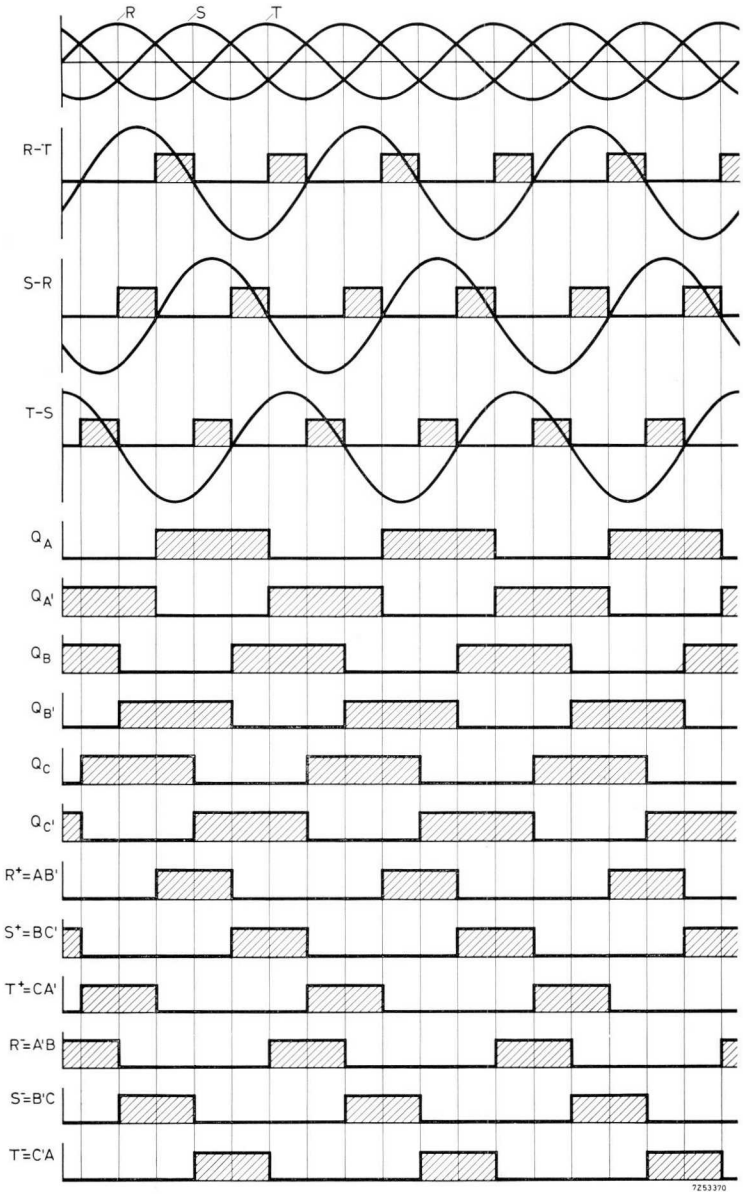


Fig. 9.17. Trigger pulse timing diagram. The topmost graph represents the supply phase voltages, and graphs R-T, S-R and T-S the phase-to-phase voltages together with pulses generated inside the PTUs (shaded portions). These pulses produce the signals Q_A, Q_A'; Q_B, Q_B'; and Q_C, Q_C' from PTUs A, B and C (see Fig 9.15). Graphs R^+, S^+, T^+ and R^-, S^-, T^- represent the periods for which current could flow in the appropriate thyristors.

9.4.1 The Central Control Unit (CCU)

The central control unit (CCU) accepts both positive and negative reference voltages up to 10 V. It is equipped with a tachometer ripple suppression filter, a predetermined level adjustment of the output control voltage and has an adjustable maximum current limit. Two DOA40 blocks are used. The CCU can control a motor with a dynamic speed accuracy of better than 1 %, independent of the current flowing in the motor.

The input requirements are as follows:

— A reference voltage, variable between −10 V and +10 V.
— A d.c. tachometer voltage output of about 100 V at 1500 r.p.m.
— A control current input of up to 100 mA (using a current transformer with a turns ratio of 1 : 1000, motor currents of up to 100 A can be controlled).
— A limit signal L fed back from the PLU (maximum amplitude about −3 V to +3 V, dependent on motor terminal voltage; negative voltages are required when the motor acts as a generator).
— A so-called "lock" signal (when this signal is positive, the control output voltage is 0 V).

There are two outputs:

— A control voltage output, variable from 0 to +5 V to control the phase shift trigger units.
— An output signal A, giving information concerning the difference in V_{tacho} and V_{ref}. This signal will indicate which of the two bridges has to be selected in a twin bridge motor control system.

9.4.2 The Logic Control Unit (LCU)

The logic control unit (LCU) controls the switch-over from one current direction in the motor to the opposite one. In twin bridge motor control systems, it takes care of the switch-over from one bridge ot the other. It also contains a pulse generator for the drive of the PTUs and the TTUs. The pulse generator delivers pulses with a repetition rate of 10 kHz, remaining at 0 V for 80 μs approximately. The LCU also produces the "lock" signal for the CCU. The unit contains eight 2.NOR60s and two 2.IA60s.

The LCU is controlled by two input signals, namely:

— the A signal from the CCU
— the current input (I) signal; the LCU outputs may only be switched over when I is virtually 0.

The outputs of the LCU are:

— Signal *CW*, having voltage levels of either +12 V or 0 V, for clockwise rotation of the motor.
— Signal *CCW*, having the same voltage levels as the *CW* signal, for counter-clockwise rotation of the motor.
— A "lock" signal, which can temporarily make the control voltage of the CCU equal to 0 V.
— Output pulses for driving the PTUs and the TTUs (repetition rate 10 kHz, remaining at 0 V for 80 μs approximately).
— Two output signals, X and X', necessary for the proper operation of the PLU.

9.4.3 The Phase Shift Limit Unit (PLU)

The PLU limits the control output voltage of the CCU to such a value that the average output voltage of the bridge is limited to a value slightly in excess of the motor terminal voltage. In this way, excessive peak currents in the motor are avoided during the transient times, e.g. from motoring to generating and vice versa.

The unit is composed of one DOA40 and five 2.NOR60s.

The input requirements are:

— Motor terminal voltage, via an integrating network.
— An asymmetrical tachometer input voltage for the detection of the sense of rotation of the motor.
— Input signals X and X' from the LCU, indicative of the sign of the difference in V_{tacho} and V_{ref}.

The output from this unit is a signal L proportional to the input motor terminal voltage, from 0 to +3 V when the motor acts as a motor, and from 0 to −3 V when the motor acts as a generator. Also available is a signal wich indicates whether the motor is braking or accelerating.

9.4.4 The Phase Shift Trigger Unit (PTU)

The PTU is able to control four thyristors of a single-phase full-controlled bridge. Three PTUs are required for a three-phase full-controlled bridge.

The circuit blocks it contains are one PSM40, three 2.NOR60s and two PA60s.

The input requirements are as follows:

— A synchronisation voltage of 2×24 V, 50 Hz, in antiphase.
— A control voltage, variable between 0 and 5 V.
— An input pulse at the "pulse" terminal from the LCU.

— Two inputs signals, X_1 and X_2, in the case of 3-phase operation, to reduce the triggering period from 180° to 120° (to this end the terminals have to be connected to the output terminals Q_1 and Q_2 of another PTU).
— A 10 kHz input pulse from the LCU.
— An input signal S, that can switch off the output stages, when this signal exceeds 10 V.

A special pulse output transformer is to be used with the PA60 to trigger two thyristors simultaneously down to temperatures of −55 °C. The trigger phase angle can be controlled from 10° to 170° with a control input voltage of 0-5 V. The PTU ensures that the average output voltage of the thyristor bridge is proportional to the control voltage, thus giving linear control possibilities. The thyristors can be made to pass current over the whole conduction period by means of repetitive pulses with a pulse duration of 20 μs and a repetition rate of 10 kHz.
The outputs available are:
— Two output signals to be taken to the pulse transformers, each giving repetitive pulses of 24 V, 600 mA.
— Two outputs Q_1 and Q_2 that can be connected to the inputs X_1 and X_2 of another PTU for three-phase operation.

9.4.5 The Twin-Trigger Unit (TTU)

The TTU is intended to be used mainly in combination with the PTU. With three PTUs and three TTUs, it is possible to control two 3-phase thyristor bridges. The TTU, furthermore, is suitable for triggering a field-current reversing thyristor system.

It comprises one 2.NOR60 and two PA60s. A specially developed pulse output transformer is to be used in combination with the PA60.
The input requirements are:
— In the case of a double three-phase thyristor bridge, the TTU must be connected parallel to the PTUs, the inputs Q_1 and Q_2 being connected to the outputs Q_1 and Q_2 of the relevant PTU. The inputs X_1 and X_2 should be connected to the same terminals as the X_1 and X_2 inputs of the relevant PTU. When the TTU is used as a field current reversing thyristor circuit triggering unit, the Q_1, Q_2 and X_1, X_2 terminals can be left unconnected.
— A 10 kHz input pulse from the LCU.
— An input signal S to switch off the input stages when it should exceed 10 V.

The thyristors can be made to pass current over the whole conduction period by means of repetitive pulses with a pulse duration of 20 μs and a repetition rate of 10 kHz. The two output terminals can be connected to the trigger transformers, each being able to give repetitive pulses of 24 V, 600 mA.

10 Testing and Maintenance

10.1 Testing

The prototype or breadboard model of a control system should be thoroughly tested to make sure that the unit performs as required. It is good practice to test the equipment on the bench using small lamps for load indicators and switches to provide the various input conditions.

If the system does not immediately perform as expected (which may happen on a prototype), careful reasoning and a few checks will usually provide a clue to the error. The application of supply voltage to the control circuit should be preceded by a check on the connections of the power supply to the circuit; make sure that both polarity and points of connection are in accordance with the design. Furthermore check the power supply voltage and make sure that it is within the tolerances (18-30 V or, in the case of 12 V operation, 12 V, $\pm$ 5%).

In the case where a particular control output does not behave as intended a methodical approach will give the answer:

(a) check the presence of power supply voltage;
(b) check the presence of input signal;
(c) check the logic levels at various points, working backwards from the output to the input, at the same time verifying that all interconnections are according to the design diagram.

The logic level testing can be done with a 20 kΩ/V voltmeter or with the two-lamp test circuit given in Fig. 10.1. The function of the circuit is to give a positive indication of the voltage level at the LPA input, i.e. one of the two lamps will glow for a "high" level (lamp *A*), the other will glow when a "low" level is applied (lamp *B*). The circuit also has an outstanding safety feature: positive indication of lamp failure. If lamp *A* blows, lamp *B* will immediately extinguish.

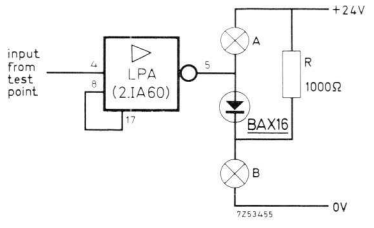


Fig. 10.1. Logic level indication with 2.IA60 block.

Being so simple, the circuit has many other advantages. It is inexpensive; it is compact; it is robust (no mechanical movement such as relays and meters); and it weighs very little — an ideal design to incorporate into a hand-held tester. A unit could also be permanently installed in a system to monitor a large number of voltage levels, by connecting the LPA input to a multi-position switch.

Use is made of two lamps having different ratings, in series. The LPA is connected in parallel with lamp *B*. If the LPA input is at the "low" level (i.e. LPA not driven) lamp *B* will glow, drawing current from the supply via lamp *A* and resistor *R*. (Owing to the presence of resistor *R*, the current through *A* will be a "dark" current i.e. insufficient to make *A* glow, but serving as a pre-heating current.)

If the LPA input goes to the "high" level, lamp "*B*" is short-circuited. Full supply voltage appears across lamp "*A*" and it glows. A dark current is now provided for *B* by resistor *R*. The diode ensures that the dark current intended for lamp *B* will flow through the lamp, and not through the LPA.

Always use the correct lamps, as regards both the voltage and the current ratings. The code numbers for these lamps are:

Lamp *A*	(28 V - 0.1 A)	9234 640 21700
Lamp *B*	(16 V - 40 mA)	9235 063 18703

Lamp *A* will glow with a "high" level input of between +11.4 V and +30 V, and lamp *B* at a "low" level input of between 0 and +0.3 V. These voltage levels are applicable to all systems using 60-Series circuit blocks.

Now if all the components function properly, the design is correct, and the reset of memories at supply turn-on works correctly, the system should be operative. If not, it should be checked whether some unit is not functioning properly.

Going through the test procedure, one will often have to make sure that a particular unit is capable of switching. In so doing, it should be realized that putting a hard voltage on an input is not allowed, since the previous unit gets this voltage directly on its output (Fig. 10.2); in this

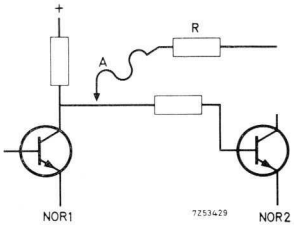


Fig. 10.2. Testing NOR (2). Probe A carrying +12 V test voltage should incorporate a series resistor of at least 7.5 kΩ to limit the current to NOR (1).

way damage may occur. Therefore, never apply a "test voltage" to a terminal without having a series resistor of at least 7.5 kΩ in the test signal line.

A number of other terminals should not be subjected to a "hard" voltage either. These points are indicated in the relevant data sheets. The series resistor should therefore be permanently incorporated in a "1" level test lead.

After the system has been brought to the condition required it should be completely documented as to the true layout to avoid errors in production. Nevertheless, taking the circuit from the bench to the application can still give rise to errors. First of all there are the risks of transient voltages on input lines — they should be eliminated at the system input by either to terminating the lines having mechanical switch signals by means of switch filters or by capacitively loading the input line.

If possible a check for transient interference voltages on incoming lines should be made. This can be done by terminating the line with a "memory connected" 2.NOR60 — taking care to apply a reset signal after the connections have been made. Observing the output of the Memory with the two-lamp circuit given above will tell whether interference could upset system performance.

Now even if the system inputs are "clean", further possible reactions from the system output will still have to be investigated. Intersystem switching will hardly affect the operation, provided that the recommendations from Chapter 6 have been followed. However, the output circuit might switch high power loads which, under certain circumstances, could interfere with the control system. The best way to avoid this type of interference is by physically separating the power carrying lines, taking them as far away as possible from the logic wiring. An interference signal of short duration will be particularly annoying if it sets a memory. If the inputs to the memories can be decoupled with capacitors (within the requirements of the operating speed of the system), effective interference elimination can be obtained at critical points.

10.2 Maintenance

It has been observed in actual practice with static control systems that virtually zero maintenance is necessary — the system will work for many years after the initial commissioning. Strangely enough, this very attractive characteristic introduces difficulty from the maintenance point of view.

It can hardly be expected that, say, 5 years after the design was made, the designer will still be familiar with all its details. This creates the need for a complete, ready-to-use check sequence instruction. The instruction should specify check points and levels at various points in order to allow quick servicing. For this reason printed wiring board mounted units are generally preferred to systems using direct point-to-point wire wrapping or soldered connections. The circuit blocks should be grouped into functions, each board with a particular function, so that localization of a fault can be quickly achieved.

11 Examples of Machine Tool Control

Despite the huge variety which exists in machine tool design, most machining processes consist of continual repetitions of four basic movements of the cutting tool as shown by Fig. 11.1 (the movements are relative, that is, in some cases it is the work which moves in relation to a fixed tool; however, the following analysis still holds):

I — towards the work;
II — along the work (machining action);
III — away from the work;
IV — return to initial position.

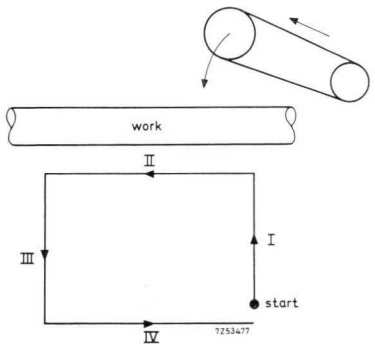


Fig. 11.1. The four basic cutting tool movements.

There are of course any number of variations of the pattern; and the pattern (cycle) of movements may be either repetitive or programmed to give a different operation at each cycle (automatic tool changing, speed changing, etc.) until the work is fully machined.

11.1 Repetitive Cycling of Operations

This situation is the simplest and most common one met with in practice; below is given the scheme used in a motor commutator finishing machine, shown in Fig. 11.2.

VSOs are used at several points as position indicators. A belt is lowered by an arm onto the armature surface to drive it, speed of descent being limited by an oil-damped mechanism. The tool is mounted on a cross-slide which is placed on a carriage.

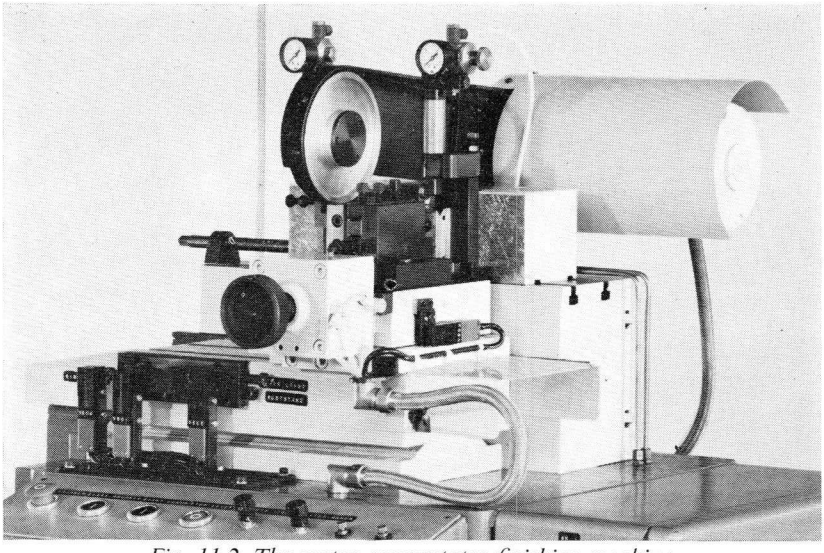


Fig. 11.2. The motor commutator finishing machine.

Pressing the "Start Programme" push button results in the following actions:

(*a*) The belt driving motor starts and the arm descends until a vane enters the slot of VSO(1); this halts the motion and initiates (*b*).

(*b*) The cross-slide is moved, so that the tool contacts the work. VSO2 signals this, stops the motion and starts (*c*).

(*c*) The carriage is advanced slowly. This is the machining action, and continues until VSO3 is reached. VSO3 stops the carriage motion and initiates (*d*).

(*d*) The cross-slide returns quickly to VSO4, which stops the motion and initiates (*e*).

(*e*) The carriage returns rapidly to VSO5 (initial position).

VSO5 could initiate a start signal to re-cycle the whole series of four operations. This process is similar to the one described in Chapter 8 for sequential control, but in which timers are used. The time diagram, Fig. 11.3, illustrates the above sequence.

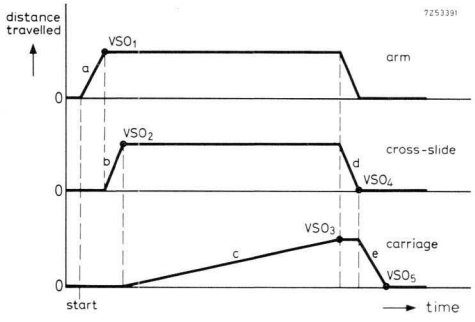


Fig. 11.3. Time diagram. The letters (a) to (e) refer to the sequence of operations given on p. 165.

11.2 Machine Tool Control with Provision for Variation of Machining Operations

The example below gives the possibility of performing a different operation at each pass of the tool, i.e. a machining operation could consist of a number of passes, each different (for example turning, then grinding, then knurling).

The logic circuit necessary to cause the cycle of Fig. 11.1 to be traced out could be similar to Fig. 8.24. Limit switches LS_1, LS_2, LS_3, LS_4 are closed at the completion of each movement of the tool. As each movement occupies a certain time, memories M_1, M_2, M_3, M_4 are used, and these signals activate the appropriate circuits. Closing of a limit switch resets the preceding memory.

The memory outputs M can be used to drive four motor contactors, connected for example in the field of a d.c. motor to control speed and direction for each movement as in Example 1, or they can be used to initiate a different programme for the movement, for example the motor speed over path BC may be required to be halved at the second cycle of operations. This simply means that M_2 must be fed to a counter whose No. 1 output closes a full-speed contactor, whilst No. 2 output closes a half-speed contactor.

Of course not only change of the motor speed, but change of tool, change of cutting fluid, change of work speed or change of distance travelled are also controllable by the counter output. The distance travelled can be detected in many ways (e.g. by VSOs as in Example 1), but if a continuous adjustable control over travel is required this can be done with the aid of a potentiometer. With a second potentiometer pre-set in the programming control circuit, action could be made to result when zero difference is detected between the two potentiometer settings.

It should be remembered that this circuit is basic, and the outputs M are signals only. For driving relays or solenoids the IA60 or PA60 should be used, with the appropriate safety precautions given in Chapter 14. For driving the counter, a pulse is required, obtained by connecting a one-shot circuit between M and the counter input.

11.3 Control Circuit for an Assembly Process

As a practical example of machine control, we shall now discuss in some detail the control of an assembly process. The process involves assembly, in a definite sequence, of three components. An alarm signal must be produced if the sequence in which the components appear prior to assembly is incorrect. The control system can be divided into the following functions:

— detection of the arrival of the components in the correct sequence;
— memorization of the input signals;
— comparison of the input signals with the memories and thus verification of the correctness of the component sequence;
— production of an alarm signal upon detection of incorrect sequence, or production of a signal to activate the assembly mechanism and reset the memories, upon detection of correct sequence.

Various input devices can be used to produce the input signals. Let us call the input signals from the three components A, B and C, and assume that this is the correct sequence in which they must arrive. In order to establish this sequence, A and B must be memorized, so that when C becomes available the sequence can be checked. There is, however, a difficulty which could arise: signals A or B could occur more than once, and if this happens an alarm signal must also be given. A special type of memory is thus required for A and B.

Fig. 11.4 shows such a configuration for A. At the start of operations, both memory outputs are at 0. If component A now produces signal A, M_a' is 1 and $\overline{M_a}'$ goes to 0 and remains in this state. Thus when A returns

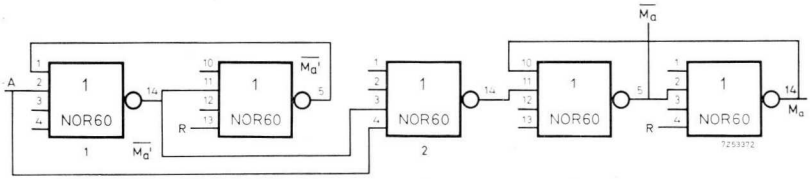


Fig. 11.4. The special memory circuit.

to 0, the input to the second memory goes to 1 and M_a becomes 1. The important characteristic of the circuit is that M_a stays 0 only until A has gone to 0 the first time. (Note that under certain conditions this may not be entirely correct: M_a could go to 1 during the time that A is going to 1 and $\bar{A}'$ to 0, then go to 0 when A reaches full 1 level, and subsequently 1 again when A drops to 0. This effect could be eliminated by placing a 47 kΩ resistor at the A input to NOR(1), thus slowing it down, or paralleling two inputs for A at NOR(2), thus speeding up this NOR.

Detection of the correct sequence is done by comparing the signals A, M_a, B, M_b and C. These five variables give a total of 32 possible combinations. Looking at the problem from a practical point of view, it is easy to see that the following actions should arise for correct working, in the sequence given:

action 1: reset to zero;
action 2: arrival of first component; A appears;
action 3: A disappears;
action 4: arrival of second component; B appears;
action 5: B disappears;
action 6: arrival of third component; C appears and assembly starts.

These 6 combinations, out of the 32 possible, should *not* result in an alarm; the other 26 should. The table expresses the above conditions in terms of the signals.

action	signal				
	A	M_a	B	M_b	C
1	0	0	0	0	0
2	1	0	0	0	0
3	0	1	0	0	0
4	0	1	1	.0	0
5	0	1	0	1	0
6	0	1	0	1	1

A rather lengthy formula in switching algebra is required for expressing the conditions which cause an alarm. However, by using the techniques discussed in Ch. 7, it can be reduced to the following:

$(M_a + B + M_b + C)(A + \bar{M}_a + M_b + C)(A + \bar{M}_a + B + \bar{M}_b) = Y$

where Y designates an alarm signal. Fig. 11.5 shows the logic circuit necessary to achieve this.

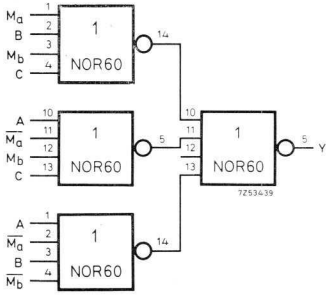


Fig. 11.5. Logic circuit producing the fault signal Y.

The output stages of the system are given in Fig. 11.6. The alarm signal Y sets a memory whose output M_y causes visual and audible warnings (L_F and B). The memory can be reset by either signal L (push button acknowledge) or by removal of C (i.e. appearance of $\bar{C}$). An alarm signal must also be given if the assembly mechanism is working (PA60 output is 0) and another component A appears ($A = 1$, $\bar{A} = 0$); thus, the PA60 output and signal $\bar{A}$ are brought to a NOR performing the AND function.

The signal N which appears after the three components have arrived in correct sequence, is derived from:

$$M_a \cdot M_b \cdot C \cdot \bar{M}_y = N.$$

N must not appear if a fault memory signal M_y is present.

The TU60 ensures that an adequate time is allowed for the assembly operation. The PA60 output is used to light the lamp L_B, warning that the assembly mechanism is operating, and the LPA provides a signal for the TTM which, in turn, switches on the two thyristors to supply a.c. current to the load.

At switch-on of supply voltage to the system, the TU60 will deliver a pulse output. To guard against this effect, an interlock memory E is used to produce signal M_e, which, together with the TU60 output, is fed to a NOR gate whose output switches on the PA60 and LPA units, and thus the assembly mechanism. The fault memory signal M_y can also reset this memory, so that assembly cannot start if M_y is present, despite, any pulse output from the TU60 unit.

The memories mentioned above (for E, Y and the input signals A and B) need to be reset according to the table on p. 171.

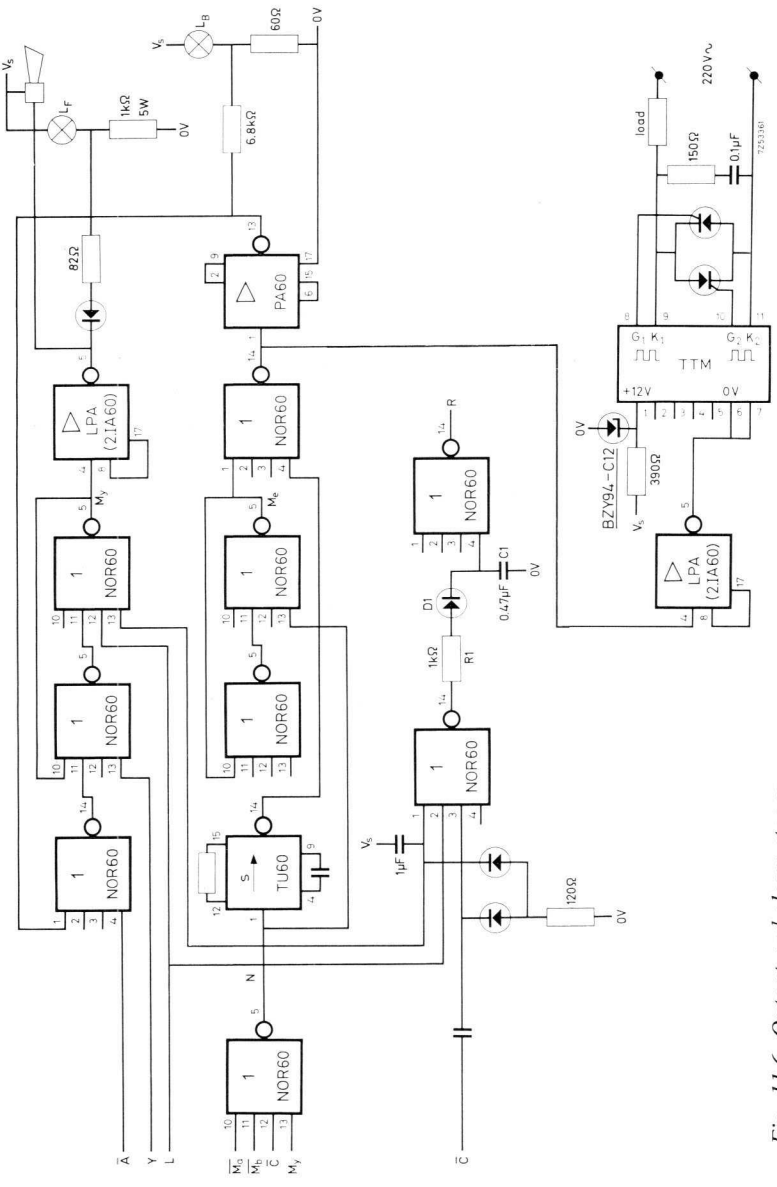


Fig. 11.6. Output and alarm stages.

memory	condition:		dis-appearance of C	appearance of M_y
	switch-on of supply	acknow-ledge alarm push-button		
Input signal memories M_a', M_a, M_b', M_b	reset	reset	reset	—
Interlock memory E	reset	—	—	reset
Fault memory Y	reset	reset	—	—

The reset signal R for the input signal memories, derived from $\bar{C}$ (disappearance of C), is slightly delayed by the $R_1C_1D_1$ network shown in Fig. 11.7, to allow for contact bounce on closure of the switch delivering signals C and $\bar{C}$.

12 Examples of Alarm Systems

Generally, an alarm system works on the following basis: the abnormal condition is detected and signaled to a central control, where intermittent aural and visual signals are produced, warning the operator to push an "acknowledge" button. This cuts off the aural warning and changes the visual warning from a flashing light to a steady one. When the abnormal condition returns to normal ("clears"), the steady light must disappear. Fig. 12.1 shows a practical circuit.

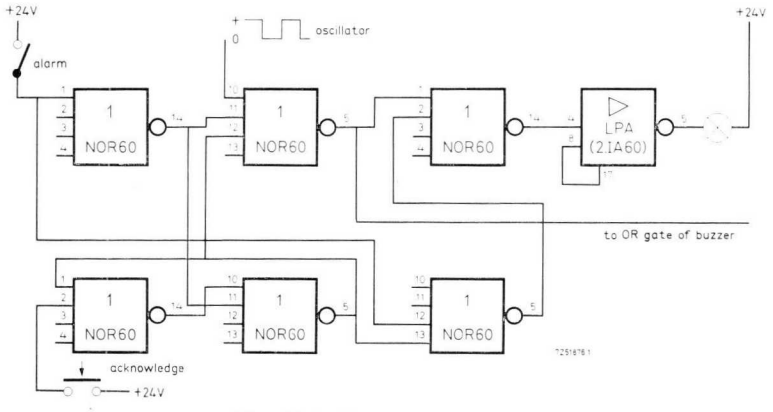


Fig. 12.1. Basic alarm circuit.

The square-wave signal which determines the lamp and buzzer activating frequency may be obtained from the circuit of Fig. 8.68. The abnormal condition may, however, have ceased before the operator was able to take note of it. A solution to this problem is to use a memory of two NORs to store the input condition as shown in Fig. 12.2. The memory can be reset only by pushing the "acknowledge" button.

The above circuits merely give the logic involved for basic alarm systems. In practice, the input requirements, power supply and method of deployment of the alarm system must be given consideration. At the input side either normally open or normally closed contacts can be used. The input voltage level can be chosen rather arbitrarily, by using step-down resistors. To eliminate interference on long cables, *RC* filtering can

be applied. By using 100 V on the contacts and the switch filters 2·SF60, complete immunity from interference voltages of over 20 V can be obtained on lines. The degree of elimination of transients depends on the value of the filter capacitor.

By using three inputs in parallel, alarm indication can be obtained with input currents of 0.1 mA at 4.4 V only, which should enable the system to meet requirements of intrinsic safety for the input lines. Electronic devices, such as the EPD or VSO (Chapter 5) give very much greater reliability than electromechanical switches.

The power supply is often the least reliable section of the equipment. To guard against its failure, and to retain supervision in case of mains

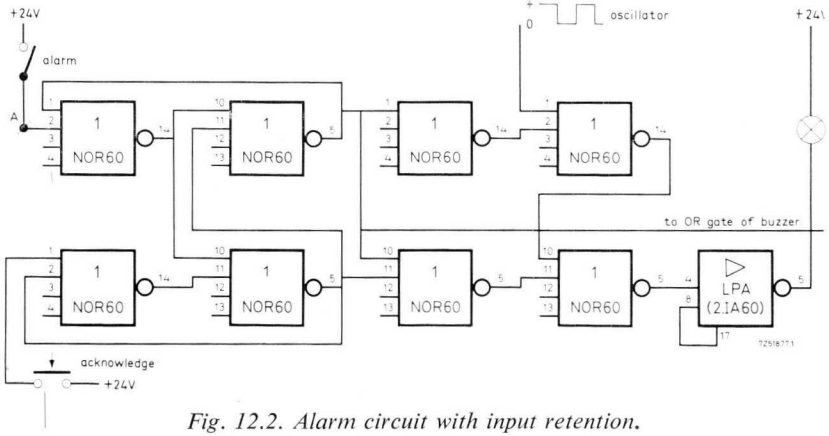


Fig. 12.2. Alarm circuit with input retention.

outages, storage batteries are commonly used. The terminal voltage should be such as to allow periodic discharging and trickle charging as the supply voltage fluctuates about its normal value (approx. 24 V for NORBIT systems). Further details on power supplies are contained in Chapter 3; Section 3.5 deals with battery operation. As an example of the power requirements of an alarm system using 60-Series circuit blocks, a system of the type given in Fig. 12.2 above, monitoring 40 points in a production process, is as follows:

logic section,	500 mA	(24 V operation);
power section,	5 A max.	(all buzzers and lights on).

The average power drain will of course be very much lower.

Many variations on the basic scheme described above are possible. For smaller systems it is usually sufficient to provide a light and "acknowledge" button for every monitoring point and let the operator have complete manual and logical control. However, in a power station alarm system, for example, the number of monitoring points can easily run into hundreds, and more efficient usage of the alarm system is thus essential.

In such large systems, it is often possible to relegate each monitoring point to a classification within each of two divisions: fault type and group. In a power station these could be temperature, pressure, water level, etc. (fault type classifications), and boilers Nos 1, 2, 3, 4 (group classifications). All the sensors for one fault type could thus activate a single warning light in a central display panel for faults, and all fault types for one group similarly brought to a "group" push-button. Thus, if m = number of fault types and n = number of groups, the number of annunciators required between the plant and the control desk is reduced from mn to $m + n$; space is thus saved and readability improved.

Applications for this type of alarm or surveillance are in fire alarms, where the situation is divisible into n groups with m check points (the display panel with m lights could be an actual machine floor plan or a machine); detection of unoccupied places in a store (m places in n areas); and automated production processes (m checking points per process for n processes).

Another requirement of an alarm system can be that alarms be dealt with in the order of appearance. To this end the queueing circuit of Section 8.4.2 could be directly inserted in the output of the alarm circuits. Data-logging is also a common requirement; this shows another advantage of the system just described, in that the number of channels required is only $m + n$ instead of mn. Priority of alarm is required in some cases and this can be simply achieved with NOR gating. Any of the circuits given in Chapter 8 can in fact be used with the basic alarm circuits for further adaptions.

13. Examples of Elevator Controls

13.1 Introduction

Static control offers particular advantages when applied to elevator control systems. The three systems described here use static control throughout, and the only mechanical action in the systems could be at the push-buttons and the hoist motor contactor (although even these could be made static). High reliability and safety are thus ensured.

Four main types of elevator system can be distinguished; these are listed here in order of complexity:

— Simple "Call-Send" ("dumbwaiter"). This type is used as a goods elevator; little control circuitry is required, and that mainly for safety purposes.

— "Personnel Call-Send". When a call is placed, this is registered and the elevator immediately proceeds to that floor, all other calls being ignored during the transit time. Push-button control may be installed in the elevator cabin, and special safety precautions are usually required.

— "Collective Down". This system is commonly used in apartment buildings and offices. When descending, the elevator cabin will stop at all the lower calls registered whether made from inside the cabin ("cabin calls") or from the floor push-buttons ("floor calls"). When ascending, however, only cabin calls are obeyed, and of these, only those which request a higher floor. After all cabin calls have been satisfied, the cabin will move to the highest floor call registered. All calls are registered, whether obeyed immediately or not.

— "Collective Up-and-Down". Still more sophisticated, this system provides that the cabin will stop at all calls in both the up and the down directions. All calls received are carried out in ascending *or* descending numerical order, except when a cabin call would result reversal of motion with a previous higher call unsatisfied. As for Collective Down, all calls received are registered.

More advanced systems are of course possible, such as the duplex and triplex types (two and three elevators respectively). In this publication, however, we shall consider merely the control circuits for three of the systems listed above — the Call-Send, Collective Down, and Collective Up-and-Down.

The three schemes described have been designed for flexibility in application. In these schemes, adaption of the circuit to serve any number of floors is a simple matter: since part of the circuit is repeated for each intermediate floor, this part may be added (e.g. in the form of a ready-wired unit), as many times as necessary for the number of floors.

All schemes provide for floor lights indicating cabin arrival or that the cabin is in use, and the usual safety interlocks are incorporated (open door and hoist motor direction interlocks).

Depending on the application, various extra facilities and safety devices (e.g. homing circuits, floor position memory) can be connected. The supply voltages required are as follows:

— Single-rail $+24\ V_{dc}$ for 60-Series logic units.
— $+100\ V_{dc}$ for push-buttons and switches.
— Mains supply for lamps, contactors and bells; these are switched on by means of thyristors serving as simple and inexpensive low-power amplifiers. (The thyristors should be shunted by an RC filter, as shown by R_2, C_2 in Fig. 13.17). The thyristor supply should be taken from a mains transformer secondary winding, to isolate the mains ground from the logic system common.

The description of rather complex logic schemes such as elevator control systems is much assisted by the use of switching algebra (Boolean Algebra) and we use it in the following descriptions. However, only a basic knowledge is required as the circuits are evolved in simple steps and the equations are not complicated. (Cf. Ch. 7 for the necessary information on switching algebra.) To further simplify the description, the complete circuit for each scheme has been divided into a number of sub-circuits corresponding to the functions given in the block diagram for the scheme.

13.2 One Speed Call-Send Goods Elevator

A complete wiring scheme is described here for a multiple-stop call-send elevator. The electronic system can be extended for any number of floors, merely by adding extra floor units as drawn for the nth floor in Fig. 13.1. (No push-buttons are installed in the cabin.)

The position of the cabin is determined by Electronic Proximity Detectors placed in the shaft. These EPDs are activated by a vane mounted on the cabin.

At each floor a number of push-buttons are available, one for calling the cabin and others for sending it to another floor. As soon as a call

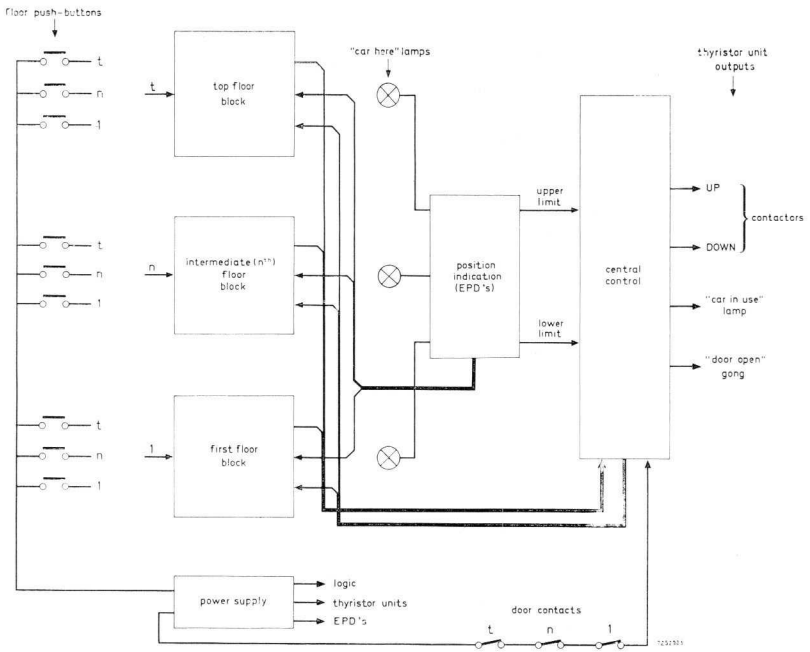


Fig. 13.1. Block diagram of the call/send goods elevator.

is registered in the electronic system, all other calls are blocked. The system is also blocked when the doors are open; unblocking occurs upon cabin arrival after an adjustable time if the doors have not been opened. Pushing a call-button with the doors open will give a gong signal.

When the power supply of the electronic system is switched on a reset signal is given to all memories to ensure that the cabin remains stationary until a floor push-button is pressed. If, however, the homing circuit is connected, the cabin will immediately go to the first floor as soon as the doors are closed, when the power supply is switched on.

If the brakes of the hoist motor become worn it may happen that the cabin does not stop exactly in front of the EPD. This will not affect proper functioning of the electronic circuit because a memory system gives an additional approximate indication of the position of the cabin. Two extra EPDs are installed as limit switches, at the top and bottom of the elevator shaft.

"Car in use" and "Car here" lamps on each floor give information about the position of the car.

The list below contains the symbols used for the various signals appearing in the circuit for different situations.

Symbol	*significance*	*occurs when:*
C_n	call signal floor n	floor push-button is pressed
F_n	position signal floor n from EPD via associated NOR	cabin is at floor n
L_n	position signal (floor n) from EPD	cabin is between floors $n+1$ and $n-1$
U_n	up-call to floor n	cabin is below floor n and X_n is present
D_n	down-call to floor n	cabin is above floor n and X_n is present
X_n	call memory	floor push-button is pressed, doors are closed, and cabin not at n
Y_n	position memory	cabin is at floor n
B	block signal	(up/down +5 s) or (door-open) signals are present
R	reset signal	system is switched on
DO	open-door signal	any door is open
ODG	open-door going	any door is open and a floor push-button is pressed
UL	upper-limit signal	cabin is at top floor
LL	lower-limit signal	cabin is at bottom floor
UP	up-signal for hoist motor	cabin is required above
$DOWN$	down-signal for hoist motor	cabin is required below

The call-signal C_n becomes "1" (via a switch filter) when one of the floor push-buttons is pressed. This signal will set the call memory X when there is no blocking signal (Fig. 13.2).

Reset occurs when the cabin arrives at floor n or when a general reset R is present:

$$(C_n\bar{B} + X_n)\bar{L}_n\bar{R} = X_n.$$

The signal X_n of this memory will give an "up" signal (U_n) to central control, when the cabin is at any floor below floor n:

$$(L_1 + L_2 + \ldots + L_{n-1})(X_n + C_n\bar{B}) = U_n.$$

A "down" signal is given to central control when the cabin is at any floor higher than floor n:

$$(L_{n+1} + L_{n+2} + \ldots + L_t)(X_n + C_n\bar{B}) = D_n.$$

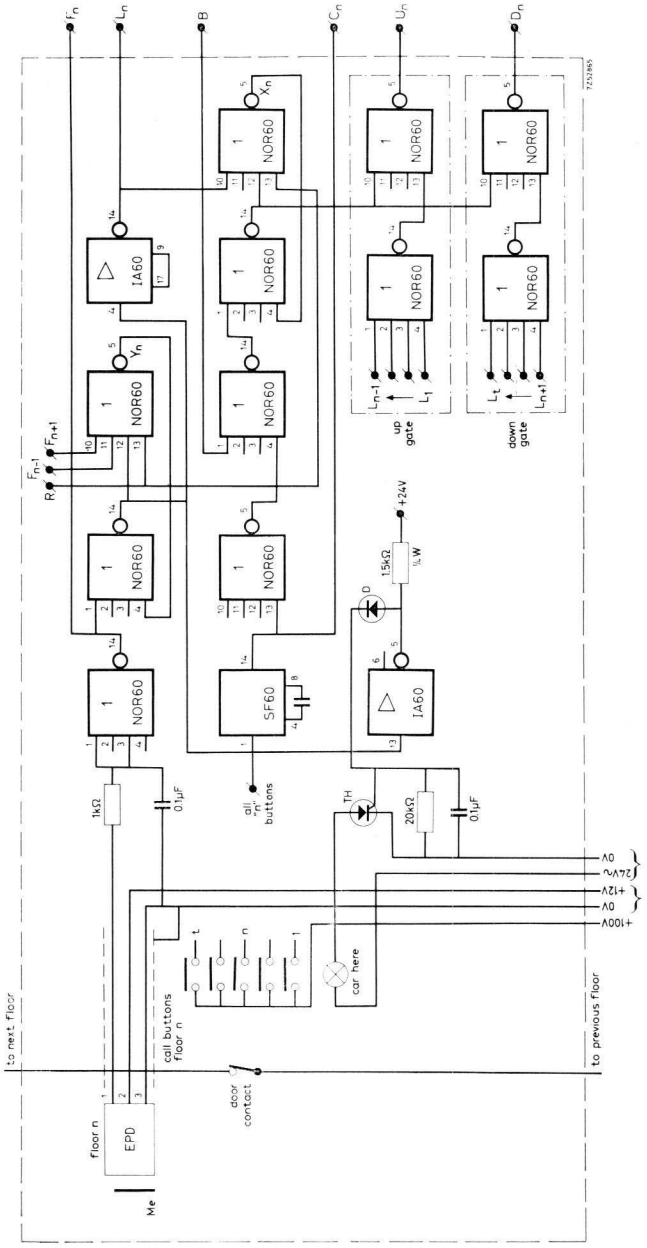


Fig. 13.2. Intermediate (nth) floor block.

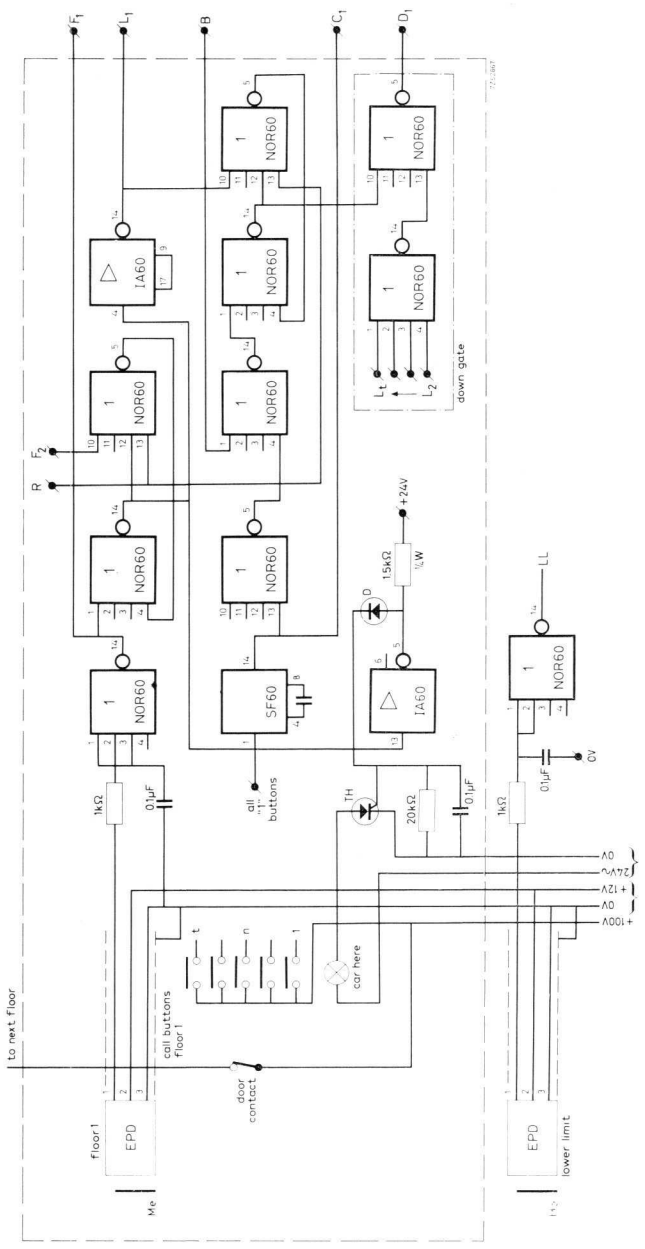


Fig. 13.3. First floor block.

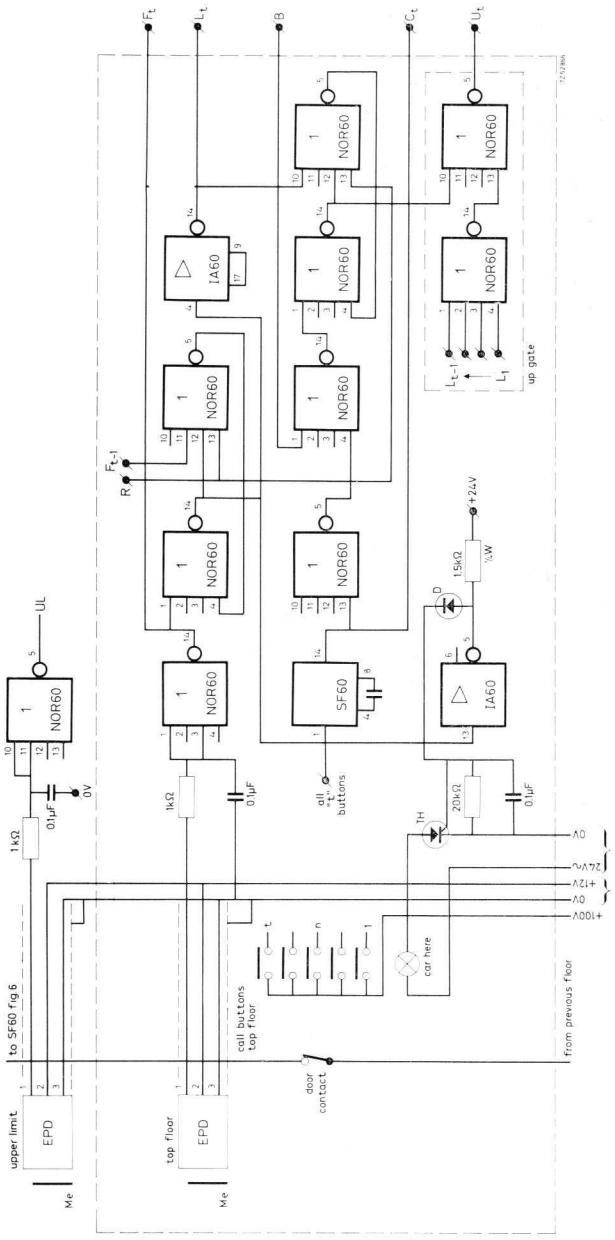


Fig. 13.4. Top floor block.

Where more than four gate inputs for U_n or D_n signals are required, (i.e. more than five floors), extra inputs can be obtained by using additional NOR60 units with their outputs paralleled. (Care should be taken that in this case only one of these NORs is connected to the positive supply voltage.)

The "up" gating circuit can be omitted for the first floor circuit (Fig. 13.3) and similarly the "down" gate can be omitted for the top floor circuit (Fig. 13.4). This is the only difference between these circuits and the circuits for the intermediate floors. When the cabin is at floor n, the EPD gives a 0. After the input NOR, this gives an $F_n = 1$ signal. The F_n signal will set memory Y_n giving the cabin position L_n. The memory is reset by the signal R or when the cabin arrives at floor $n + 1$ or at floor $n - 1$:

$$(F_n + Y_n)\bar{R} \cdot \overline{F_{n+1}} \cdot \overline{F_{n-1}} = Y_n$$

and

$$F_n + Y_n = L_n.$$

The "elevator here" light for floor n will light up when $L_n = 1$. The U_n or D_n signal is taken to the central control section (the Up/Down control circuit, Fig. 13.5) producing an *UP* or *DOWN* signal when the following conditions are satisfied:

$$(U_2 + U_3 + \ldots + U_t)\overline{UL} \cdot \overline{DO} \cdot \overline{DOWN} = UP,$$

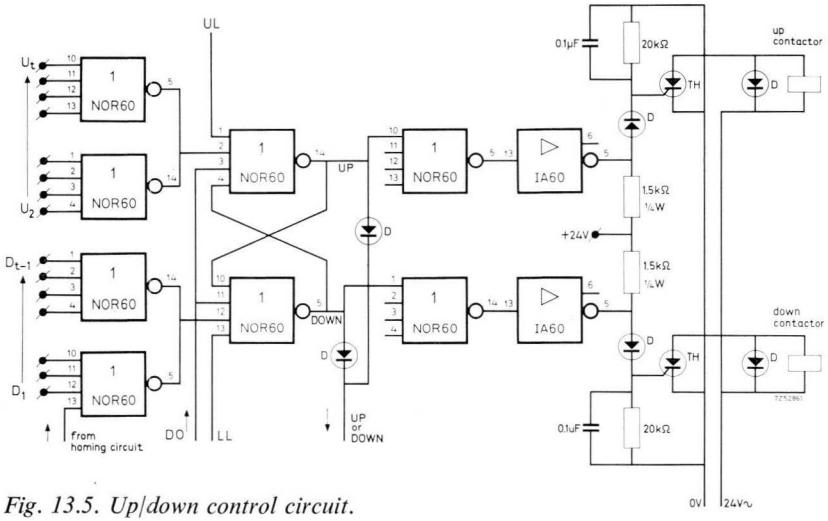


Fig. 13.5. Up/down control circuit.

or, respectively:

$$(D_1 + D_2 + \ldots + D_{t-1})\overline{LL} \cdot \overline{DO} \cdot \overline{UP} = DOWN.$$

UP and *DOWN* are interlocked; *DO* is given by a series connection of normally closed contacts.

The *UP* and *DOWN* signals are fed to the input of a TU60 unit, as shown in Fig. 13.6. This gives a time delay (depending on the external capacitor *C*) when the input goes from 1 to 0. The blocking signal *B* is derived from the TU60 output or door open signal. Thus $B = 1$ if any door is open, or if the cabin is in motion, or if less than the time interval set by TU60 has elapsed since cabin arrival.

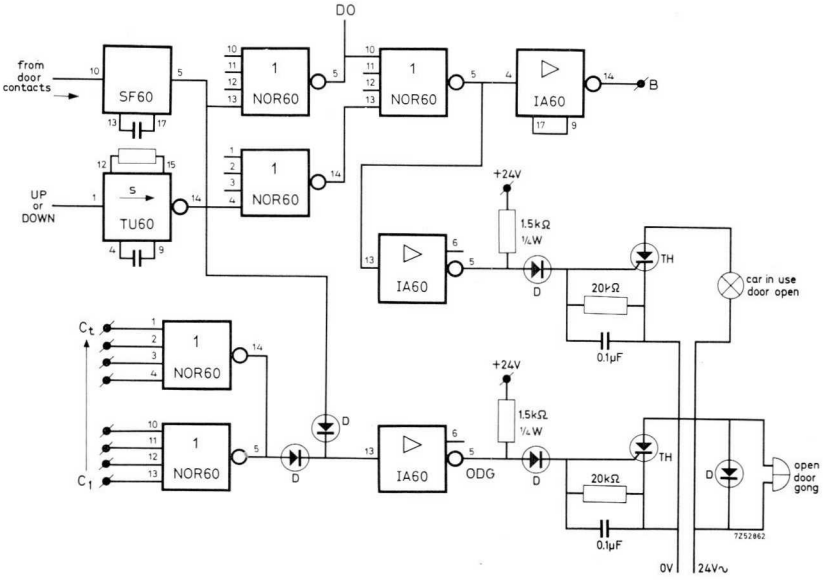


Fig. 13.6. Door logic circuit.

When $B = 1$ the lamp "Car in Use, Door Open" will light up. The gong is activated if there is a call signal and a door is open:

$$(C_1 + C_2 + \ldots + C_t)\mathrm{DO} = \mathrm{ODG}.$$

The automatic reset circuit (Fig. 13.7) will deliver a short $R = 1$ pulse when the power supply is switched on. This pulse will reset all the memories in the system. In addition, it can be used to set a memory in the homing circuit. This memory will give a *DOWN* signal (when all doors are closed) until the memory is reset by F_1 (or *LL*) at the first floor.

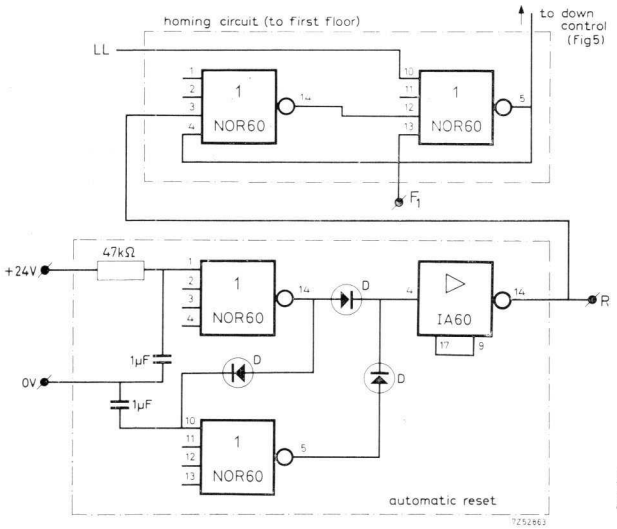


Fig. 13.7. Reset and homing circuits.

13.3 One-Speed Collective-Down Elevator

13.3.1 General

The general specifications for this system are assumed to be:

— Single speed operation.

— Position indication by ratchet-type stepping switches.

— Collective Down System (see Section 13.1 for definition).

— Braking zone inhibit; when the cabin is already moving towards a floor it will not stop at an intermediate floor if the call for the latter floor is given after the cabin has entered its braking zone.

— Automatic door control and timing.

— Provision for safety circuits; several safety circuits are incorporated in the system and others can easily be included.

— For the 60-series circuit blocks the power supply is single rail, 24 V ($\pm$ 25%).

— Thyristor output amplifiers; simple and inexpensive output amplifiers are obtained with small thyristors for driving lamps or motor-contactors from the a.c. supply.

— Separate Up, Down and Main Contactors to control the hoist motor.

13.3.2 Detailed Circuit Description

Block Diagram

The block diagram for the system is given in Fig. 13.8. At the left are the floor blocks. The top and the first floor block are special circuits, those for all intermediate floors are similar. For the sake of simplicity only one intermediate floor is drawn.

An important principle should be noted here: the up call signals are fed to the central control via the top floor block only, and down call signals via the lowest (first) floor block only. The intermediate floor blocks form a chain to pass these signals to the top or first floor blocks. However, some control signals (e.g. stop signals and floor calls in order to open the doors) are fed to the central control unit direct from each floor block, while others (reset etc.) flow through lines common to all floor blocks. The floor call buttons can be made inoperative with the lockable service switch.

The floor blocks each have an output terminal for connection of a "Cabin in Use" lamp, which will light up when a call is registered. In the same way "Cabin position" lamps can be connected to a position indicator.

The central control unit delivers Up, Down and Main Contactor commands, and also produces the commands for operating the doors. The following limit switches and safety contacts are connected to this part of the system:

— up limit (activated when cabin is at top floor);
— down limit (activated when cabin is at first floor);
— M-contact (interrupted when motor is running);
— "door opened" contact;
— "door closed" contact;
— hall lock and car lock.

Other safety switches or contacts could be connected in series with the supply voltage to the output contactors (Up, Down and Motor), if considered necessary. The doors can be operated from the cabin by means of push buttons.

A general reset signal R is used to reset all memories in the system at initial switch-on of the supply voltage.

The detailed description which follows considers each of the main sections in turn, using Boolean Algebra. The following symbols are used:

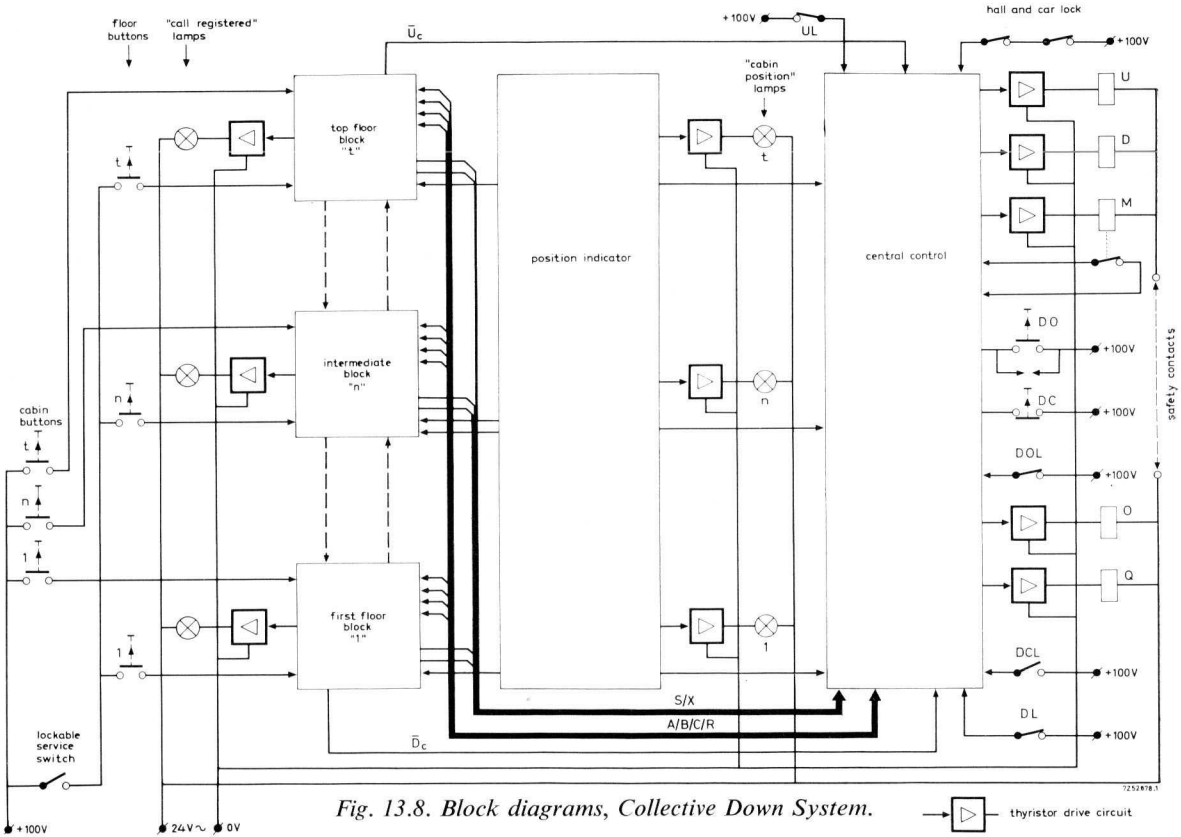


Fig. 13.8. Block diagrams, Collective Down System.

Symbol	*Significance*
suffix n	nth floor
suffix 1	first (lowest) floor
suffix t	top floor
suffix f	floor (hall)
suffix c	cabin
B_{cn}	cabin button nth floor
B_{fn}	hall floor button nth floor
M_{cn}	cabin call memory nth floor (from cabin push button memory)
M_{fn}	hall floor call memory nth floor (from floor push button memory)
U_n	up call from nth floor
D_n	down call from nth floor
X_n	hall call from nth floor
Z_n	zone signal nth floor (cabin in zone n)
S_n	stop signal from nth floor
U	up call (at end of up-chain)
D	down call (at end of down-chain)
UL	normal up limit switch
DL	normal down limit switch
UP	motor contactor command up
$DOWN$	motor contactor command down
M	motor contactor command on/off
DOL	"door opened" limit
DCL	"door closed" limit
B_{do}	"open door" button
B_{dc}	"close door" button
O	"open door" contactor command
Q	"close door" contactor command
R	general reset signal
A	special reset signal
B	prevents cabin stopping when ascending
C	blocks hall calls when door opened

Position Indicator

A stepping switch is used to detect the cabin position. The circuit drawn in Fig. 13.9 must be installed for each floor. The signal Z_n indicates the position; it is "1" when the cabin is in zone n (i.e. between floors $n+1$ and $n-1$).

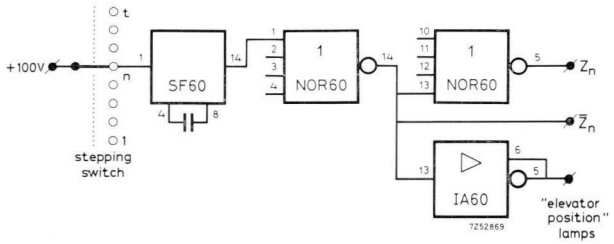


Fig. 13.9. Stepping switch position indicator.

Intermediate Floor Block

The cabin button n and the call button at floor n are each connected to a memory via a switch filter, SF60 (Fig. 13.10). When a button is pushed, the appropriate memory is set. Reset may occur in two ways, either when the car stops at the floor, or when a general reset R is present. Expressed in symbols, for a cabin call M_{cn}, this becomes:

$$B_{cn} = \text{set}, \quad R + \bar{A}Z_n = \text{reset},$$

and for a floor call B_{fn} it is:

$$B_{fn} = \text{set}, \quad R + \bar{A}Z_n = \text{reset}.$$

The cabin memory signal M_{cn} and floor memory signal M_{fn} may be derived:

$$(B_{cn} + M_{cn}) \cdot \overline{\text{reset}} = M_{cn},$$

and

$$(B_{fn} + M_{cn}) \cdot \overline{\text{reset}} = M_{fn}.$$

Thus:

$$(M_{cn} + B_{cn}) \cdot \bar{R}(A + \bar{Z}_n) = M_{cn},$$

and

$$(M_{fn} + B_{fn}) \cdot \bar{R}(A + \bar{Z}_n) = M_{fn}.$$

The two signals obtained here are used:

(a) to give the stop signal;
(b) to determine the direction of travel, up or down;
(c) to drive the "call registered" lamp; and
(d) to give a "door open" signal to the central control.

(a) The stop signal S_n will appear when the cabin is in zone n and there is a cabin call n; alternatively, it will appear when the cabin is in zone n and a floor call M_{fn} is present, provided that the cabin is

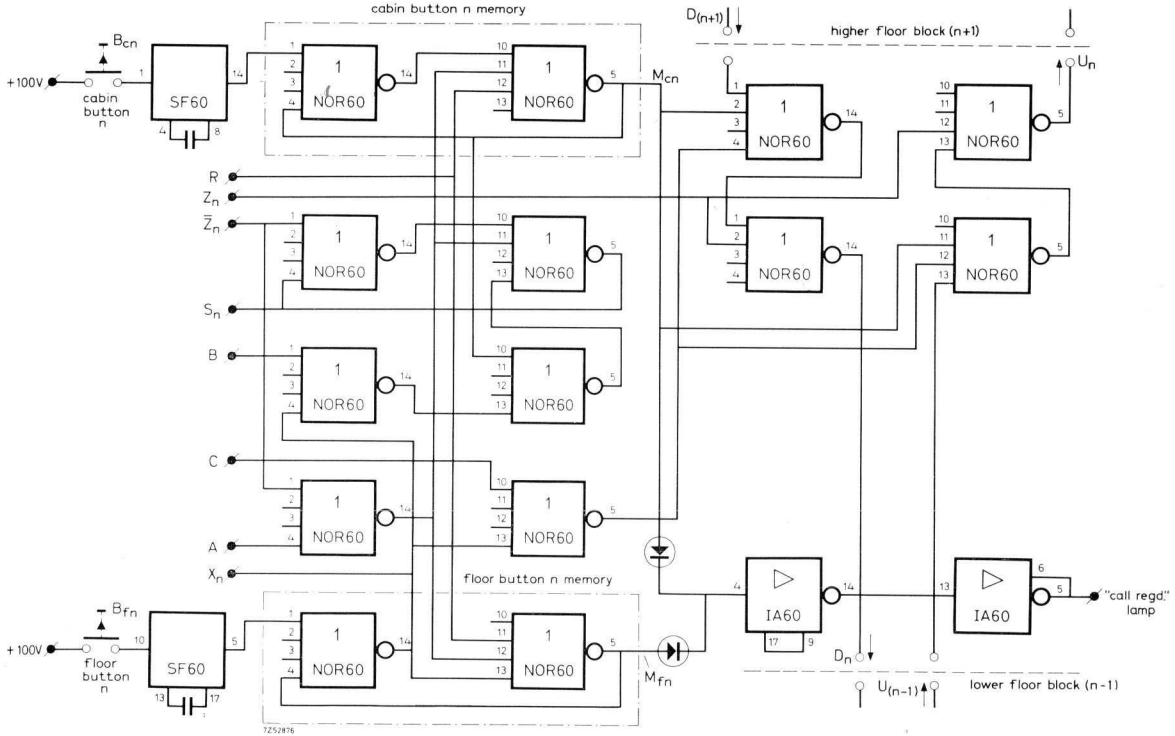


Fig. 13 10. Intermediate (nth) floor block.

moving down, or at least, no further up. The signal B will be 0 if either of the latter two statements is true. We can now formularize S_n (a memory function is involved):

$$(\bar{Z}_n + S_n)(M_{cn} + M_{fn}\bar{B} + B_{fn}\bar{B}) = S_n.$$

This special arrangement with the memory function gives the "braking zone inhibit" feature, meaning that S_n will only be 1 if the call signals M_{cn} or M_{fn} (or B_{fn}) are available *before* the car comes into zone n. If this order is interchanged S_n will remain 0. The result is that the cabin will not stop at a call given when the car has already entered that zone.

(b) The chain arrangement for up-and-down calls passes the up calls through the intermediate floor blocks to the top floor and the down calls to the first floor. Both signals leave the floor block (unless the car is at floor n), but only one will reach the top or first floor, as the other will be blocked at the floor where the cabin is at that moment. If the car is below floor n the down call will be blocked before reaching the first floor, but the up call will reach the top floor. If the car is above floor n it will be the other way around. (If the car passes floor n without stopping, the up call will change into a down call).

Thus an up call from floor n will be inserted in the "up chain" if the cabin is not at floor n and there is a call from the cabin for floor n or, alternatively, if there is a call from floor n and the blocking signal C is not present ($C = 1$ when the doors of the cabin are opened and this will block the floor calls as long as the doors remain open). This results in the following expression for an up call U_n from floor n:

$$[U_{n-1} + C_{cn} + (C_{fn} + B_{fn})\bar{C}]\bar{Z}_n = U_n.$$

and for a down call D_n:

$$[D_{n+1} + C_{cn} + (C_{fn} + B_{fn})\bar{C}]\bar{Z}_n = D_n$$

(c) A "call registered" lamp can be driven via a low power amplifier (2.IA60) and the special thyristor output stage given in Fig. 13.10.

(d) When the cabin is at floor n and the doors are closed (car not in use), pushing the floor button must result in opening the doors. For this reason the signal X is introduced (X_n becomes 0 on pushing n floor button):

$$\bar{M}_{fn} \cdot \bar{B}_{fn} = X_n.$$

(The stop signal S_n cannot be used for this purpose because it disappears as soon as the A signal has been given.)

Top Floor Block and First Floor Block

The top and first floor blocks (Fig. 13.11) are of simpler design than those for the intermediate floors; this is due to two reasons. Firstly, the car must always stop when it reaches either the top or the bottom; thus the stop signal S_n can be made equal to Z_n. Secondly, the up and down chains end at these floors. The down call signal D is taken directly from the first floor block and the up call signal U is taken from the top floor block. (Note that an up call is given here by $U = 0$, not by 1 as for other signals. Thus an up call signal is equivalent to $\bar{U} = 1$; similarly $\bar{D} = 1$ for down calls.)

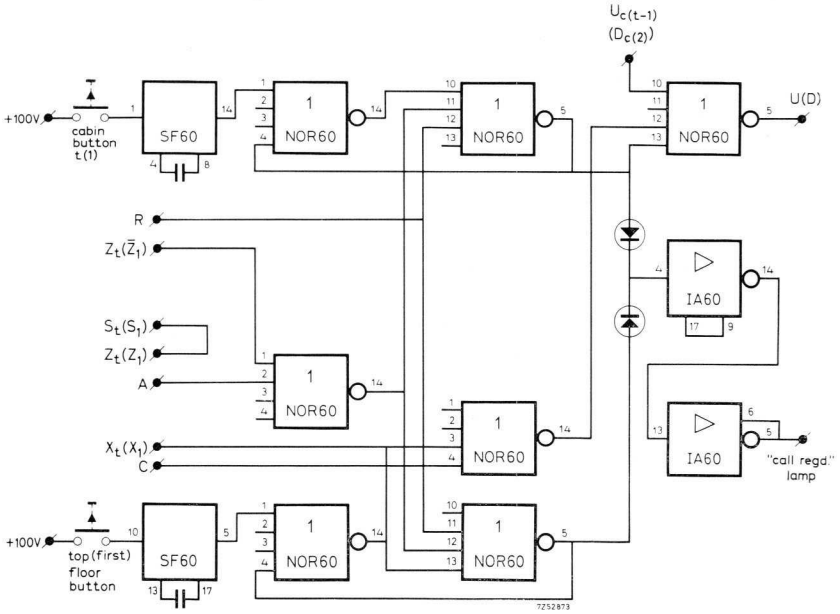


Fig. 13.11. Top and first floor block.

Up/Down Control

In up/down control circuit (Fig. 13.12) two memories are used to maintain the up or down direction. Referring to the diagram, signal U' is 1 if $\bar{U}$ and U_L and D_m are 0. $\bar{U}'$ is used to set memory U_m and reset signal A will reset U_m when the cabin starts to descend (A = O). The up limit switch UL will prevent setting of U_m, and signals U_m and the down memory D_m are interlocked.

Formularizing this, we obtain for U_m:

$$(U' + U_m)\,(\overline{\bar{A} \cdot \bar{U}'}) = U_m,$$

thus:

$$(\overline{D_m} \cdot \overline{UL} \cdot U + U_m)\,(A + \overline{D_m} \cdot \overline{UL} \cdot U)\,\bar{R} = U_m.$$

Similarly, for D_m

$$(\overline{U_m} \cdot \overline{DL} \cdot D + D_m)\,(A + \overline{U_m} \cdot \overline{DL} \cdot D)\,\overline{R} = D_m.$$

The Up signal which finally switches on the motor to raise the cabin is the signal U' (via double inversion and amplification). Similarly, the down signal is D'.

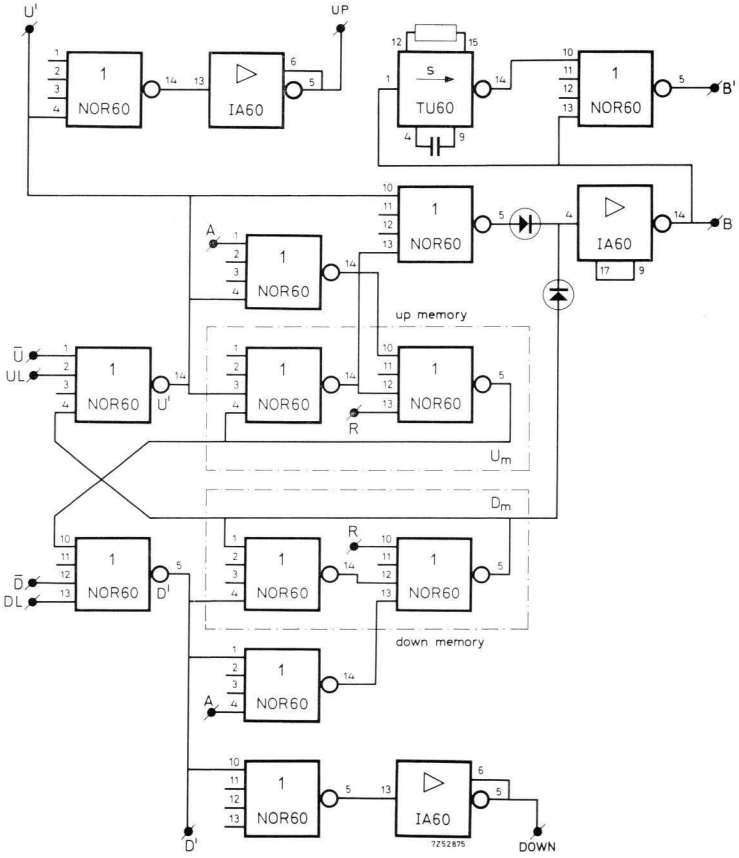


Fig. 13.12. Up/down control circuit.

A second important function is performed by the circuit: creation of the B signal. B is 1 when the cabin is ascending, thus preventing floor call stops on the way up (this is the characteristic of the Collective Down System). From the diagram it is clear that:

$$(U' + \bar{U}_m)\bar{D}_m = B,$$

or

$$(\bar{D}_m \cdot \overline{UL} \cdot U + \bar{U}_m)\overline{D_m} = B.$$

A pulse appears at B' as soon as B drops to zero.

Motor Control

Fig. 13.13 shows the motor control circuit. The complete list of stop signals is:

B'	end of up-direction
Z_t	top floor is reached
Z_1	first floor is reached
$S_2, S_3, \ldots S_{t-1}$	stop signals from the floor blocks

Any of the stop signals can be used to set the stop memory F. A pulse signal S' is obtained from the signals Z_t and Z_1 by using a timer unit

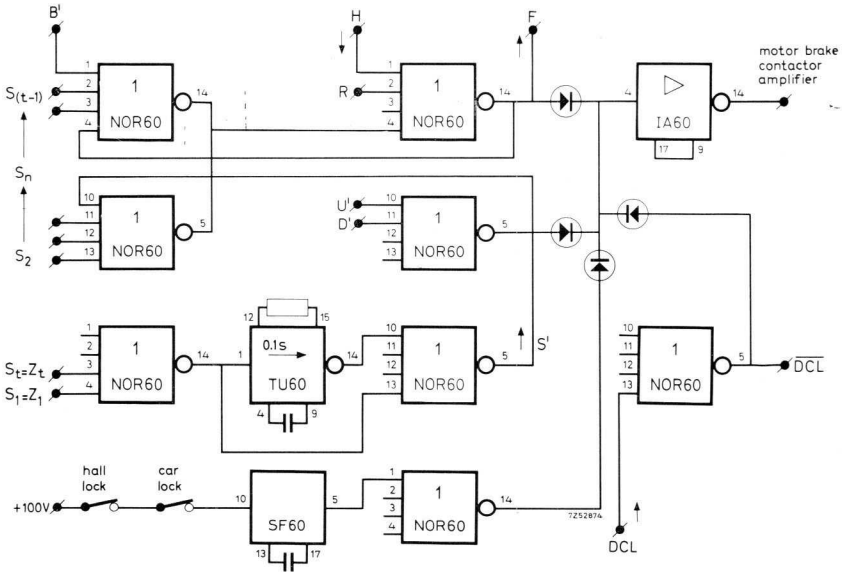


Fig. 13.13. Motor control circuit.

(otherwise it would not be possible to move the cabin from these positions). Reset H of the stop memory occurs when doors are closed again (see Door Control), thus the formula for the stop memory is:

$$(F + B' + S_2 + \ldots + S_{t-1} + S')\bar{H}\bar{R} = F.$$

The signal F is used to control the motor contactor and to start the door operation. Motor contactor is off (brake is on) when either a stop signal F is present; *or* hall lock is not closed; *or* car lock is not closed; *or* doors are not closed; *or* there is no up or down call. Thus:

$$F + \overline{\text{hall lock}} + \overline{\text{car lock}} + \overline{DCL} + \overline{U' + D'} = 1.$$

Cabin Door Control

The cabin door control circuit is shown in Fig. 13.14. The doors may be opened only when the motor is off. This condition is specified by signal $M = 1$ (e.g. from a switch operated by the motor contactor.) In the diagram of Fig. 13.14 two memories are given: one controls opening of the doors, the other closing of the doors. Opening continues until the "door opened" limit DOL is reached; closing until the "door closed" limit DCL is reached. Door movement can be controlled by two push-buttons in the cabin, while "safety edges" on the doors will open them at an obstruction. Calling the open memory signal O', the set signals are:

$$(\text{safety edge} + B_{do})\bar{M} + G.$$

Pushing the "door open" button when the motor is off ($M = 1$), gives the O' signal.

The signal G is the delayed signal T_2 (see Fig. 13.15). T_2 occurs when the doors must open automatically, the car having stopped at a certain floor (signal F from the stop memory) or a hall button having been pressed with the car at that particular floor (signals X_n and Z_n). Thus we have:

$$\overline{(\bar{X}_1 Z_1 + \ldots + \bar{X}_n Z_n + \ldots + \bar{X}_t Z_t + F)\bar{M}} = T_2.$$

G, derived from T_2 opens the doors after the cabin has had the opportunity to stop properly.

Reset of the O' memory occurs when Q' memory is set; *or* when door opened limit DOL is reached; *or* when the "door close" button is pushed:

$$Q' + \text{DOL} + B_{dc}\bar{G} = \text{reset } O'.$$

(The signal G is used here to prevent persons in the cabin closing the

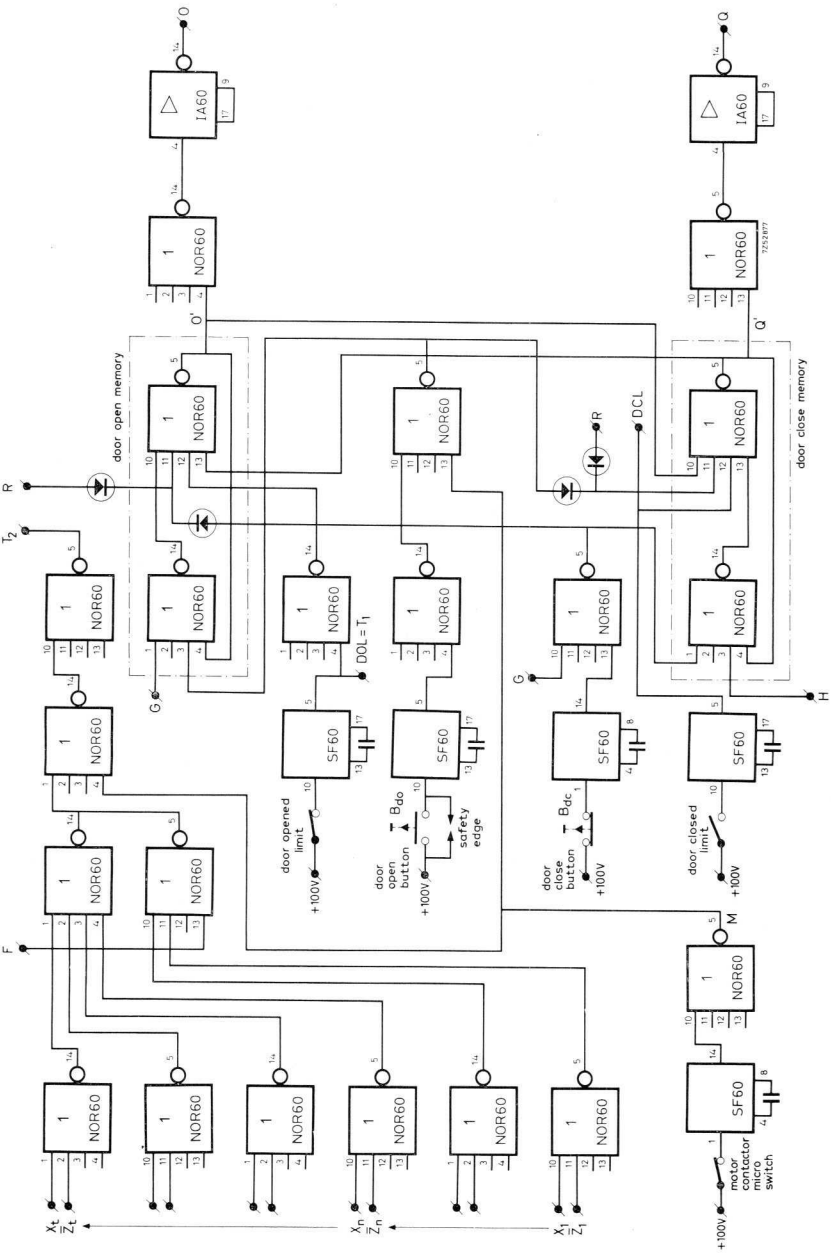


Fig. 13.14. Cabin door control circuit. The floor doors could be operated with signals O or Q, and Z_n.

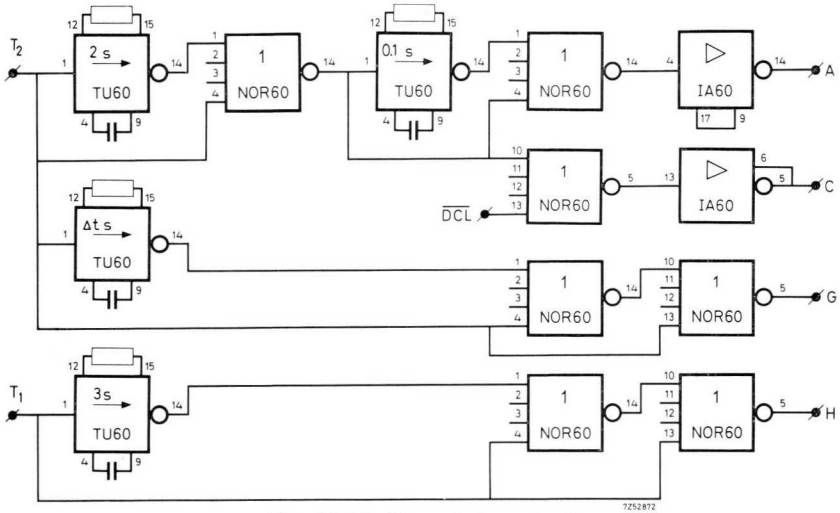


Fig. 13.15. Door timing circuit.

doors when these should remain open for a short time to pick up calls from the floor.)

A complete formula for O' is very hard to give because of the delay units incorporated in the circuit. The command for door closure Q' is obtained in a similar way to that described above for O'. Automatic closing occurs when doors have remained opened for a certain time (signal H).

Fig. 13.16 shows the timing diagram for the door control. A short 0.1 s

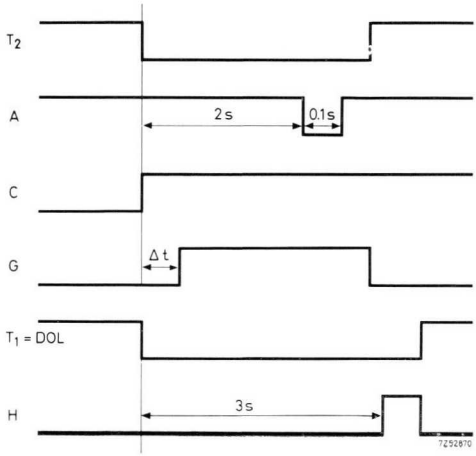


Fig. 13.16. Timing diagram door control.

reset pulse A is given about 2 s after the signal T_2 appears. Doors open with a delay of Δt after T_2, as a result of signal G. The blocking signal for hall calls, C, is available as soon as T_2 appears and until the doors are closed again. Doors close automatically when a *DOL* signal has been present for about 3 s. All delays can be adjusted by changing the external resistor or capacitor connected to the timer units.

Lamp and Relay Driver Unit

Conversion of the output signals into useful power signals may be done in a number of ways, but the method using thyristors shown by Fig. 13.17 has distinct advantages over other types; it is relatively inexpensive, and the heavy load currents can be supplied from a separate winding on the transformer secondary side, thus reducing the influence of output changes on the logic system.

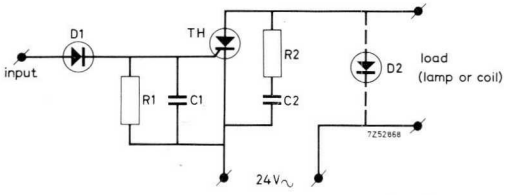


Fig. 13.17. Thyristor output circuit.

Limit Switches and Reset

Figs 13.18 and 13.19 show the circuits for the limit switches and for the reset, respectively. The signals *UL* and *DL* become 1 when the cabin is at the top and first floors respectively. The reset unit gives an $R = 1$ pulse as soon as the power supply $+24$ V for the circuit blocks is switched on. This results in resetting of all memories used in the electronic system.

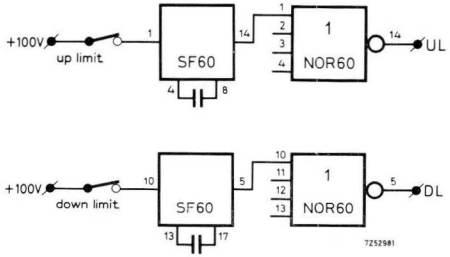


Fig. 13.18. Limit switch configuration.

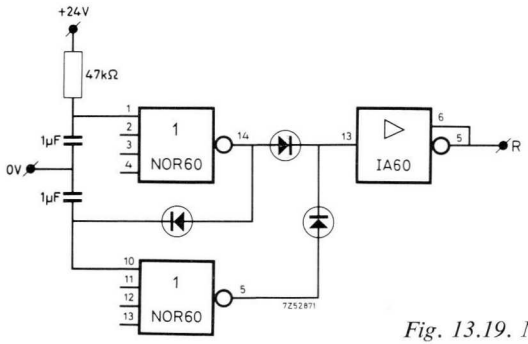


Fig. 13.19. Memory reset circuit.

13.4 Collective Up/Down Elevator

A collective Up/Down system has been built as a model using 60-Series circuit blocks. Only a brief description of the system is given here, as a full description would not be warranted in a book of this scope.

The design includes provisions for deceleration of the cabin upon its entering the slow zone of a floor at which it must stop, and means for control by an attendant. The system can be divided into five main units. These are given in the table below, together with the quantity and type of circuit blocks necessary for an elevator serving five floors. There will thus be three intermediate floor units and triple the quantity of circuit blocks quoted for the intermediate floor unit.

unit	quantity and type of circuit blocks per unit				
	2.NOR60	2.IA60	TU60	2.SF60	PA60
intermediate floor	11	2	—	$1\frac{1}{2}$	1
terminal (highest or lowest) floor	9	2	—	2	—
selector	17	—	—	1	—
central control	25	$3\frac{1}{2}$	1	$2\frac{1}{2}$	5
central adaptor	5	1	—	—	—

The central adaptor unit circuitry depends to some extent on the number of floors. Generally, a change in system requirements will affect only the central control unit; the floor blocks remain unchanged.

Two push buttons are present on every floor, one for "up" and one

for "down". A panel is provided in the cabin with a push button for each floor to be served. If a call is made by pressing a button, the call is stored and the button can be released.

Direction of the cabin movement is governed by several conditions. If the cabin is actually moving, call priority is determined by the direction of movement. The cabin will continue in a certain direction as long as calls exist "in front" of it (i.e. higher calls if ascending, lower calls if descending). If there are no such calls, the direction of travel will be reversed on reception of a call behind it. If there is both an up and a down call at one floor, priority will go to the call requesting the forward direction of travel. The cabin stops if it arrives at:

— a floor for which a cabin call has been placed;
— a floor where a floor call has been made requesting the same direction as prior to arrival;
— a floor beyond which there are no further calls.

A separate publication containing a complete description of the system is available (Application Information No. 845).

14 Specifications

This chapter contains the more important specifications of each of the units mentioned in the foregoing chapters. For the latest information, reference should be made to the Data Handbook System.

The following is a list of the units for which specifications are given. The number of the chapter in which the application of the unit is described is given in brackets.

Section 14.1 — The 60-Series units: 2.NOR60, 2.IA60, TU60, 2.SF60, PA60 (Chapter 2)

Section 14.2 — Input devices: IVSR, MPD, VSO, EPD, CSPD, LIP1, Thumbwheel Switches (Chapter 5)

Section 14.3 — Output unit: TTM (Chapter 9)

Section 14.4 — Mounting Chassis: Types 4322 026 38230, . . . 38240 and . . . 38250 (Chapter 4)

Section 14.5 — Power Supply Units: PSU60 and PSU61 (Chapter 3)

Section 14.6 — Mains Filter: MF 0.5 A (Chapter 6).

Where applicable, the specification has been divided into General Data, containing data on weight and dimensions and other general information, and Performance Data, concerning electrical performance.

14.1 The 60-Series Units

General Data. The circuit elements are housed in a transfer-moulded encapsulation, size A or size B (dimensions in mm are shown in Figs 14.1 and 14.2 respectively; inch equivalents are given in brackets). Pin numbering is moulded on both top and bottom of the unit, and all pins are also

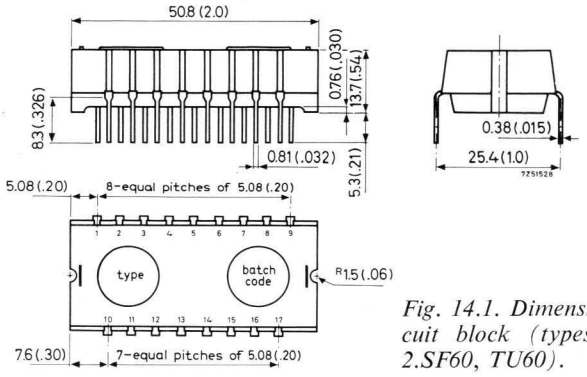


Fig. 14.1. Dimensions of the size A circuit block (types 2.NOR60, 2.IA60, 2.SF60, TU60).

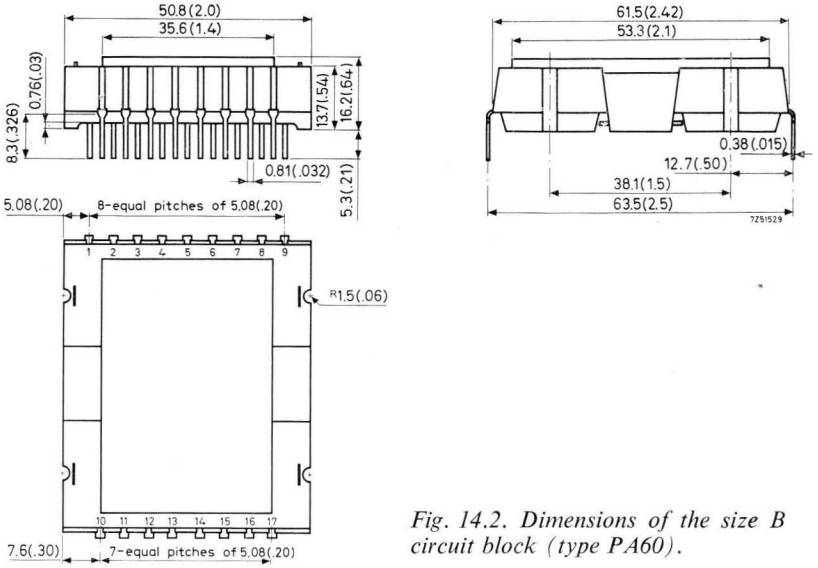


Fig. 14.2. Dimensions of the size B circuit block (type PA60).

accessible from the top of the unit to facilitate testing. The terminals are suitable for either soldering or mini-wrap connections. The weight of the size A unit is 30 g, that of the size B is 85 g (approximately).

The units conform to the standards set in IEC68 and MIL-STD-202C for the following tests: dry heat life, long-term damp heat (non-operating and operating), temperature cycle, vibration, shock, robustness of terminations, solderability and solder heat.

Ambient temperature limits are as follows: storage, —40 °C to +85 °C; operating, —10 °C to +70 °C.

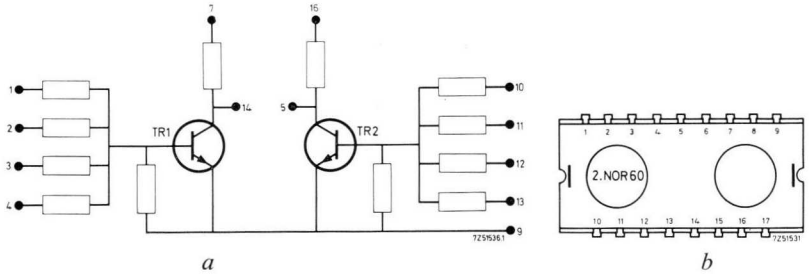
The supply voltage (V_s) is +24 V ± 25%, or +12 V ± 5% at reduced ratings.

The logic levels are as follows: for $V_s = 24$ V (nom.), the 0 level is between 0 V and +0.3 V, the 1 level between 11.4 V and V_s. For $V_s =$ 12 V (nom.), the 0 level is between 0 V and +0.3 V, the 1 level between 8.3 V and V_s.

The immunity to d.c. noise is as follows. With a 0 level input, a d.c. voltage of +1 V with respect to the 0 V line, applied to any one input (the other inputs floating), will not cause a change of output voltage. With a 1 level input, a variation of 2 V ($V_s = 24$ V nom.) or 0.25 V ($V_s = 12$ V nom.) will not cause a unit to change its output voltage.

Performance Data. The table opposite gives specifications common to all the units. Further details on individual units are given below.

2.NOR60 (Cat.No. 2722 008 00001). This unit has a size A black case. Fig. 14.3 shows the circuit (*a*) and the terminal locations (*b*) of the 2.NOR60; the terminals are listed below (n.c. = not connected).



a *b*

Fig. 14.3. The 2.NOR60. (a) circuit diagram; (b) terminal location.

terminal	connection	terminal	connection
1, 2, 3, 4	inputs, NOR1	10, 11, 12, 13	inputs, NOR2
5	output, NOR2	14	output, NOR1
6	n.c.	15	n.c.
7	for supply NOR1 (V_s)	16	for supply NOR2
8	n.c.	17	n.c.
9	0 V common		

Switching speed:

t_f = 1.25 μs (max.)
t_{fd} = 6.0 μs (max.)

The fall time t_f for the 2.NOR60 is defined as the time required for the output voltage V_{out} to change from 90% of its full value to 1 V, after application of a step input (see Fig. 14.4).

The fall delay time t_{fd} for the 2.NOR60 is defined as the time between the 1 V points of the negative-going input and output voltages of two cascaded units, each being loaded with 200 pF (see Fig. 14.5).

type	characteristics										limiting values of voltage				
	$V_s = 24\ V \pm 25\%$				$V_s = 12\ V \pm 5\%$				independent of V_s						
	supply current (mA) at V_s nominal	supply current (mA) at V_s maximum	input requirement (DU)	output capability (DU)	supply current (mA) at V_s nominal	supply current (mA) at V_s maximum	input requirement (DU)	output capability (DU)	input impedance (kΩ)	input current (mA) for 0 output	maximum supply voltage (V)	minimum supply voltage (V)	positive transients (V) on supply (10 μs duration)	positive voltages (V)	negative voltages (V)
2.NOR60	3.2	⩽ 4.2	1	6	1.6	< 1.8	1	4	90-30*	0.13-0.1*	30	0	10	90 V (input)	−8 (input)
2.IA60 per function as an LPA	10.9 10.9 (I_{load} 0 mA)	⩽ 14.0 ⩽ 114 (R_{load} 300 Ω)	2 2	20 140 300 Ω)	5.5 5.5 (I_{load} 0 mA)	⩽ 5.9 ⩽ 89.9 (R_{load} 150 Ω)	2 2	70 13 (150 Ω)	45 45	0.285 0.285	30	0	10	70 (pins 4.13) 4** (pin 8)	−16 (pins 3,13) −5 (pin 8)
TU60	6.9	10.1	1	5	1.9	2.1	1	3	90	0.125	30	0	10	10 (input)	−16 (input)
2.SF60														125 (pins 1,10)	−100 (pins 1,10)
PA60	18.8 (excl. I_{load})	< 26.2 (excl. I_{load})	1	> 30 Ω	15.1	< 28.8 (excl. I_{load})	1	> 13 Ω			30	0	10 (pin 6) 5 (pin 13)	100 (pin 1+) 5 (pin 3**)	−15 (pin 1+) −4.5 (pin 3**)

* four inputs in parallel

** via a resistor, minimum 500 Ω

+ pins 2 and 9 connected

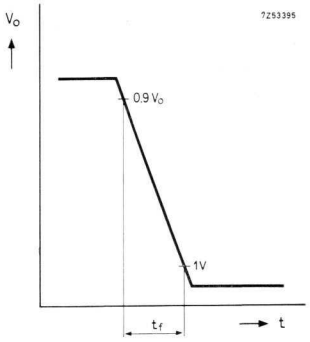
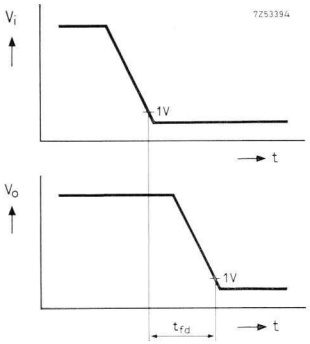


Fig. 14.4. Diagram illustrating t_f (for the 2.NOR60 and 2.IA60).



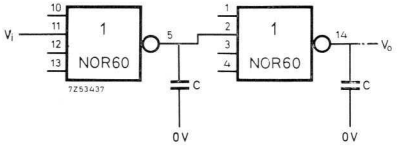
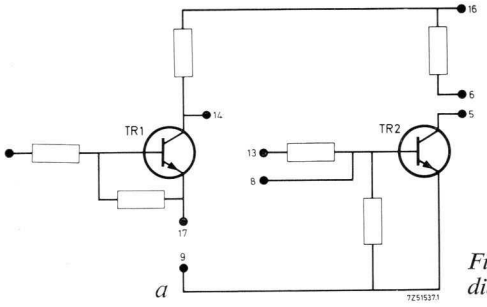


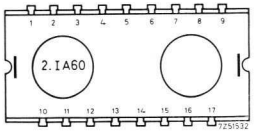
Fig. 14.5. Diagram illustrating t_{fd} (for the 2.NOR60 and 2.IA60).

2.IA60 (Cat.No. 2722 008 01001). This unit has a blue size A case.

Figs 14.6*a* and *b* show the circuit and terminal locations of the 2.IA60; terminals are listed below (n.c. = not connected).



a



b

Fig. 14.6. The 2.IA60. (a) circuit diagram; (b) terminal location.

terminal	connection	terminal	connection
1, 2, 3	n.c.	10, 11 ,12	n.c.
4	input, IA1	13	input, IA2
5	output, IA2	14	output, IA1
6	collector resistor, TR_2	15	n.c.
7	n.c.	16	supply (V_s)
8	base of TR_2	17	emitter of TR_1
9	0 V common		

Switching speed:

$t_f = 1$ μs (max.)
$t_{fd} = 3$ μs (max.)

The definitions of t_f and t_{fd} are the same as those given for the 2.NOR60 in the section above.

TU60 (Cat.No. 2722 008 03001). The TU60 has a size A red case. Figs. 14.7*a* and *b* give the circuit and terminal locations; the terminals are listed below (n.c. = not connected).

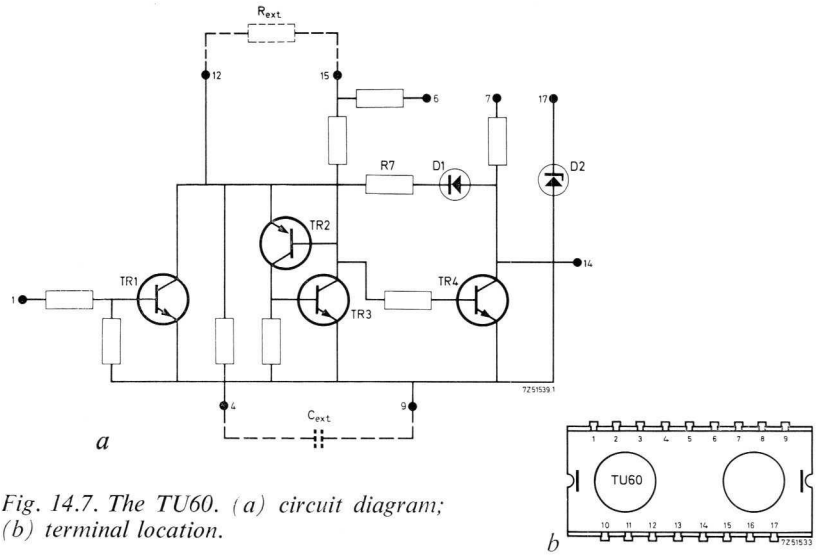


Fig. 14.7. The TU60. (a) circuit diagram; (b) terminal location.

terminal	connection	terminal	connection
1	input	10, 11	n.c.
2, 3	n.c.	12	ext. res.
4	ext. cap.	13	n.c.
5	n.c.	14	output
6	resistor *	15	ext. res.
7	supply (V_s)	16	n.c.
8	n.c.	17	diode *
9	0 V common		

* If the nominal supply voltage V_s is 24 V, interconnect terminals 6 and 7, and interconnect terminals 15 and 17. If V_s is 12 V, interconnect terminals 15 and 17 (do not interconnect terminals 6 and 17).

Switching speed:

$t_f = 1.25$ μs (max.)
$t_r = 6$ μs (max.)

The definition of fall time t_f for the TU60 is the same as that given above for the 2.NOR60.

The rise time t_r for the TU60 is defined as the time required for the output voltage V_{out} to change from 1 V to 90% of its full value, after application of a step input.

External resistor R_{ext} and capacitor C_{ext}:
R_{ext} should be not less than 100 kΩ and not more than 1 MΩ. C_{ext} should have a leakage current not exceeding 100 nA and its voltage rating should be at least 10 V.
Delay time and timing requirements:

$t_{delay} = R_{ext}C_{ext}$ (approximately)

set time, $t_{set} > 11.9$ ms per μF

recovery time, $t_{rec} > 11.9$ ms per μF

start inhibit before end of delay, $t_{st\ inh} > 18.9$ ms per μF

inhibit duration, $t_{inh} > 18.9$ ms per μF (a shorter t_{inh} gives a shorter delay)

Fig. 14.8 illustrates the terms used above.

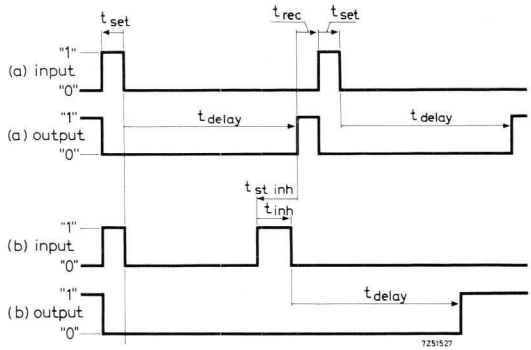


Fig. 14.8.

2.SF60 (Cat.No. 2722 008 02001). The 2.SF60 is housed in a size A green case. Figs 14.9*a* and *b* give the circuit and terminal locations of the 2.SF60. Terminals are listed below (n.c. = not connected).

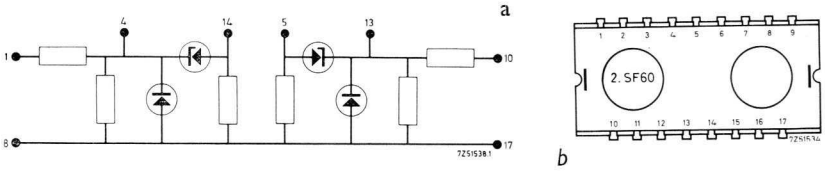


Fig. 14.9. The 2.SF60. (a) circuit diagram; (b) terminal location.

terminal	connection	terminal	connection
1	input, SF1	10	input, SF2
2, 3	n.c.	11, 12	n.c.
4	ext. cap., SF1	13	ext. cap., SF2
5	output, SF2	14	output, SF1
6, 7	n.c.	15, 16	n.c.
8	0 V common	17	0 V common, to be taken to central earth
9	n.c.		

Further characteristics (per filter):

input voltage to give 1 level output: $+100$ V $\pm$ 25%
input current: < 3.3 mA
input surge current peak: < 4.8 mA
output capability: 2 DU
contact bounce elimination time: 1.7 ms/μF of C.

Switching speed:

turn-on time: 41 ms per μF of C.

The maximum operating frequency with a 1 to 1 mark/space ratio for the circuit of Fig. 14.10*a* is 6.3 Hz divided by the capacitance of C (in μF). For the circuit of Fig. 14.10*b*, this is 11.08 Hz divided by the capacitance of C (in μF).

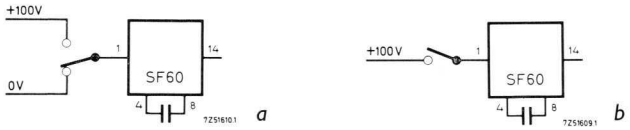
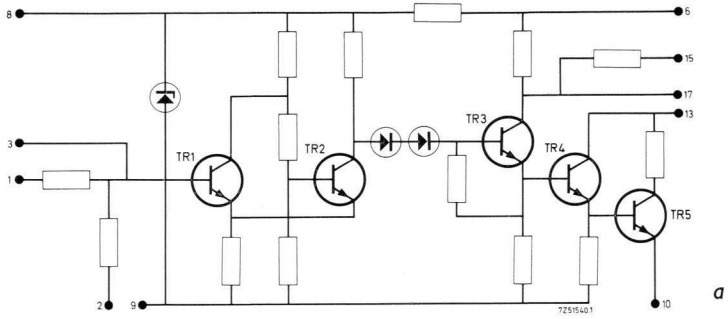


Fig. 14.10. Switch configurations.

PA60 (Cat.No. 2722 032 00031). The PA60 is housed in a size B blue case. Fig. 14.11 shows the circuit and terminal positions. The list below gives the terminal locations (n.c. = not connected).



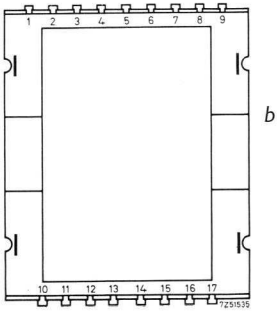


Fig. 14.11. The PA60. (a) circuit diagram; (b) terminal location.

terminal	connection	terminal	connection
1	input	10	0 V, output stage (see below)
2	base resistor of TR_1		
3	base of TR_1	11, 12	n.c.
4, 5	n.c.	13	output (load to be connected between 13 and supply)
6	supply (V_s): connect to 15		
7	n.c.	14	n.c.
8	zener diode	15	supply (V_s); connect to 6
9	0 V common		
		16	n.c.
		17	collector, TR_3

Terminal 10 facilitates the connection of a 0 V load supply line which is separated from the 0 V logic supply line up to the power supply unit; in this way common wire impedance is avoided. If a second power supply unit is used for the PA60, common impedance with the 0 V logic supply line should be avoided in the connecting wire necessary between terminal 9 (0 V logic supply) and terminal 10 (0 V supply of PA60).

If the input (terminal 1) is driven by a standard 1 level (e.g. from a NOR unit), interconnect terminals 2 and 9.

If the nominal supply voltage V_s is 12 V, connect a resistor of 330 Ω between terminals 6 and 8, and a resistor of 1.5 kΩ between terminals 15 and 17, both resistors to be $\pm$ 5%, $\frac{1}{4}$ W types.

The metal centre part of the case is a heat sink. It should not be touched by electrical conductors.

Switching speed:

$$t_f = 1.0\ \mu s\ (\text{max.}) \qquad t_r = 5.0\ \mu s\ (\text{max.})$$

The fall time t_f for the PA60 is defined as the time required for the output to change from 90% to 10% of its full value, after application of a step input, at a supply voltage $V_s = 30$ V and a load resistance of 30 Ω (see Fig. 14.12).

The rise time t_r for the PA60 is defined as the time required for the output to change from 10% to 90% of its full value, after application of a step input, at a supply voltage $V_s = 30$ V and a load resistance of 30 Ω (see Fig. 14.13).

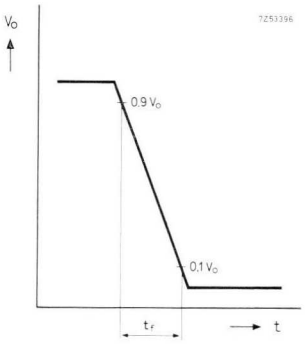


Fig. 14.12.

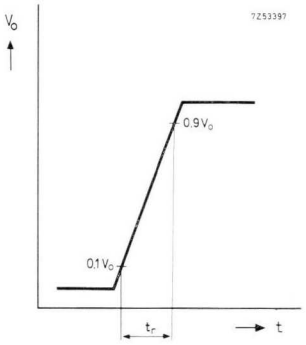


Fig. 14.13.

Further characteristics of the PA60 are listed below.

For an input signal applied at terminal 1, switching on current in the load requires an input voltage of 8 V, and a current of 75 μA with terminals 2 and 9 connected. Switching off requires the input voltage to be less than 2.5 V.

For an input signal applied at terminal 3, switching on of the load current requires an input voltage of 1.6 V via a minimum resistance of 500 Ω, and an input current of 75 μA (terminals 7 and 9 interconnected) or 30 μA (terminals 2 and 9 not interconnected). Switching off requires the input voltage to be less than 0.65 V. The on-off input voltage difference in this case (with a source resistance of less than 56 kΩ) is greater than 0.32 V.

14.2 Input Devices

14.2.1 Iron Vane Switched Reed, IVSR (Cat.No. 2722 031 00011)

General Data

The dimensions of the IVSR are given in Fig. 14.14.
Weight: 20 g (approx.)
Minimum distance between housings: 36 mm mounted side by side, or 60 mm stacked one above the other.
Connections: 0.25 in. "Fastons", or by soldering.

Performance Data

The data given are based upon a movement of a mild steel vane 30 mm × 10 mm × 4 mm, placed centrally in the gap, in longitudinal direction.

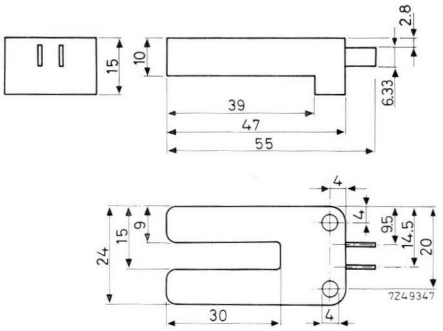
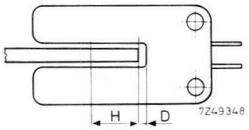


Fig. 14.14. The IVSR dimensions

The operating distance (D) is the distance between the front edge of the vane and the rear of the gap at which the reed switch opens; $D = 4 \pm 3$ mm (see Fig. 14.15).

The hysteresis (H) is defined as the distance between the vane position at which the reed switch opens and that at which the reed switch closes; $H = 10 \pm 3$ mm.

Fig. 14.15. Illustrating D and H.



Load switching capacity (non-inductive)	$\leqslant$ 1.2 VA
Maximum voltages	$\leqslant$ 32 V d.c., $\leqslant$ 50 V a.c.
Current switching capacity (non-inductive)	$\leqslant$ 0.1 A d.c.
Switching frequency	$\leqslant$ 100 Hz
Contact resistance, measured at 10 mV (open circuit)	$\leqslant$ 150 mΩ
Contact capacitance	$<$ 5 pF
Insulation resistance, measured at 250 V d.c. (open circuit)	$\geqslant 10^8$ Ω
Test voltage during 1 min (open circuit)	500 V d.c.
Permissible operating temperature range	-25 to $+70$ °C
Permissible storage temperature range	-40 to $+85$ °C

14.2.2 Magnetic Proximity Detector, MPD (Cat.No. 2722 031 00031)

General Data

Fig. 14.16 shows the dimensions of the MPD. Connections can be made by 0.25 in. "Fastons".

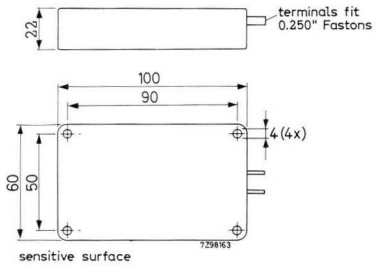


Fig. 14.16. The MPD dimensions.

Mounting arrangements are as follows. The minimum distance between two units side by side to give a change in detection range of < 0.1 mm is 170 mm, with the sensitive surfaces in the same direction; or 155 mm, with these surfaces in opposite directions. Any point of the unit must be no less than 200 mm from ferrous objects to avoid the detection range being altered by more than 0.1 mm.

Performance Data.

The data given below are based upon the use of a mild steel (free cutting quality) reference plate 76 mm $\times$ 76 mm $\times$ 1.9 mm.

Detection range (distance between sensitive surface and front face of reference plate for switch-on, at frontal approach)	$\geqslant$ 17 mm at 20 °C
Hysteresis (distance between "switch on" and "switch off" points, at frontal approach)	$\leqslant$ 6 mm at 20 °C
Repeatability with a supply voltage of 30 V and a current of 7.5 mA after 10 000 operations	detection range and hysteresis unchanged
after one million operations	possible decrease of detection range and hysteresis appr. 0.4 mm
Change of "switch on" point with a temperature variation from +25 or to +70 °C	$\leqslant$ 0.5 mm
Change of hysteresis with a temperature variation from +25 °C to +70 °C	$\leqslant$ 0.75 mm

Fig. 14.17 gives a typical detection graph for the passage of the reference plate. With the plate approaching from the opposite side, the curves are a mirror image of those shown.

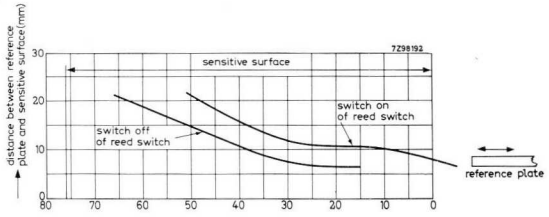


Fig. 14.17. Typical detection curves for the MPD.

Load switching capacity	$\leqslant$ 25 W
Voltage switching capacity	$\leqslant$ 200 V d.c.
Current switching capacity	$\leqslant$ 1 A d.c.
Switching frequency	$\leqslant$ 100 Hz
Contact resistance (initial)	$\leqslant$ 100 mΩ
Operating temperature range	-25 to $+70$ °C
Storage temperature range	-25 to $+85$ °C

14.2.3 Vane Switched Oscillator, VSO (Cat.No. 2722 031 00001)

General Data

Fig. 14.18 gives the dimensions of the VSO. The terminal arrangement is as follows:

Terminal 1: supply, negative
Terminal 2: supply, positive
Terminal 3: output, positive
Terminal 4: output, negative

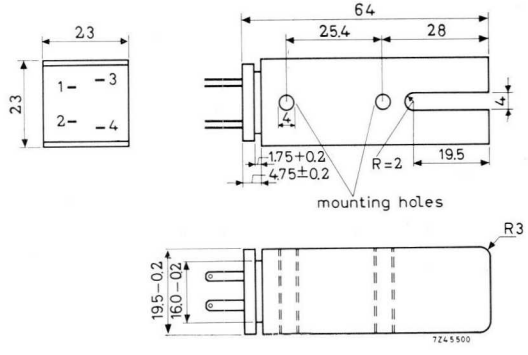


Fig. 14.18. The VSO dimensions

The weight of the unit is 42 g. Stacking of units is permitted. Connections can be made by 0.11 in. "Fastons", or by soldering. A cable anchoring cover (not shown) is supplied with each VSO.

The vane can be of any metal. For aluminium, the minimum dimensions are 8 mm wide by 30 μm thick. Alternatively, a disc with holes of the dimensions indicated in Fig. 14.19 may be used instead of a vane.

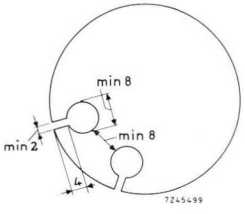


Fig. 14.19. Disc vane.

Performance Data

The data given below are based on a movement of an aluminium vane 50 mm × 50 mm × 2 mm in longitudional direction. The operating distance *D* (see Fig. 14.20) is the distance at which the output just drops to zero (measured from the centre of the hole nearest to the gap).

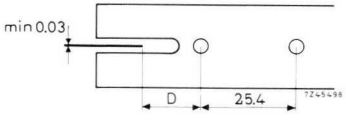


Fig. 14.20. Illustrating distance D.

Hysteresis is defined as the distance between the vane position at which oscillation ceases and that at which oscillation starts.

Operating distance *D* open circuit	14.6 ± 1.5 mm
Hysteresis (open circuit)	< 1 mm
Variation of *D* with supply voltage	
at undervoltage of 5%	± 0.06 mm
at overvoltage of 5%	0.06 mm
Decrease of *D* with temperature (from −25 to +85 °C)	< 2.7 mm
Variation of *D* with time (at T_{amb} = 25 °C and V_{supply} = 12 V ± 1%; reference point half the unloaded output voltage of VSO without vane)	< 0.02 mm
Supply voltage	+12 V ± 10% +6 V ± 10% and −6 V ± 10% (with common 0 V)

Current drain	12 mA $\pm$ 10%, in both oscillating and non-oscillating condition
Output voltage (open circuit, isolated from the supply)	5.75 V $\pm$ 15%
Maximum permissible voltage between terminals 1-2 and 3-4	100 V
Output impedance (without vane)	4.1 kΩ $\pm$ 10%
Maximum detection frequency	1 kHz
Permissible noise (over supply lines)	$< 100\ mV_{p-p}$
Ambient temperature range	
operating	-25 to $+85$ °C
storage	-40 to $+85$ °C

14.2.4 Electronic Proximity Detector, EPD (Cat.No. 2722 031 00021)

General Data

Fig. 14.21 gives the dimensions of the EPD; its weight is 120 g. The terminals are arranged as follows:

Terminal 1: output
Terminal 2: supply, positive
Terminal 3: supply, negative

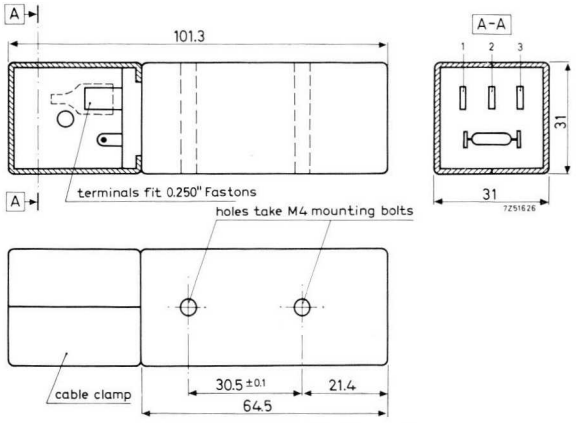


Fig. 14.21. The EPD dimensions.

Mounting requirements are as follows. Minimum clearance between sensitive face of EPD and metallic surrounding should be 30 mm. Minimum spacing required between two detector axes with sensitive faces

in the same plane is 60 mm. Minimum spacing required between two reference objects to give discrete detection is 50 mm.

Connections can be made with 0.25 in. "Fastons", or by soldering.

Performance Data

The data below are based on movement of a rectangular mild steel plate, 50 mm × 25 mm × 1 mm (the reference object). The "sensitive surface" is the surface at the opposite end of the EPD to the terminals; the "axis" a line perpendicular to the centre of the sensitive surface; the "operating point" the point at which the output voltage of the EPD is reduced to 100 mV (moment of detection); the "operating distance" x the distance from the leading edge of the reference (detecting) object at the operating point to the axis; the "detection range" y the distance between the object and the sensitive surface.

Figs 14.22 and 14.23 show y as a function of x for the passage of detecting objects of mild steel and aluminium respectively. In Fig. 14.24, y is given as a function of object width for mild steel and aluminium objects, which approach the centre of the sensitive surface, perpendicularly to it.

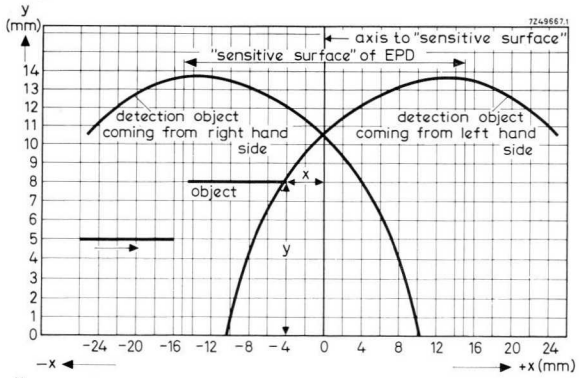


Fig. 14.22. y as a function of x; mild steel object.

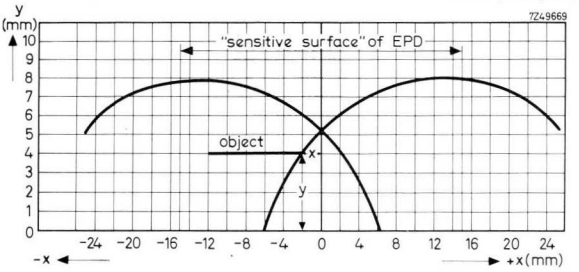


Fig. 14.23. y as a function of x; aluminium object.

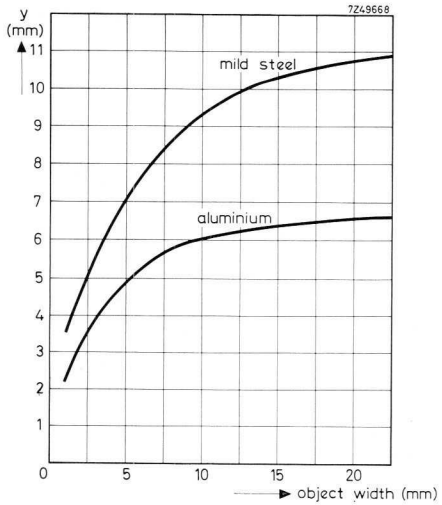


Fig. 14.24. y as a function of object width.

Fig. 14.25 shows the output voltage as a function of y for the mild steel reference object. Upon frontal approach of the object to the sensitive surface, V_o will change from over 11 V to 100 mV within 1 mm of the position at which V_o starts to change.

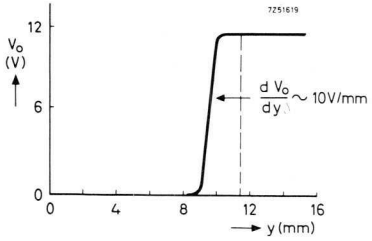


Fig. 14.25. Output voltage as a function of y.

Supply voltage (V_s)*	12 V d.c. $\pm$ 5%; abs.max. 15 V (destructive at $T_{amb} \geqslant 40$ °C)
Consumed current (nominal value)	16 mA
Output voltage, no object being detected (approx.)	$V_s - 0.5$ V
Output resistance	
no object being detected	680 Ω $\pm$ 10%
object being detected	3.3. kΩ

* Wrong polarity will damage unit.

Output voltage range for 0 mm hysteresis	100 mV to 11 V
Minimum load resistance	1 kΩ
Maximum detection frequency	1 kHz
Noise (over supply lines)	< 10 mV
Ambient temperature range	
operating	—25 to +85 °C
storage	—40 to +85 °C
Change in y at supply voltage variation of ± 5%	± 0.1 mm (y = 10 mm)
Change in y at temperature change of 100 deg C (—25 °C to +85 °C)	< 2 mm (y = 10 mm)

14.2.5 Photo-Electric Detector, CSPD (Cat.No. 2722 031 00041)

General Data

Fig. 14.26 shows the dimensions. The weight of the unit is 130 g approximately. The CSPD can be used in conjunction with the lamp unit 1 MLU (Cat.No. 2722 031 00051) whose dimensions are the same as those of the CSPD. The IMLU uses a 6 V, 3 W lamp (socket type B15d).

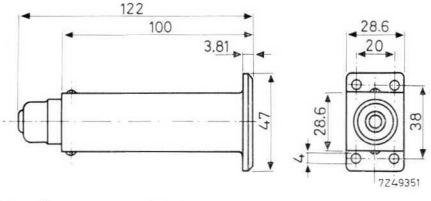


Fig. 14.26. The CSPD dimensions.

Performance Data

Dark value (in total darkness)	> 10 mΩ
Light value (at 1000 lx)	< 300 Ω
Recovery rate at falling light intensity	> 200 kΩ/s
Maximum permissible voltage	150 V
Maximum dissipation at 40 °C	0.2 W
Maximum capacitance	6 pF
Maximum switching frequency (typical)	6 Hz
Maximum operating distance when used with lamp unit 1 MLU	1 m
Permissible operating temperature range	—10 °C to +50 °C (max. dissipation 0.1 W at +50 °C)
Permissible storage temperature range	—20 °C to +60 °C

14.2.6 Light Interruption Probe, LIP1 (Cat. No. 2722 031 00081)

General Data

The dimensions of the LIP1 are shown in Fig. 14.27. Its weight is 170 g approximately.

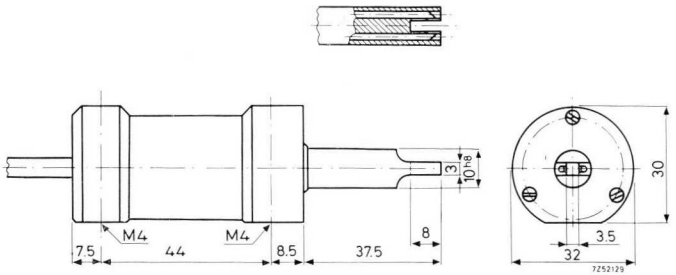


Fig. 14.27. The LIP1 dimensions.

A four-core colour-coded shielded cable is provided to make the electrical connections:

white lead : $+V_s$
yellow lead : $+V_s$ via resistor of 36 Ω ± 2% (supplied)
brown lead : 0 V of supply
green lead : output
cable shield : to central earth point

Performance Data

For the data below, use was made of a metal disc with slots, the slot width, equal to the distance between slots, being 1 mm. The slot length was 5 mm.

Maximum 0 level (no object)	+1.25 V	unloaded output
Minimum 0 level (no object)	0 V	
Minimum 1 level (with object)	+ 4.8 V	
Maximum 1 level (with object)	$+V_s$	
Detection frequency	> 10 kHz	
Maximum output impedance		
no object in gap	2.1 kΩ	
light beam completely intercepted	1.1 kΩ	
Supply voltage	+12 V ± 5%	
Supply current (nominal)	180 mA	
Operating temperature range	0 °C to +50 °C	
Storage temperature range	−10 °C to +70 °C	

14.2.7 Thumbwheel Switches

The thumbwheel switches (see Fig. 14.28) have been developed for use as pre-set devices in digital control systems. Figs 14.29*a* and *b* show the major dimensions of the two styles, Façade Mounting (type FM) and Block Mounting (BM). The housings are of shock-resistant high-grade plastic. Tin-plated copper terminals (suitable for soldered or wire-wrap connections) and type 721 alloy copper beryllium contacts are used. The contacts of all the switches break before make.

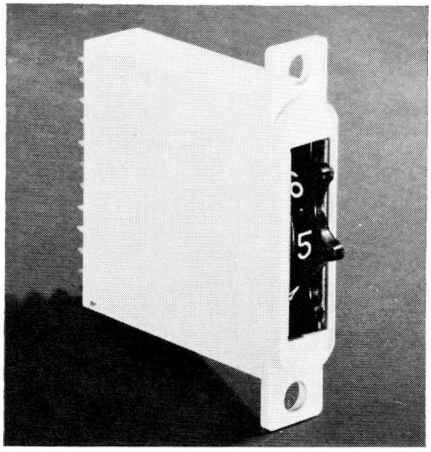


Fig. 14.28. External appearance of a thumbwheel switch.

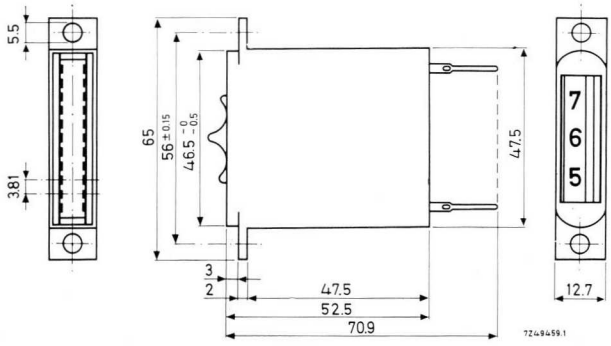


Fig. 14.29a. Dimensions of type FM thumbwheel switches

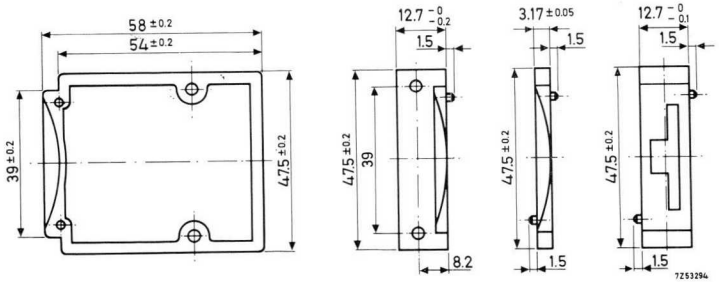


Fig. 14.29b. Dimensions of type BM switches

Type FM switches can be mounted in panels of up to 4 mm thickness by means of mounting façades and the screws and washers supplied (see Fig. 14.30). If the panel thickness is less than 4 mm, additional washers must be used between the panel and the switch. Fig. 14.31 shows six of the front mounting façades (façades giving facilities for mounting up to 10 switches are available). The dimensions of the necessary panel holes are indicated in Fig. 14.32.

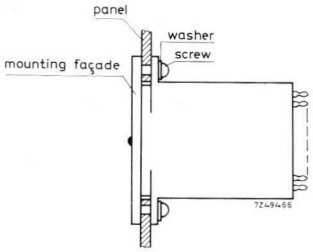


Fig. 14.30. Mounting of type FM.

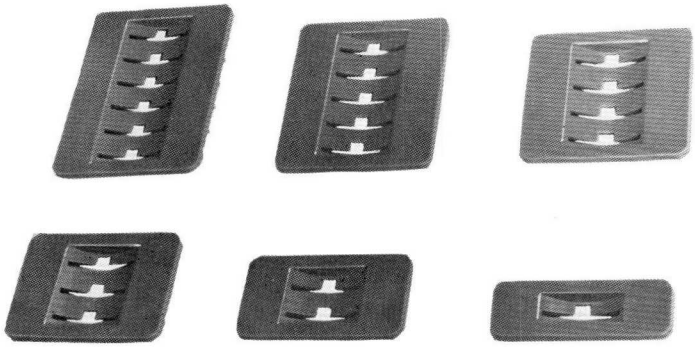


Fig. 14.31. Six front mounting façades (type FMF).

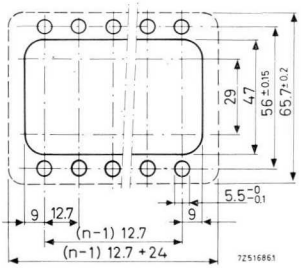


Fig. 14.32. Façade dimensions; n = number of switches to be accommodated.

Type BM switches, which do not require a front façade, can be mounted by means of mounting brackets and 3 mm tie bolts.

The thumbwheel switches available, together with their catalogue numbers, are given on p. 223. The type abbreviation is prefixed with the letters "BM" for switches of this type.

Listed below are the catalogue numbers of the front mounting façades (FMF) for the FM type switches.

type abbrev.	number of switches per façade	last 5 digits of cat.no. (4311 027 . . . . .)
FMF1	1	80598
FMF2	2	80608
FMF3	3	80618
FMF4	4	80628
FMF5	5	80638
FMF6	6	80648
FMF7	7	81162
FMF8	8	81172
FMF9	9	81182
FMF10	10	81192

14.3 Output Unit (Cat.No. 2722 032 00001)

The Thyristor Trigger Module (TTM) output unit contains a blocking oscillator circuit, potted in epoxy resin, inside a high-grade plastic case (Fig. 14.33). Connections can be made with 0.25 in. "Fastons". The weight of the unit is 280 g approximately. Terminals of the TTM are shown in Fig. 14.34*a* and the dimensions in Fig. 14.34*b*. The terminals are listed below.

switch type	type abbrev.	index	last 5 digits of cat.no. (4311 027 . . . . .)	
			FM type	BM type
Decimal and two-position:				
10 position 2 pole numerical	10P2C	0-9	82201	82521
10 pos. 1 pole num.	10P1C	0-9	82321	82401
2 pos. 4 pole sign	2P4+—	+, —	82231	82641
2 pos. 2 pole sign	2P2+—	+, —	82341	82601
2 pos. 4 pole sign	2P4×÷	×, ÷	82311	82651
2 pos. 2 pole sign	2P2×÷	×, ÷	82351	82611
2 pos. 4 pole sign	2P401	0,1	82281	82661
2 pos. 2 pole sign	2P201	0,1	82361	82501
2 pos. 4 pole sign	2P4MA	M, A[1]	82291	82671
2 pos. 2 pole sign	2P2MA	M, A[1]	82371	82621
2 pos. 4 pole sign	2P4AvAr	Av, Ar[2]	82301	82681
2 pos. 2 pole sign	2P2AvAr	Av, Ar[2]	82381	82631
Binary decoding switches:[3]				
1248 negative logic	1248N	0-9	82221	82391
1248 positive logic	1248P	0-9	82251	82411
1242 negat. logic (Berkeley)	1242N	0-9	82211	82711
1242 posit. logic (Berkeley)	1242P	0-9	82241	82721
1248 negative logic[4]	1248N/C	0-9	82451	82541
1248 positive logic[4]	1248P/C	0-9	82431	82551
1242 (jump at 8) negative logic[4]	1242N/C	0-9	82441	82571
1242 (jump at 8) positive logic[4]	1242P/C	0-9	82421	82581
Binary coding switches:				
1248	1248C	0-9	82271	82531
1242 (jump at 8)	1242C	0-9	82261	82701
1248[5]	1248C/C	0-9	82471	82561
1242 (jump at 8)[5]	1242C/C	0-9	82461	82591
1248[6]	1248S	0-9	82511	

[1] "Start" and "Stop" for Latin-based languages
[2] "Forward" and "Reverse" for Latin-based languages
[3] Including four BAX13 diodes and one 12 kΩ resistor
[4] Switch decodes 9-complement of decimal digit on thumb-wheel
[5] Switch encodes 9-complement of decimal digit on thumb-wheel
[6] The four wiper contacts are brought out to terminals; with external diodes, the switch could be used as a decoder.

Terminal 1 :	+12 V
Terminals 2 and 3:	to be interconnected.
Terminals 4 and 5:	interconnected, except for control with a switch that is normally open
Terminal 6:	0 V (supply)
Terminal 7:	"safety-catch" input
Terminal 8:	gate, thyristor 1
Terminal 9:	cathode, thyristor 1
Terminal 10:	gate, thyristor 2
Terminal 11:	cathode, thyristor 2

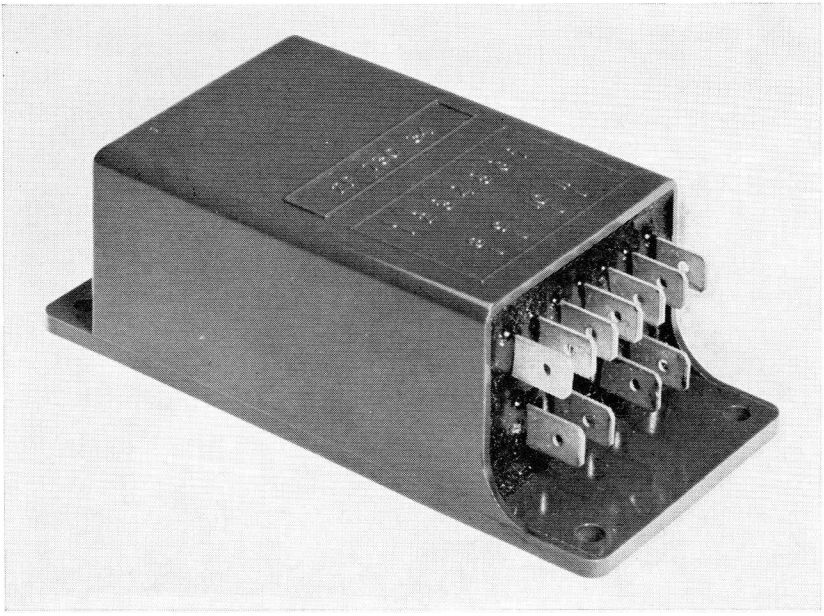


Fig. 14.33. The Thyristor Trigger Module, TTM.

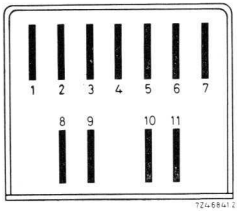


Fig. 14.34a. The TTM terminal positions.

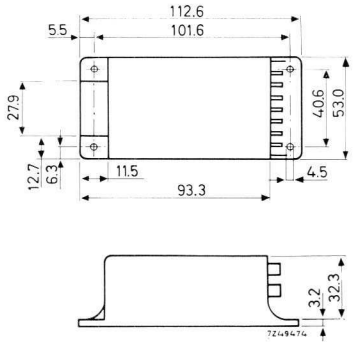


Fig. 14.34b. The TTM; dimensions.

Performance Data

Supply voltage	$+12$ V $\pm$ 5%
Supply current	35 mA nominal
Operating temperature	-25 °C to $+85$ °C
Storage temperature	-40 °C to $+85$ °C
Current from control terminals (typical values)	
terminals 4/5 to 6:	1.5 mA
terminals 6 to 7:	35 mA (I_{peak} = 57 mA)
Number of outputs (output voltages are in phase)	2, isolated
Isolation of outputs	500 V_{rms}
Voltage	$<$ 10 V d.c.
Current (one output loaded with 16 Ω, the other short-circuited)[1]	250 mA
Impedance (both outputs or one output loaded with 16 Ω)	25 Ω
Nominal pulse frequency (both outputs loaded with 16 Ω)	2.3 kHz approx.
Pulse width at 3 V (both outputs loaded with 16 Ω)	$>$ 20 μs
Pulse rise time	$<$ 0.5 μs

"Safety-catch" operation is possible with the TTM (terminal 7). This gives a safeguard against spurious trigger pulses. If safety-catch operation is

[1] Short-circuiting of both outputs will not impair the reliability of the TTM and will not damage the power supply.

employed the TTM is controlled via two control terminals requiring phase opposition of the control voltages; see Fig. 14.35. If an interference pulse appears at both control lines in phase, inadvertent triggering will be eliminated to a very large extent. It should be noted that the employment of safety-catch operation introduces a switching-time delay of the TTM of approximately 400 μs.

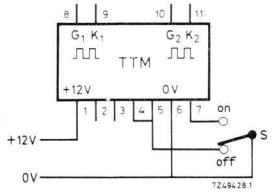


Fig. 14.35. Safety-catch operation. Required capacity of switch S is 50 mA.

14.4 Mounting Chassis

14.4.1 Chassis Cat.Nos 4322 026 38230 and 4322 026 38240

The above types are designed for use in 19 in. racks. They can accommodate standard printed wiring boards of the dimensions shown in Figs 14.36 and 14.37. The height, depth and length of the chassis are 133 mm $\times$214 mm$\times$444 mm. The weight is 3 kg approximately. The minimum spacing between boards is 19.05 mm, and this can be increased in steps

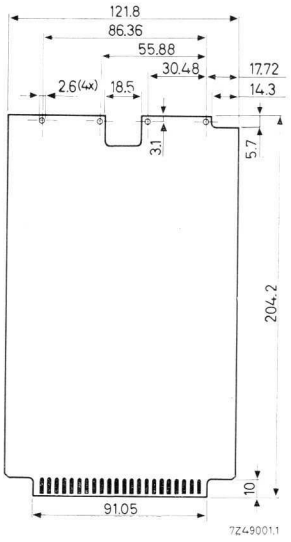


Fig. 14.36. Dimensions of the printed wiring board to fit chassis type 4322 026 38230. Thickness is 1.6 ± 0.2 mm.

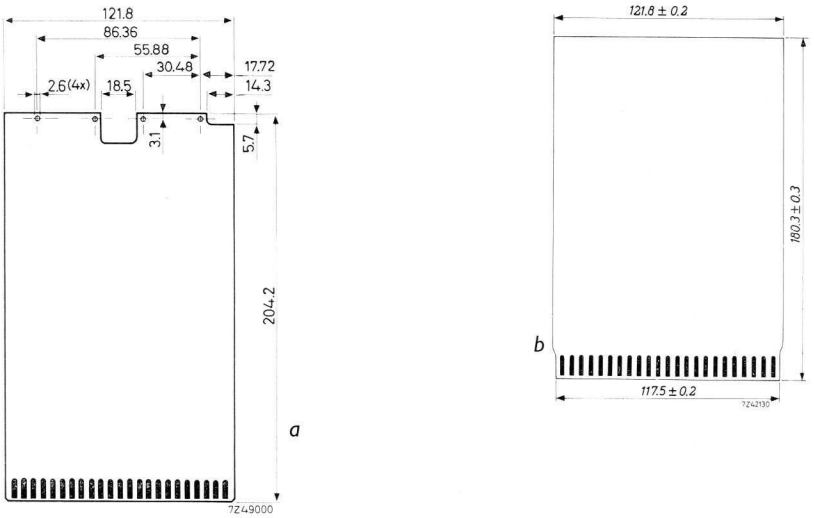


Fig. 14.37. Dimensions of printed wiring boards to fit chassis type 4322 026 38240; (a) standard. (b) short (chassis depth adjusted by using extra holes in side panels). Board thickness: 1.6 ± 0.2 mm.

of 6.35 mm. Compatible connectors and boards are given in the Table on p. 31. The chassis are of anodized aluminium.

The following accessories for the chassis are available. Set of ten numbering strips and holders for a single chassis (Cat.No. 4322 026 38410) and between two chassis (Cat.No. 4322 026 38240); aligning kit for chassis type 3422 026 38230 (Cat.No. 4322 026 38430) and for chassis type 4322 026 38240 (Cat.No. 4322 026 38440); set of two mounting brackets with screws and nuts for fixing a single chassis to a 19 in. rack (Cat.No. 4322 026 38450); extender boards for chassis 4322 026 38230 (Cat.No. 4322 026 44290) and for chassis 4322 026 38240 (Cat.No. 4322 026 03910) (these extender boards facilitate the testing of printed wiring assemblies outside the chassis). An extractor is available to facilitate extraction and locking of boards with the above dimensions. A set of 25 extractors, consisting of holder, text strip, locking lever, spring and four rivets, has the catalogue number 4322 026 38400.

14.4.2 Chassis Cat.No. 4322 026 38250

This type of chassis also fits the 19 in. rack. It can accommodate miniature

boards of the dimensions shown in Fig. 14.38. Height, depth and width of the chassis are 130 mm × 123 mm × 436 mm. The weight is 2 kg approximately. Minimum spacing between boards is 19.05 mm. The material is NiCr plated steel.

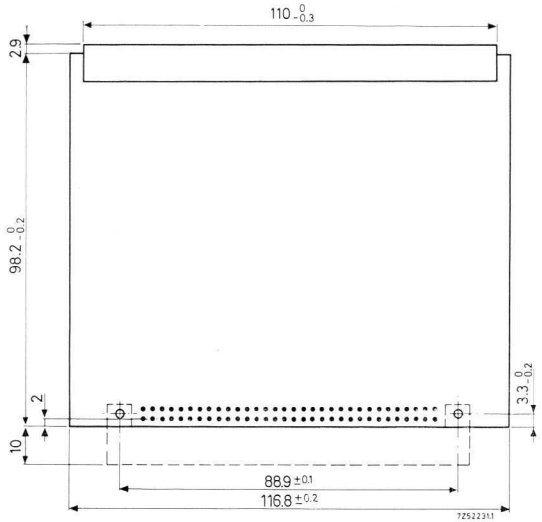


Fig. 14.38. Dimensions of the printed wiring board to fit chassis type 4322 026 38250. Board thickness is 1.5 ± 0.2 mm.

14.5 Power Supply Units

There are two power supply units designed for use with the 60-Series; PSU60 and PSU61. They are similar except that PSU61 has an extra output of 100 V. Dimensions of the units are given in Fig. 14.39. The case is of aluminium.

Specifications are as follows

A.C. input voltage	110 V, 120 V, 220 V, 230 V, 240 V; +10%-15%
Input frequency	47 to 440 Hz
D.C. output of PSU60 and PSU61	between 30 V (at 0 mA) and 18 V (at 500 mA)
PSU61	+100 V ± 25%, at 0.25 mA
Ambient temperature (operating)	−10 °C to +60 °C

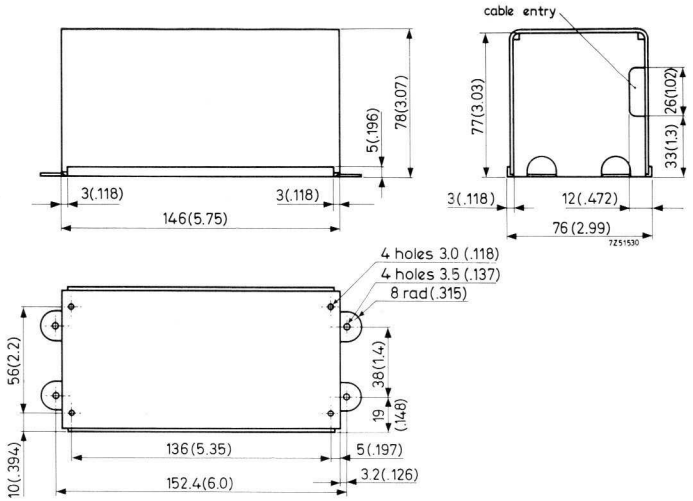


Fig. 14.39. PSU60 and PSU61 dimensions in mm (inch equivalents in brackets).

Figs 14.40 and 14.41 show the effect on output of load and temperature; Fig. 14.42 shows the circuit.

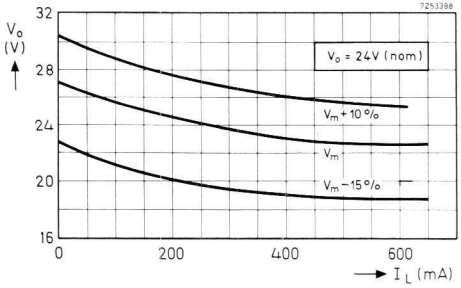
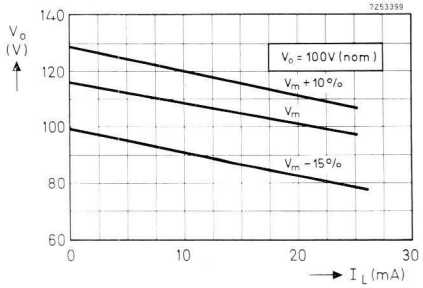


Fig. 14.40. PSU60 and PSU61 performance curves: output voltage V_o vs. load current I_L.



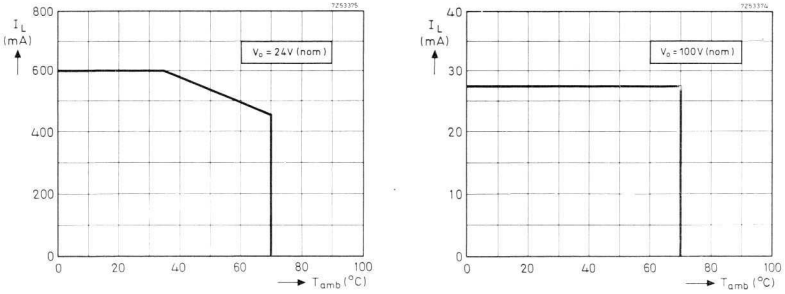


Fig. 14.41 Load current I_L vs. amb. temperature T_{amb}.

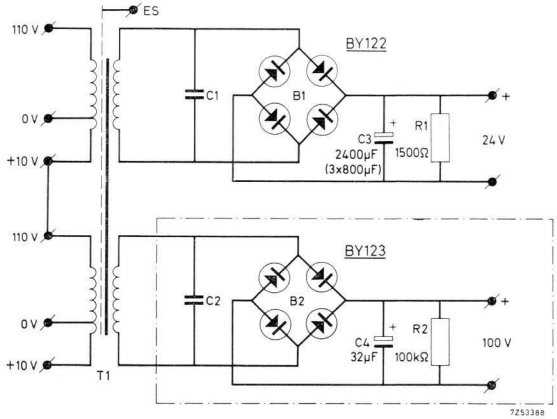


Fig. 14.42. Circuit of the PSU61. The PSU60 has the circuitry within the dotted line omitted.

Catalogue numbers of the components are given below.

One transformer (T_1),	cat.no. 4313 080 0331.
Three capacitors each 800 μF, totalling 2400 μF (C_3),	cat.no. 2222 060 17801
One capacitor 32 μF (C_4),	cat.no. 2222 040 11329
One capacitor 0.1 μF (C_2),	cat.no. 2222 341 59104
One capacitor 1.0 μF (C_1),	cat.no. 2222 341 89105
One resistor 1.5 kΩ (R_1),	cat.no. 2822 101 73152
One resistor 100 kΩ (R_2),	cat.no. 2322 101 43104
One bridge rectifier (B_1),	type BY122
One bridge rectifier (B_2),	type BY123

14.6 Mains Filter (Cat. No. 8222 279 13562)

The circuit of the Mains Filter, type MF 0.5 A, is shown in Fig. 14.43. Its dimensions are shown in Fig. 14.44. The housing is of metal and the circuit is encapsulated in resin. Further data are given below.

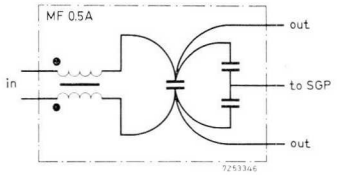


Fig. 14.43. The MF 0.5 A circuit.

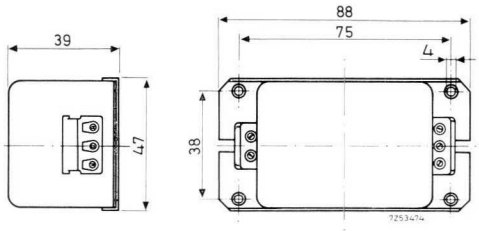


Fig. 14.44. Dimensions of the MF 0.5 A.

Maximum current	0.5 A
Maximum voltage	250 V
Test voltage	2 kV for 1 min
Attenuation (for input frequencies between 100 kHz and 10 MHz)	> 50 dB
Temperature range	
operating	-25 °C to $+70$ °C
storage	-40 °C to $+85$ °C
Weight	250 g

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