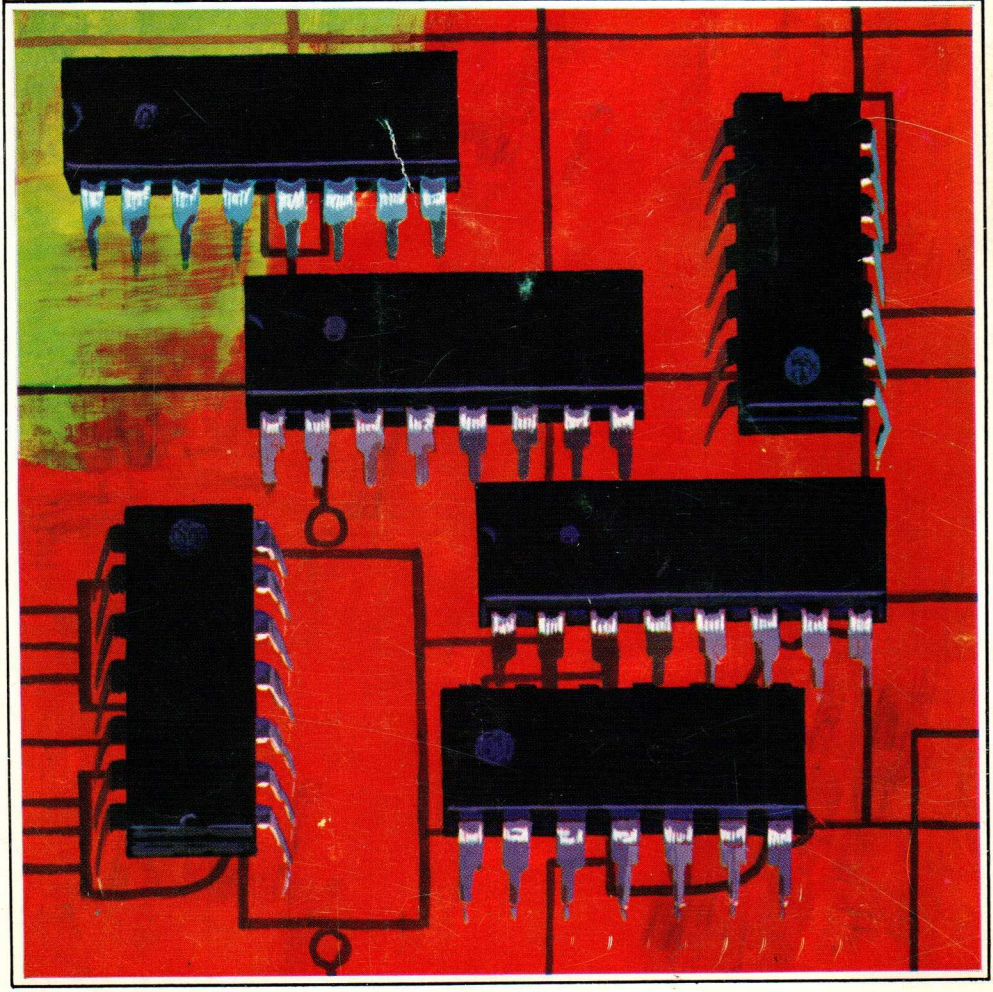
PHILIPS

APPLICATION BOOK

ELECTRONIC COMPONENTS AND MATERIALS DIVISION

FJ RANGE OF TTL INTEGRATED CIRCUITS



FJ Range of TTL integrated Logic Circuits

The text of this book was first published by Mullard Ltd.; it is based on information supplied by B. S. Cowle and J. E. Gilliam of the Mullard Central Application Laboratory.

First edition July 1969

Second edition January 1971

FJ Range of TTL Integrated Logic Circuits

Publications Department

ELECTRONIC COMPONENTS AND MATERIALS DIVISION

Contents

1. FJ Range of TTL Integrated Logic Circuits 1

2. What is TTL? 3
Introduction 3
What is TTL? 3
Operation of TTL Gate 6

3. How to use TTL 11
Operating Conditions and Ratings of the FJ Range of TTL Circuits 11
Using TTL with Long Transmission Lines 14
Coupling between Adjacent Signal Lines 17
Effects of Supply Voltage Variations 19
Hazard Conditions in Logic Systems 20
Special Purpose Gates 25
Bistable Elements 30

4. Comparators 34
Comparators using FJH231 35
Comparators using AND-OR-NOT Gates 35
Exclusive-OR Circuits 36
Multiple-Bit Comparator 36

5. Shift Registers 37
Shift Registers using Bistable Elements 38
Parallel-Input Shift Registers 39
Reversible Shift Registers 41
Reversible Parallel-Input Shift Register 43

6. Code Converters 44
1248BCD to Decimal Converter 45
1248BCD to Decimal Converters and Numerical Indicator Tube Drivers . . 46
Excess-Three Code to Decimal Converter 48
Gray Code to Decimal Converter 49
Johnson Code to Decimal Converter 50
Decimal to 1248BCD Converter 51
Decimal to 1242BCD Converter 52
Decimal to Aiken Code Converter 53
Decimal to Excess-Three Code Converter 54
Decimal to Johnson Code Converter 55
Johnson Code to 1248BCD Converter 56
Gray Code to 1248BCD Converter 57
Gray Code to Binary Converter 58

7. Error Detectors 59
1248BCD Error Detector 60
Excess-Three Code Error Detector 61
Aiken Code Error Detector 62
Parity Checker 63

8. Adders 65
Half Adders 66
Full Adders 68
Four-Bit Binary Adder 69
Serial Adder 70

9. Counters 71
Asynchronous Binary "Up Counter" 72
Synchronous Binary "Up Counter" 73
Asynchronous Binary "Down Counter" 74
Synchronous Binary "Down Counter" 75
Reversible Synchronous Binary Counter 76
Synchronous Modulo-3 "Up Counter" 77
Synchronous Unweighted Modulo-5 "Up Counter" 78
Synchronous Modulo-5 "Up Counter" 78
Synchronous Modulo-6 "Up Counter" 79
Asynchronous 1248BCD "Up Counter" 80
Synchronous 1248BCD "Up Counter" 81
Asynchronous 1248BCD "Down Counter" 82
Synchronous 1248BCD "Down Counter" 83
Synchronous Reversible 1248BCD Counters 84
Asynchronous 1245BCD "Up Counter" 86
Synchronous Excess-Three Code "Up Counter" 87
Synchronous Aiken Code "Up Counter" 88
Twisted ring Counter 89
Synchronous 1248 Weighted "Up Counter" with a Cycle Length of Twelve . 90

10. Counters Using the FJJ141 91
1248BCD Decade Counter 92
Modulo-5 Counter 93
1245BCD Counter 94

11. Chain Code Generators 95
Three-Stage Chain Code Generator with Cycle Length of Seven 96
Four-Stage Chain Code Generator with Cycle Length of Fifteen 98
Alternative Four-Stage Chain Code Generator with Cycle Length of Fifteen 99
Chain Code Generator with Shortened Cycle Length 100
Five-Stage Chain Code Generator with Cycle Length of 31 101
Six-Stage Chain Code Generator with Cycle Length of 63 103
Six-Stage Chain Code Generator with Cycle Length of Twelve 106

12. Gated Staticisers 107

13. Monostable Circuits 109

14. Multivibrators 111

15. Level Detectors 113

List of Organizations 115

1. The FJ range of TTL Integrated Logic Circuits

Several ranges of integrated circuits are available to engineers in the digital applications field. The chief difference between these ranges is in their operating speed, but they also differ in logic levels, power dissipation, supply voltage and in many other respects.

Most applications require devices which operate with propagation delays of the order of 10 to 100 ns. These medium-speed devices are used in small and medium-sized computers, peripheral equipment, telephone exchanges, instrumentation and control equipment and in many items of digital equipment associated with telecommunications. In this speed range, two configurations are common–diode-transistor logic (DTL) and transistor-transistor logic (TTL). Of these two, DTL is currently the more familiar and has become established as a solution to many problems. There are, however, many applications in which only TTL can give the required performance, and for this reason its use will increase considerably.

The FJ range of integrated logic circuits employs transistor-transistor logic. It conforms to what is becoming a standard TTL configuration in terms of voltage supply, logic levels and pinning. The FJ range is made in large quantities, resulting in an economic range in which the number of types available is likely to be very great.

The 12 ns propagation delay, at 10 mW dissipation per gate, of the FJ range is acceptable for many logic applications. However, technological developments will enable compatible ranges in speed and power to be offered alongside the standard range, giving either increased speed or reduced power. All these devices will be available in a dual-in-line 14- or 16-lead package.

An extended temperature range, to military specifications, is also available in the FJ range, with flatpack outline alternative to the dual-in-line package.

The first part of the range consists of the simpler devices providing a variety of gate functions, bistable circuits, a two-level logic element and an expander element.

The range will also contain an increasing number of complex elements

performing logic functions such as shift registers, and a variety of elements for counting purposes.

The latest, full details on the induvidual types are to be found in our Data Handbook System.

2. What is TTL?

Introduction

Electronic logic elements have evolved through a number of stages, beginning with systems consisting of diode AND and OR gates. Advances in semiconductor technology fostered rapid developments in electronic logic circuitry of the active type, and various circuits – such as resistor-transistor logic (RTL), direct-coupled-transistor logic (DCTL), diode-transistor logic (DTL) and modified forms of DTL – were produced. The first integrated logic elements were simply translations of discrete component circuits directly into silicon circuits. The earliest types were, in fact, composed of several silicon chips with wire interconnections. As integrated circuit techniques developed, the design approach changed and the circuits began to be designed to suit the manufacturing technology instead of being duplicates of discrete component prototypes. Once it was realised that circuit complexity was not a limiting factor, the way was open to the production of high-performance, complex circuit elements. Transistor-Transistor Logic (TTL) is one product of this philosophy.

What is TTL?

Integrated circuit techniques allow a number of transistors, diodes and resistors to be made on a single chip of silicon. The various components are then connected to form the required circuit by means of an aluminium interconnection pattern which is deposited on the chip. A cross-section through part of a silicon chip is shown, in diagrammatic form, in Fig. 1 and the plan view of the same chip is shown in Fig. 2. The buried layer is a low-resistivity n-type material compared with the epitaxial n-type layer. This improves the saturation characteristics of the transistor by providing a low resistance path for the collector current.

The TTL gate forms the basis of the complete FJ range of integrated logic circuit elements. The layout of a single TTL gate on a silicon chip is shown in Fig. 3 and the circuit diagram of the gate is shown in Fig. 4. Each transistor lies in a separate isolation region, and all the resistors share the same isolation area, unless otherwise dictated by layout problems. The epitaxial layer surrounding the resistors is connected to the

positive supply, thus reverse-biasing the p-n junction formed between the resistor and the epitaxial layer.

The basic TTL gate is formed by transistors TR_1 and TR_2 as shown in Fig. 4. Transistor TR_1 is a multi-emitter transistor which, together with R_1, is analogous to the input gate of a DTL circuit, as illustrated in Fig. 5. In the DTL circuit, and for one of the signal paths of the TTL circuit, transistor TR_2 is an inverter transistor. For the other signal path of the TTL gate, TR_2 is an emitter-follower stage. In the DTL gate, TR_2 also serves as the output transistor, whereas in the TTL gate, it is the driver for the push-pull "totem-pole" output stage made up of TR_3, TR_4 and D_1 in Fig. 4. Transistor TR_3 is sometimes known as the "pull-up" transistor. In the TTL range, the output stage is used as an interface between the gate and external circuitry, and acts as an inverter in one of the signal paths.

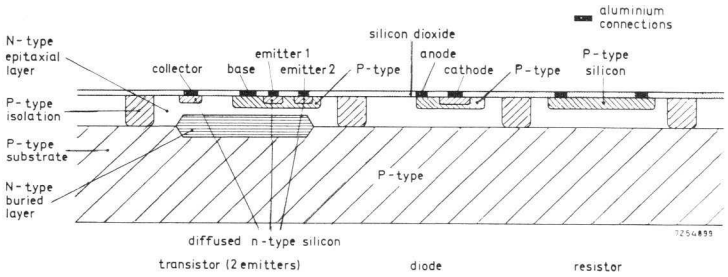


Fig. 1. Cross-section through part of a silicon chip.

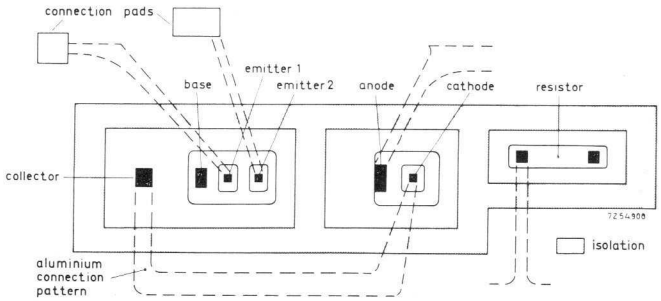


Fig. 2. Plan view of a silicon chip.

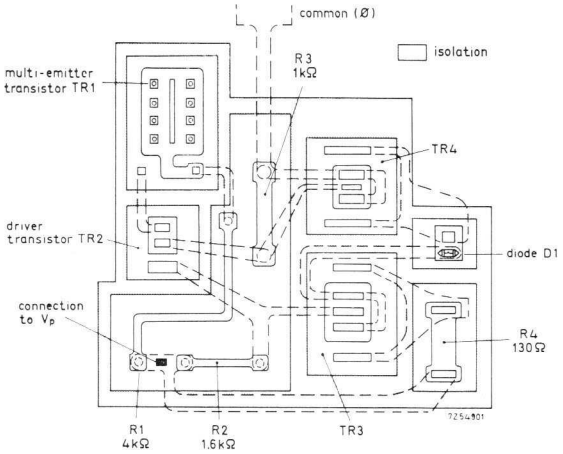


Fig. 3. TTL gate on a silicon chip.

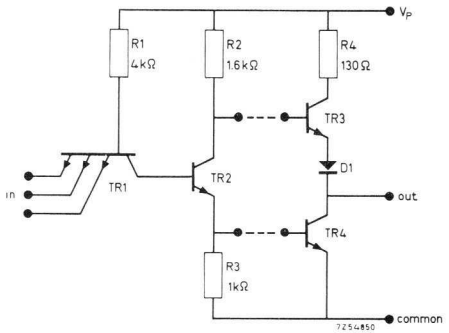


Fig. 4. TTL gate and output stage.

The TTL gate in the FJ range of circuits gives high operating speeds (propagation delay, $t_{pd} = 13$ ns), low power dissipation (10 mW) and high logical voltage output (> 2.4 V).

In the more complex elements – such as bistable circuits – internal gating functions are performed by that part of the circuit formed by TR_1 and TR_2.

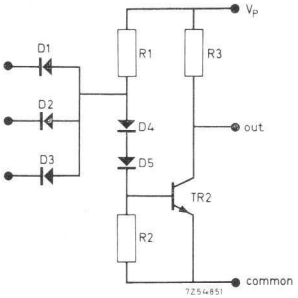


Fig. 5. DTL gate.

Operation of the TTL Gate

The explanation of the TTL gate can be simplified by considering the quiescent, or d.c., conditions and switching action separately. The d.c. conditions are considered first for the ON state and then for the OFF state.

D.C. Conditions: ON State—All Inputs "HIGH"

The circuit conditions when all inputs are HIGH are shown in Fig. 6. In the HIGH input state, each input requires a maximum input current, I_I, of 40 μA at the logical HIGH input level. The collector of TR_1 is held at the base potential of TR_2; that is, 2 V_{BE} above zero, say 1.4 V. The collector-base diode of TR_1 is forward-biased by the supply voltage via R_1 and the base is therefore at a potential equal to one forward diode voltage drop above the collector potential. The approximate circuit voltages are shown in Fig. 6.

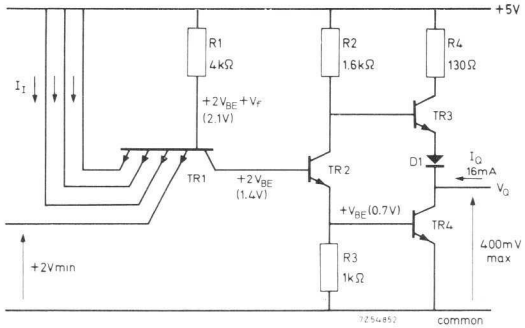


Fig. 6. TTL gate showing the conditions with all inputs HIGH.

Transistor TR_2 is conducting and is in saturation. The emitter current of TR_2 flows partly in R_3 and partly in the base of TR_4 which is also held in saturation. The voltage at the base of TR_3 is above zero by a value equal to the sum of $V_{CE(sat)}$ of TR_2 and V_{BE} of TR_4. The voltage on the emitter has a value equal to the sum of $V_{CE(sat)}$ of TR_4 and the forward voltage drop of diode D_1. These voltages are equal, so there is no base drive to TR_3. Transistor TR_3 therefore remains cut off. In this condition, TR_4 can pass a current of 16 mA without allowing the logical LOW voltage at the output to exceed 400 mV. A typical value for the low-state output voltage at 16 mA is 220 mV. A current of 16 mA is sufficient to drive ten gate inputs in the low state. Somewhat greater output currents may be taken by the gate without damage, but the output voltage rises.

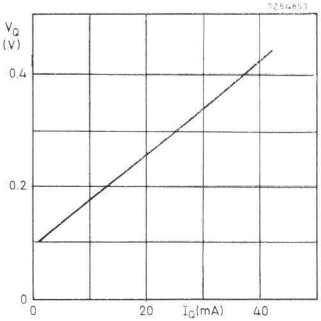


Fig. 7. Typical output characteristic of a TTL gate in the LOW state.

This effect is illustrated in Fig. 7. The output resistance in the LOW state is about 12 Ω.

To maintain the circuit in the ON state, the lowest input emitter potential must be sufficiently high to maintain the conditions shown in Fig. 6. The threshold voltage at the input – that is, the input voltage which just causes the output to change state – is about 1.5 V, and therefore, all inputs must be above this level. The test condition used is an input voltage of +2 V, under which condition an output voltage of less than 0.4 V at 16 mA is guaranteed.

D.C. Conditions: OFF State—One or More Inputs "LOW"

The circuit conditions for the OFF state are shown in Fig. 8. In this diagram, all the input emitters but one are again shown connected to the

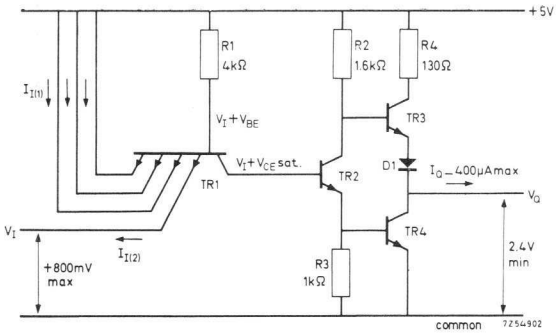


Fig. 8. TTL gate showing the conditions in the OFF state.

positive line. The "LOW" emitter, however, has a voltage of 800 mV applied to it in the test conditions. In practice, as explained in the discussion of the ON state, the input voltage can never exceed 400 mV if it is supplied by the output of a similar circuit.

The current $I_{I(2)}$ consists of two parts – I_b and $I_{I(1)}$. The greater part, I_b, is supplied via R_1 and the emitter-base diode. The smaller part, $I_{I(1)}$, flows as a result of lateral transistor action which occurs between the emitters of the multi-emitter transistor. The maximum total input current, $I_{I(2)}$, is 1.6 mA, and thus the output current of 16 mA of a gate in the ON state is sufficient to supply ten inputs. The collector of TR_1 is at a voltage $V_{CE(sat)}$ above the input voltage. This voltage is insufficient to turn both TR_2 and TR_4 on fully, although TR_2 may, in the test condition with 800 mV at the input, be conducting slightly. Transistor TR_4 remains cut off. The collector voltage of TR_2 is high, and TR_3 is, therefore, turned ON. Under the conditions stated, the output voltage, with an output of 400 μA, which is the input current of ten gates in the HIGH state, is guaranteed to be not less than 2.4 V. With an input voltage of less than 800 mV, a typical value for the output voltage is 3.3 V.

A typical output characteristic of a gate in the HIGH state is shown in Fig. 9. The output current into a short circuit has a minimum value of 18 mA and a maximum value of 55 mA. The current is limited by R_4 and, to some extent, by D_1. In a multiple gate, not more than one output must be connected to the "common" line at any one time, since damage may be caused due to excessive dissipation. The output resistance of the circuit is typically 100 Ω in the HIGH state.

A typical transfer characteristic of the TTL gate is shown in Fig. 10.

In the HIGH state, if a current greater than the normal maximum of 400 μA is taken, the output voltage begins to fall.

Switching Action

In switching from the HIGH, or OFF, state to the LOW, or ON, state, the sequence of operations is as follows:

One input is assumed to be initially at zero potential and the others are connected to the positive line. The HIGH inputs have a current flowing into them, as discussed earlier, and the current flowing out from the LOW input is about 1.6 mA. As the voltage of the LOW input is raised, the input current begins to fall. When the input reaches about 0.8 V, the collector voltage of TR_2 is 0.8 V plus $V_{CE(sat)}$ and TR_2 begins to conduct, and its collector voltage falls. The output voltage, therefore, also falls and this process continues until the input reaches the threshold value of about 1.4 or 1.5 V. At this point, the output has fallen to about 2 V. The base of TR_2 is now at a voltage of about 1.4 V, and both TR_2 and TR_4 are conducting. The output falls rapidly to the value of $V_{CE(sat)}$ of TR_4. At the same time, TR_2 is saturated, and TR_3 is turned OFF. There is a short time during which both TR_3 and TR_4 are conducting, and during this time a current flows from the positive line, via R_4, TR_3, D_1 and TR_4, to the "common" line.

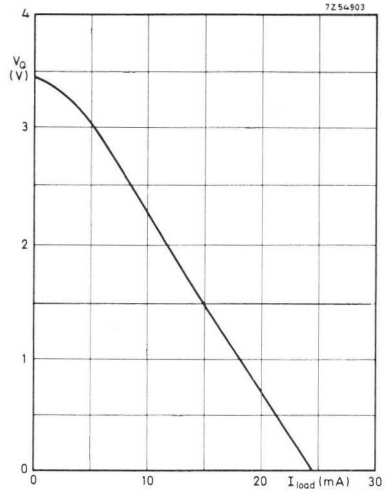


Fig. 9. Typical output characteristic of a TTL gate in the HIGH state.

In switching from the LOW to the HIGH state, the inputs are initially HIGH. As the voltage of one or more inputs is reduced to a value of about 1.4 V, the collector voltage of TR_1 falls below the voltage required to hold both TR_2 and TR_4 in conduction. The current in TR_2 falls, and the collector voltage rises, turning TR_3 ON. The output then rises to a logical HIGH level.

If the gate is used with a capacitive load of 15 pF, typical values for the propagation delay are 8 ns to set a logical LOW and 18 ns to set a logical HIGH. The total value of t_{pd} is, therefore, $(8 + 18)/2$, which is equal to 13 ns. The low output impedance in both states allows the TTL gate to drive capacitive loads effectively, and an increase from 15 to 150 pF in the capacitive load produces an increase in typical propagation delay from 13 ns to about 23 ns. The short propagation delay and the ability to drive capacitive loads are the two most important advantages of TTL. They make TTL suitable for applications where a clock frequency of 4 MHz is required and where cable connections give rise to capacitive loads.

3. How to use TTL

Operating Conditions and Ratings of the FJ Range of TTL Circuits

A summary of the most important data for the FJ range of TTL circuits is given in Table 1.

TABLE 1. Summarised Data for the FJ Range of TTL Circuits

Absolute maximum supply voltage	7 V
Operating supply voltage	4.75 to 5.25 V
Absolute maximum input voltage	5.5 V
Maximum input current requirements:	
"LOW" state (measured at $V_I = 0.4$ V)	−1.6 mA per input
"HIGH" state (measured at $V_I = 2.4$ V)	+40 μA per input
Fan-out over full operating temperature range:	
for gates	10
for buffer gates	30
Temperature range for commercial types:	
operating	0 to +70 °C
storage	−55 to +150 °C
Temperature range for military types:	
operating	−55 to +125 °C
storage	−65 to +150 °C

Noise Margin

Each gate has, associated with it, two d.c. noise margins – one for the HIGH input state and the other for the LOW input state. These margins may be quoted in relation to typical values or worst-case values of logic level and transfer characteristic.

The 'typical' noise margins may be defined by reference to the typical transfer characteristic shown in Fig. 10. The gates are assumed to be operating at full fan-out and the temperature is assumed to be 25 °C. The HIGH state noise margin at the input to gate Y is the difference between the typical logical HIGH level from gate X and the value of V_G associated with the value of V_Q for gate Y which gives a maximum logical LOW level. From the figures given in Fig. 10, this value can be calculated as 3.3–1.4, which is equal to 1.9 V.

The LOW-state noise margin is the difference between the typical value of logical LOW level from gate X and the value of V_G associated with the

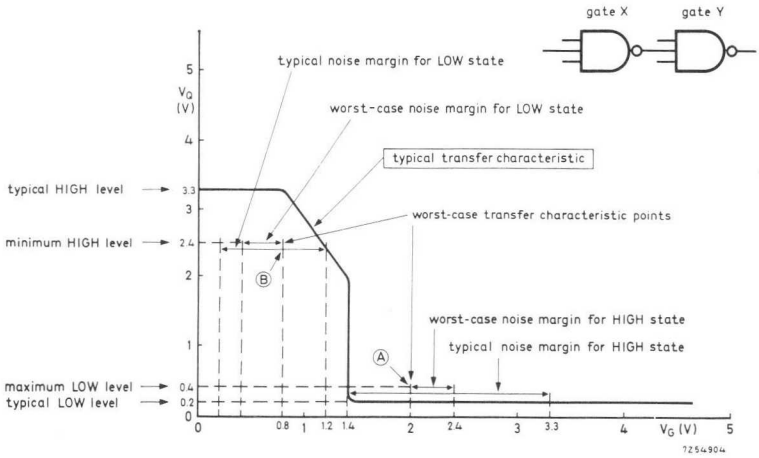


Fig. 10. Typical transfer characteristic of a TTL gate.

value of V_Q for gate Y which gives a minimum logical HIGH level. Again, numerical values can be obtained from Fig. 10 giving a value of noise margin of 1.2–0.2, or 1 V.

The 'worst-case' noise margins may also be defined by considering Fig. 10. These noise margins are based on the assumptions that the gates are operating at full fan-out over the full temperature range and that the transfer characteristic is the worst possible. The worst possible transfer characteristic passes through points A and B in Fig. 10. In the HIGH input state, the minimum logical HIGH level acceptable from gate X is 2.4 V, and the worst-case transfer characteristic gives an input threshold value of 2 V for a maximum value of logical LOW at the output of gate Y. The HIGH-state noise margin is therefore 2.4–2, or 0.4 V. In the LOW state, the maximum value of logical LOW acceptable from gate X is 0.4 V, and for a minimum value of logical HIGH at output of the gate Y, the worst-case transfer characteristic gives an input value of 0.8 V. The LOW-state noise margin is therefore 0.8–0.4, or 0.4 V.

Supply-Line and "Common"-Line Noise

Any "common"-line noise appears at the gate output in the LOW state. In the HIGH state the output is isolated from this noise source.

Noise on the supply line is fed via R_2 and TR_3 to the output in the HIGH state. In the LOW state this noise source has no effect.

When circuits of the FJ range are used, it is advisable, if long supply leads are used, to decouple the supply leads by means of a capacitor of about 10 nF or greater.

Noise Coupled to Signal Lines

Because of the low output impedance of the gate in either the HIGH or the LOW state, noise coupled to signal lines has no effect except when very long signal paths are used.

Power Dissipation

The supply current to a normal TTL gate at a supply level of 5 V and at output LOW has a typical value of 3 mA. With output HIGH, the current required is 1 mA in the unloaded condition.

The total power dissipation with a 1 : 1 duty ratio is therefore $(5\times3 + 5\times1)/2$ or 10 mW. The dissipation is increased slightly with loading and pulse repetition frequency as shown in Fig. 11.

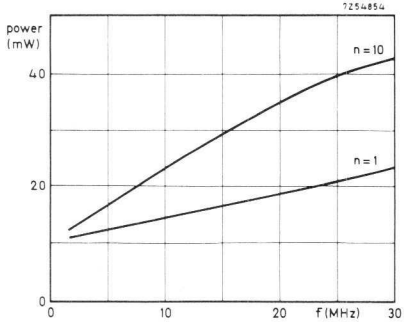


Fig. 11. Typical variation in dissipation with loading and frequency.

Unused Inputs

Unused gate inputs may be left open-circuit, connected to a positive supply of between 2.4 and 5.5 V or connected in parallel with a driven input of the same gate. Leaving inputs open-circuit, however, can give rise to unwanted pick-up. Pick-up noise can be eliminated by connecting unused inputs to a positive supply, and this connection also gives slightly faster gate operation than leaving the unused inputs open-circuit.

The fastest and safest method of dealing with unused gate inputs is to connect them in parallel with used inputs. This methods prevents pick-up noise, eliminates the danger of over-voltage at the input caused by supply

voltage variations, and gives an improvement in speed of between 0.5 and 1 ns per paralleled input.

Unused $\overline{J}$ and $\overline{K}$ inputs, J_3* and K_3*, *must* be connected to the "common" line.

Using TTL with Long Transmission Lines

In a self-contained logic system, logic elements are usually connected together by short wires or by printed wiring connections. However, it is sometimes necessary to connect circuits which are separated by a distance of tens of metres; for instance, when connections are required between circuits mounted on different racks. When long interconnections are needed, they must be effected by means of transmission lines to preserve the pulse edges and to prevent noise pick-up. These lines may be coaxial or twisted-pair transmission lines. The lines used in practice normally have a characteristic impedance of between 50 and 100 Ω and, when these lines are used, the gates must have a high input impedance and a low output impedance. These lines, which have a velocity ratio between 0.7 and 0.9, introduce delays into the system. Where this delay is less than the switching time of the gate, the effects of the line need not be considered. This is so for lines up to 30 cm long because the delay for a 30 cm line is approximately 1 ns.

However, with longer lines, delays of about 5 ns/m are common. These delays can be explained by studying Fig. 12 and the equivalent circuits for transition and d.c. states shown in Fig. 13. Gate 1 drives gate 2 directly, and gate 3 via a transmission line. The open-circuit voltage of gate 1 is E volts and is fed from a source resistor $R_{S(1)}$. The input resistances of gates 2 and 3 are termed $R_{L(2)}$ and $R_{L(3)}$ respectively, and the line has a characteristic impedance Z_0.

There are three conditions to be considered with different relative magnitudes for line impedance and gate input and output impedances. The first condition is when $R_{L(2)}$ and $R_{L(3)}$ are low compared with Z_o, and $R_{S(1)}$ is high. The second is when the impedances are matched and the third is when $R_{L(2)}$ and $R_{L(3)}$ are high compared with Z_o, and $R_{S(1)}$ is low.

For the first condition, when gate 1 switches, the instantaneous voltage at the input to the line is some fraction of E, the actual value being determined by $R_{S(1)}$, $R_{L(2)}$ and Z_o which act as a resistive divider network.

For the amplitude of this initial voltage to be sufficient to act as a

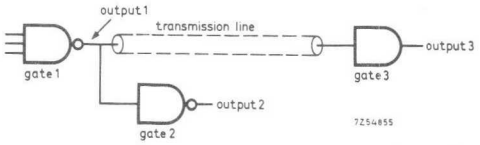


Fig. 12. Gates connected by a long transmission line.

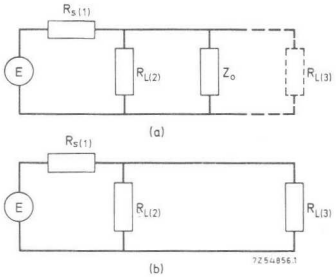


Fig. 13. Equivalent circuit of transmission line connection of gates: (a) during switching transient; (b) under static conditions.

logical HIGH at gate 2, the value of E must be much higher than the gate input threshold voltage. Apart from the difficulty of generating high voltage logical signals, the noise margin of such a system would be very poor. When the signal travels down the line to gate 3, it is reflected in antiphase, because Z_o is greater than $R_{L(3)}$, subtracting from the initial signal but still leaving a signal great enough to switch gate 3. Had the signal been reflected in phase, it would have added to the initial signal and so assisted gate 2 to turn on.

With input, output and line impedances as described above, a satisfactory logic system cannot be designed. No fan-out is possible, since loading extra gates on the output of gate 1 only reduces the signal levels. Much of the above argument applies equally to matched input, output and lines impedances, where useful fan-out cannot be obtained without a very high source e.m.f. or, more precisely, a high ratio between source e.m.f. and input threshold voltage. Reflections do not occur in a matched system, but if more than one gate of impedance Z_o is connected to the line output, a mismatched condition is set up.

The next condition to consider is that in which $R_{S(1)}$ is low compared with the line impedance and the input resistances, $R_{L(2)}$ and $R_{L(3)}$, are very much higher than the line impedance. When gate 1 switches, the initial

voltage level at the input to the line is approximately $EZ_o/(R_{S(1)} + Z_o)$. This voltage is high enough to exceed the threshold level of gate 2 immediately, and gate 2 switches. The signal then travels down the line and, after a period of one line delay, gate 3 switches. The termination presented by $R_{L(3)}$ is almost the same as an open-circuit and the signal is therefore reflected at double the amplitude. On reaching the input to the line, the reflected signal meets a low impedance, and the excess charge in the line is dissipated in this low impedance. During this process a number of small reflections occur, but these are not of sufficient amplitude to be of any consequence.

The output impedance, $R_{S(1)}$, of the TTL gate in the LOW state is 10 to 12 Ω. In the HIGH state it has a typical value of 70 Ω and a maximum value of 100 Ω. The input impedance in the HIGH state is very high – of the order of 100 kΩ. In the LOW state, the input impedance is normally about 4 kΩ, but if the input potential is made negative, the input impedance falls to about 500 Ω.

The waveforms obtained when TTL gates are used with a 50 Ω cable as shown in Fig. 12 are shown in Fig. 14. In Fig. 14, gate delays are not shown. The waveforms may be interpreted as follows. At the positive edge of the input signal, gate 1 switches to the LOW state. The output impedance of gate 1 is low and the line input voltage immediately falls to the logical LOW level, switching gate 2. A wavefront travels down the line until it arrives, after a period of one line delay, at gate 3. The input impedance appears to be an open-circuit termination on the line, and the wavefront is reflected at twice the original amplitude (t_1). Gate 3 switches. The reflected wave travels back down the line, reaching gate 1 at t_2 and attempts to cause a negative voltage step at the input to the line. The output impedance of gate 1 is, however, low and therefore the incident wave is attenuated and reflected with a phase reversal. The effect of this is to produce a small negative voltage step at t_2.

After two more line delays, this step has travelled down the line and back and is attenuated once again at the input to the line (t_3).

When the input signal falls at the end of the input pulse (t_4), gate 1 switches off, but, since its output impedance in the HIGH state can be as high as 100 Ω, the rise in voltage at the input to the line is attenuated to a value $V_H Z_o/(Z_o + Z_G)$, where V_H is the HIGH state output voltage of gate 1, Z_o is the characteristic impedance of the line and Z_G is the gate output impedance in the HIGH state. This initial step is insufficient to switch gate 2. A wave now travels down the line and is reflected in phase

(t_5). At t_6 the reflected wave reaches the beginning of the line and a signal level of sufficient amplitude to switch gate 2 is established. The output pulse at gate 2 is, therefore, delayed by a period equal to two line delays.

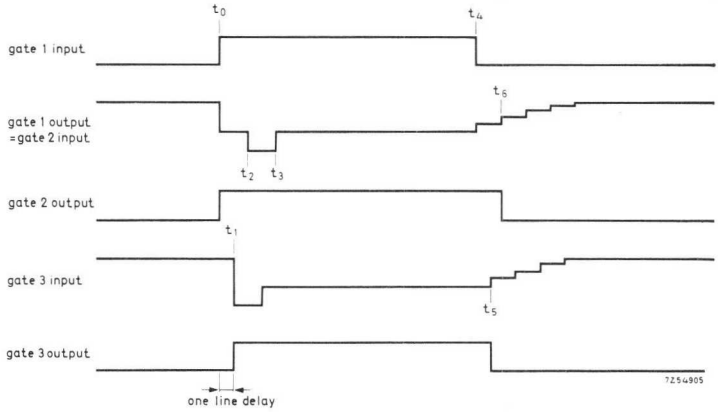


Fig. 14. Waveforms with 50 Ω line.

When low impedance lines – for instance, 50 Ω – are used, or when the loading at the input to the lines is heavy, the gates connected to the input of the line may not switch until the second reflection occurs.

If an 80 Ω line is used and typical values for E and $R_{S(1)}$ are assumed to be 3.5 V and 70 Ω respectively, a triggering potential of 1.9 V is available which is just greater than the threshold potential of gate 2, which therefore switches at time t_4. Operation under these conditions is, therefore, possible but the threshold potential is exceeded by such a small margin that reliable operation cannot be guaranteed.

The best method of improving the situation is to use a buffer gate to drive an 80 Ω line. This method ensures reliable triggering even under extremely bad conditions.

Coupling between Adjacent Signal Lines

A connection using a length of twin cable is shown in Fig. 15. Since the conductors are parallel to each other, capacitive coupling exists between them. The waveforms obtained when switch S_1 is open – that is, when gate 2 is in the LOW state – are shown in Fig. 16. When gate 1 switches, an overswing appears on the waveform at C due to reflections in the line. Because of the low impedance presented by the output of gate 2, the

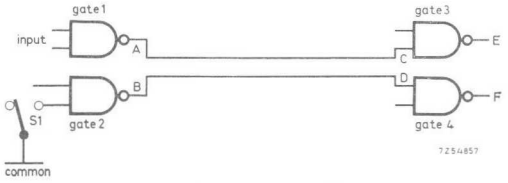


Fig. 15. Gates connected by twin pair.

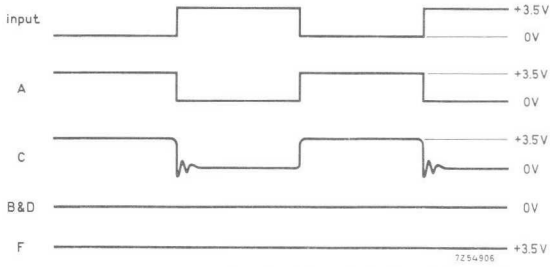


Fig. 16. Waveforms obtained with switch S_1 of Fig. 15 open.

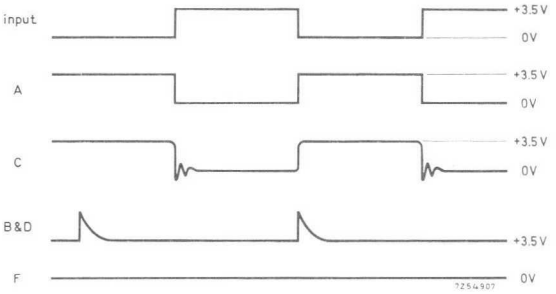


Fig. 17. Waveforms obtained with switch S_1 of Fig. 15 closed.

voltage coupled to the other line is very small – some tens of millivolts. No effect is observed at F.

The waveforms obtained when switch S_1 is closed – that is, when gate 2 is in the HIGH state – are shown in Fig. 17. With S_1 closed, capacitively-coupled negative-going edges are conducted away by the output impedance of gate 2. When this occurs, the line becomes charged, the capacitively-coupled signal becomes positive and the voltage at B is raised. The diode in the totem-pole output is now reverse-biased and the line is discharged by the leakage current of the output stage and the reverse input

current of the multi-emitter transistor of the driven gate. Therefore, a new d.c. level is established on the line and on the output of gate 2.

With a high pulse repetition frequency – higher than about 1 MHz – the waveform at B and D does not have time to decay, and the negative level only falls to about 3.5 or 4 V, which is well above the minimum logical HIGH level. Gate 4, therefore, does not switch.

With a pulse repetition frequency so low that the line discharges via the various leakage resistances between pulses, the negative-going edge capacitively-coupled to B is conducted away by the low output impedance of gate 2. Again, gate 4 is not affected.

Effects of Supply Voltage Variations

The performance of TTL gates as quoted in published data is guaranteed over a supply voltage range from 4.75 to 5.25 V. Supply voltage variations outside this range affect both fan-out and, to a lesser extent, speed.

The effects on the d.c. output conditions at 25 °C are shown for the HIGH state in Fig. 18 and for the LOW state in Fig. 19. From these figures it can be seen that, as the supply voltage is increased, the fan-out capability increases.

The effect on propagation delay is shown in Fig. 20 for fan-outs of 1 and 10. From this graph it can be seen that as the supply voltage is increased, the propagation delay decreases slightly.

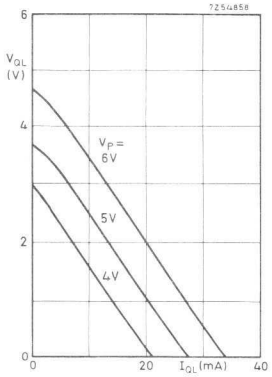


Fig. 18. Typical variation in output characteristic with variation in supply voltage in the HIGH state.

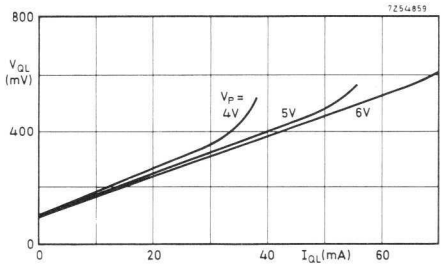


Fig. 19. Typical variation in output characteristic with variation in supply voltage in the LOW state.

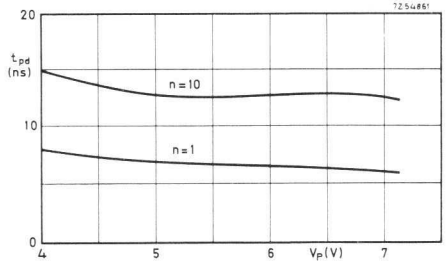


Fig. 20. Variation in propagation delay with variation in supply voltage.

Hazard Conditions in Logic Systems

In some systems it is possible for "race" conditions to develop because of differences in propagation delays and in signal path lengths. For example, two supposedly identical systems could be built, in each of which two signals from separate sources are fed to a common gate. In one system, signal A might arrive before signal B, whereas in the other system, signal B might arrive first, resulting in a different logical action being performed. This type of condition can occur in closed loop systems such as d.c.-coupled bistable elements.

In a bistable circuit used as a triggered element, the new state of the internal gates depends upon the previous state. Whilst the previous state information is necessary to determine the new state, this information must also be destroyed in setting up the new state. In edge-triggered d.c.-coupled bistable elements, this information is sometimes stored only for the duration of one or two gate propagation delays and it is possible that,

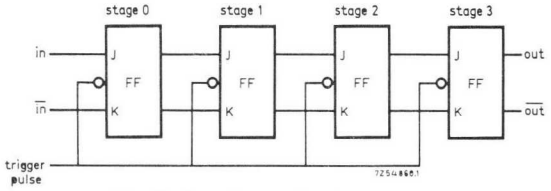


Fig. 21. Shift register using J-K bistable elements.

when a very slow transition from one state to the other is made, the stored information will be lost or confused. This can also result from race conditions outside the bistable element.

When the two edge-triggered elements in the FJ range are used, a maximum trigger pulse rise time of 150 ns prevents the occurrence of this kind of race condition hazard.

When a number of bistable elements are connected together, a different kind of race condition may occur. For instance, a shift register using J-K bistable elements is shown in Fig. 21. At each trigger pulse, the information held in the shift register is required to shift one place to the right. In the argument which follows, the threshold voltage level at which stage 2 triggers is assumed to be lower than that of the other stages. The threshold voltages of stages 0, 1, 2 and 3 are known as $V_{th(0...3)}$ respectively. If, initially, the state of the shift register is 0101 and a further LOW is shifted into stage 0 at the trigger pulse, the shift register should assume the state 0010. However, if a slowly rising edge is applied to the trigger line, when $V_{th(2)}$ is reached, stage 2 sets to HIGH and later, when $V_{th(0)}$, $V_{th(1)}$ and $V_{th(3)}$ are reached, these three stages operate according to the input information present at the time. In the example being considered, the final state of the register would be 0011.

This condition can only occur if the trigger pulse transition time from $V_{th\,min}$ to $V_{th\,max}$ is longer than the sum of the minimum propagation delay and the minimum set-up time of the bistable element. The trigger pulse should, ideally, pass through $V_{th\,min}$ to $V_{th\,max}$ in less than 15 ns in circuits where hazard conditions could arise.

This requirement indicates a trigger ramp rate of about 30 mV/ns for the FJJ101. This figure, which is based on worst-case temperature conditions, corresponds to a trigger pulse rise time of approximately 60 ns. For operation at uniform temperature, maximum trigger pulse rise times of 100 ns are recommended for this device.

Transient Hazards

Transient hazard conditions can occur when, for instance, gates are connected as shown in Fig. 22, and signals A and B change state simultaneously in opposite directions. This results in both inputs to gate 3 being above the threshold voltage for a short time which, in turn, results in the generation of an output pulse of very short duration. This effect is illustrated in Fig. 23. In some circumstances, the generation of this unwanted pulse can cause unpredictable errors.

A hazard condition could arise where each of the two gate inputs is fed from the Q output of a bistable element when the two bistable elements are fed from a common trigger pulse. The propagation delay to set HIGH in the bistable element might be as much as 50 ns and as little as 10 ns, whilst the propagation delay to set LOW might lie between 10 and 35 ns. If one of the bistable elements were fast and the other were slow, the overlap at the input to the gate could be 25 ns in one direction and 40 ns in the other. This could cause an output pulse from the gate of 25 ns duration for one transition and no pulse from the other transition. A 25 ns pulse is sufficient to set a bistable element connected to the output of the gate.

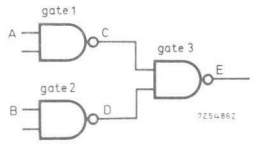


Fig. 22. Connection which may give rise to transient hazards.

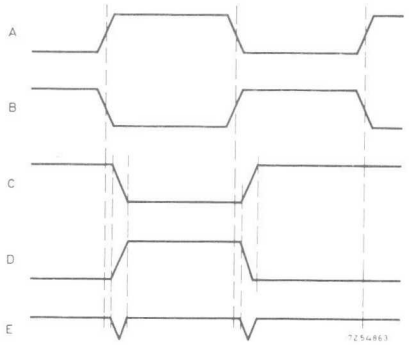


Fig. 23. Waveforms illustrating transient hazards.

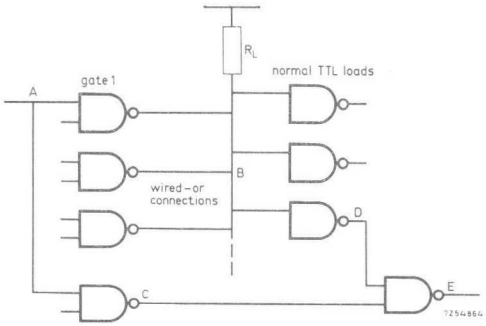


Fig. 24. Connection which may give rise to more severe transient hazards.

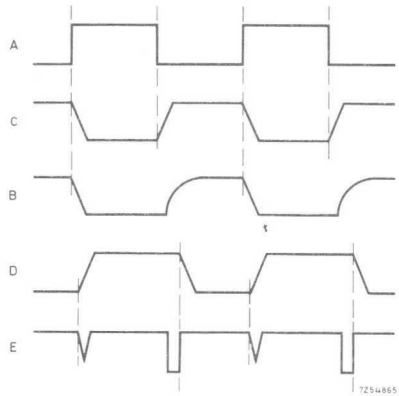


Fig. 25. Waveforms illustrating severe transient hazards.

The situation is aggravated when one of the signals to gate 3 is supplied from a gate with passive pull-up, as shown in Fig. 24. In these circumstances, the delay in changing from LOW to HIGH is longer, resulting in the effect illustrated in Fig. 25. From this diagram, it can be seen that the first unwanted negative-going pulse, at point E, is narrow because it is generated in the way described above, but the second unwanted pulse is much longer because of the delay in the gate with passive pull-up. This pulse may be above the threshold voltage for a period of several nanoseconds.

The severity of the hazard depends upon the exact operating conditions

TABLE 2. Effect of Operating Conditions on Pulse Duration

Wired-OR Connections	TTL Loads	R	Output Pulse Duration (ns)
0	1	330 Ω	11
0	1	1 kΩ	20
0	1	4.7 kΩ	26
0	5	330 Ω	13
0	5	1 kΩ	25
0	5	4.7 kΩ	28
7	1	330 Ω	20
7	1	1.2 kΩ	35
7	7	1 kΩ	30

of the circuit. There are several variables which must be considered. The value of propagation delay of gate 1 depends on the value of resistor R_1 and on the capacitive loading. Both of these values are determined by the number of wired-OR connections at B and the number of normal TTL loads at B. Examples of the duration of the pulse at E are given in Table 2 for an output pulse of 4 V amplitude. The use of the lowest possible resistor value reduces the error pulse width and gives the greatest operating speed but increases the power dissipation.

Timing Problems Encountered when using Edge-Triggered and Master-Slave Bistable Elements.

Logic signals in a system are frequently derived from bistable elements, processed by a number of gating stages and, finally, stored in a second group of bistable elements. If the sending and receiving bistable elements are either both of the master-slave type or both of the edge-triggered type, only the timing problems already discussed are likely to arise. If the sending bistable element is of the master-slave type and the receiving bistable element is of the edge-triggered type, the behaviour of the system is predictable although not always immediately obvious. If, however, the sending element is of the edge-triggered type and the receiving element is of the master-slave type, the behaviour of the system is unpredictable because the J and K signals to the receiving element are derived at the leading edge of the trigger pulse, which is the time when the master-slave element is reading J and K information in. The J and K information at the receiving element may be incorrectly registered. This type of connection is, therefore, undesirable and should be avoided if possible.

Special-Purpose Gates

The FJ range of TTL integrated circuits contains three types of special-purpose gate:

FJH151	Dual AND-OR-NOT gate
FJH171	Quadruple AND-OR-NOT gate
FJH231	Quadruple two-input gate without pull-up transistor, for wired-OR use

FJH151 Dual AND-OR-NOT Gate

The circuit diagram of the FJH151 dual AND-OR-NOT gate is shown in Fig. 26. The output of this gate is given by:

$$(\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D}) \text{ or } \overline{A \cdot B + C \cdot D}$$

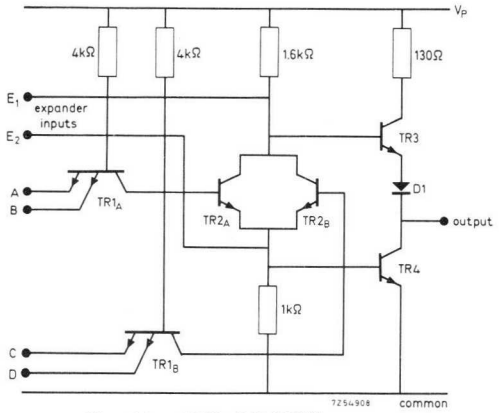


Fig. 26. AND-OR-NOT gate.

The FJH151 gate can be expanded by means of the FJY101 which is shown in Fig. 27.

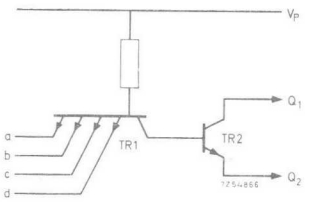
If the expander inputs are used, the output becomes:

$$\overline{A \cdot B + C \cdot D + E_I + E_{II} + E_{III} \ldots}$$

where E_I, E_{II}, E_{III} are the outputs of expanders I, II, III respectively and, in general, $E = a \cdot b \cdot c \cdot d$.

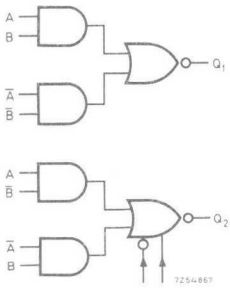
Not more than four FJY101 expanders may be connected to one FJH151.

This gate may be used to provide the exclusive-OR function or as an equality gate in a comparator. The necessary inputs are shown in Fig. 28.



Terminals Q_1 and Q_2 are to be connected to inputs E_1 and E_2 respectively, of FJH151 or FJH171; suggested resistor value 4 kΩ.

Fig. 27. One gate of the FJY101 element.



$$Q_1 = \overline{A \cdot B + \bar{A} \cdot \bar{B}} = (A + B)(\bar{A} + \bar{B})$$
$$= A \cdot \bar{B} + \bar{A} \cdot B \text{ (exclusive OR)}$$

$$Q_2 = \overline{A \cdot \bar{B} + \bar{A} \cdot B} = (\bar{A} + B)(A + \bar{B})$$
$$= \bar{A} \cdot \bar{B} + A \cdot B \text{ (equality)}$$

Fig. 28. Use of the AND-OR-NOT gate type FJH151.

FJH171 Quadruple AND-OR-NOT Gate

The circuit diagram of the FJH171 quadruple AND-OR-NOT gate is shown in Fig. 29. The output of this gate is given by:

$$\overline{A \cdot B + C \cdot D + E \cdot F + G \cdot H}$$

Expander, or node, inputs are provided for use with the expander FJY101. If the expander inputs are used the output becomes:

$$\overline{A \cdot B + C \cdot D + E \cdot F + G \cdot H + E_I + E_{II} + E_{III} \ldots}$$

where E_I, E_{II}, E_{III} are the outputs of expanders I, II, III respectively and, in general, $E = a \cdot b \cdot c \cdot d$.

If the expander inputs are neglected, the gate can perform a double exclusive-OR function. This is achieved by feeding the gate inputs with

$$A \cdot B,\ \bar{A} \cdot \bar{B},\ C \cdot D,\ \bar{C} \cdot \bar{D}.$$

The output then becomes

$$(A \cdot \bar{B} + \bar{A} \cdot B) \cdot (C \cdot \bar{D} + \bar{C} \cdot D).$$

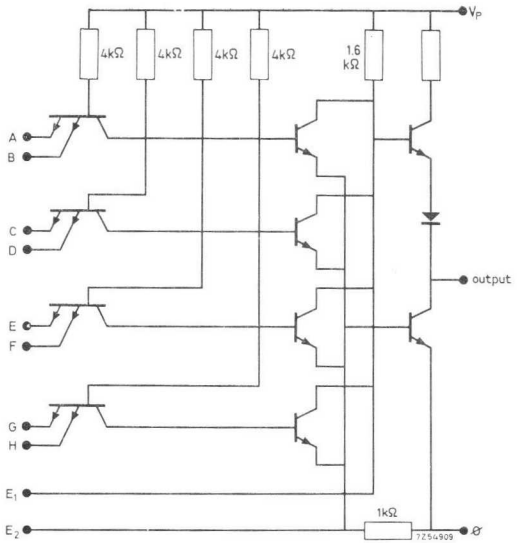


Fig. 29. Circuit diagram of the quadruple AND-OR-NOT gate type FJH171.

If the inputs are fed with the functions

$$A \cdot \overline{B},\ \overline{A} \cdot B,\ C \cdot \overline{D},\ \overline{C} \cdot D$$

the output is

$$(A \cdot B + \overline{A} \cdot \overline{B}) \cdot (C \cdot D + \overline{C} \cdot \overline{D})$$

which is the required output for a two-stage comparator. This function would normally be written

$$(A_1 \cdot B_1 + \overline{A}_1 \cdot \overline{B}_1) \cdot (A_2 \cdot B_2 + \overline{A}_2 \cdot \overline{B}_2)$$

where A_1A_2 and B_1B_2 are the quantities being compared.

FJH231 Quadruple Wired-OR Gate

The FJH231 is similar to the FJH131 but without the isolation diode and pull-up transistor. The circuit diagram of the FJH231 i given in Fig. 30. The load resistor is provided externally by the user, and with the proper choice of this resistor for any particular application, gates may be connected together to perform the wired-OR function and still be capable of driving up to nine TTL loads. The connections to perform the basic wired-OR function are shown in Fig. 31.

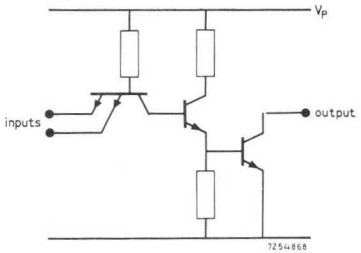


Fig. 30. One section of the FJH231.

If the inputs are fed with

$$A \cdot \overline{B}, \quad \overline{A} \cdot B,$$

the output becomes

$$A \cdot B + \overline{A} \cdot \overline{B},$$

and if the inputs are fed with

$$A \cdot B, \quad \overline{A} \cdot \overline{B},$$

the output is

$$A \cdot \overline{B} + \overline{A} \cdot B.$$

It is evident, therefore, that the gate performs a similar function to the FJH151 dual AND-OR-NOT gate.

The wired-OR function may be expanded to provide a similar function to the FJH171 as shown in Fig. 32.

The switching speeds associated with a resistive pull-up are similar to those of a normal TTL gate when switching from HIGH to LOW, but the transition from LOW to HIGH is slower because output and circuit capacitances must be charged via the load resistor. Minimum rise times are achieved by using a low value of collector resisor, but since this increases the collector current of the output transistor, less current is available for driving other loads.

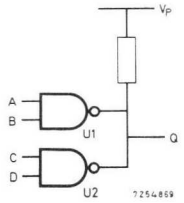
Increasing the value of collector resistor to give a higher fan-out decreases the operating speed as already explained, but it also introduces an additional difficulty; namely, that when other TTL gates are being driven, the HIGH-state input current of these gates must not cause the output voltage of the driving gate to fall below the minimum logical HIGH level.

To calculate the maximum and minimum permitted values for the load

resistor, R_L, the following equations are used. The load current, I_L, is given by:

$$I_L = NI_{IH} + PI_{oeH}$$

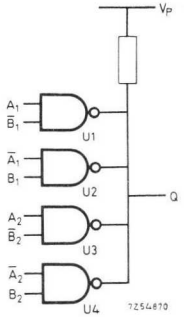
where N = fan-out to TTL loads
I_{IH} = input current of a gate in the HIGH state
P = fan-out to wired-OR loads
I_{oeH} = leakage current of the output transistors.



$$U_1 + U_2 = \tfrac{1}{2}\,\text{FJH231}$$

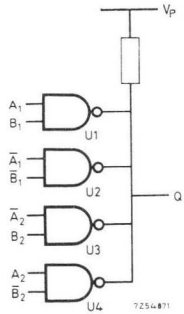
$$Q = \overline{A \cdot B + C \cdot D} = (\bar{A} + \bar{B})(\bar{C} + \bar{D})$$

Fig. 31. Wired-OR connection.



$$U_1 + U_2 + U_3 + U_4 = \text{FJH231}$$

$$Q = (A_1 \cdot B_1 + \bar{A}_1 \cdot \bar{B}_1)(A_2 \cdot B_2 + \bar{A}_2 \cdot \bar{B}_2)$$



$$U_1 + U_2 + U_3 + U_4 = \text{FJH231}$$

$$Q = (A_1 \cdot \bar{B}_1 + \bar{A}_1 \cdot B_1)(\bar{A}_2 \cdot B_2 + A_2 \cdot \bar{B}_2)$$

Fig. 32. Wired-OR connection of more than two gates.

Therefore, the maximum value of the load resistance, R_L, is given by:

$$R_{L\,max} = \frac{V_P - V_{QH\,min}}{NI_{IH\,max} + PI_{oe\,max}}$$

where V_P = supply voltage
V_{QH} = HIGH state output voltage.

The maximum current to be supplied by the output transistor, $I_{QL\,max}$, is given by:

$$I_{QL\,max} = \frac{V_P - V_{QL\,max}}{R_{L\,min}} + NI_{IL\,max}$$

where V_{QL} = output voltage of a gate in the LOW state
I_{IL} = input current of a gate in the LOW state

Therefore

$$R_{L\,min} = \frac{V_P - V_{QL\,max}}{I_{QL\,max} - NI_{IL\,max}}$$

In the LOW state, the maximum output current that can be taken without exceeding the guaranteed output voltage of 0.4 V is 16 mA, and this is the value which should be used for I_{QL} in the calculation. The chosen load resistor must lie between $R_{L\,min}$ and $R_{L\,max}$.

It is possible to connect as many as seven gates by the wired-OR method and still maintain a fan-out of seven into TTL loads. Five wired-OR connections allow the fan-out to be increased to eight and two gates connected by the wired-OR method allow a fan-out of nine.

When the FJH231 is used to drive only TTL loads and a 4 kΩ collector resistor is used, a fan-out of ten is available.

The minimum value of supply voltage should be used in the calculation of $R_{L\,max}$, and the maximum value should be used to calculate $R_{L\,min}$.

Bistable Elements

The FJ range of TTL integrated circuits contains three types of bistable element:

FJJ111, FJJ121	Master-slave J-K bistable element
FJJ101	Edge-triggered J-K bistable element
FJJ131	D bistable element

FJJ111, FJJ121 Master-Slave J-K Bistable Element

The single master-slave bistable element, FJJ111, has three J and three K inputs. It has a maximum operating frequency of at least 10 MHz but typically 15 MHz. The truth table of a J-K bistable element is given in Table 3. In this table, $Q_{1(n+1)}$ and $Q_{2(n+1)}$ are the states at the Q_1 and

TABLE 3. Truth Tables of J-K Bistable Element

J	K	$Q_{1(n+1)}$	$Q_{2(n+1)}$
0	0	Q_{1n}	$\overline{Q}_{1n}$
1	0	1	0
0	1	0	1
1	1	$\overline{Q}_{1n}$	Q_{1n}
S_1	S_2	Q_1	Q_2
0	0	1	1
1	0	0	1
0	1	1	0
1	1	Q_{1n}	$\overline{Q}_{1n}$

Q_2 outputs after the action of a trigger pulse. The functions performed at the J and K inputs are $J = J_1 \cdot J_2 \cdot J_3$ and $K = K_1 \cdot K_2 \cdot K_3$.

The S_1 and S_2 direct inputs set the state of the Q_1 and Q_2 outputs independently of the trigger input.

A waveform diagram illustrating the operation of the J-K bistable element is given in Fig. 33 (positive logic is assumed ,"1" = HIGH). Before the trigger pulse arrives, the element is shown in the LOW state. At time t_1, the master circuit is disconnected from the slave. This occurs when the trigger voltage reaches about 1 V. At time t_2, information is read in from the J and K inputs to the master circuit. This occurs when

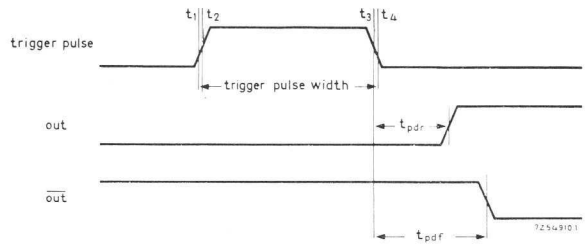


Fig. 33. Operation of master-slave bistable element with J = HIGH and K = LOW.

the trigger input reaches a level of approximately 2 V. At time t_3, the input AND gates are disconnected from the master circuit, and at time t_4, the master information is transferred to the slave circuit. After the propagation delay, the appropriate voltage levels appear at the output terminals.

The trigger pulse duration must be at least 20 ns, and the J and K information must be held static during the trigger pulse and for a total time of at least 25 ns. Changes of J and K information during the trigger pulse may cause the output to set accordingly. Typical values for propagation delay are 26 ns to set LOW and 34 ns to set HIGH.

The set and trigger inputs each represent two TTL loads while the J and K inputs represent one load each. The fan-out from the bistable element as with the other TTL elements is 10 from each output. The supply current required is 8 mA, corresponding to a dissipation of 40 mW.

The FJJ121 is a dual version of the master-slave element which has only single J and K inputs to each bistable circuit.

FJJ101 Edge-Triggered J-K Bistable Element

The logic diagram of the FJJ101 edge-triggered J-K bistable element is given in Fig. 34. The element may be used at a frequency of maximum 20 MHz and will operate typically up to 35 MHz. It is provided with multiple J and K inputs but, unlike the master-slave elements, the FJJ101 has two direct inputs to each of the J and K AND gates, and one input to each of these gates via an inverter. The logic functions performed at the J and K inputs are, therefore, $J = J_1 \cdot J_2 \cdot J_3{}^*$ and $K = K_1 \cdot K_2 \cdot K_3{}^*$.

In the edge-triggered bistable element, the input information is transferred to the output on the rising, or positive-going, edge of the trigger pulse. Typical values of propagation delay are 27 ns to set HIGH and 18 ns to set LOW. The time taken to read in the J and K information is known as the "set-up" time and has a maximum value of 20 ns. This time occurs before the trigger pulse reaches the threshold value. After the trigger pulse threshold value has been reached, the input information must remain for

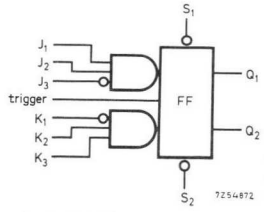


Fig. 34. Edge-triggered J-K bistable element type FJJ101.

* Inverted input

at least 5 ns. This is known as the "hold" time. The J and K information must therefore be present at least 20 ns before the trigger pulse threshold and must remain for at least 5 ns after it. After this time, J and K information is locked out and can have no further effect on the state of the bistable element until the trigger pulse is discontinued.

In the bistable element, the trigger pulse must rise to the HIGH level in less than 150 ns. Slower rates of rise than this introduce the possibility of race conditions which could cause an erroneous output as described under the heading "Hazard Conditions in Logic Systems" (p. 20).

FJJ131 Dual D Bistable Element

This D bistable element is a delay element which delays information between input and output by one trigger period. The truth table for a D bistable element is given in Table 4. The states shown are those after the rising edge of the trigger pulse.

TABLE 4. Truth Table for D Bistable Element

D	$Q_{1(n+1)}$
0	0
1	1

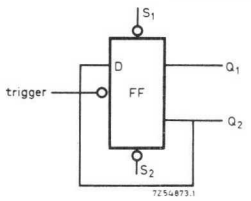


Fig. 35. D bistable element connected as a T bistable element.

The D bistable element may be used as a triggered element if Q_2 is connected to D as shown in Fig. 35. The FJJ131 is also provided with S_1 and S_2 inputs.

The rated operating frequency is 15 MHz (typically 25 MHz). The set-up and hold times have minimum values of 20 ns and 5 ns respectively and a trigger pulse rise time of not more than 150 ns is allowed. The waveform diagram given in Fig. 36 shows the typical propagation delays of 28 ns to set HIGH and 20 ns to set LOW. The maximum values for these delays are 35 ns and 50 ns respectively.

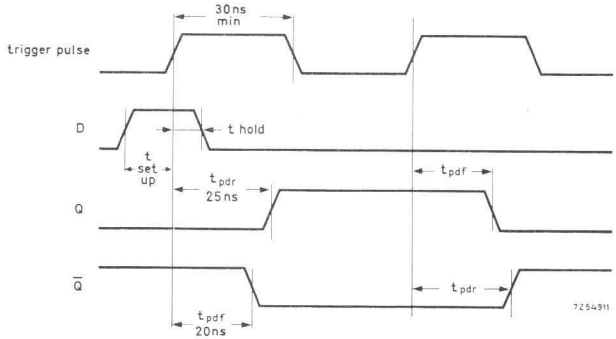


Fig. 36. Waveforms of D bistable element FJJ131.

4. Comparators

Comparators are used to determine whether two binary numbers are equal. For two single-bit numbers A and B to be equal, the required function is

$$A \cdot B + \overline{A} \cdot \overline{B}.$$

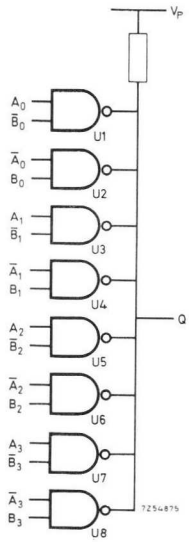
This can be achieved by the use of an AND-OR-NOT gate or by connecting two NAND gates by the wired-OR method as explained in Chapter 3.

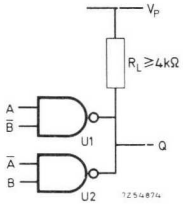
To compare two multi-bit numbers A_0 to A_n and B_0 to B_n, the required function is

$$(A_0 \cdot B_0 + \overline{A}_0 \cdot \overline{B}_0) \cdot (A_1 \cdot B_1 + \overline{A}_1 \cdot \overline{B}_1) \cdot (A_2 \cdot B_2 + \overline{A}_2 \cdot \overline{B}_2) \ldots \cdot (A_n \cdot B_n + \overline{A}_n \cdot \overline{B}_n).$$

When comparators are used in conjunction with counters, the complements of the signals are usually available as well as the signals themselves, but if the complements are not available, they must be generated.

Comparators using FJH231





$$U_1 + U_2 = \tfrac{1}{2}\text{FJH231}$$

$$Q = \overline{\overline{A \cdot \bar{B}} \cdot \overline{\bar{A} \cdot B}} = A \cdot B + \bar{A} \cdot \bar{B}$$

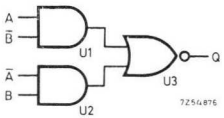
Fig. 37. One-bit comparator using FJH231.

$$U_1 = U_2 = U_3 = U_4 = U_5 = U_6 = U_7 = U_8 = \tfrac{1}{4}\text{FJH231}$$

$$Q = (A_0 \cdot B_0 + \bar{A}_0 \cdot \bar{B}_0)(A_1 \cdot B_1 + \bar{A}_1 \cdot \bar{B}_1) \cdot \cdot (A_2 \cdot B_2 + \bar{A}_2 \cdot \bar{B}_2)(A_3 \cdot B_3 + \bar{A}_3 \cdot \bar{B}_3)$$

Fig. 38. Four-bit binary comparator for use as a BCD comparator

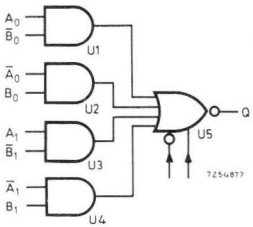
Comparators using AND-OR-NOT Gates



$$U_1 + U_2 + U_3 = \tfrac{1}{2}\text{FJH151}$$

$$Q = \overline{\overline{A \cdot \bar{B}} \cdot \overline{\bar{A} \cdot B}} = A \cdot B + \bar{A} \cdot \bar{B}$$

Fig. 39. One-bit comparator using an AND-OR-NOT gate.

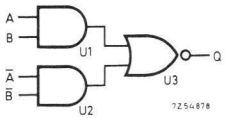


$$Q = \overline{A_0 \cdot \bar{B}_0 + \bar{A}_0 \cdot B_0 + A_1 \cdot \bar{B}_1 + \bar{A}_1 \cdot B_1} = (A_0 \cdot B_0 + \bar{A}_0 \cdot \bar{B}_0)(A_1 \cdot B_1 + \bar{A}_1 \cdot \bar{B}_1)$$

$$U_1 + U_2 + U_3 + U_4 + U_5 = \text{FJH171}$$

Fig. 40. Two-bit comparator using a quadruple AND-OR-NOT gate.

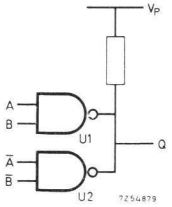
Exclusive-OR Circuits



$U_1 + U_2 + U_3 = \frac{1}{2}$FJH151

$Q = \overline{A \cdot B + \bar{A} \cdot \bar{B}} = A \cdot \bar{B} + \bar{A} \cdot B$

Fig. 41. Exclusive-OR circuit using an AND-OR-NOT gate.

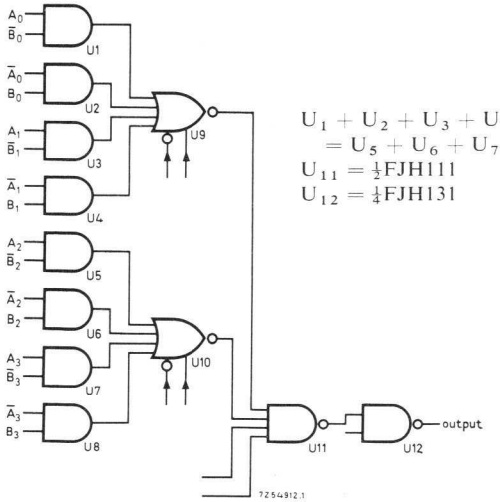


$U_1 + U_2 = \frac{1}{2}$FJH231

$Q = \overline{A \cdot B + \bar{A} \cdot \bar{B}} = A \cdot \bar{B} + \bar{A} \cdot B$

Fig. 42. Exclusive-OR circuit using NAND gates.

Multiple-Bit Comparator



$U_1 + U_2 + U_3 + U_4 + U_9 =$
$= U_5 + U_6 + U_7 + U_8 + U_{10} =$ FJH171

$U_{11} = \frac{1}{2}$FJH111

$U_{12} = \frac{1}{4}$FJH131

Fig. 43. Four-bit comparator using NAND and quadruple AND-OR-NOT gates. The system can be extended to any number of bits.

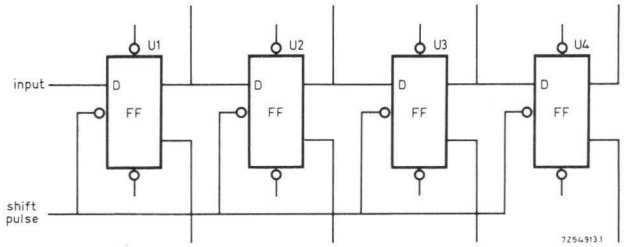
5. Shift Registers

A shift register shifts the contents of one bistable element in a series into the next when a "shift" pulse is received. If the contents are shifted into the following bistable element, the shift register is said to be forward-shifting but if the contents are shifted into the preceding bistable element, the shift register is said to be reverse-shifting. A reversible shift register has its stage interconnections changed from forward to reverse, or vice-versa, by gates.

Shift registers are the basis of stores, sequence control units, chain code generators and some counters. Shift registers may either be built to accept information sequentially or in parallel. Bistable elements of the D or J-K types are suitable for use in shift registers but, when edge-triggered bistable circuits are used, the trigger pulse rise times must be short enough to preclude the occurrence of any interstage hazard conditions as explained in Chapter 3.

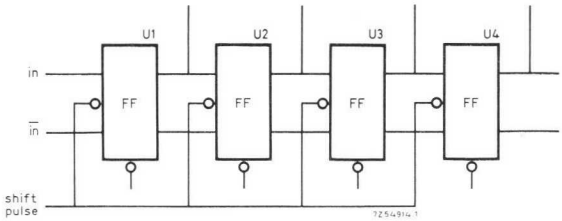
Where wired-OR connections using the FJH231 are used, the value of the pull-up resistor may need to be changed if further loads are added. The method of selecting a suitable value has already been explained in Chapter 3.

Shift Registers using Bistable Elements



$U_1 = U_2 = U_3 = U_4 = \frac{1}{2}$FJJ131

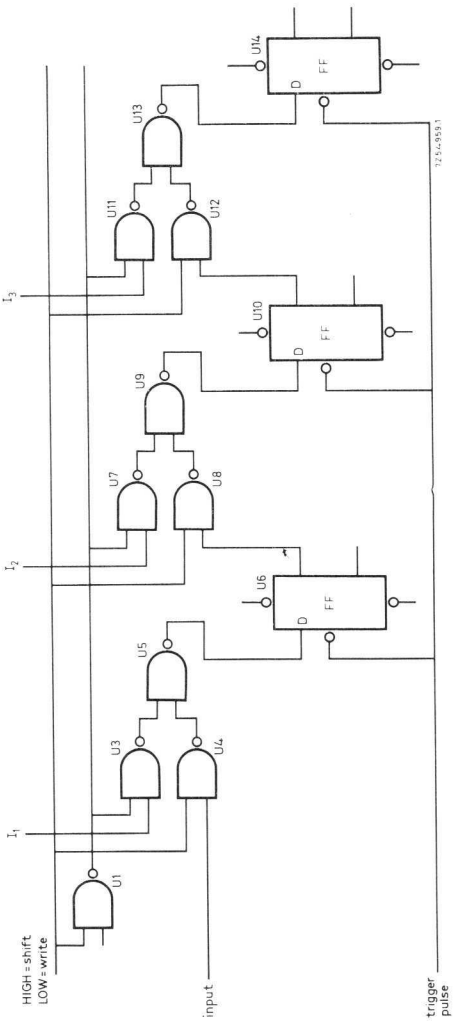
Fig. 44. Shift register using dual D bistable elements.



$U_1 = U_2 = U_3 = U_4 = \frac{1}{2}$FJJ121

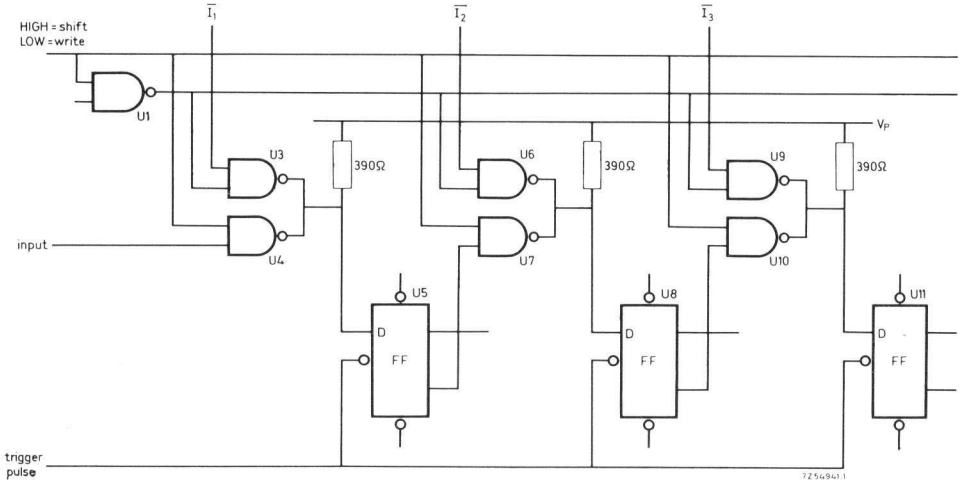
Fig. 45. Shift register using dual J-K bistable elements.

Parallel-Input Shift Registers



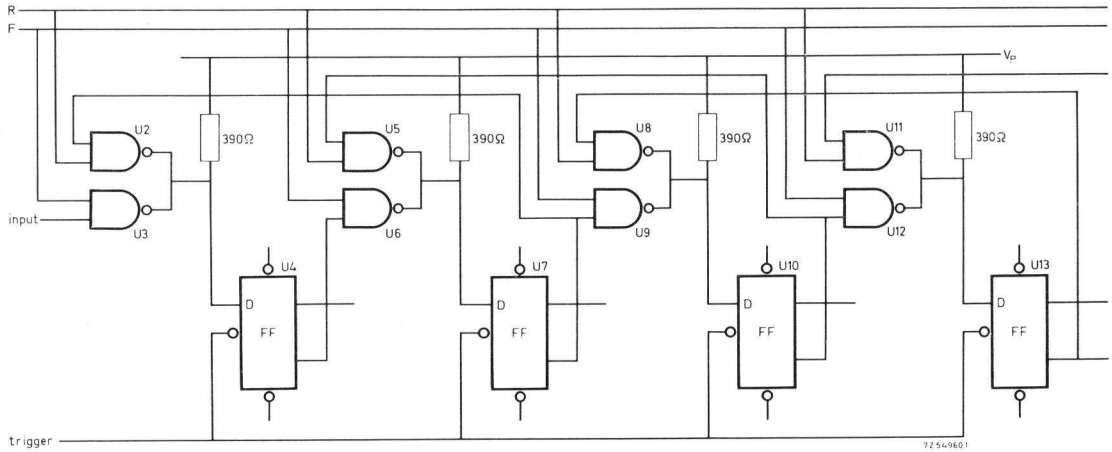
$U_6 = U_{10} = U_{14} = \frac{1}{2}FJJ131$

Fig. 46. Parallel-input shift register using dual D bistable elements and NAND gates.



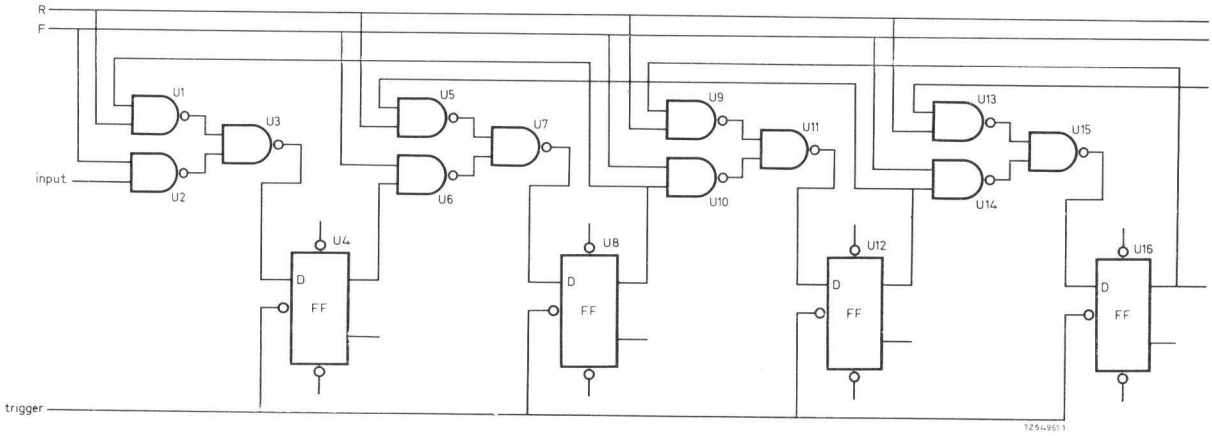
$U_3 = U_4 = U_6 = U_7 = U_9 = U_{10} = \frac{1}{4}$FJH231
$U_5 = U_8 = U_{11} = \frac{1}{2}$FJJ131

Fig. 47. Parallel-input shift register using dual D bistable elements and NAND gates with the wired-OR connection.



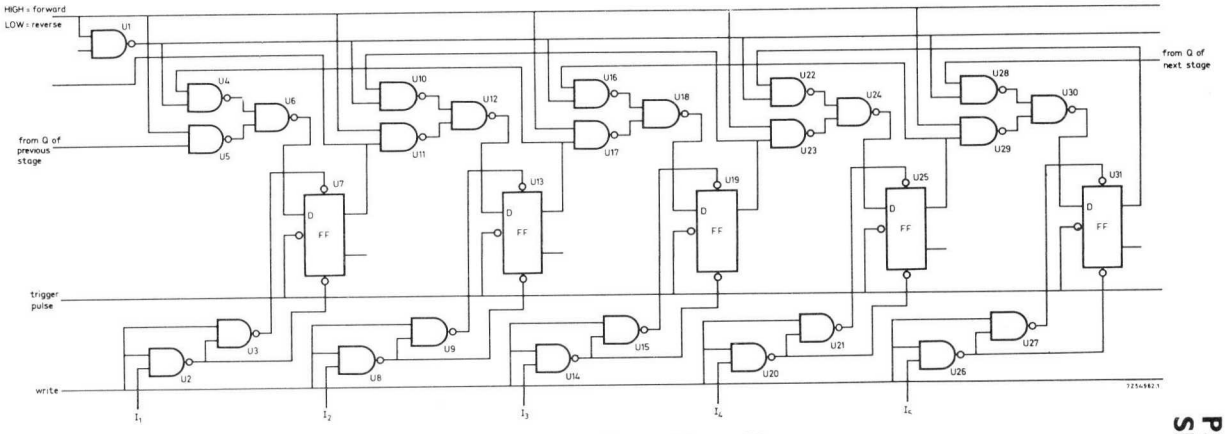
$U_2 = U_3 = U_5 = U_6 = U_8 = U_9 = U_{11} = U_{12} = \frac{1}{4}$FJH231
$U_4 = U_7 = U_{10} = U_{13} = \frac{1}{2}$FJJ131

Fig. 48. Reversible shift register using dual D bistable elements and NAND gates with the wired-OR connection. R = Reverse, F = Forward.



$U_1 = U_2 = U_3 = U_5 = U_6 = U_7 = U_9 = U_{10} = U_{11} = U_{13} = U_{14} = U_{15} = \frac{1}{4}$FJH131
$U_4 = U_8 = U_{12} = U_{16} = \frac{1}{2}$FJJ131

Fig. 49. Reversible shift register using dual D bistable elements and NAND gates. R = Reverse, F = Forward.



$U_4 = U_5 = U_6 = U_{10} = U_{11} = U_{12} = U_{16} = U_{17} = U_{18} = U_{22} = U_{23} = U_{24} =$
$= U_{28} = U_{29} = U_{30} = U_2 = U_3 = U_8 = U_9 = U_{14} = U_{15} = U_{20} = U_{21} =$
$= U_{26} = U_{27} = \frac{1}{4}$FJH131
$U_7 = U_{13} = U_{19} = U_{25} = U_{31} = \frac{1}{2}$FJJ131

Fig. 50. Reversible parallel-input shift register with inputs independent of a trigger, using dual D bistable elements and NAND gates. A LOW I input gives a HIGH output from the associated flip-flop output.

6. Code Converters

Code converters are gating systems which convert information from one coded form to another. The most common code converters are used to convert information from binary-coded-decimal, excess-three code or some other coded form into decimal numbers. These code converters are also known as decoders. Code converters which convert decimal numbers into some coded form are sometimes known as encoders.

In some codes, such as binary-coded-decimal, not all the possible states are used; for instance, in 1248BCD the states 1010, 1011, 1100, 1101, 1110 and 1111 are not used. These unused states are known as redundancies* and their existence enables the number of gate inputs of code converters to be reduced.

Resistors are shown on converters with decimal inputs because these may be supplied from mechanical switches. The resistors ensure that open inputs are held at a logical HIGH level and reduce the possibility of pick-up. If these converters are fed from other gate circuits, the resistors may be omitted.

* Also known as illegitimate states

1248BCD to Decimal Converter

All outputs are HIGH except the energised number.

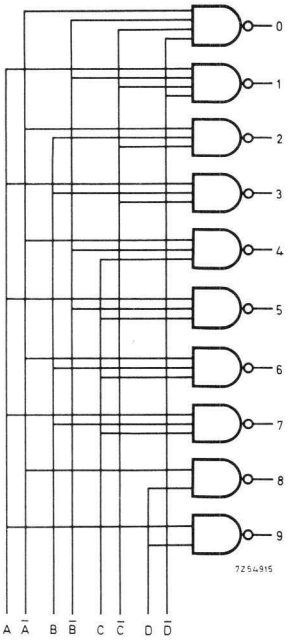


Fig. 51. 1248BCD to decimal converter.

Truth Table

Weight =	D 8	C 4	B 2	A 1	Simplification
0	0	0	0	0	$\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}$
1	0	0	0	1	$A\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}$
2	0	0	1	0	$\overline{A}\cdot B\cdot\overline{C}$
3	0	0	1	1	$A\cdot B\cdot\overline{C}$
4	0	1	0	0	$\overline{A}\cdot\overline{B}\cdot C$
5	0	1	0	1	$A\cdot\overline{B}\cdot C$
6	0	1	1	0	$\overline{A}\cdot B\cdot C$
7	0	1	1	1	$A\cdot B\cdot C$
8	1	0	0	0	$\overline{A}\cdot D$
9	1	0	0	1	$A\cdot D$

1248BCD to Decimal Converters and Numerical Indicator Tube Drivers

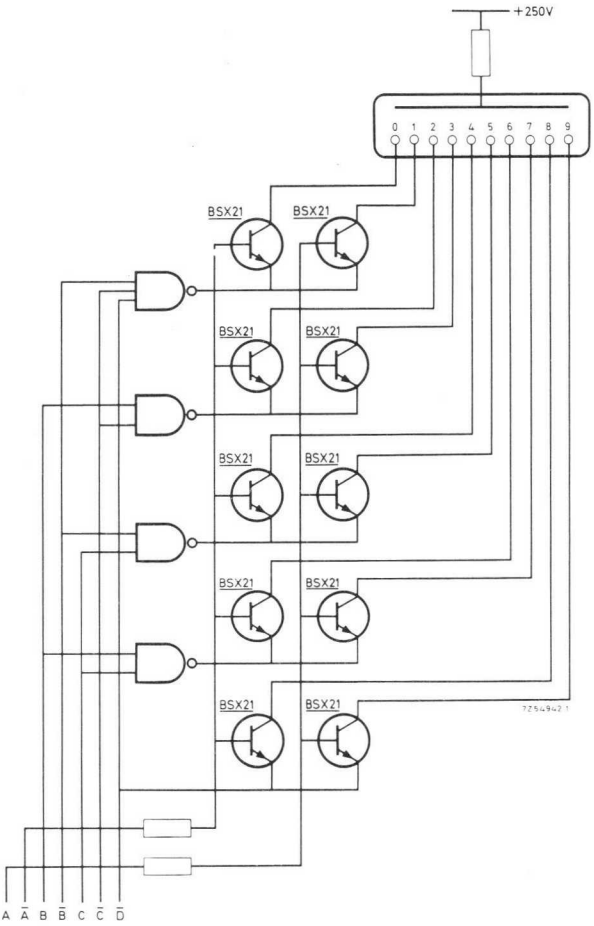


Fig. 52. 1248BCD to decimal converter and numerical indicator tube driver.

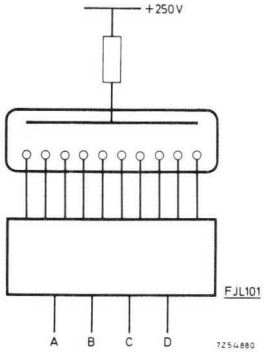


Fig. 53. 1248BCD to decimal converter and numerical indicator tube driver using FJL101.

Truth Table

	D	C	B	A	
	Weight = 8	4	2	1	Simplification
0	0	0	0	0	$\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}$
1	0	0	0	1	$A\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}$
2	0	0	1	0	$\overline{A}\cdot B\cdot\overline{C}$
3	0	0	1	1	$A\cdot B\cdot\overline{C}$
4	0	1	0	0	$\overline{A}\cdot\overline{B}\cdot C$
5	0	1	0	1	$\overline{A}\cdot\overline{B}\cdot C$
6	0	1	1	0	$\overline{A}\cdot B\cdot C$
7	0	1	1	1	$A\cdot B\cdot C$
8	1	0	0	0	$\overline{A}\cdot D$
9	1	0	0	1	$A\cdot D$

Excess-Three Code to Decimal Converter

All outputs are HIGH except the energised number.

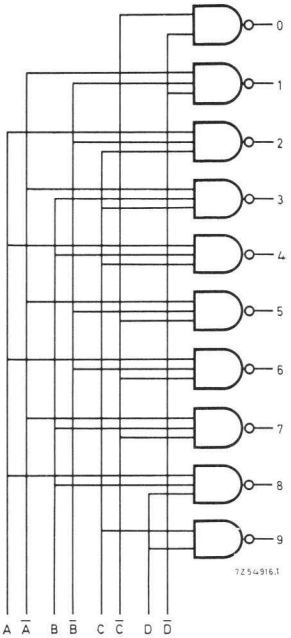


Fig. 54. Excess-three code to decimal converter.

Truth Table

	D	C	B	A	simplification
0	0	0	1	1	$\overline{C}\cdot\overline{D}$
1	0	1	0	0	$\overline{A}\cdot\overline{B}\cdot\overline{D}$
2	0	1	0	1	$A\cdot\overline{B}\cdot C$
3	0	1	1	0	$\overline{A}\cdot B\cdot C$
4	0	1	1	1	$A\cdot B\cdot C$
5	1	0	0	0	$\overline{A}\cdot\overline{B}\cdot\overline{C}$
6	1	0	0	1	$A\cdot\overline{B}\cdot\overline{C}$
7	1	0	1	0	$\overline{A}\cdot B\cdot\overline{C}$
8	1	0	1	1	$A\cdot B\cdot D$
9	1	1	0	0	$C\cdot D$

Gray Code to Decimal Converter

Gray code with a cycle length of 10.
All outputs are HIGH except the energised number.

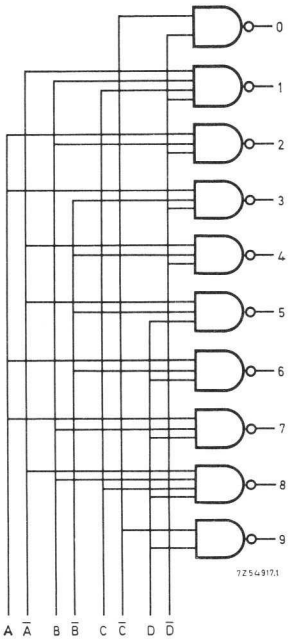


Fig. 55. Gray code to decimal converter.

Truth Table

	D	C	B	A
0	0	0	1	0
1	0	1	1	0
2	0	1	1	1
3	0	1	0	1
4	0	1	0	0
5	1	1	0	0
6	1	1	0	1
7	1	1	1	1
8	1	1	1	0
9	1	0	1	0

Johnson Code to Decimal Converter

All outputs are HIGH except the energised number.

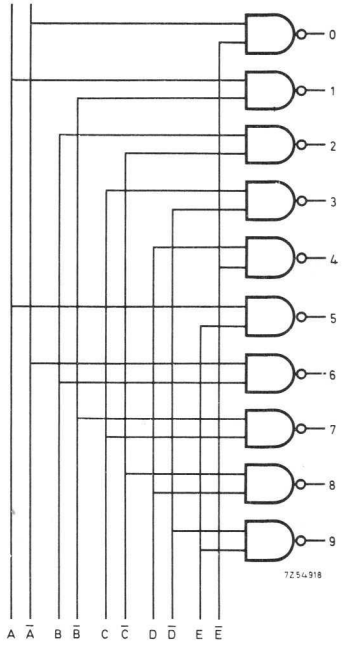


Fig. 56. Johnson code to decimal converter.

Truth Table

	E	D	C	B	A	Simplification
0	0	0	0	0	0	$\overline{A}\cdot\overline{E}$
1	0	0	0	0	1	$A\cdot\overline{B}$
2	0	0	0	1	1	$B\cdot\overline{C}$
3	0	0	1	1	1	$C\cdot\overline{D}$
4	0	1	1	1	1	$D\cdot\overline{E}$
5	1	1	1	1	1	$A\cdot E$
6	1	1	1	1	0	$\overline{A}\cdot B$
7	1	1	1	0	0	$\overline{B}\cdot C$
8	1	1	0	0	0	$\overline{C}\cdot D$
9	1	0	0	0	0	$\overline{D}\cdot E$

Decimal to 1248BCD Converter

All inputs are HIGH except the energised number.

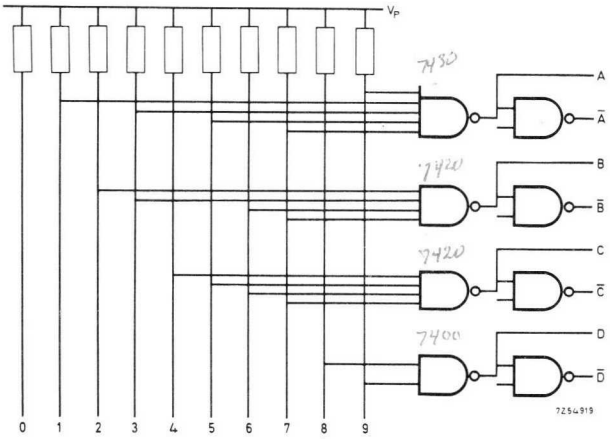


Fig. 57. Decimal to 1248BCD converter.

Truth Table

	D	C	B	A
Weight =	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Decimal to 1242BCD Converter

All inputs are HIGH except the energised number.

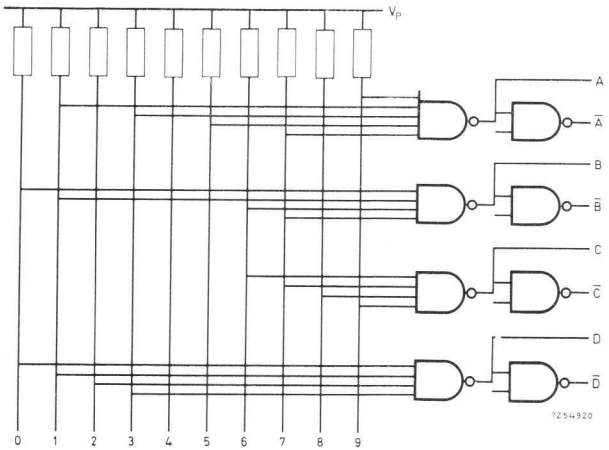


Fig. 58. Decimal to 1242BCD converter.

Truth Table

	D	C	B	A
Weight =	2	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	1	0	1	0
5	1	0	1	1
6	1	1	0	0
7	1	1	0	1
8	1	1	1	0
9	1	1	1	1

Decimal to Aiken Code Converter

All inputs are HIGH except the energised number.

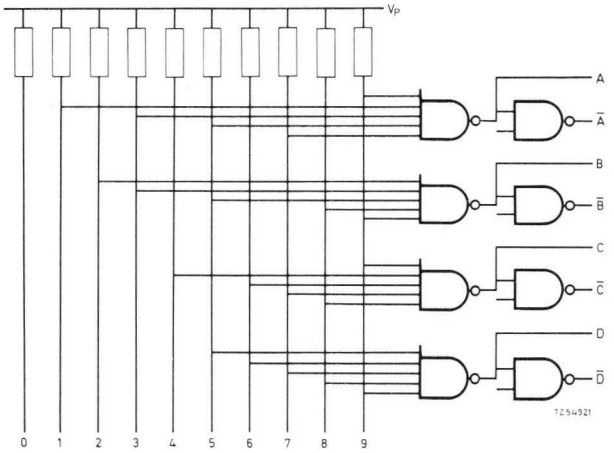


Fig. 59. Decimal to Aiken code converter.

Truth Table

	D	C	B	A
Weight =	2	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	1	0	1	1
6	1	1	0	0
7	1	1	0	1
8	1	1	1	0
9	1	1	1	1

Decimal to Excess-Three Code Converter

All inputs are HIGH except the energised number.

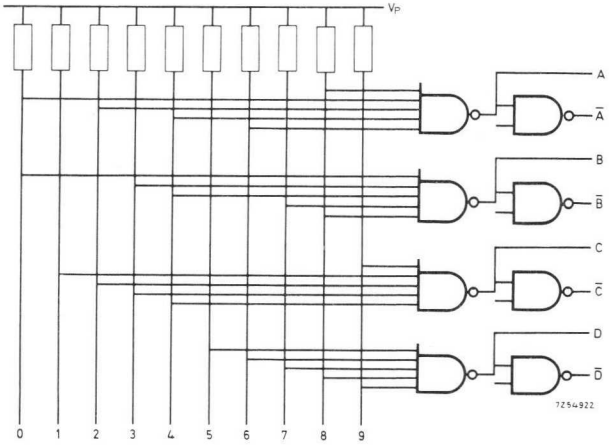


Fig. 60. Decimal to excess-three code converter.

Truth Table

	D	C	B	A
0	0	0	1	1
1	0	1	0	0
2	0	1	0	1
3	0	1	1	0
4	0	1	1	1
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	0	0

Decimal to Johnson Code Converter

All inputs are HIGH except the energised number.

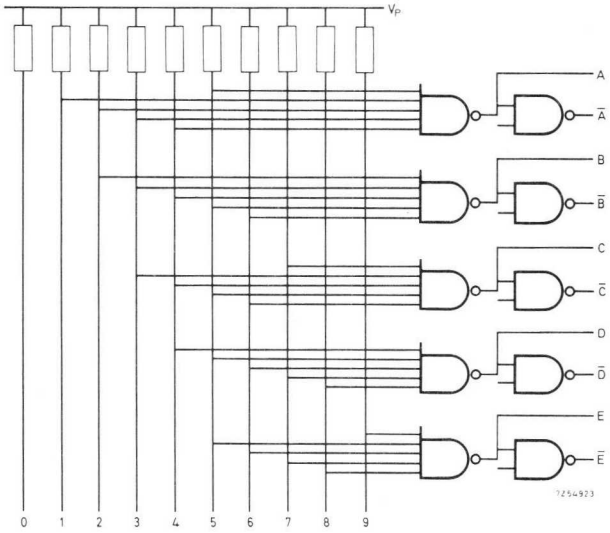


Fig. 61. Decimal to Johnson code converter.

Truth Table

	E	D	C	B	A
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	1
3	0	0	1	1	1
4	0	1	1	1	1
5	1	1	1	1	1
6	1	1	1	1	0
7	1	1	1	0	0
8	1	1	0	0	0
9	1	0	0	0	0

Johnson Code to 1248BCD Converter

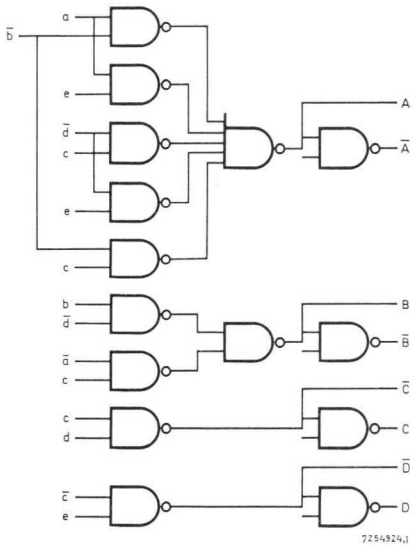


Fig. 62. Johnson code to 1248BCD converter.

Truth Table

Johnson					1248BCD			
e	d	c	b	a	D	C	B	A
0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	1
0	0	0	1	1	0	0	1	0
0	0	1	1	1	0	0	1	1
0	1	1	1	1	0	1	0	0
1	1	1	1	1	0	1	0	1
1	1	1	1	0	0	1	1	0
1	1	1	0	0	0	1	1	1
1	1	0	0	0	1	0	0	0
1	0	0	0	0	1	0	0	1

Gray Code to 1248BCD Converter

Gray code with a cycle length of 10.

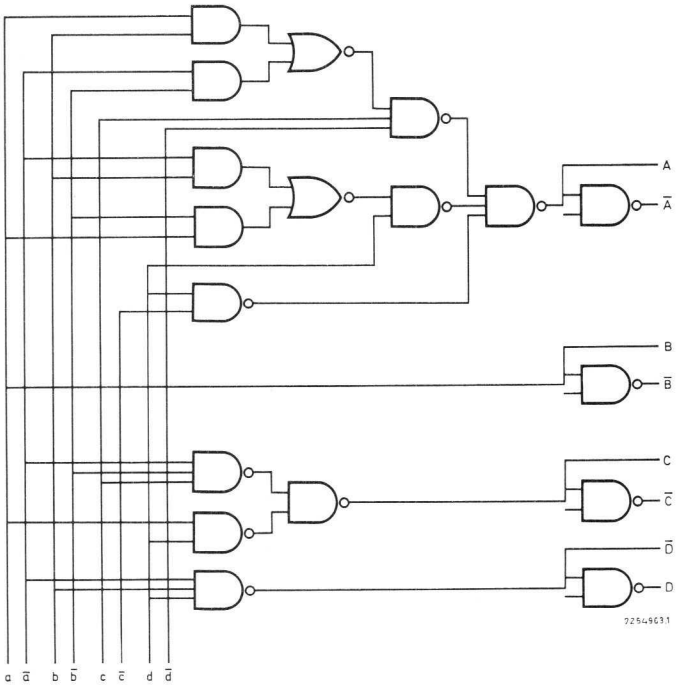


Fig. 63. Gray code to 1248BCD converter.

Truth Table

Gray				1248BCD			
d	c	b	a	D	C	B	A
0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1
0	1	1	1	0	0	1	0
0	1	0	1	0	0	1	1
0	1	0	0	0	1	0	0
1	1	0	0	0	1	0	1
1	1	0	1	0	1	1	0
1	1	1	1	0	1	1	1
1	1	1	0	1	0	0	0
1	0	1	0	1	0	0	1

Gray Code to Binary Converter

Gray code with a cycle length of 16.

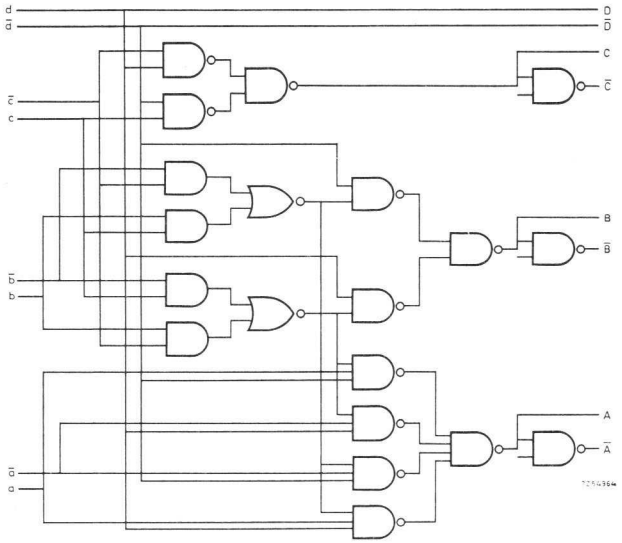


Fig. 64. Gray code to binary converter.

Truth Table

Gray				Binary			
d	c	b	a	D	C	B	A
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

7. Error Detectors

Errors can be detected either by recognising redundant states and giving a signal if one occurs or by means of a "parity check". In this chapter, three circuits of the "redundant state detector" type and one of the "parity check" type are given.

A parity check is effected by generating a signal – the parity signal – which is either a HIGH or a LOW depending on whether the number of HIGH bits in the relevant row of the truth table is even or odd respectively. The sum of the HIGH bits in a number, together with its parity signal should, therefore, always be an even number. An error becomes evident if the number, together with its parity bit, is found to contain an odd number of HIGH bits.

1248BCD Error Detector

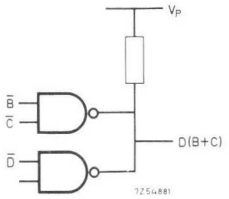


Fig. 65. 1248BCD error detector circuit.

Truth Table

	D	C	B	A
Weight =	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
Redundant	1	0	1	0
	1	0	1	1
	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1

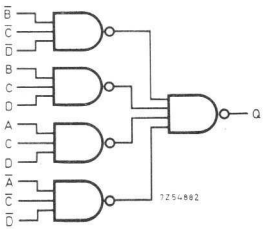
The Boolean expression for the presence of a redundant state is:

$\overline{A}\cdot B\cdot\overline{C}\cdot D + A\cdot B\cdot\overline{C}\cdot D + \overline{A}\cdot\overline{B}\cdot C\cdot D + A\cdot\overline{B}\cdot C\cdot D + \overline{A}\cdot B\cdot C\cdot D + A\cdot B\cdot C\cdot D,$

which can be simplified to

$$D(B + C).$$

Excess-Three Code Error Detector



$$Q = \bar{B} \cdot \bar{C} \cdot \bar{D} + B \cdot C \cdot D + A \cdot C \cdot D + \bar{A} \cdot \bar{C} \cdot \bar{D}$$

Fig. 66. Excess-three code error detector.

Truth Table

	D	C	B	A
Redundant	0	0	0	0
	0	0	0	1
	0	0	1	0
0	0	0	1	1
1	0	1	0	0
2	0	1	0	1
3	0	1	1	0
4	0	1	1	1
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	0	0
Redundant	1	1	0	1
	1	1	1	0
	1	1	1	1

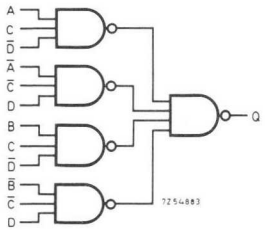
The Boolean expression for the presence of a redundant state is:

$$\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} + A \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} + \bar{A} \cdot B \cdot \bar{C} \cdot \bar{D} + A \cdot \bar{B} \cdot C \cdot D + \bar{A} \cdot B \cdot C \cdot D + A \cdot B \cdot C \cdot D,$$

which can be simplified to:

$$\bar{B} \cdot \bar{C} \cdot \bar{D} + B \cdot C \cdot D + A \cdot C \cdot D + \bar{A} \cdot \bar{C} \cdot \bar{D}.$$

Aiken Code Error Detector



$$Q = A \cdot C \cdot \bar{D} + \bar{A} \cdot \bar{C} \cdot D + B \cdot C \cdot \bar{D} + \bar{B} \cdot \bar{C} \cdot D$$

Fig. 67. Aiken code error detector.

Truth Table

	D	C	B	A
Weight =	2	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	1	0	1	1
6	1	1	0	0
7	1	1	0	1
8	1	1	1	0
9	1	1	1	1
The following states are redundant				
	0	1	0	1
	0	1	1	0
	0	1	1	1
	1	0	0	0
	1	0	0	1
	1	0	1	0

The Boolean expression for the presence of a redundant state is:

$$A \cdot \bar{B} \cdot C \cdot \bar{D} + \bar{A} \cdot B \cdot C \cdot \bar{D} + A \cdot B \cdot C \cdot \bar{D} + \\ + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D + A \cdot \bar{B} \cdot \bar{C} \cdot D + \bar{A} \cdot B \cdot \bar{C} \cdot D,$$

which can be simplified to:

$$A \cdot C \cdot \bar{D} + \bar{A} \cdot \bar{C} \cdot D + B \cdot C \cdot \bar{D} + \bar{B} \cdot \bar{C} \cdot D.$$

Parity Checker

The parity checker shown in Fig. 68 operates in the serial mode.

Initially the J-K bistable circuit is set to HIGH. Information from the sending register is then transferred to the series of D bistable elements which form a shift register. The RESET terminal of the J-K bistable element is released, and the contents of the shift register are fed serially, via routing circuits, to the receiving register. Each time a LOW appears in the final stage of the shift register, the J-K bistable element changes state. The final state of the J-K bistable element is, therefore, determined by whether the number of HIGH bits is odd or even.

The shift register is controlled by a pulse generator which is inhibited when the contents of the shift register is 000.

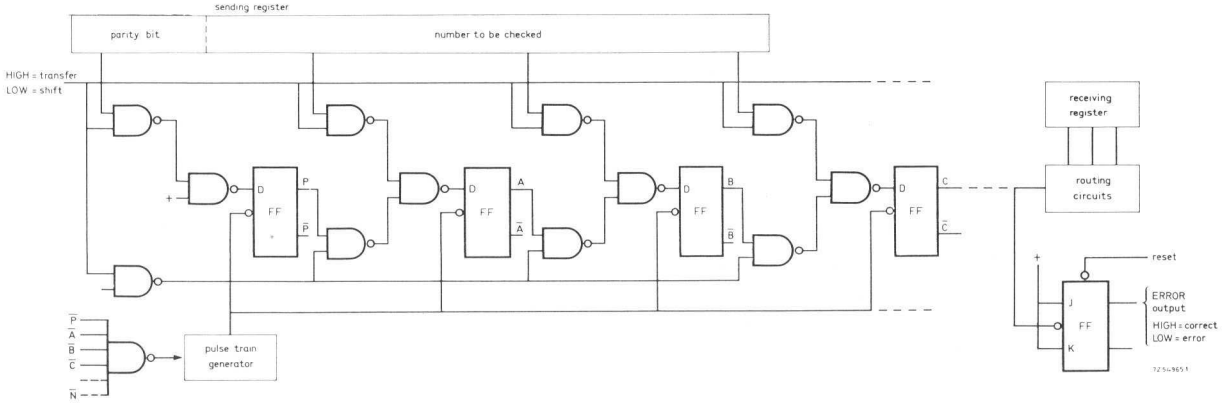


Fig. 68. Parity checker for N bits.

8. Adders

The four most important arithmetic operations – addition, subtraction, multiplication and division – can all be performed by manipulations of addition, and, for this reason, addition is a very important operation. The circuits used to perform the function of addition fall into two groups – half adders and full adders.

A half adder produces the sum of two bits, together with a carry if necessary. Each stage of a full adder can handle one bit of each of the numbers to be added and the carry from the previous stage. Adders can operate in a serial or parallel model. In the serial mode, addition occurs sequentially, starting with the least significant bit. In the parallel mode, addition of all the bits is effected simultaneously. Parallel adders perform the total addition operation much more quickly than serial adders but are more complex and therefore more expensive.

Half Adders

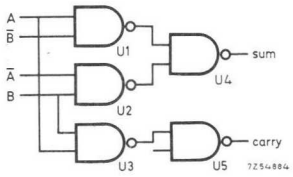


Fig. 69. Half adder using one FJH131.

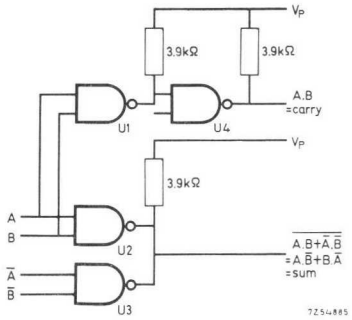
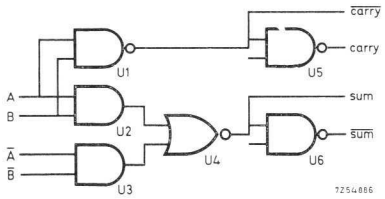
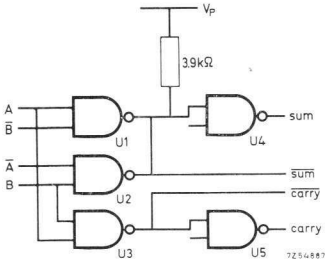


Fig. 70. Half adder using one FJH231.



$U_1 = U_5 = U_6 = \frac{1}{4}$FJH131
$U_2 + U_3 + U_4 = \frac{1}{2}$FJH161

Fig. 71. Half adder using AND-OR-NOT and NAND gates.



$U_1 + U_2 = \frac{1}{2}$FJH231
$U_3 = U_4 = U_5 = \frac{1}{4}$FJH131

Fig. 72. Half adder using NAND gates.

Truth Table

Inputs		Outputs	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The Boolean expressions for the sum and carry are:

$$S = A \cdot \bar{B} + B \cdot \bar{A}, \quad C = A \cdot B.$$

Full Adders

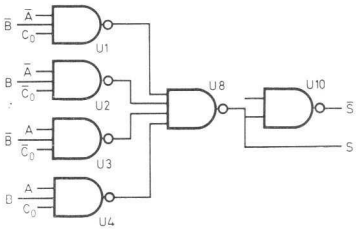
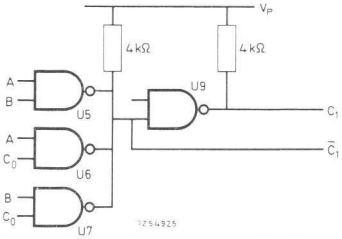


Fig. 73. Full adder using NAND gates.
$U_1 = U_2 = U_3 = U_4 = \frac{1}{3}$FJH121
$U_8 = \frac{1}{2}$FJH111
$U_{10} = \frac{1}{4}$FJH131



$U_5 + U_6 + U_7 + U_9 =$ FJH231

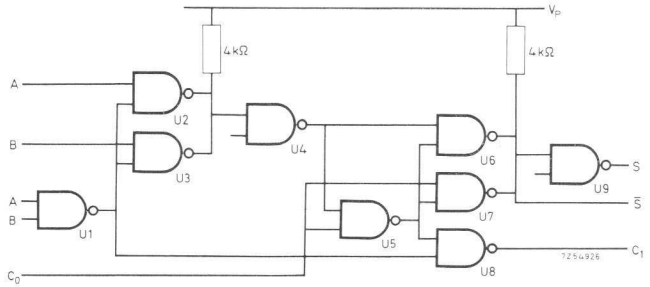


Fig. 74. Full adder using NAND gates.

$U_2 + U_3 + U_6 + U_7 =$ FJH231
$U_1 = U_4 = U_5 = U_8 = U_9 = \frac{1}{4}$FJH131

Truth Table

Inputs			Outputs	
C_0	A	B	S	C_1
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	1	0	0	1
1	0	1	0	1
1	1	1	1	1

The Boolean expressions for the sum and carry are:

$$S_1 = \overline{A} \cdot \overline{B} \cdot C_0 + \overline{A} \cdot B \cdot \overline{C}_0 + A \cdot \overline{B} \cdot \overline{C}_0 + A \cdot B \cdot C_0$$

$$C_1 = A \cdot B + A \cdot C_0 + B \cdot C_0$$

Four-Bit Binary Adder

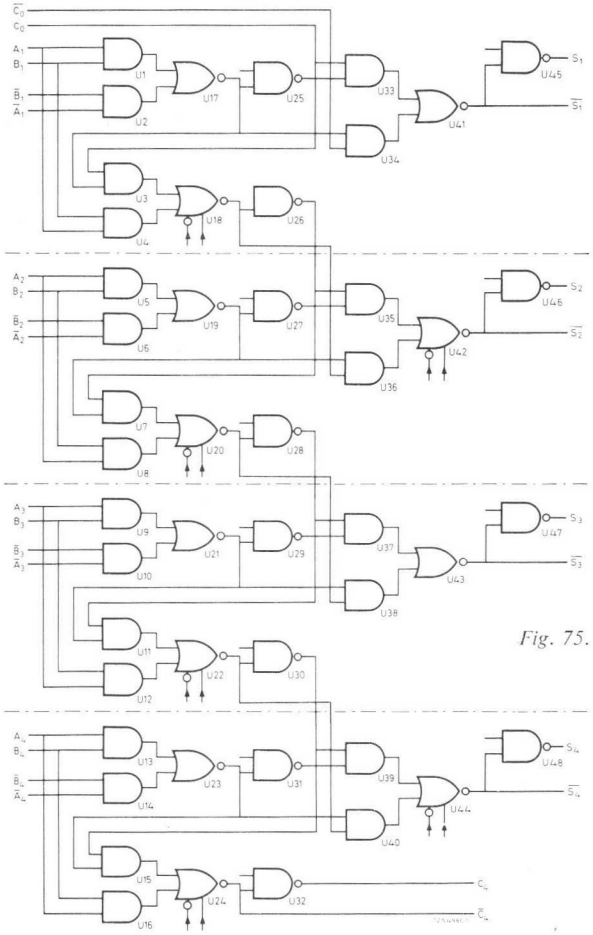


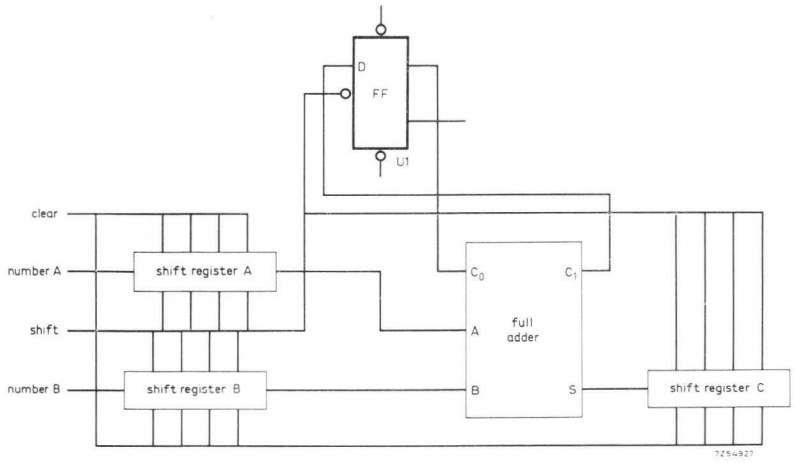
Fig. 75. Four-bit binary adder.

$U_1 + U_2 + U_3 + U_4 + U_{17} + U_{18} =$ FJH151
$U_5 + U_6 + U_7 + U_8 + U_{19} + U_{20} =$ FJH151
$U_9 + U_{10} + U_{11} + U_{12} + U_{21} + U_{22} =$ FJH151
$U_{13} + U_{14} + U_{15} + U_{16} + U_{23} + U_{24} =$ FJH151
$U_{33} + U_{34} + U_{35} + U_{36} + U_{41} + U_{42} =$ FJH151
$U_{37} + U_{38} + U_{39} + U_{40} + U_{43} + U_{44} =$ FJH151
$U_{25} + U_{26} + U_{27} + U_{28} = U_{29} + U_{30} + U_{31} + U_{32} =$ FJH131
$U_{45} + U_{46} + U_{47} + U_{48} =$ FJH131

Serial Adder

The carry signal is stored in the D bistable element. The input to shift registers A and B may be serial or parallel.

Three shift registers are shown although the sum could be stored in one of the input shift registers.



$U_1 = \frac{1}{2}$FJJ131

Fig. 76. Block diagram of serial adder. Shift registers A, B and C must change state at the same trigger edge as that of flip-flop U_1.

9. Counters

The FJ range of integrated bistable circuits can be used to make synchronous or asynchronous counters operating in any desired code and counting to any desired number.

If in an asynchronous counter the trigger input of each bistable circuit is connected to the output of the preceding bistable circuit, the result is a "ripple-through" of the count pulses, so that the last bistable circuit cannot change its state until all the preceding bistable circuits have changed state. The delay inherent in ripple-through counters is avoided in synchronous counters by using the outputs of bistable circuits as gating signals to the count pulses which are fed to all bistable circuits in the counter. In this way, all those stages that are required to change state when a particular count pulse arrives will change simultaneously.

The differences between synchronous and asynchronous counters are illustrated in Figs. 77 and 79, which show an asynchronous and a synchronous binary counter respectively.

The use of multiple-input J-K bistable elements simplifies gating and reduces the number of devices required.

Asynchronous Binary "Up Counter"

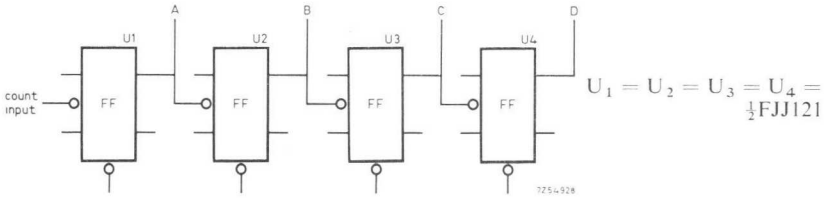


Fig. 77. Asynchronous binary "up counter".

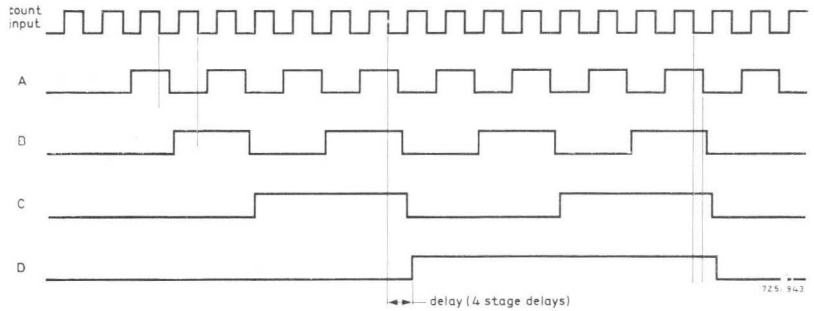


Fig. 78. Waveforms for asynchronous binary "up counter".

Truth Table

	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Synchronous Binary "Up Counter"

$U_1 = U_2 = U_3 = U_4 = FJJ111$

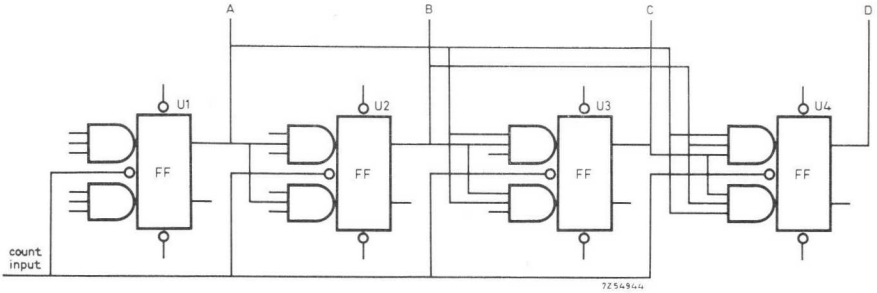


Fig. 79. Synchronous binary "up counter".

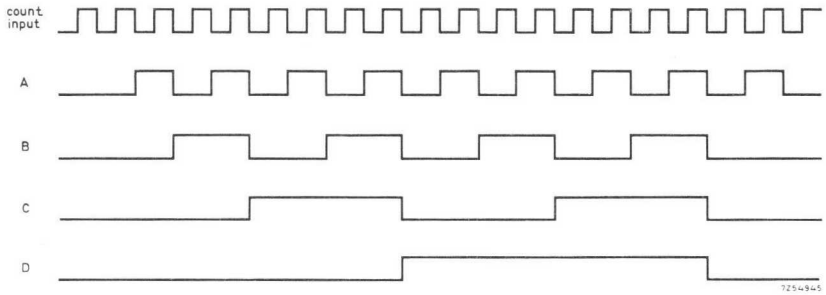
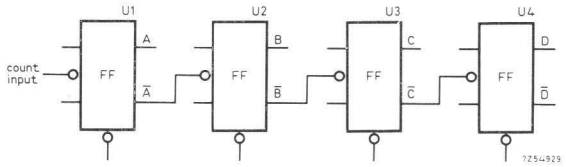


Fig. 80. Waveforms for synchronous binary "up counter".

Truth Table

	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Asynchronous Binary "Down Counter"



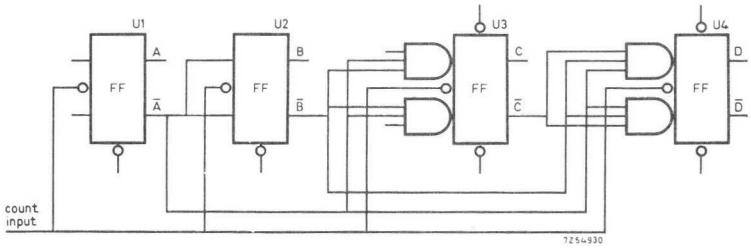
$U_1 = U_2 = U_3 = U_4 = \frac{1}{2}$FJJ121

Fig. 81. Asynchronous binary "down counter".

Truth Table

	D	C	B	A
0	0	0	0	0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1

Synchronous Binary "Down Counter"



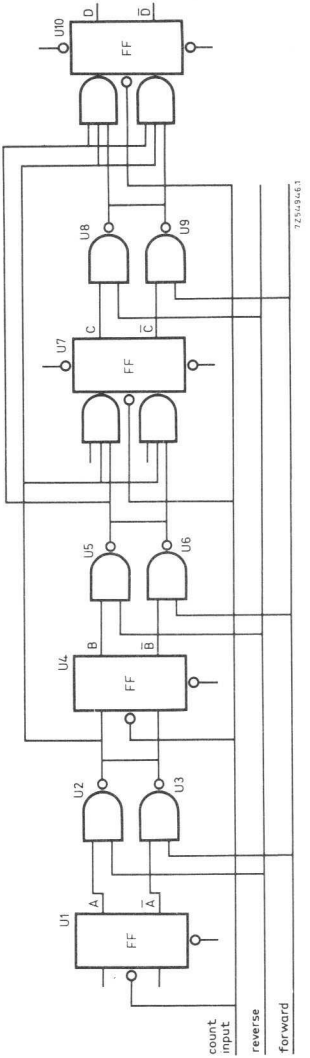
$U_1 + U_2 = FJJ121$
$U_3 = U_4 = FJJ111$

Fig. 82. Synchronous binary "down counter".

Truth Table

	D	C	B	A
0	0	0	0	0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1

Reversible Synchronous Binary Counter



$U_1 = U_4 = \frac{1}{2}$FJJ121
$U_7 = U_{10} =$ FJJ111

Fig. 83. Reversible synchronous binary counter.

Truth Table

	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Synchronous Modulo-3 "Up Counter"

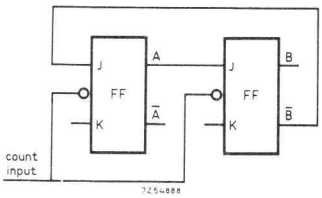
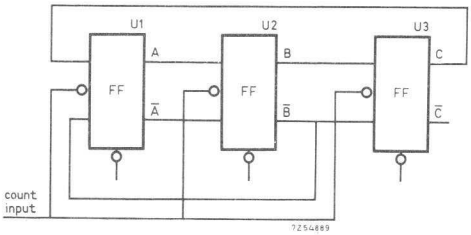


Fig. 84. Synchronous modulo-3 "up counter".

Truth Table

	B	A
0	0	0
1	0	1
2	1	0

Synchronous Unweighted Modulo-5 "Up Counter"



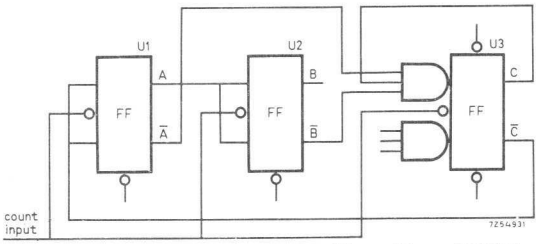
$U_1 = U_2 = U_3 = \frac{1}{2}$FJJ121

Fig. 85. Synchronous unweighted modulo-5 "up counter".

Truth Table

	C	B	A
0	0	0	0
1	0	0	1
2	0	1	1
3	1	1	0
4	1	0	0

Synchronous Modulo-5 "Up Counter"



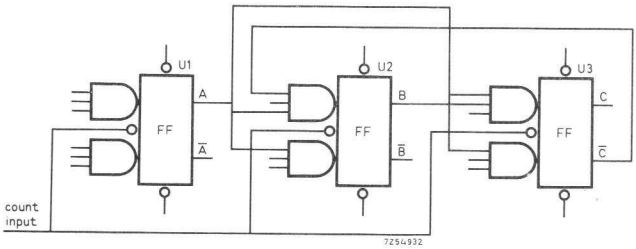
$U_1 + U_2 =$ FJJ121
$U_3 =$ FJJ11

Fig. 86. Synchronous modulo-5 "up counter".

Truth Table

	C	B	A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0

Synchronous Modulo-6 "Up Counter"



$U_1 = U_2 = U_3 = FJJ111$

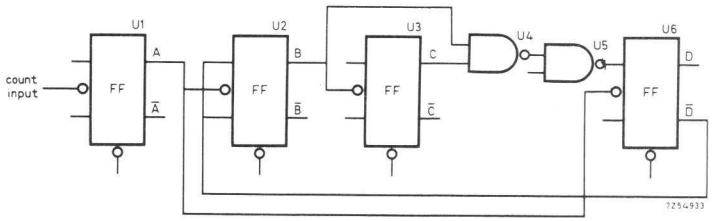
Fig. 87. Synchronous modulo-6 "up counter".

Truth Table

	C	B	A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1

Asynchronous 1248BCD "Up Counter"

Operating frequency $\geqslant$ 10MHz.



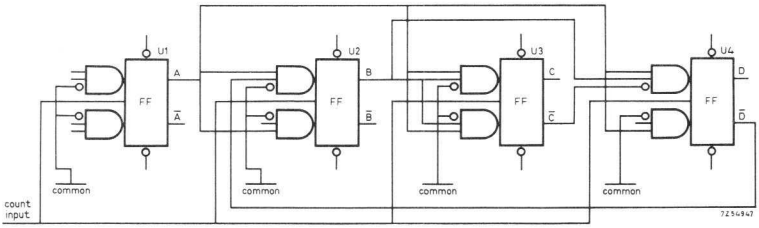
$U_1 = U_2 = U_3 = U_6 = \frac{1}{2}$FJJ121
$U_4 + U_5 = \frac{1}{2}$FJH131

Fig. 88. Asynchronous 1248BCD "up counter".

Truth Table

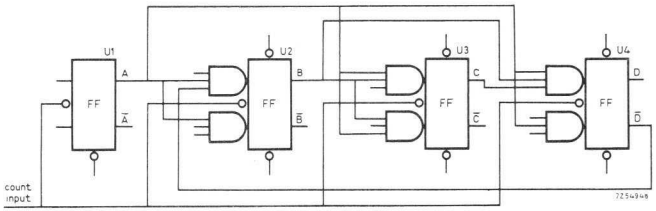
	D	C	B	A
	Weight = 8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Synchronous 1248BCD "Up Counters"



$U_1 = U_2 = U_3 = U_4 = FJJ101$

Fig. 89. Synchronous 1248BCD "up counter" using FJJ101 elements.



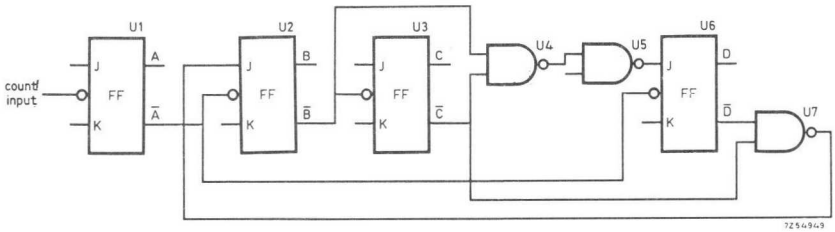
$U_1 = \frac{1}{2}FJJ121$
$U_2 = U_3 = U_4 = FJJ111$

Fig. 90. Synchronous 1248BCD "up counter" using FJJ111 and FJJ121 elements.

Truth Table

	D	C	B	A
Weight =	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Asynchronous 1248BCD "Down Counter"



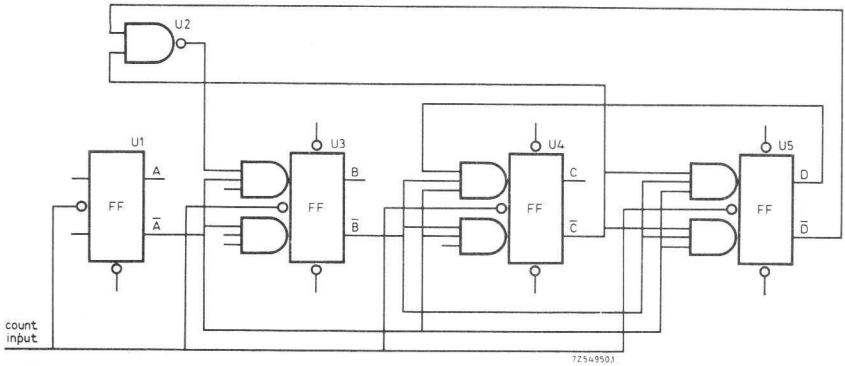
$U_4 = U_5 = U_7 = \frac{1}{4}$FJH131

Fig. 91. Asynchronous 1248BCD "down counter".

Truth Table

	D	C	B	A
Weight =	8	4	2	1
0	0	0	0	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1

Synchronous 1248BCD "Down Counter"



$U_1 = \frac{1}{2}$FJJ121 $\quad U_2 = \frac{1}{4}$FJH131
$U_3 = U_4 = U_5 =$ FJJ111

Fig. 92. Synchronous 1248BCD "down counter".

Truth Table

	D	C	B	A
Weight =	8	4	2	1
0	0	0	0	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1

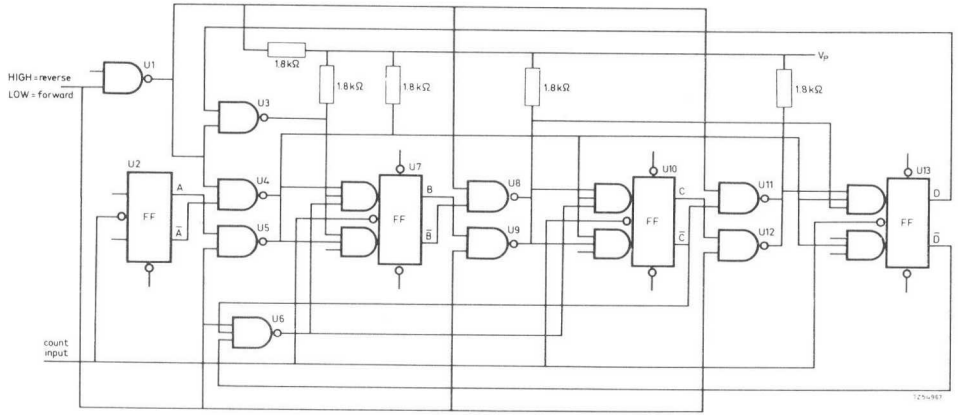


Fig. 93. Reversible 1248BCD counter using multiple-input J-K bistable elements and NAND gates.

Truth Table

	D	C	B	A
Weight =	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

$U_1 = U_3 = U_4 = U_5 = U_8 = U_9 = U_{11} = U_{12} = \frac{1}{4}$FJH231
$U_2 = \frac{1}{2}$FJJ121
$U6 = \frac{1}{3}$FJH121 $\quad U_7 = U_{10} = U_{13} =$ FJJ111

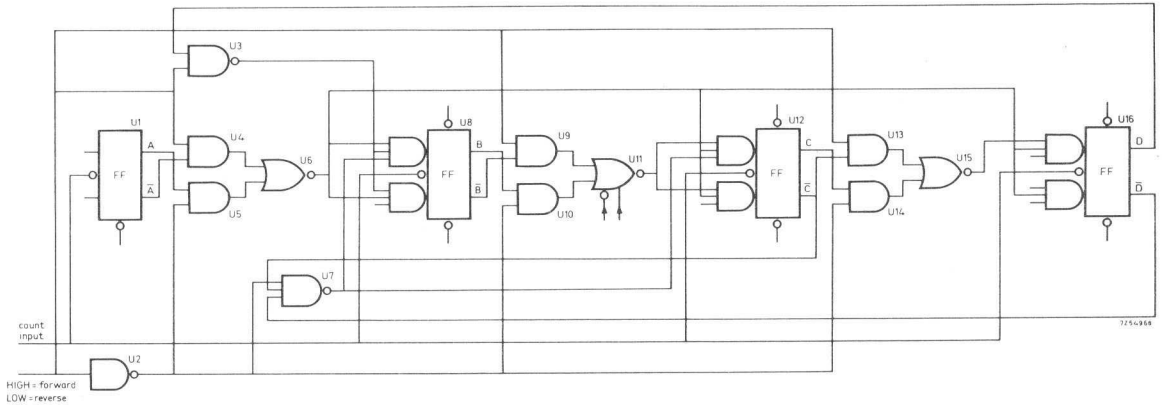


Fig. 94. Reversible 1248BCD counter using multiple-input J-K bistable elements, NAND gates and AND-OR-NOT gates.

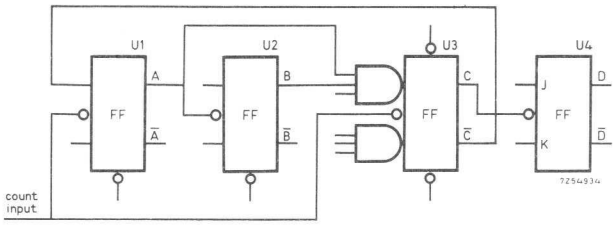
Truth Table

Weight =	D 8	C 4	B 2	A 1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

$U_8 = U_{12} = U_{16} =$ FJJ111
$U_4 + U_5 + U_6 + U_9 + U_{10} + U_{11} =$ FJH151
$U_{13} + U_{14} + U_{15} = \frac{1}{2}$FJH151
$U_1 = \frac{1}{2}$FJJ121

Asynchronous 1245BCD "Up Counter"

This is a divide-by-ten counter with symmetrical output at D.



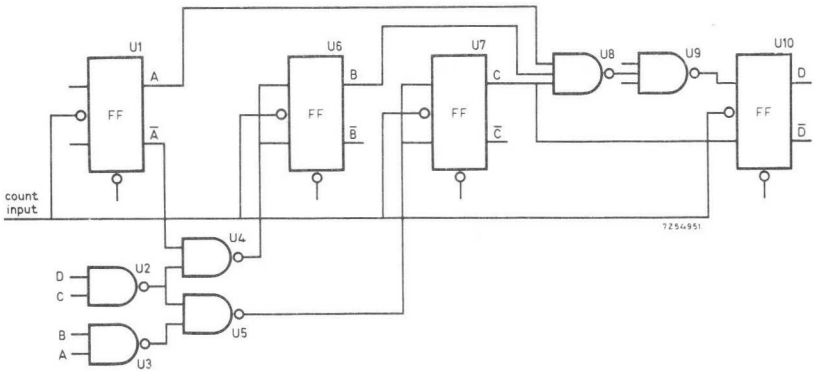
$U_1 + U_2 = FJJ121$
$U_3 = FJJ111$

Fig. 95. Asynchronous 1245BCD "up counter".

Truth Table

	D	C	B	A
Weight =	5	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	0	0

Synchronous Excess-Three Code "Up Counter"



$U_1 = U_6 = U_7 = U_{10} = \frac{1}{2}$FJJ121
$U_2 + U_3 + U_4 + U_5 =$ FJH131
$U_8 = U_9 = \frac{1}{3}$FJH121

Fig. 96. Excess-three code "up counter".

Truth Table

	D	C	B	A
0	0	0	1	1
1	0	1	0	0
2	0	1	0	1
3	0	1	1	0
4	0	1	1	1
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	0	0

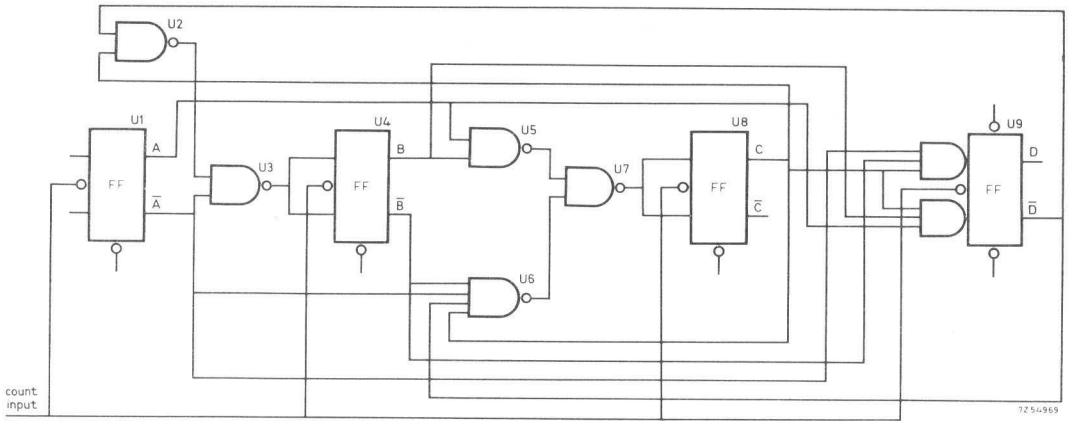


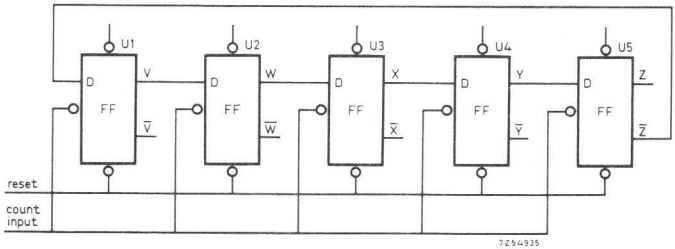
Fig. 97. Synchronous Aiken code "up counter".

Truth Table

	D	C	B	A
Weight =	2	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	1	0	1	1
6	1	1	0	0
7	1	1	0	1
8	1	1	1	0
9	1	1	1	1

$U_2 + U_3 + U_5 + U_7 = \text{FJH131}$
$U_1 = U_4 = U_8 = \frac{1}{2}\text{FJJ121}$
$U_9 = \text{FJJ111} \qquad U_6 = \frac{1}{2}\text{FJH111}$

Twisted-ring Counter



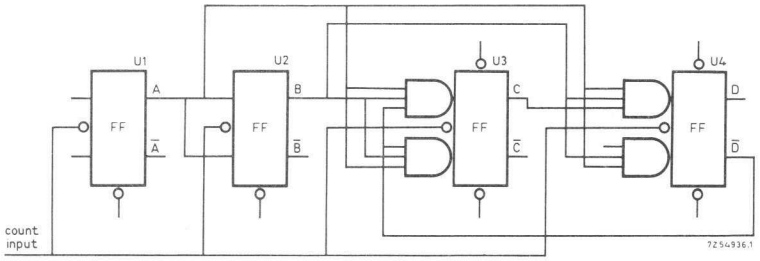
$U_1 = U_2 = U_3 = U_4 = U_5 = \frac{1}{2}$FJJ131

Fig. 98. Twisted-ring, counter.

Truth Table

	Z	Y	X	W	V
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	1
3	0	0	1	1	1
4	0	1	1	1	1
5	1	1	1	1	1
6	1	1	1	1	0
7	1	1	1	0	0
8	1	1	0	0	0
9	1	0	0	0	0

Synchronous 1248 Weighted "Up Counter" with a Cycle Length of Twelve



$U_1 + U_2 = FJJ121$
$U_3 = U_4 = FJJ111$

Fig. 99. Synchronous 1248 weighted counter with a cycle length of twelve.

Truth Table

	D	C	B	A
	Weight = 8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1

10. Counters using the FJJ141

The FJJ141 consists of four master-slave J-K bistable elements with internal gating which enables a count of ten to be obtained in two ways. Alternatively, counts of 2 and 5 may be obtained independently. While counting is in progress, pins 2 or 3 and 6 or 7 must be connected to the "common" line.

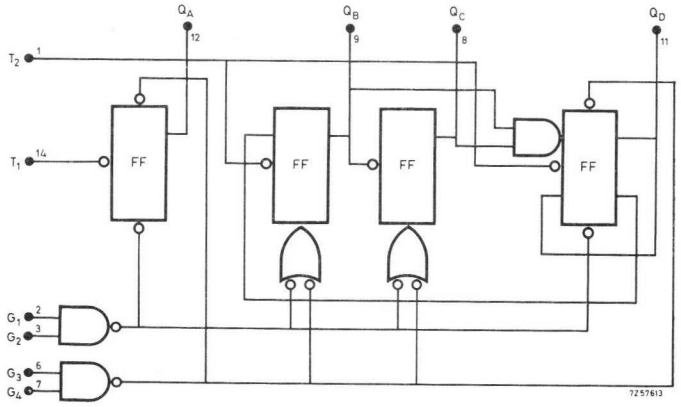


Fig. 100. Circuit diagram of FJJ141 element.

1248BCD Decade Counter

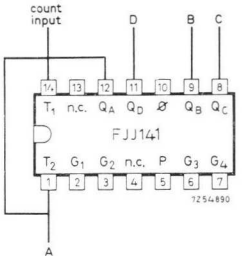


Fig. 101. The FJJ141 element connected as a 1248BCD decade counter.

Truth Table

	D	C	B	A
Weight =	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

To set to zero, pins 2 and 3 must be made HIGH.

Modulo-5 Counter

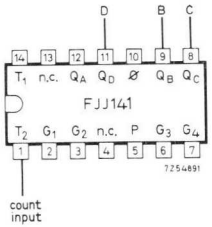


Fig. 102. The FJJ141 element used as a modulo-5 counter.

Truth Table

	D	C	B
	Weight = 4	2	1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0

To set to zero, pins 2 and 3 must be made HIGH.

The first bistable element in the unit may be used independently. The input to the first bistable element in the unit is pin 14 and the output pin 12.

1245BCD Counter

This is a divide-by-ten counter which gives a mark: space ratio of 1 : 1 on pin 12.

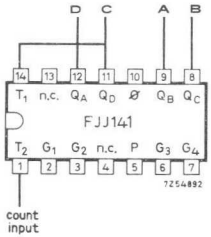


Fig. 103. The FJJ141 connected as a divide-by-ten counter counting in 1245BCD.

Truth Table

	D	C	B	A
Weight =	5	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	0	0

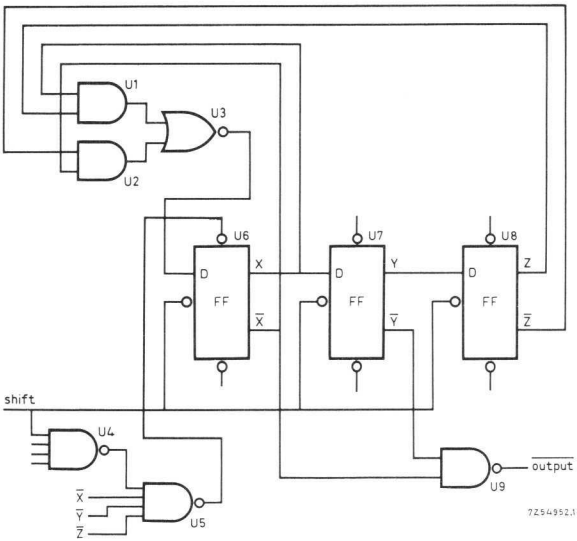
To set to zero, pins 2 and 3 must be made HIGH.

11. Chain Code Generators

Chain code generators, sometimes referred to as pseudo-random generators, are used to provide division by some whole number. Chain code generators are made by applying feedback to a shift register and feeding a LOW or a HIGH into the shift register, depending upon its current contents. The maximal code generators give a cycle length of 2^n-1 states, where n is the number of stages. Generators which do not generate the maximal code – that is, with cycle lengths of less than 2^n-1 – can easily be made by applying different feedbacks to the shift register. One example of this is the Johnson counter. In the event of each stage being in the LOW state when the counter is switched on, a gate is inserted to detect this condition and to set up the correct initial state.

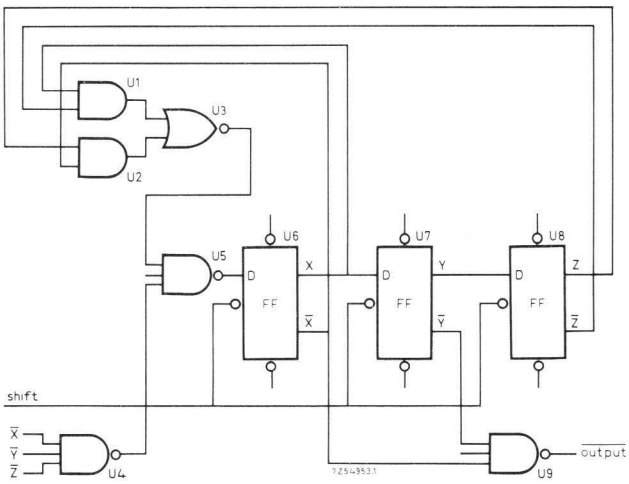
An alternative method of generating a shorter cycle length is to detect one state, by means of a gate, and use the output of the gate to set a different state in the chain code generator. This causes part of the normal sequence to be omitted, and thereby shortens the cycle length.

Three-Stage Chain Code Generators with Cycle Lengths of Seven



$U_1 + U_2 + U_3 = \frac{1}{2}$FJH151
$U_6 = U_7 = U_8 = \frac{1}{2}$FJJ131
$U_4 = U_5 = \frac{1}{2}$FJH111
$U_9 = \frac{1}{4}$FJH131

Fig. 104. Three-stage chain code generator with cycle length of seven.



$U_1 + U_2 + U_3 = \frac{1}{2}$FJH151
$U_4 = U_5 = U_9 = \frac{1}{3}$FJH121
$U_6 = U_7 = U_8 = \frac{1}{2}$FJJ131

Fig. 105. Alternative three-stage chain code generator with cycle length of seven.

Truth Table

Z	Y	X	F
0	0	1	1
0	1	1	1
1	1	1	0
1	1	0	1
1	0	1	0
0	1	0	0
1	0	0	1

The Boolean expression for the feedback factor, F, is given by

$$F = \overline{X} \cdot Z + X \cdot \overline{Z}.$$

Four-Stage Chain Code Generator with Cycle Length of Fifteen

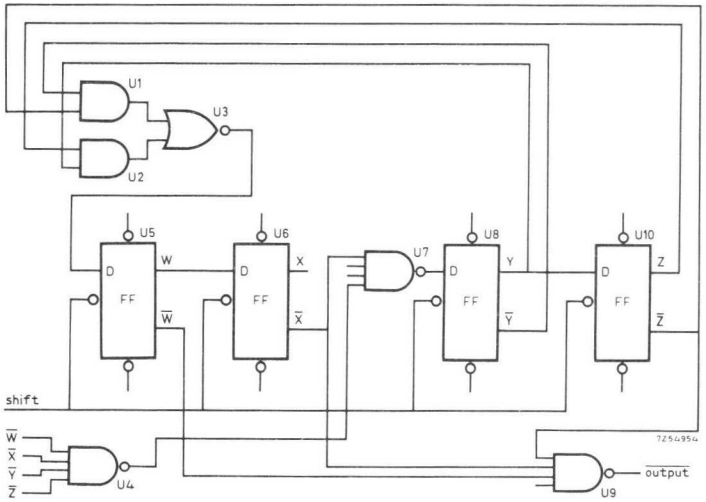


Fig. 106. Four-stage chain code generator with cycle length of fifteen.

$U_1 + U_2 + U_3 = \frac{1}{2}$FJH151
$U_5 = U_6 = U_8 = U_{10} = \frac{1}{2}$FJJ131
$U_4 = U_7 = U_9 = \frac{1}{2}$FJH111

Truth Table

Z	Y	X	W	F
0	1	0	0	1
1	0	0	1	1
0	0	1	1	0
0	1	1	0	1
1	1	0	1	0
1	0	1	0	1
0	1	0	1	1
1	0	1	1	1
0	1	1	1	1
1	1	1	1	0
1	1	1	0	0
1	1	0	0	0
1	0	0	0	1
0	0	0	1	0
0	0	1	0	0

The Boolean expression for the feedback factor, F, is given by

$$F = Y \cdot \overline{Z} + \overline{Y} \cdot Z.$$

Alternative Four-Stage Generator with Cycle Length of Fifteen

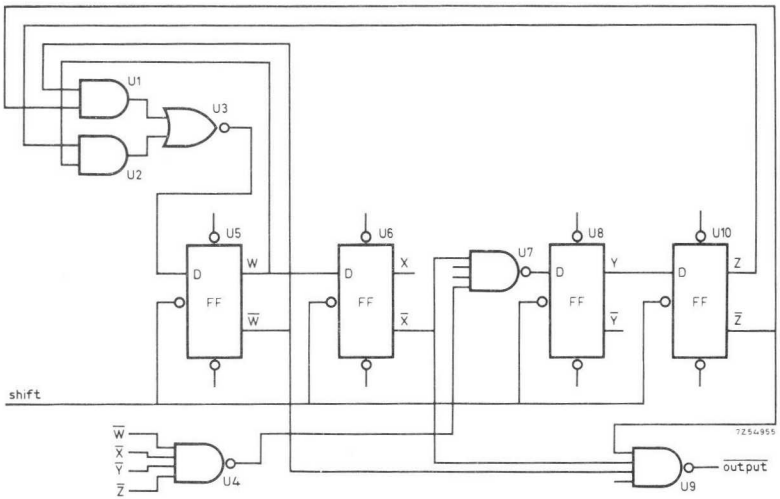


Fig. 107. Alternative four-stage chain code generator with cycle length of fifteen.

$U_1 + U_2 + U_3 = \frac{1}{2}$FJH151
$U_5 = U_6 = U_8 = U_{10} = \frac{1}{2}$FJJ131
$U_4 = U_7 = U_9 = \frac{1}{2}$FJH111

Truth Table

Z	Y	X	W	F
0	1	0	0	0
1	0	0	0	1
0	0	0	1	1
0	0	1	1	1
0	1	1	1	1
1	1	1	1	0
1	1	1	0	1
1	1	0	1	0
1	0	1	0	1
0	1	0	1	1
1	0	1	1	0
0	1	1	0	0
1	1	0	0	1
1	0	0	1	0
0	0	1	0	0

The Boolean expression for the feedback factor, F, is given by

$$F = \overline{W} \cdot Z + W \cdot \overline{Z}.$$

Chain Code Generator with Shortened Cycle Length

Four stages, cycle length of six.

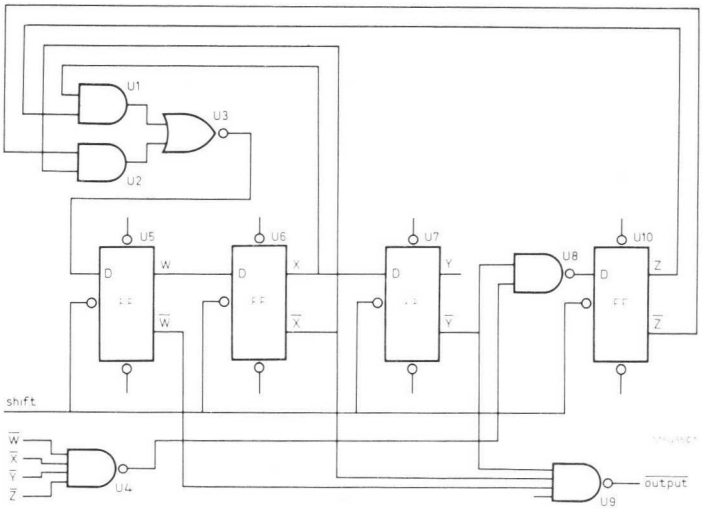


Fig. 108. Example of a chain code generator with cycle length of less than 2^n-1.

$U_1 + U_2 + U_3 = \frac{1}{2}$FJH151
$U_5 = U_6 = U_7 = U_{10} = \frac{1}{2}$FJJ131
$U_4 = U_9 = \frac{1}{2}$FJH111
$U_8 = \frac{1}{4}$FJH131

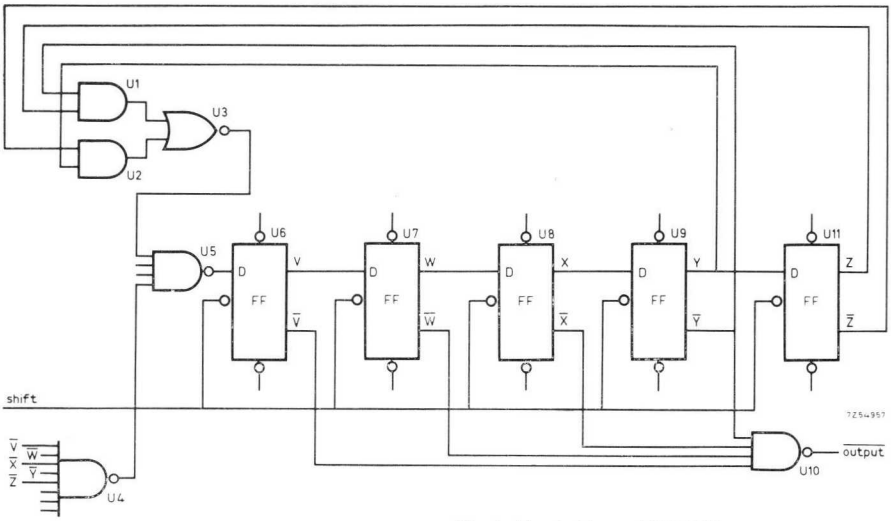
Truth Table

Z	Y	X	W	F
0	0	0	1	0
0	0	1	0	1
0	1	0	1	0
1	0	1	0	0
0	1	0	0	0
1	0	0	0	1

The Boolean expression for the feedback factor, F, is given by

$$F = \overline{X} \cdot Z + X \cdot \overline{Z}.$$

Five-Stage Chain Code Generator with Cycle Length of 31



$U_1 + U_2 + U_3 = \frac{1}{2}$FJH151
$U_6 = U_7 = U_8 = U_9 = U_{11} = \frac{1}{2}$FJJ131
$U_4 =$ FJH101
$U_5 = U_{10} = \frac{1}{2}$FJH111

Fig. 109. Five-stage chain code generator with cycle length of 31.

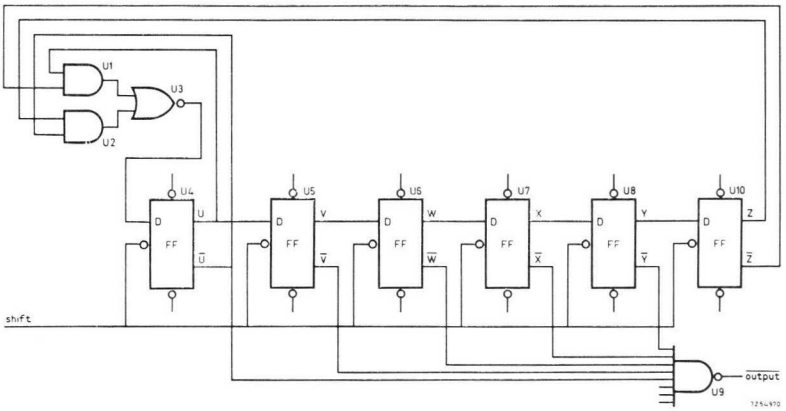
Truth Table

Z	Y	X	W	V	F
0	0	0	0	1	0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	1	0	1
0	0	1	0	1	1
0	1	0	1	1	0
1	0	1	1	0	0
0	1	1	0	0	1
1	1	0	0	1	1
1	0	0	1	1	1
0	0	1	1	1	1
0	1	1	1	1	1
1	1	1	1	1	0
1	1	1	1	0	0
1	1	1	0	0	0
1	1	0	0	0	1
1	0	0	0	1	1
0	0	0	1	1	0
0	0	1	1	0	1
0	1	1	0	1	1
1	1	0	1	1	1
1	0	1	1	1	0
0	1	1	1	0	1
1	1	1	0	1	0
1	1	0	1	0	1
1	0	1	0	1	0
0	1	0	1	0	0
1	0	1	0	0	0
0	1	0	0	0	0
1	0	0	0	0	1

The Boolean expression for the feedback factor, F, is given by

$$F = X \cdot \bar{Z} + \bar{X} \cdot Z.$$

Six-Stage Chain Code Generator with Cycle Length of 63



$U_1 + U_2 + U_3 = \frac{1}{2}$FJH151 $\qquad U_9 =$ FJH101
$U_4 = U_5 = U_6 = U_7 = U_8 = U_{10} = \frac{1}{2}$FJJ131

Fig. 110. Six-stage chain code generator with cycle length of 63.

Truth Table

Z	Y	X	W	V	U	F
0	0	0	0	0	1	1
0	0	0	0	1	1	1
0	0	0	1	1	1	1
0	0	1	1	1	1	1
0	1	1	1	1	1	1
1	1	1	1	1	1	0
1	1	1	1	1	0	1
1	1	1	1	0	1	0
1	1	1	0	1	0	1
1	1	0	1	0	1	0
1	0	1	0	1	0	1
0	1	0	1	0	1	1
1	0	1	0	1	1	0
0	1	0	1	1	0	0
1	0	1	1	0	0	1
0	1	1	0	0	1	1
1	1	0	0	1	1	0
1	0	0	1	1	0	1
0	0	1	1	0	1	1
0	1	1	0	1	1	1
1	1	0	1	1	1	0
1	0	1	1	1	0	1
0	1	1	1	0	1	1
1	1	1	0	1	1	0
1	1	0	1	1	0	1
1	0	1	1	0	1	0
0	1	1	0	1	0	0
1	1	0	1	0	0	1
1	0	1	0	0	1	0
0	1	0	0	1	0	0
1	0	0	1	0	0	1
0	0	1	0	0	1	1

continued

Truth Table (continuation)

Z	Y	X	W	V	U	F
0	1	0	0	1	1	1
1	0	0	1	1	1	0
0	0	1	1	1	0	0
0	1	1	1	0	0	0
1	1	1	0	0	0	1
1	1	0	0	0	1	0
1	0	0	0	1	0	1
0	0	0	1	0	1	1
0	0	1	0	1	1	1
0	1	0	1	1	1	1
1	0	1	1	1	1	0
0	1	1	1	1	0	0
1	1	1	1	0	0	1
1	1	1	0	0	1	0
1	1	0	0	1	0	1
1	0	0	1	0	1	0
0	0	1	0	1	0	0
0	1	0	1	0	0	0
1	0	1	0	0	0	1
0	1	0	0	0	1	1
1	0	0	0	1	1	0
0	0	0	1	1	0	0
0	0	1	1	0	0	0
0	1	1	0	0	0	0
1	1	0	0	0	0	1
1	0	0	0	0	1	0
0	0	0	0	1	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
1	0	0	0	0	0	1

The Boolean expression for the feedback factor, F, is given by

$$F = \bar{U} \cdot Z + U \cdot \bar{Z}.$$

Six-Stage Chain Code Generator with Cycle Length of Twelve

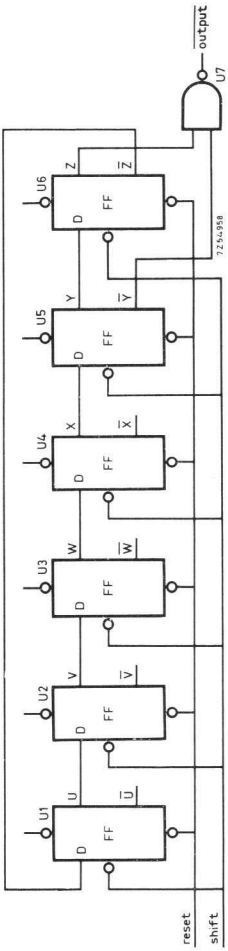


Fig. 111. Six-stage code generator with cycle length of twelve.

$U_1 = U_2 = U_3 = U_4 = U_5 = U_6 = \frac{1}{2}FJJ131$
$U_7 = \frac{1}{4}FJH131$

Truth Table

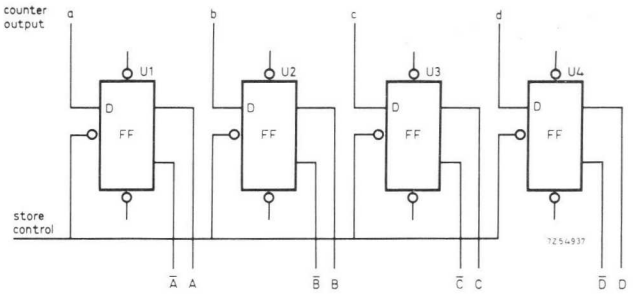
Z	Y	X	W	V	U
0	0	0	0	0	0
0	0	0	0	0	1
0	0	0	0	1	1
0	0	0	1	1	1
0	0	1	1	1	1
0	1	1	1	1	1
1	1	1	1	1	0
1	1	1	1	0	0
1	1	1	0	0	0
1	1	0	0	0	0
1	0	0	0	0	0

12. Gated Staticisers

A gated staticiser is for use between a source of information which is to be sampled – such as a counter, shift register, or adder – and a store or indicator. The purpose of the gated staticiser is to sample information and hold it until the next sampling time. A signal on the store control line enables information to be transferred from the counter to the staticiser.

A common example of the use of gated staticisers is in counting instruments where the contents of the last count must be displayed while the current count is in progress.

Gated Staticisers



$U_1 = U_2 = U_3 = U_4 = \frac{1}{2}$FJJ131

Fig. 112. Gated staticiser using D bistable elements for use between a four-bit counter and a decoder.

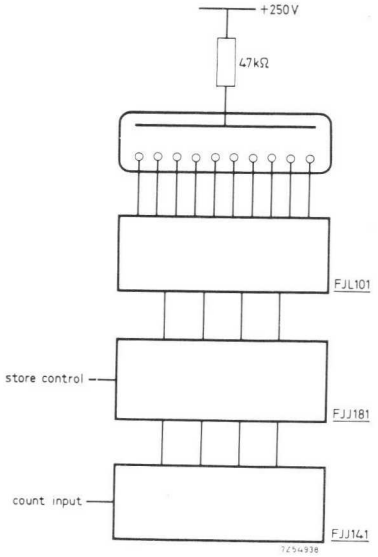


Fig. 113. Block diagram illustrating use of quadruple D bistable element FJJ181 as gated staticiser in conjunction with a decade counter and a numerical indicator tube driver.

13. Monostable Circuits

A monostable circuit is sometimes known as a "one-shot" multivibrator. Its chief function is as a timing circuit because it gives a pulse of any required length when triggered by something less predictable – for example, a manually operated push-button.

Three-Gate Monostable Circuits

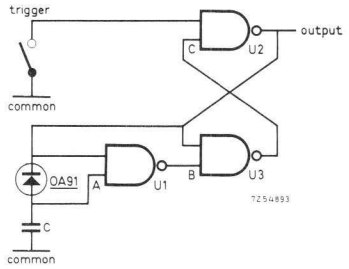


Fig. 114. Three-gate monostable circuit without triggering circuit.

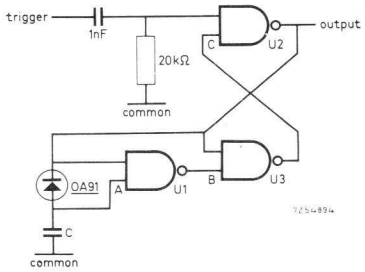


Fig. 115. Three-gate monostable circuit with triggering circuit.

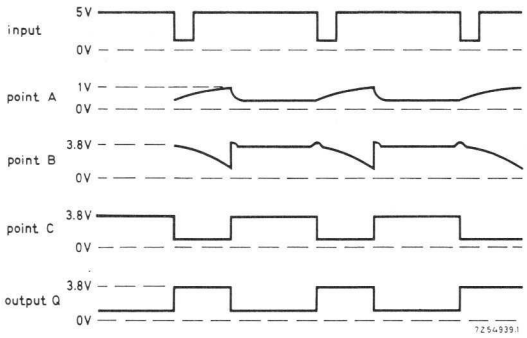


Fig. 116. Waveforms for three-gate monostable circuits.

Performance of Three-Gate Monostable Circuit

C	Pulse duration
1 μF	1.5 ms
100 nF	140 μs
10 nF	15 μs
1 nF	1.4 μs
100 pF	140 ns

The pulse width is independent of frequency down to a duty cycle of 1 : 1.

The triggering circuit incorporated in Fig. 115 responds to negative-going pulses. For 3 V amplitude, the fall rate can be as slow as 0.1 μs/V with a triggering capacitor of 100 pF. The advantage of this triggering method is that the trigger pulse can be of a longer duration than the output pulse of the monostable circuit.

The stability of the pulse duration, despite variations in supply voltage, is such that a 10% increase in supply voltage causes the pulse duration to decrease by about 6%. The stability despite variations in temperature is such that an increase of 20 °C above room temperature causes the pulse duration to increase by about 3%.

During the time in which the voltage at point C is changing, the noise margin is diminishing. At the instant before the end of the output pulse, the noise margin becomes zero.

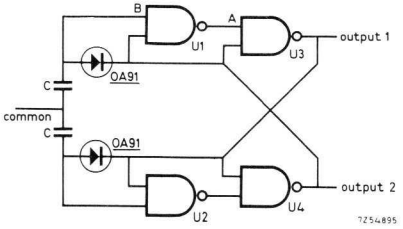
14. Multivibrators

A multivibrator is a square-wave oscillator used for generating a continuous supply of pulses. Because multivibrators are used as sources of clock pulses, they are frequently required to have a very high fan-out, making the use of a line-driver gate necessary.

With a basic multivibrator circuit there is the possibility that, if both timing capacitors become charged simultaneously, no oscillation occurs. To overcome this difficulty a self-starter gate may be incorporated.

The stability of the frequency, despite variations in supply voltage and temperature, is similar to that of the monostable circuits described in Chapter 13.

Four-Gate Multivibrators



$U_1 + U_2 + U_3 + U_4 = \text{FJH131}$

Fig. 117. Four-gate multivibrator.

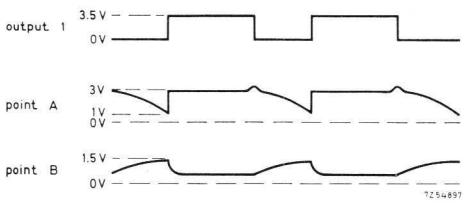
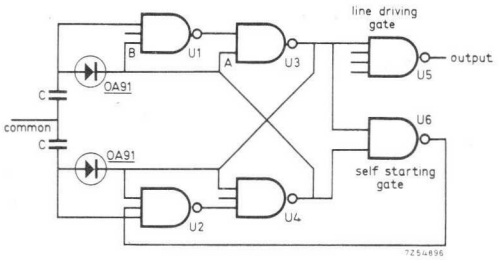


Fig. 118. Waveforms for four-gate multivibrator with a value of C of 100 nF.



$U_1 + U_2 + U_4 = \text{FJH121}$
$U_3 + U_6 = \frac{1}{2}\text{FJH131}$
$U_5 = \frac{1}{2}\text{FJH141}$

Fig. 119. Four-gate multivibrator with self-starter gate and line driver.

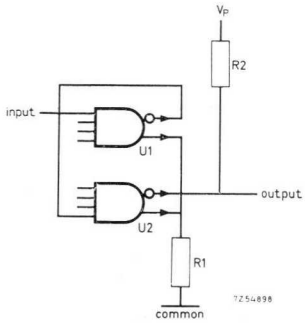
Performance

C	Maximum frequency
1 μF	330 Hz
100 nF	3.3 kHz
10 nF	33 kHz
1 nF	330 kHz
100 pF	3.3 MHz
33 pF	10 MHz

15. Level Detectors

A level detector, or Schmitt trigger, is a bistable circuit which changes state in accordance with the d.c. input level, producing a fast switching action irrespective of the rate of change of the input voltage. This action is useful for pulse shaping or reforming after the pulse has been degraded by other circuits. Another example of its use is voltage-sensitive switching of relays or lamps where it is essential because of power dissipation problems that the output transistor must operate only in the cut-off or bottomed states.

Level Detector



$U_1 + U_2 = FJY101$

Fig. 120. Level detector using FJY101.

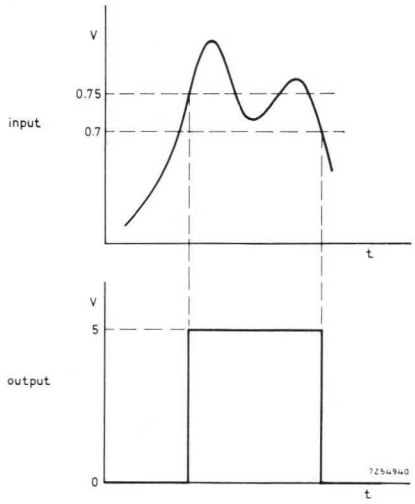


Fig. 121. Performance of level detector with values of R_1 and R_2 of 56 Ω and 3.3 kΩ respectively, and a fan-out of 1.

Technology relating to the products described in this publication is shared by the following companies.

Argentina
FAPESA I.y.C.
Melincué 2594
Tel. 50-9941/8155
BUENOS AIRES

Australia
Philips Industries Ltd.
Miniwatt Electronics Division
20, Herbert St.
Tel. 43-2171
ARTARMON, N.S.W.

Austria
WIVEG
Zieglergasse 6
Tel. 93 26 22
1072 WIEN

Belgium
M.B.L.E.
80, rue des Deux Gares
Tel. 23 00 00
1070 BRUSSELS

Brazil
IBRAPE S.A.
Av. Paulista, 2073-S/Loja
Tel. 93-5141
SAO PAULO

Canada
Philips Electron Devices
116, Vanderhoof Ave.
Tel. 425-5161
TORONTO 17, Ontario

Chile
Philips Chilena S.A.
Av. Santa Maria 0760
Tel. 39 40 01
SANTIAGO

Colombia
SADAPE S.A.
Calle 19, No. 5-51
Tel. 422-175
BOGOTA D.E. 1

Denmark
Miniwatt A/S
Emdrupvej 115A
Tel. (01) 69 16 22
DK-2400 KØBENHAVN NV

Finland
Oy Philips A.B.
Elcoma Division
Kaivokatu 8
Tel. 10 915
HELSINKI 10

France
R.T.C.
La Radiotechnique-Compelec
Avenue Ledru Rollin 130
Tel. 797-99-30
PAR S 11

Germany
VALVO G.m.b.H.
Valvo Haus
Burchardstrasse 19
Tel. (0411) 33 91 31
2 HAMBURG 1

Greece
Philips S.A. Hellénique
Elcoma Division
52, Av. Syngrou
Tel. 915.311
ATHENS

Hong Kong
Philips Hong Kong Ltd.
Components Dept.
St. George's Building 21st Fl.
Tel. K-42 82 05
HONG KONG

India
INBELEC Div. of Philips India Ltd.
Band Box House
254-D, Dr. Annie Besant Road
Tel. 45 33 86, 45 64 20, 45 29 86
Worli, BOMBAY 18 (WB)

Indonesia
P.T. Philips-Ralin Electronics
Elcoma Division
Djalan Gadjah Mada 18
Tel. 44 163
DJAKARTA

Ireland
Philips Electrical (Ireland) Ltd.
Newstead, Clonskeagh
Tel. 69 33 55
DUBLIN 14

Italy
Philips S.p.A.
Sezione Elcoma
Piazza IV Novembre 3
Tel. 69 94
MILANO

Japan
NIHON PHILIPS
32nd Fl., World Trade Center Bldg.
5, 3-chrome, Shiba Hamamatsu-cho
Minato-ku,
Tel. (435) 5204-5
TOKYO

Mexico
Electronica S.A. de C.V.
Varsovia No. 36
Tel. 5-33-11-80
MEXICO 6, D.F.

Netherlands
Philips Nederland N.V.
Afd. Elonco
Boschdijk, VB
Tel. (040) 43 33 33
EINDHOVEN

New Zealand
EDAC Ltd.
70-72 Kingsford Smith Street
Tel. 873 159
WELLINGTON

Norway
Electronica A/S
Middelthunsgate 27
Tel. 46 39 70
OSLO 3

Peru
CADESA
Av. Abancay 1176
Offs. 606-607
Tel. 7 73 17
LIMA

Portugal
Philips Portuguesa S.A.R.L.
Rua Joaquim Antonio de Aguiar 66
Tel. 68 31 21/9
LISBOA

South Africa
EDAC (Pty) Ltd.
P.O. Box 23131
Tel. 24/6701
JOHANNESBURG

Spain
COPRESA S.A.
Balmes 22
Tel. 2 32 03 00
BARCELONA 7

Sweden
ELCOMA A.B.
Lidingövägen 50
Tel. 08/67 97 80
10250 STOCKHOLM 27

Switzerland
Philips A.G.
Edenstrasse 20
Tel. 051/44 22 11
CH-8027 ZUERICH

Taiwan
Philips Taiwan Ltd.
Elcoma Div.
Plastic Building, 10th Fl.
No. 1, section 2, Nanking East Rd.
Tel. 55 97 42
TAIPEI

Turkey
Turk Philips Ticaret A.S.
EMET Department
Gümüssuyu Cad. 78-80
Tel. 45.32.50
Beyoglü, ISTANBUL

United Kingdom
Mullard Ltd.
Mullard House
Torrington Place
Tel. 01-580 6633
LONDON WC1E 7HD

United States
Amperex Electronic Corp.
Sem. and Microcircuits Div.
Tel. 401-762-9000
SLATERSVILLE R.I. 02876

Uruguay
Luzilectron S.A.
Rondeau 1567, piso 5
Tel. 9 43 21
MONTEVIDEO

Venezuela
C.A. Philips Venezolana
Elcoma Department
Colinas de Bello Monte
Tel. 72.01.51
CARACAS

R

Printed in The Netherlands

③ ⑤ ⑥ ⑦ 1-'71

9399 253 03501