PHILIPS

DATA HANDBOOK

ELECTRONIC COMPONENTS AND MATERIALS

COMPONENTS AND MATERIALS

PART 1 SEPTEMBER 1970

Circuit blocks

Input/output devices

COMPONENTS AND MATERIALS

Part 1 **September 1970**

For comprehensive contents list see back

DATA HANDBOOK SYSTEM

To provide you with a comprehensive source of information on electronic components, subassemblies and materials, our Data Handbook System is made up of three series of handbooks, each comprising several parts.
The three series, identified by the colours noted, are:

ELECTRON TUBES (9 parts) BLUE

SEMICONDUCTORS AND INTEGRATED CIRCUITS (5 parts) RED

COMPONENTS AND MATERIALS (5 parts) GREEN

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued annually; the contents of each series are summarized on the following pages.
We have made every effort to ensure that each series is as accurate, comprehensive and up-to-date as possible, and we hope you will find it to be a valuable source of reference. Where ratings or specifications quoted differ from those published in the preceding edition they will be pointed out by arrows. You will understand that we can not guarantee that all products listed in any one edition of the handbook will remain available, or that their specifications will not be changed, before the next edition is published. If you need confirmation that the pusblished data about any of our products are the latest available, may we ask that you contact our representative. He is at your service and will be glad to answer your inquiries.

January 1970

ELECTRON TUBES (BLUE SERIES)

This series consists of the following parts, issued on the dates indicated.

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Transmitting tubes (Tetrodes, Pentodes)
Associated accessories

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Special Quality tubes
Miscellaneous devices

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Part 5 — **May 1970**

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Voltage stabilizing and reference tubes
Counter, selector, and indicator tubes
Trigger tubes
Switching diodes
Thyratrons
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Part 8 — **August 1970**

T.V. Picture tubes

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Variable capacitance diodes
Voltage regulator diodes
Rectifier diodes
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Rectifier stacks
Accessories
Heatsinks

Part 2 Low frequency; Deflection — **October 1969**

General
Low frequency transistors (low power)
Low frequency power transistors
Deflection transistors
Accessories

Part 3 High frequency; Switching — **November 1969**

General
High frequency transistors
Switching transistors
Accessories

Part 4 Special types — **December 1969**

General
Transmitting transistors
Field effect transistors
Dual transistors
Diodes and transistors for thick-and thin-film circuits
Photo devices
Accessories

Part 5 Integrated Circuits — **February 1970**

General
Digital integrated circuits
- FC family; standard temperature range
- FC family; extended temperature range
- FD family
- FJ family; standard temperature range

Linear integrated circuits

COMPONENTS AND MATERIALS (GREEN SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1 Circuit Blocks, Input/Output Devices — **September 1970**

Circuit blocks 100kHz Series
Circuit blocks 1-Series
Circuit blocks 10-Series
Circuit blocks 20-Series
Circuit blocks 40-Series
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Norbits 60-Series, 61-Series
Circuit blocks 90-Series
Circuit blocks for ferrite core memory drive
Input/output devices

Part 2 Resistors, Capacitors — **November 1969**

Fixed resistors
Variable resistors
Non-linear resistors
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Electrolytic capacitors
Variable capacitors

Part 3 Radio, Audio, Television — **January 1970**

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Components for colour television
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Part 4 Magnetic Materials, White Ceramics — **March 1970**

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Part 5 Memory Products, Magnetic Heads, Quartz Crystals, Microwave Devices, Variable Transformers, Electro-mechanical Components — **June 1970**

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Variable mains transformers
Electro-mechanical components

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Preface

Circuit blocks offer their user a number of important advantages; paramount among these are simplicity and greater reliability at lower cost. Principally for these reasons they have gained almost universal acceptance among designers and manufacturers of electronic equipment.

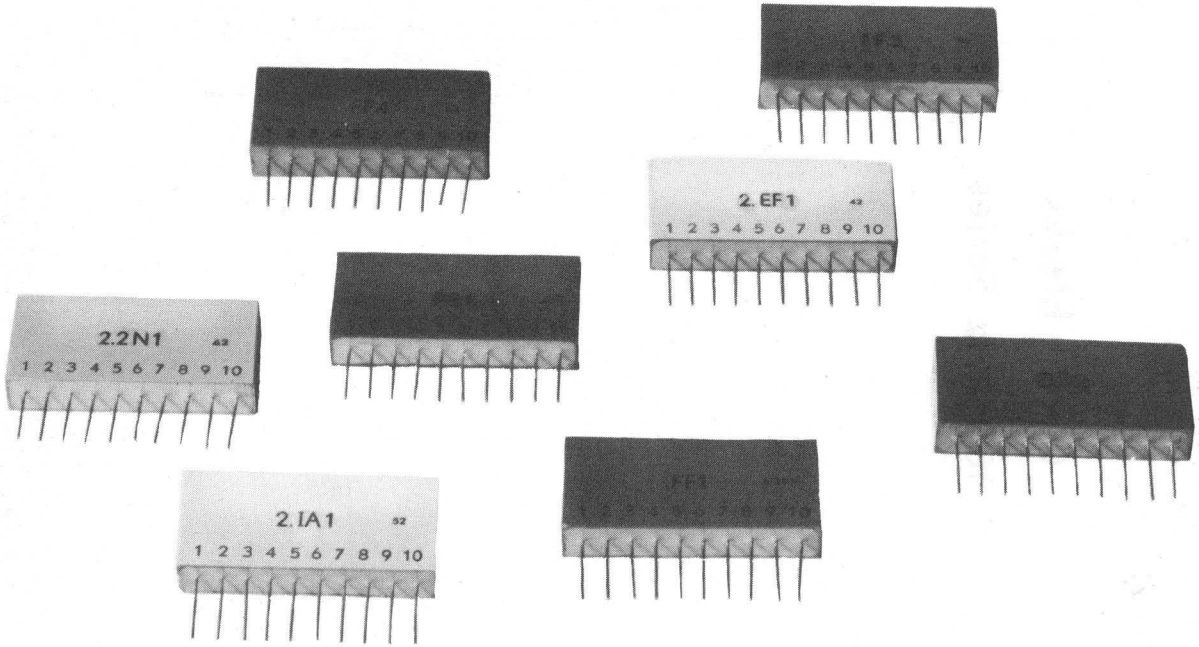
We have developed a comprehensive range of circuit blocks, ranging in capability from low-speed industrial logic to medium-speed computer logic functions.

This part of the Handbook gives the essential operational information about the various series of our circuit blocks. There is one chapter for each series; at the end of each chapter the user will find the description of the appropriate accessories. The final chapter is devoted to input/output devices.

The fundamentals of logic circuits and the use of functional blocks therein are discussed in the publication Logic Elements in Digital Equipment (No. 32/048). Our engineering staff will also be pleased to furnish supplementary information or application assistance on request.

Circuit blocks

100 kHz Series



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INTRODUCTION

A circuit block is a small encapsulated unit containing a basic electronic circuit, designed to accept and operate upon a specific type of input signal and to produce a specific type of electrical output. A number of different blocks can be combined to form larger parts of an electronic digital system.

In this series the following units and assembled panels are available:

description	colour	abbreviation	catalog number	page
Flip-flop	red	FF1	2722 001 00001	A57
Flip-flop	red	FF2	2722 001 00011	A61
Flip-flop	red	FF3	2722 001 00021	A65
Flip-flop	red	FF4	2722 001 00031	A69
Dual 3-input negative gate	orange	2.3N1	2722 001 01001	A73
Dual 2-input negative gate	orange	2.2N1	2722 001 01011	A75
Dual 3-input positive gate	orange	2.3P1	2722 001 02001	A77
Dual 2-input positive gate	orange	2.2P1	2722 001 02011	A79
Dual pulse logic	orange	2.PL1	2722 001 03001	A81
Dual pulse logic	orange	2.PL2	2722 001 03011	A85
Emitter follower/inverter amplifier	yellow	EF1/IA1	2722 001 07001	A89
Dual emitter follower	yellow	2.EF1	2722 001 05001	A91
Dual inverter amplifier	yellow	2.IA1	2722 001 06001	A95
Dual emitter follower	yellow	2.EF2	2722 001 05011	A99
Dual inverter amplifier	yellow	2.IA2	2722 001 06011	A103
Dual gate inverter	yellow	2.GI1	2722 001 08001	B31
Pulse shaper	green	PS1	2722 001 11001	A107
Pulse shaper	green	PS2	2722 001 11011	A111
Positive reset unit	blue	PR1	2722 001 22001	A117
One-shot multivibrator	green	OS1	2722 001 10001	A121
One-shot multivibrator	green	OS2	2722 001 10011	A125
Pulse driver	green	PD1	2722 001 13011	A131
Printed-wiring board for PD1		PDA1	4322 026 34710	A181
Power amplifier	-	PA1	2722 032 00011	A137
Printed-wiring board for PA1		PAA1	4322 026 33630	A179
Decade counter	-	DC1	2722 009 00001	A141
Dual decade counter	-	2.DCA2	2722 009 00011	A147
Reversible counter	-	BCA1	2722 009 00021	A153
Decade counter and numerical indicator tube driver assembly		DCA3	2722 009 00031	A159
Dual numerical indicator tube driver assembly		2.ID1	2722 009 05001	A167

A number of static input and output devices can be used in conjunction with 100 kHz circuit blocks, see chapter "INPUT/OUTPUT DEVICES"

For power supplies, printed-wiring boards, etc. see section "ACCESSORIES FOR CIRCUIT BLOCKS 100 kHz SERIES"

ADVANTAGES OF CIRCUIT BLOCKS

Some of the outstanding advantages of circuit blocks are:

- saving of time and effort in the development and manufacture of electronic equipment;
- saving of handling, mounting and testing costs in manufacture;
- high and constant quality level;
- simplification of stock-keeping and ordering;
- rationalisation through standardised units.

FIELDS OF APPLICATION

Circuit blocks can in general be used in all digital data-handling equipment, such as for:

- signalling;
- computing;
- controlling;
- measuring and testing;
- data handling;
- laboratory uses.

For detailed design and application information section "Some Practical Circuits", should be consulted.

CONSTRUCTION

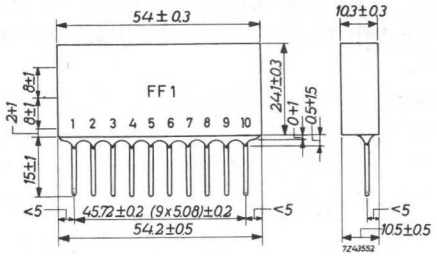


Fig. 1 Dimensional drawing of the circuit block

The dimensions of all 100 kHz circuit blocks are approximately 54 mm x 24 mm x 11 mm (see fig. 1). Out of one side of 54 mm x 11 mm emerge ten wire terminals of 0.7 mm diameter and 15 mm length. The distances between the wires are 5.08 mm (0.2 in) in accordance with the I.E.C. standard hole grid for printed-wiring boards.

The blocks are colour-coded, a different colour being used for each group of functions.

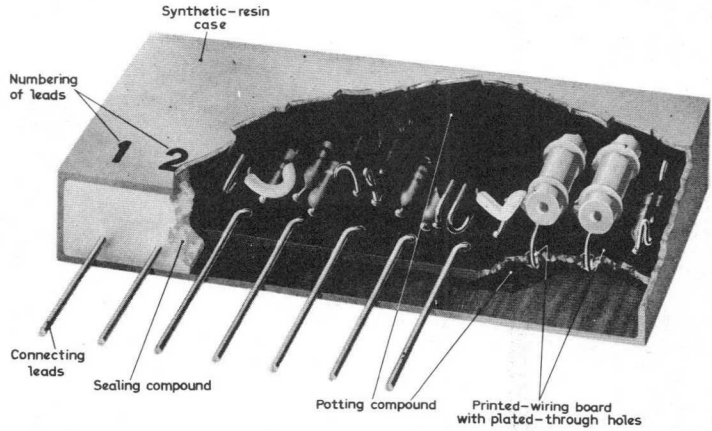


Fig. 2 Cut-away view of a circuit block

The construction of a 100 kHz circuit block can easily be seen in the cut-away view of Fig. 2.

The electronic components, of which the circuit is made up (transistors, diodes, resistors, capacitors) are mounted on a printed-wiring board. This board is provided with plated-through holes to ensure reliable joints due to the large contact area of soldered contacts. The connecting leads are also mounted on the printed-wiring board.

Protection against mechanical shock and vibration is provided by the resilient potting compound, whilst atmospheric influences are excluded by the sealing compound, by which the synthetic resin case is hermetically closed.

For the sake of reference the connecting leads are numbered 1 to 10.

DESIGN CONSIDERATIONS AND RELIABILITY

The main problem in the design of electronic equipment is to attain an optimum level of reliability. The effective functional reliability of an electronic apparatus is - once a given circuit has been determined - exclusively dependent on the stability of the characteristics of the circuit components during their lives.

Though the drift of the characteristics of the present-day components has already been brought down to a very low value, the circuit has to be designed so as to be capable of accepting the still remaining drift. This factor and the nominal spread in the component values determines the total spread to be reckoned with during life.

A very safe design can be achieved by adopting the so-called "worst-case design" principle, in which these total spreads in their most unfavourable combination are taken as a design basis. As far as systematic failures are concerned, these considerations lead to a very safe circuit.

Generally, the performance of a circuit, designed on this basis, is rather poor, however, because of the extreme tolerance combinations that have been taken into account. On the other side, the probability that these extreme combinations occur is practically nil, the probability of "survival" of the circuit element being completely dependent on sudden failures, which are mostly of a non-systematic and catastrophic nature.

The choice of the components in the circuit blocks, the provisions taken in the manufacture of these components, as well as the special protective measures lead to a strong reduction of such sudden failures. Furthermore, a very safe electronic design procedure is followed, applying all available knowledge on the specific statistic behaviour of the components. In this way units with a high standard of reliability, a long life and a high electronic performance are obtained.

It stands to reason that a good performance of the circuit blocks can only be guaranteed, if the user, in his turn, sticks to the operating conditions given by the manufacturer. These operating conditions and guarantee, which apply to all types of circuit block, are given below.

CHARACTERISTICS

Besides passive network elements (resistors, capacitors), only semiconductor devices are incorporated in the circuit blocks, viz. transistors, Ge-diodes and Si-diodes. As a result the inherent advantages of these semiconductors are reflected in the properties of the circuit blocks, such as low supply voltages and small power dissipation.

The standard supply voltage of the circuit blocks is +6 V and/or −6 V, so that no special measures with respect to insulation and protection need be taken.

The power dissipation of the blocks is so small (20 to 100 mW) that no special precautions are necessary with regard to cooling.

The 100 kHz circuit blocks are guaranteed to work properly at the maximum speed of operation under maximum load conditions as given in the Data sheets in the temperature range of −20 °C to +60 °C (−4 °F to +140 °F).
For storage the temperature limits of −25 °C and +75 °C must not be exceeded.

Though the circuit blocks function reliably at any combination of the margins given with respect to supply voltage and ambient temperature, the maximum operational safety margin and the maximum life can be expected by operating the units as closely as possible to the given nominal values of +6 V and −6 V for the supply voltages and 25 °C (77 °F) for the ambient temperature.

Apart from some output devices the circuit blocks are designed for an operational speed of 100 kHz. Because of the large safety margin that has already been taken into account, no further speed-derating is necessary.

TEST SPECIFICATIONS

Before and during manufacture samples of circuit blocks are regularly subjected to the following tests.

(1) Shock test and vibration test according to method 202A and 201A of MIL-STD-202, terminals tested on strength, tests on mounting, soldering, lacquer and coding.

(2) corrosion test (salt haze), according to method 101A of MIL-STD-202 (condition B, 48 hours).

(3) temperature cycling test, according to method 102A of MIL-STD-202 (5 cycles from −25 °C to +65 °C).

(4) dip test, according to method 104A of MIL-STD-202 (2 cycles 65 °C/20 °C, condition B, NaCl).

(5) accelerated humidity test, according to method 106A of MIL-STD-202 (10 cycles 65 °C).

(6) Long-term humidity test (units not operating), according to I.E.C.68, C IV (40 °C, relative humidity: 90% to 95%, duration longer than 2000 hours, functional marginal measurements after 250, 1000 etc. hours).

(7) as item 6, but units operating under the most unfavourable electrical conditions.

(8) long-term test at max. temperature (60 °C), units operating under the most unfavourable electrical conditions. Duration and measurements as item 6.

THE DESIGN OF A CIRCUIT WITH CIRCUIT BLOCKS

BLOCK DIAGRAM

The growing complexity of the electronic system of to-day calls for a simple logical unambiguous way of representation in the system circuit diagram. Effective use is made of a block diagram, in which each symbol represents a specific unit function, which may represent a system component of different complexity. Such a block in the diagram may denote, for instance, anything between a complete production plant and a small basic electronic function, such as a flip-flop, a gate circuit etc. The latter can be considered as basic subassemblies for electronic systems. The circuit blocks belong to this category, each type representing a single functional element or a combination of two of such elements.

BASIC LOGIC SYMBOLS

When a logic circuit is to be designed, whether it should be equipped with circuit blocks or any other elements, it may be useful to make up a block diagram without paying any attention to the technical set-up for the time being. In such a block diagram use can be made of symbols of purely functional elements, some of which are shown in Fig.3.

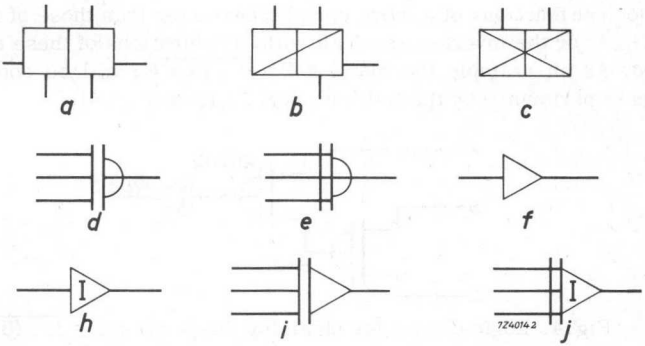


Fig.3. Symbols for logic circuits

a. bi-stable multivibrator (flip-flop)
b. mono-stable multivibrator (one-shot)
c. a-stable multivibrator
d. and-gate
e. or-gate
f. non-inverting amplifier (emitter-follower)
h. inverter
i. and-gate with emitter follower
j. or-gate with inverter

From the symbols in Fig.3 only the and-gate, the or-gate and the inverter perform a purely logic function. According to the Boolean algebra the relations between the output signal and the input signal of these elements are as follows:

AND-gate: (Fig.3d) : $P = A \,.\, B \,.\, C \,. \ldots\ldots\ldots . N$
OR-gate: (Fig.3e) : $P = A + B + C + \ldots\ldots\ldots + N$
Inverter (Fig.3h) : $P = \overline{A}$ ($\overline{A}$ = "NOT A")

A, B, C etc. can attain the values "0" (no signal) and "1" (signal). It should be remembered, that in terms of Boolean algebra $1 + 1 = 1$, so that the value of P in the OR-gate can never exceed 1. The action of the inverter is such, that an input signal "0" produces an output signal "1", or the reverse ($\overline{0} = 1$, $\overline{1} = 0$).

VOLTAGE LEVELS AND SIGNAL VALUES

In a binary system two discrete states can be distinguished, to which the logical values "0" and "1" are assigned. In electronic circuits these values are commonly allocated to the output voltage(s) of a flip-flop, which, in the case of circuit blocks, are approximately 0 V and 0.7 V_N or more negative (V_N being the negative supply voltage).
Since it is immaterial, whether one of these voltage levels is indicated by "0" or "1", or vice versa, they are denoted by "negative low" (approx. 0 V) and "negative high" (0.7 V_N or more negative).

COMBINATION OF LOGIC SYMBOLS

When Boolean functions of a more complex character than those of the AND-gate, the OR-gate or the inverter are dealt with, combinations of these elements must be used. As an example the function $P = \overline{A \,.\, (B + C)}$ will be considered. This function is performed by the following logic circuit (Fig.4).

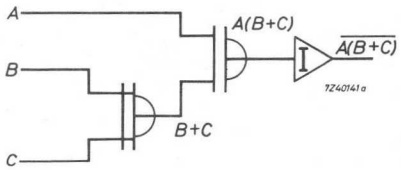


Fig.4. Logic circuit for obtaining the function $P = \overline{A \,.\, (B + C)}$.

In some cases, and specially when a particular arrangement cannot be used for technical reasons, another arrangement can be found by converting the function into an equivalent function, whereby the rules of Boolean algebra may come in useful. The function $P = \overline{A \,.\, (B + C)}$ can be converted into the function $P = \overline{A} + \overline{B} \,.\, \overline{C}$, which corresponds to the logic circuit of Fig.5. From the table below, in which all combinations of A, B and C are considered, it can easily be seen that the functions $P = \overline{A \,.\, (B + C)}$ and $P = \overline{A} + \overline{B} \,.\, \overline{C}$ are equivalent.

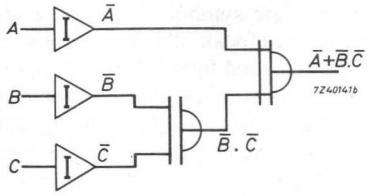


Fig.5. Logic circuit for obtaining the function $P = \overline{A} + \overline{B} . \overline{C}$.

Table

A	B	C	$\overline{A}$	$\overline{B}$	$\overline{C}$	B + C	$\overline{B} . \overline{C}$	A(B + C)	$\overline{A(B + C)}$	$\overline{A} + \overline{B} . \overline{C}$
0	0	0	1	1	1	0	1	0	1	1
1	0	0	0	1	1	0	1	0	1	1
0	1	0	1	0	1	1	0	0	1	1
0	0	1	1	1	0	1	0	0	1	1
1	1	0	0	0	1	1	0	1	0	0
0	1	1	1	0	0	1	0	0	1	1
1	0	1	0	1	0	1	0	1	0	0
1	1	1	0	0	0	1	0	1	0	0

RULES OF BOOLEAN ALGEBRA

The equations given below can be used advantageously to simplify and convert logic functions. They can easily be verified by making up tables as shown above.

$A + 0 = A$
$A + 1 = 1$
$A + A = A$
$A + \overline{A} = 1$
$A + A . B = A$
$A + \overline{A} . B = A + B$
$A . (B + C) = A . B + A . C$

$A . 0 = 0$
$A . 1 = A$
$A . A = A$
$A . \overline{A} = 0$
$A . (A + B) = A$
$A . (\overline{A} + B) = A . B$
$(A + B) . (A + C) = A + B . C$

$(A + B) . (C + D) = \overline{\overline{A} . \overline{B} + \overline{C} . \overline{D}}$

$(A . B) + (C . D) = \overline{(\overline{A} + \overline{B}) . (\overline{C} + \overline{D})}$

$A + B + C + \ldots\ldots\ldots\ldots + N = \overline{\overline{A} . \overline{B} . \overline{C} \ldots\ldots\ldots . \overline{N}}$

$A . B . C . \ldots\ldots\ldots\ldots . N = \overline{\overline{A} + \overline{B} + \overline{C} \ldots\ldots\ldots + \overline{N}}$

$\overline{A} + \overline{B} + \overline{C} + \ldots\ldots\ldots\ldots + \overline{N} = \overline{A . B . C \ldots\ldots\ldots . N}$

$\overline{A} . \overline{B} . \overline{C} . \ldots\ldots\ldots\ldots . \overline{N} = \overline{A + B + C \ldots\ldots\ldots + N}$

SYMBOLS FOR CIRCUIT BLOCKS

After the block diagram with logic symbols has been made up, the logic symbols should be translated into circuit blocks. To this end a wiring diagram is made in which the logic symbols are replaced by symbols representing the corresponding circuit blocks. The latter symbols, recommended for this purpose, are given in the Data Sheets of the circuit blocks. Each of these symbols consists of a rectangle, in which the type of circuit block and the connections are indicated (Fig.6). Since also the reference numbers of the connecting leads are indicated in the symbol, the equipment can be constructed directly from the circuit block diagram.

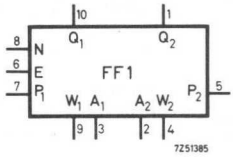


Fig.6. Typical symbol of a circuit block (FF1).

In Fig.7 an example is given of how logic symbols can be combined so as to obtain an arrangement that can be built up from circuit blocks. In this figure the convention "negative low" = "0" and "negative high" = "1" has been adopted, which involves, that the AND-operation is performed by an N-gate and the OR-operation by a P-gate (see under "Gates" in section "Operational Notes").

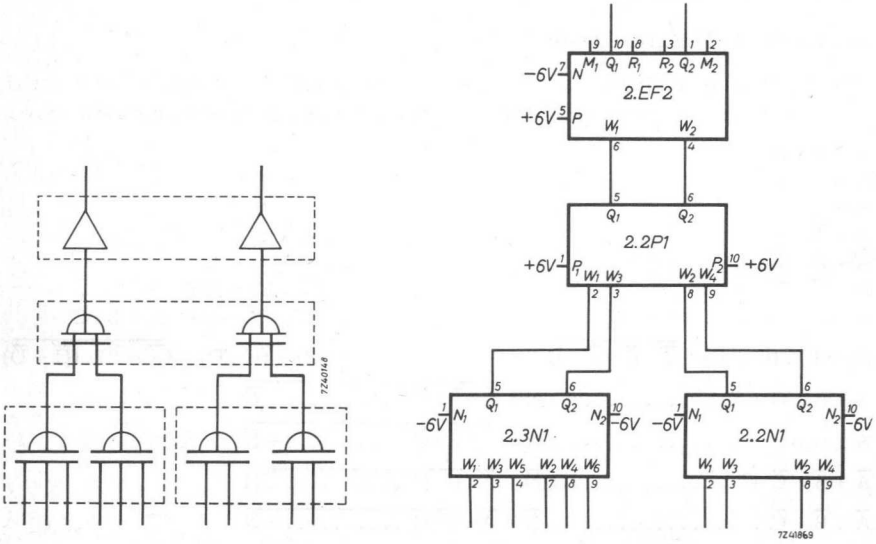


Fig.7. Translation of logic functional symbols into circuit block symbols.

THE LOADING TABLE

Since the loadability of circuit blocks is limited, they may not be arranged arbitrarily. A circuit block diagram, made up from a diagram with logic symbols, should be carefully checked on the basis of the Loading Table.
From this table the number of units that can be driven by any other unit can be taken. When a unit has output terminals with different loadability these data are given separately.

It may be noted that the Loading Table is made up for combinations of units under supply voltage tolerances of ± 5%, whilst part of the earlier types of blocks (see data sheets) allow for a supply voltage tolerance of ± 10%.
The gain in performance obtained at those reduced tolerances has been taken into account in the table. In those cases where a proper functioning is assured a pulse rise time of 0.7 μs has also been calculated with, though 0.4 μs has been prescribed earlier. The result is an overall improvement in loadability in the Loading Table compared with earlier publications.

In the case of amplifier units, the output data are dependent on the input driving signal; for these units the loadability is given for different preceding units or preceding chain of units.

The EF 2 is especially suited to drive a common-emitter stage; for this combination the loadability is also given.

The number of negative gates (N 1) which can be driven by any other unit at a "negative low" output level, depends, due to diode leakage current, on the number of other gate inputs which are at a "negative high" level. In this Loading Table the assumption is made that three other inputs of each driven gate are at a "negative high" level.

If not indicated separately in the Loading Table all N and P terminals of each unit are connected to V_N respectively V_P.

The general set-up of the Loading Table is elucidated in the diagram given below.

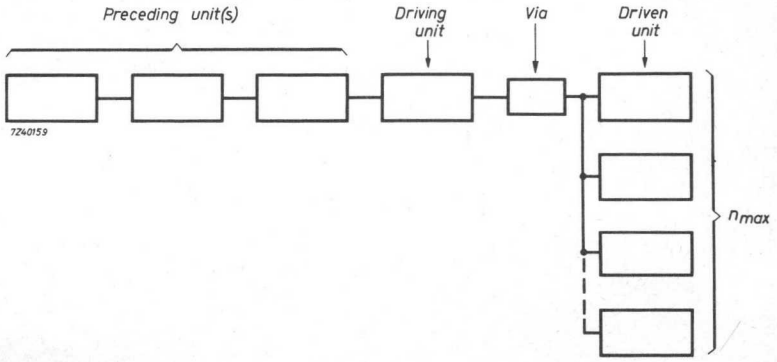


Fig.8. Diagram to explain the Loading Table.

If a specific combination of circuit blocks appears to be inadmissible, it should be rearranged into a permissible combination. Boolean algebra can be used for this purpose.

In some cases a loading, differing slightly from that given in the Loading Table, may be possible.
In this case it must be carefully checked, whether the input signal requirements of the driven units do not exceed the given corresponding output data of the driving unit. It also should be considered that the limiting values of the input signals of the driven unit are never exceeded.
This concerns the values of voltage levels, currents and switching times, which can be derived from the data sheets.

SOME PRACTICAL CIRCUITS

In this section some practical examples are given for the application of 100 kHz circuit blocks. Since most circuit blocks comprise twin units or two separate functional units in certain cases only half the symbol is given.

For the sake of simplicity the supply lines are not drawn in many of the figures given below. Normally the N terminals are connected to the −6 V supply, the P terminals to the +6 V supply and the E terminals to earth (common to both supply voltages). If a supply terminal should not be connected to the corresponding supply line this is indicated by "n.c." (not connected).

In the applications given the following convention is adopted:

"negative low" = binary "0"
"negative high" = binary "1".

According to this convention a Negative gate (2.3N1 or 2.2N1) is employed to perform the logical AND operation and a Positive gate (2.3P1 or 2.2P1) to perform the logical OR operation (see Operational Notes).

SCALERS

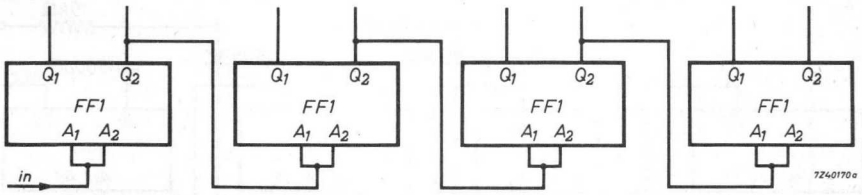


Fig.9. Scaler of 16 (Binary counter with 4 flip-flops)

Below some scalers are given in which pulse feed-back is applied to obtain a dividend that is not a power of 2.

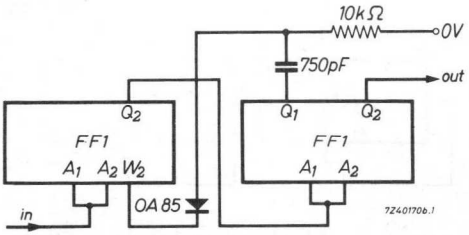


Fig.10. Scaler of 3

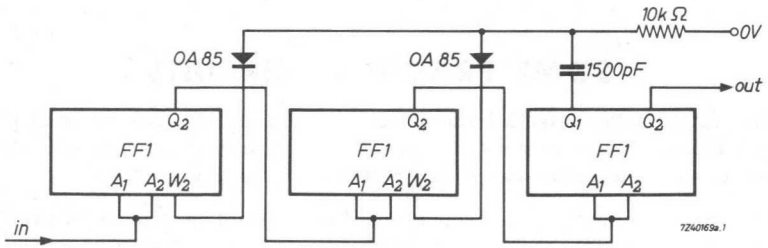


Fig.11. Scaler of 5

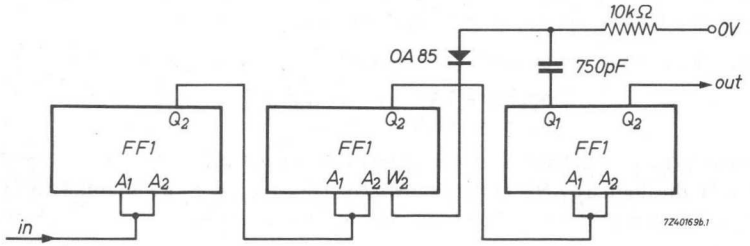


Fig.12. Scaler of 6

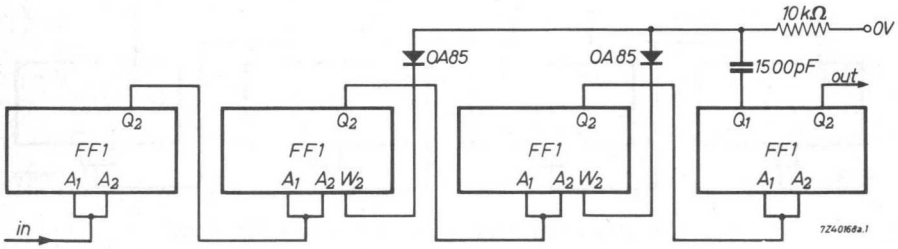


Fig.13. Scaler of 10 (decimal counter)

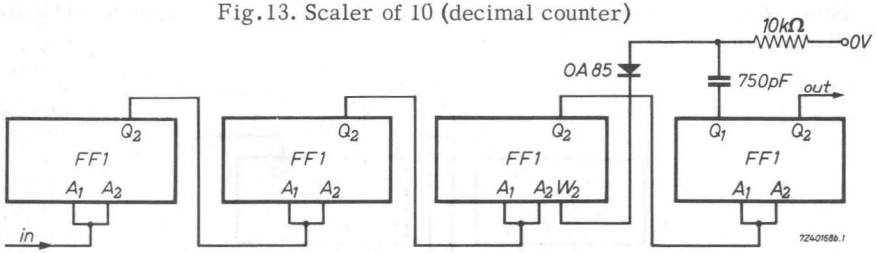


Fig.14. Scaler of 12

Apart from the above mentioned pulse feedback principle also an intermediate gate can be used to skip a number of positions in order to attain scalers of dividends that are no powers of 2. The advantages of this type of circuit is that spurious pulses, as occurring at the output of the scaler with pulse feedback, are avoided. An example of a decimal counter designed on this principle is given below.

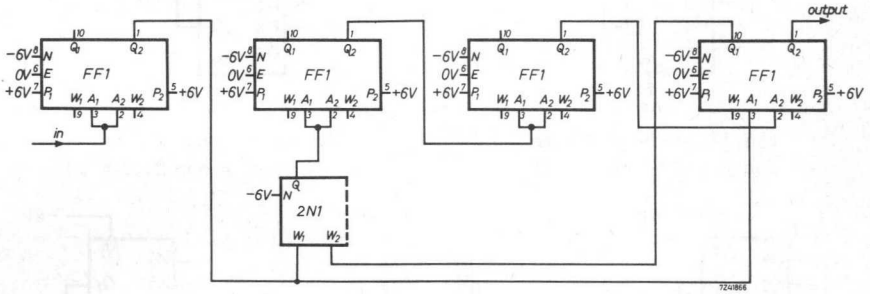


Fig.15. Decimal counter, maximum speed 60 kHz

For a speed of 100 kHz the resistor in the 2N1 block must be shunted externally by a 12 kΩ ±5% resistor or the 2N1 must be replaced by a circuit block 2.IA1, connected to perform the same gate function.

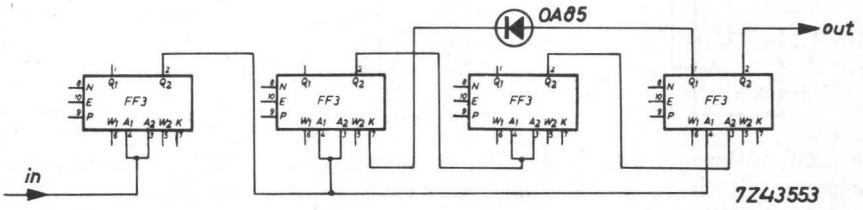


Fig.16. Decimal counter, maximum speed 100 kHz

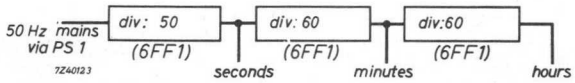


Fig.17. Time code frequency divider

MULTIPLE INPUT GATES

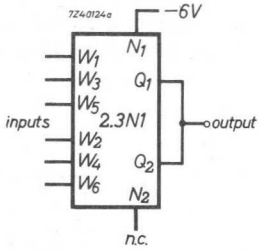


Fig.18. 6-input N-gate composed of one 2.3N1

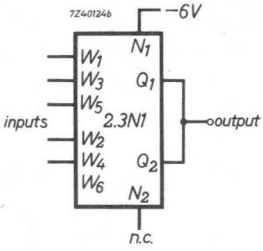


Fig.19. 5-input N-gate composed of one 2.3N1

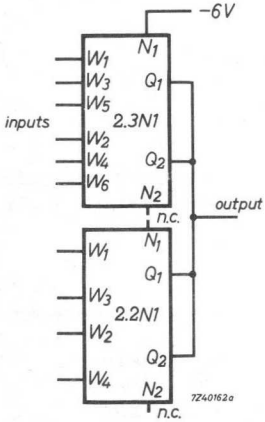


Fig.20. 10-input N-gate composed of one 2.3N1 and one 2.2N1

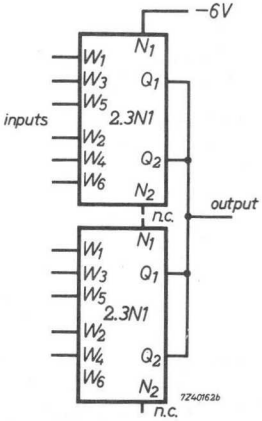


Fig.21. 11-input N-gate composed of two 2.3N1's

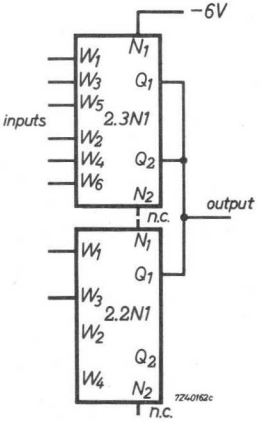


Fig.22. 8-input N-gate composed of one 2.3N1 and half a 2.2N1.

BINARY TO DECIMAL CONVERTER

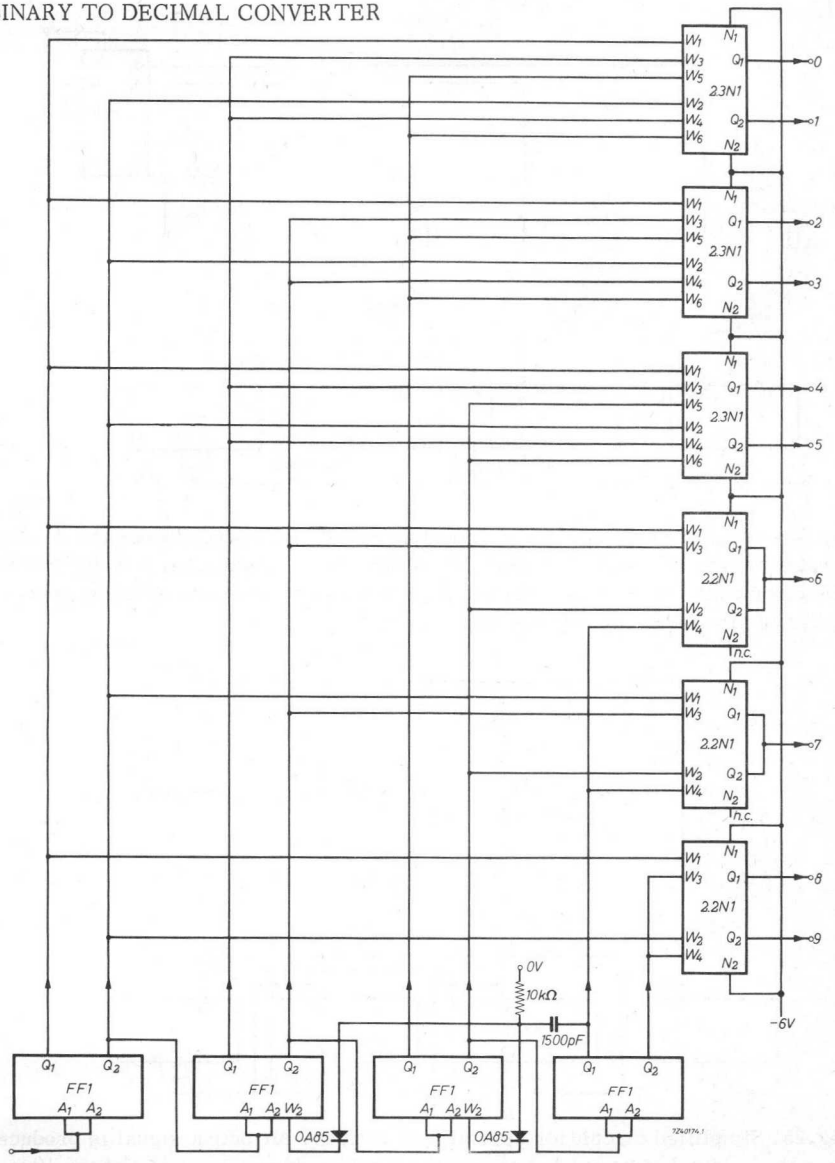


Fig.23. A count of n in the decimal counter produces a "1" signal at the output n at the right. All N, E and P terminals of the flip-flops should be connected to the corresponding supply lines.

PRESET COUNTERS

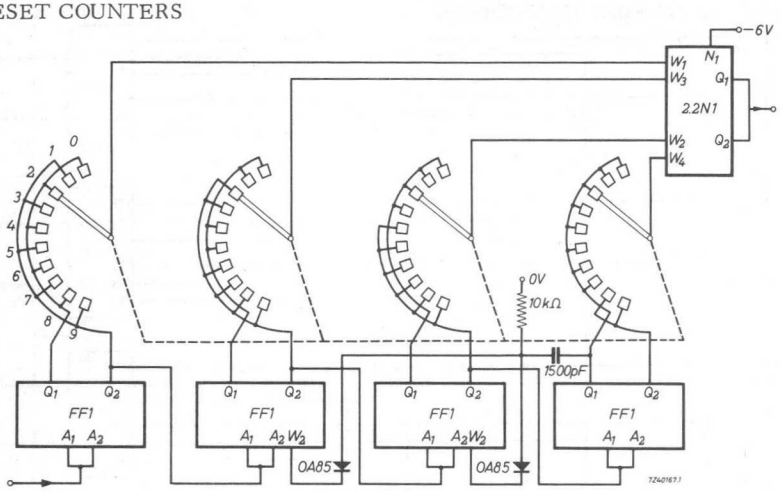


Fig.24. General purpose circuit. An output voltage is produced when the decimal counter stores the number chosen by means of the 10-position 4-wafer switch. The circuit may also be used for the determination of a time interval by counting cycles of an alternating voltage, e.g. the mains.

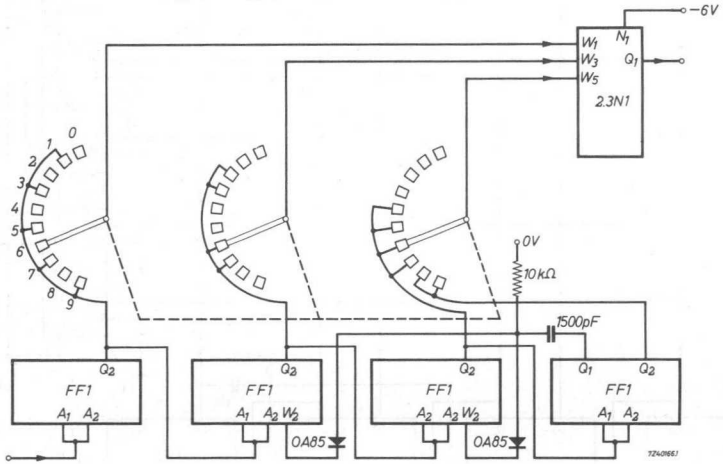


Fig.25. Simplified circuit for special applications. An output signal is produced when the decimal counter has reached the number chosen by means of the 10-position 3-wafer switch. When this number is exceeded the output signal may stay or recur. This phenomenon makes the circuit only useful for those applications in which these spurious signals do not interfere.

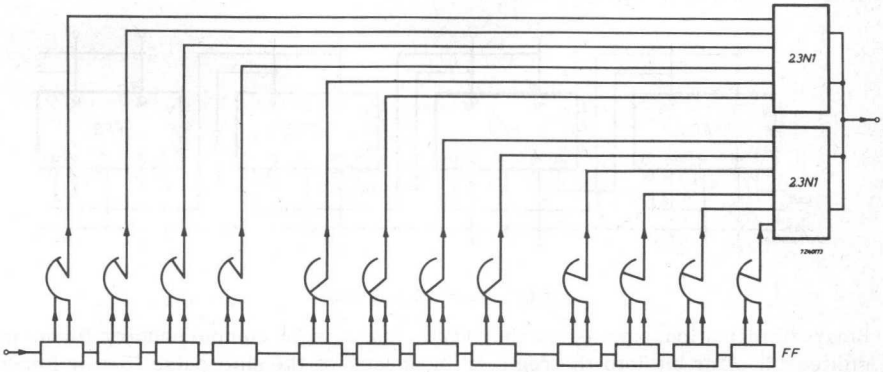


Fig.26. When the counter consists of several decades, it may be preselected by as many 10-position switches. The gates are combined to one gate. The circuit may also be of the 3-wafer switch type, as shown in Fig.19.

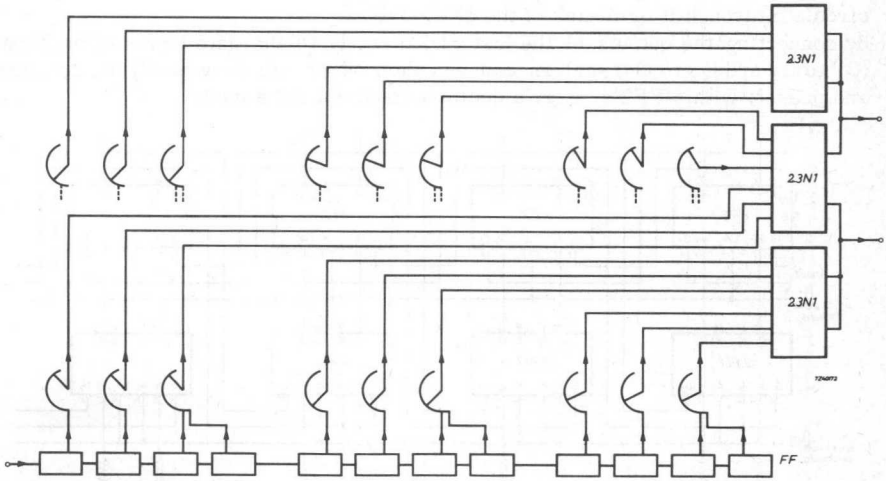


Fig.27. Preset counter with multiple programmes. More than one set of switches and gates may be connected to the same counter. Every output gives a signal when the counter has reached the number set by its associated switches. The switches may be of the 3 or 4-wafer type.

SHIFT REGISTERS

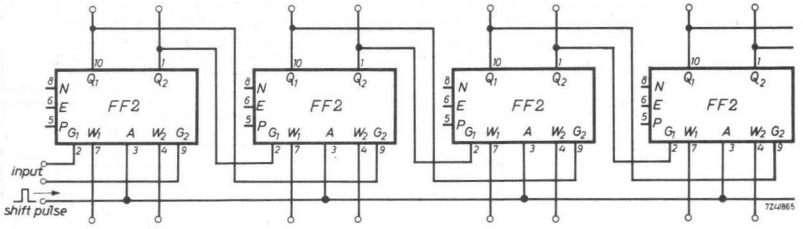


Fig.28. Shift register

Binary information, applied to the input terminals in complementary form, is shifted bit after bit into the register by means of the shift pulse. Set or Reset signals can be applied in parallel to the corresponding W terminals in the usual way (see Set and Reset circuits).

The outputs of the last FF2 can be connected crosswise to the gate inputs of the first (Q_1 to G_2 and Q_2 to G_1). A given information stored in the register will now circulate through it by means of the clock pulse.

By connecting the outputs of the last FF2 directly to the gate inputs of the first (Q_1 to G_1 and Q_2 to G_2) scalers can be made which can very easily be decoded and preset; with 5 FF2's, e.g. a decimal counter can be made.

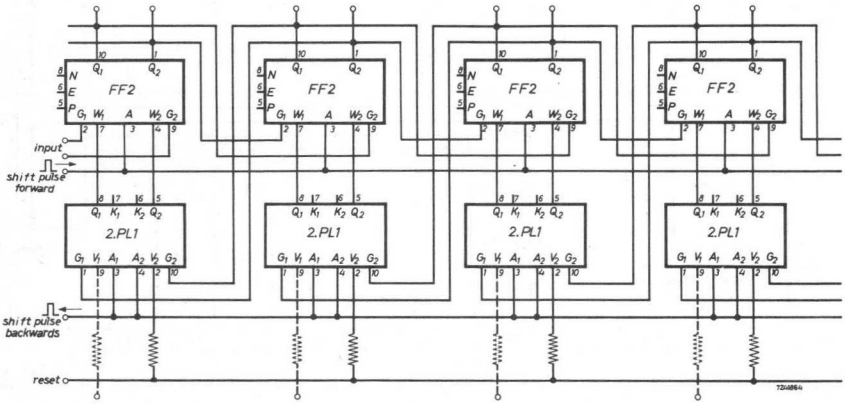


Fig.29. Bi-directional shift register

The circuit of Fig.28 can easily be converted into a bi-directional shift register by adding additional input pulse gates as incorporated in the unit 2.PL1. The information in the register can be shifted in both directions dependent on the input to which the shift pulse is applied. In the same way bi-directional decimal counters can be made according to the principle as indicated above.

The diodes, incorporated in the 2.PL1 (inputs V_1 and V_2) can be used for negative Set or Reset signals.

DRIVE CIRCUITS FOR SHIFT REGISTERS

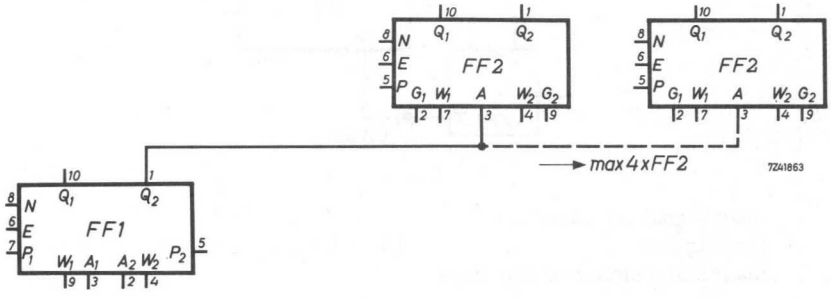


Fig.30

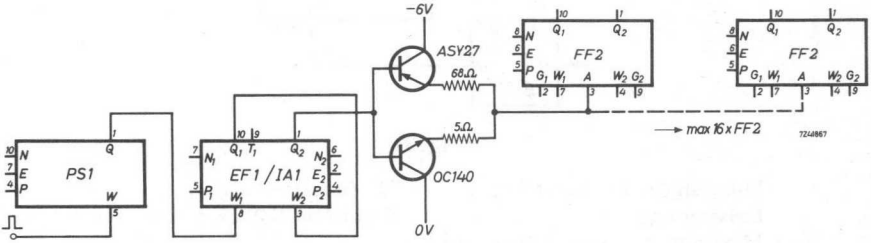


Fig.31

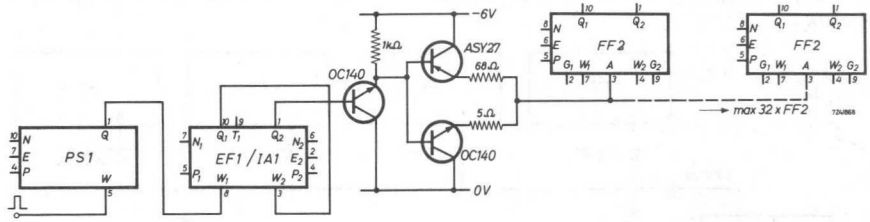


Fig.32

SET AND RESET CIRCUITS

A system in which flip-flops are used, often requires a means for setting or resetting. This can be realised as indicated in the figures below.

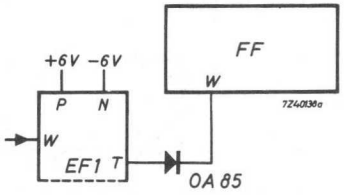


Fig.33

Input signal for resetting:	"0" (negative low)
Driving unit:	FF1, FF2, IA1, IA2, PS1 or OS1
Maximum number of flip-flops:	1

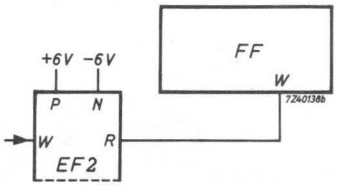


Fig.34

Input signal for resetting:	"1" (negative high)
Driving unit:	N-gate or N-P gate sequence
Maximum number of flip-flops:	1

A simple circuit for resetting flip-flops by a flip-flop FF1 is given in the figure below.

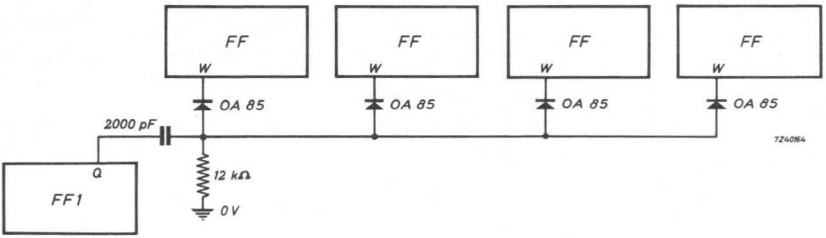


Fig.35

Resetting takes place on a positive voltage step at the Q terminal of the drving flip-flop.

When a large number of flip-flops has to be controlled, the following arrangement can be used.

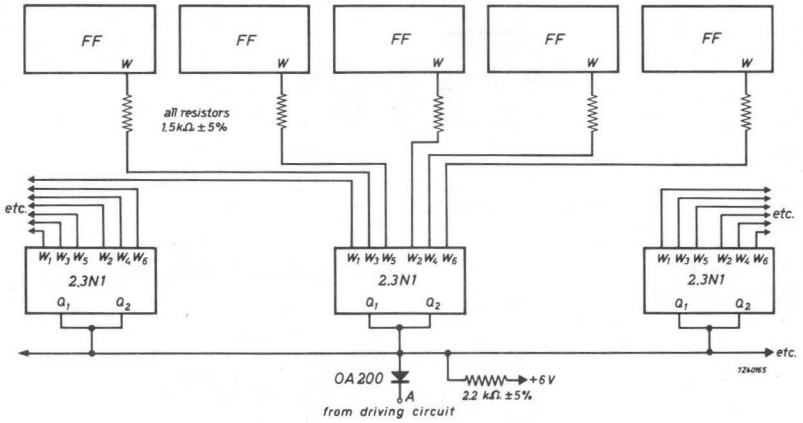


Fig.36

The circuit of Fig.36 can be driven by one of the circuits given below.

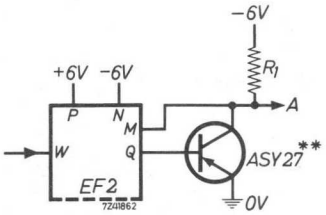


Fig.37

Input signal for resetting:	"0" (negative low)		
Driving unit	FF1, FF2, IA1, IA2, PS1 or OS1	N1	N1-P1
Value of resistor R_1 in Ω ±5 % [1])	82	150 (82)	330 (200)
Max. number of flip-flops[1])	32	15 (32)	5 (10)

[1]) The values between brackets apply to the circuit without the anti-bottoming connection (EF2-M terminal to collector ASY27). Consequently this circuit is for low speed operation only.

**) See Fig.45.

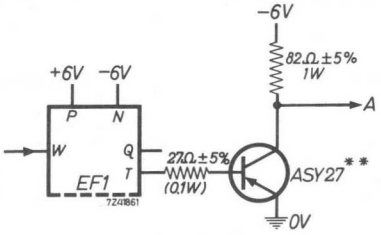


Fig.38. (Low speed operation only)

Input signal for resetting: "0" (negative low)
Driving unit: FF1, FF2, IA1, IA2, OS1 or PS1
Maximum number of flip-flops: 32

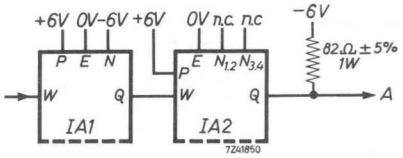


Fig.39

Input signal for resetting: "1" (negative high)
Driving unit: FF1, FF2, IA1, IA2, OS1 or PS1
Maximum number of flip-flops: 32

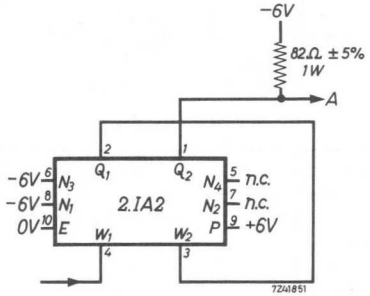


Fig.40

Input signal for resetting: "1" (negative high)
Driving unit: N1, N1-P1, IA1, IA2 or PS1
Maximum number of flip-flops: 32

**) See Fig.45

AMPLIFIER CIRCUITS FOR GATE SIGNALS

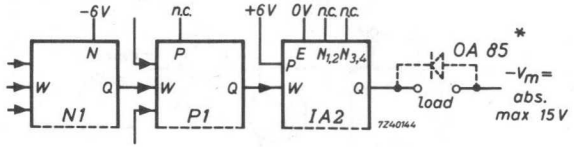


Fig.41. I_{load} = max. 5.5 mA

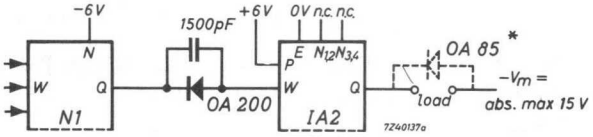


Fig.42. I_{load} = max. 5.5 mA

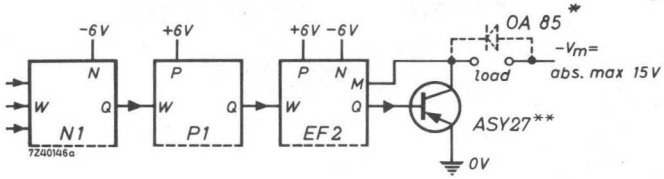


Fig.43. I_{load} = max. 13 (29) mA [1])

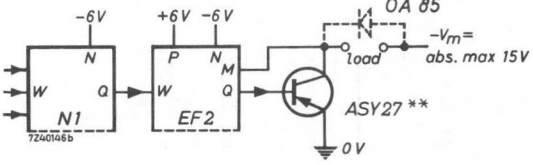


Fig.44. I_{load} = max. 35 (50) mA [1])

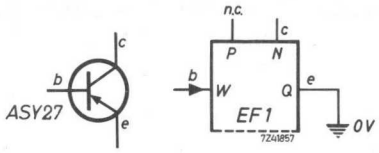


Fig.45. In the circuits given the transistor ASY27 can be replaced by the EF1 circuit.

---

[1]) The values between brackets apply to the circuit without the anti-bottoming connection (EF2-M terminal to collector ASY27). Consequently this circuit is for low speed operation only.

*) In case of inductive load.

**) See Fig.45.

AMPLIFIER CIRCUITS

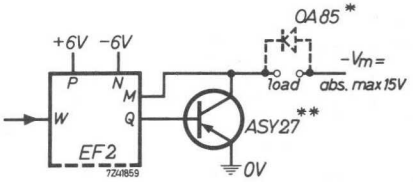


Fig.46

Driving circuit: FF1, FF2, IA1, IA2, OS1 or PS1
I_{load}: max. 70 (85) mA [1])

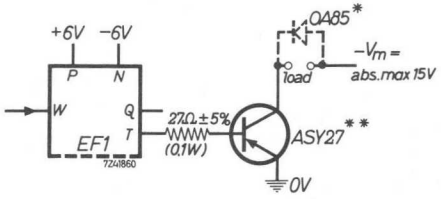


Fig.47

Driving circuit: FF1, FF2, IA1, IA2, OS1 or PS1
I_{load}: max. 85 mA

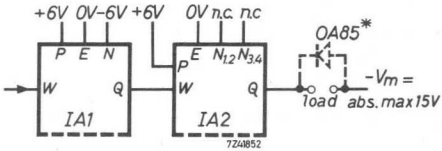


Fig.48

Driving circuit: FF1, FF2, IA1, IA2, OS1 or PS1
I_{load}: max. 85 mA

---

[1]) The values between brackets apply to the circuit without the anti-bottoming connection (EF2-M terminal to collector ASY27). Consequently this circuit is for low speed operation only).

*) In case of inductive load.

**) See Fig.45.

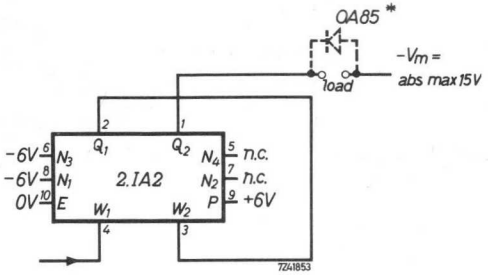


Fig.49

Driving circuit: N1, N1-P1, IA1, IA2, PS1
I_{load}: max. 70 mA

POWER AMPLIFIER CIRCUITS

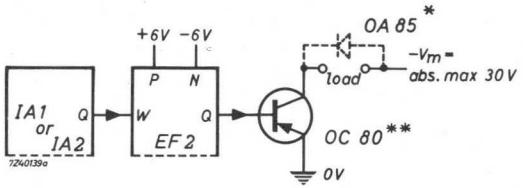


Fig.50. I_{load} = max. 250 mA

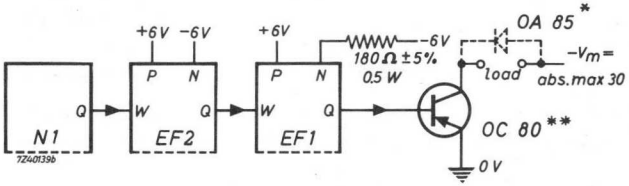


Fig.51. I_{load} = max. 300 mA

*) In case of inductive load

**) The transistors have to be mounted on a heatsink (see relevant transistor data).

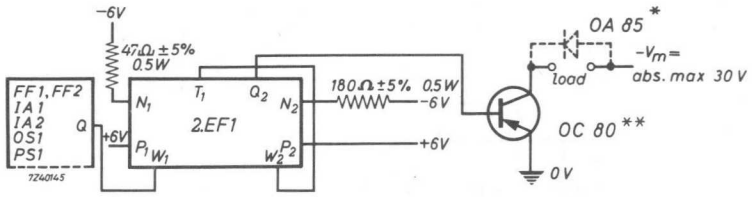


Fig.52. I_{load} = max. 300 mA

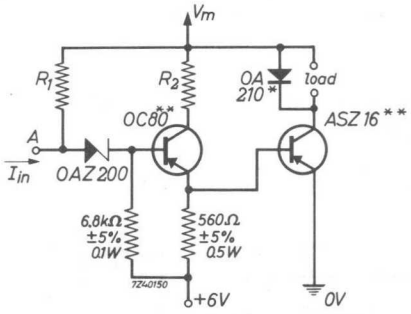


Fig.53

Voltage	$-V_m$	12 V ±15 %	24 V ±15 %
Resistors	R_1	470 Ω ± 5 %, 1 W	2.4 kΩ ± 5 %, 0.5 W
	R_2	68 Ω ± 5 %, 5 W	150 Ω ± 5 %, 10 W
Input current	$-I_{in}$	min. 35 mA	min. 13.5 mA
Load current	I_{load}	max. 2.6 A	max. 2.6 A
Driving circuits		Fig.44 to 49	Fig.43 to 49

If there is a preference to use an output transistor ASZ17 or ASZ18 instead of the ASZ16, the stated maximum load current I_{load} has to be multiplied by 0.6.

*) To be used in case of inductive load.

**) The transistors have to be mounted on a heatsink (see relevant transistor data).

PHOTO-ELECTRIC PICK-UPS

With a circuit block PS1 very simple photo-electric pick-ups can be made. For the output data of the circuits given below see the PS1 data sheet.

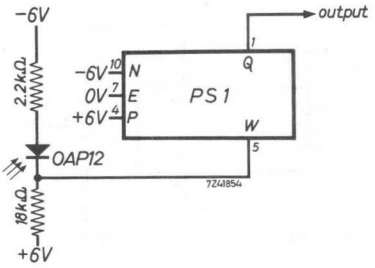


Fig.54

Switching level: min. 13000 Lux (this lighting level can be achieved with a lens-end incandescent lamp of 2.2 V; 0.25 A)

Max. ambient temperature: 60 °C

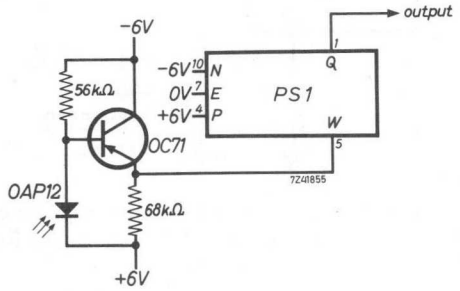


Fig.55

Switching level: min. 3000 Lux (this lighting level can be achieved with a lens-end incandescent lamp of 2.2 V; 0.25 A)

Max. ambient temperature: 60 °C (only if the OAP12 and OC71 have been matched for proper leakage current compensation).

OSCILLATOR CIRCUITS

With a circuit block PS1 it is possible to make square wave oscillator circuits as given in the figures below.

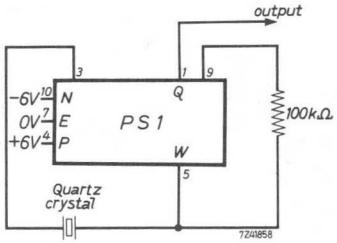


Fig.56. Crystal controlled oscillator circuit. For the output data of this circuit see the PS1 data sheet.

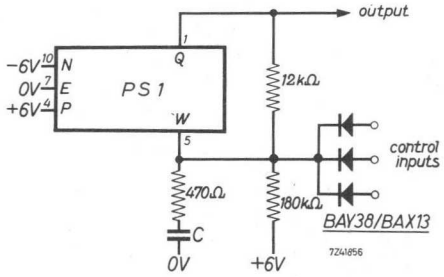


Fig.57. Relaxation oscillator circuit. The oscillator may be controlled by more control signals as indicated in the figure. A "0" (negative low) level on one of these inputs stops the oscillator.

For a capacitor value

C = 2500 pF	f	= approx.	100	kHz
C = 250 μF	f	= approx.	1	Hz

Output data:

Output level "negative low"	Voltage	$-V_Q$	max. 0.2	V
	Load current	$-I_Q$	max. 1.2	mA
Output level "negative high"	Voltage	$-V_Q$	max. -0.7	V_N
	Load current	I_Q	max. 0.3	mA

For further data see PS1 data sheet.

OPERATIONAL NOTES

This chapter contains some general and specific remarks on the application of circuit blocks.

FLIP-FLOP

D.C. input signal

The flip-flops FF1, FF2, FF3 and FF4 can be set or reset on the W terminals by a negative or positive d.c. level. Attention should be paid to the W inputs being directly connected to the transistor base. When driven by a low-impedance source (e.g. the direct output of an emitter-follower or the negative power supply line) the transistor may be seriously overdriven and hence destroyed. The maximum permissible input current should therefore never be exceeded.

If the memory property of the flip-flop has to be maintained, the driving source should have a one-way action on the flip-flop; the source should therefore be connected to the W terminal by means of a series diode (see p. A26: SET AND RESET CIRCUITS). In order to attain a correct cut-off voltage level for this diode, the emitter-follower units EF1 and EF2, which can be used as driving sources for the flip-flop, are provided with a tapped output. The voltage level on the tap has the required value if the emitter-follower is driven by a "0" (negative low) signal.
The EF2 circuit block comprises the series diode (M_1 and M_2 output terminals).

Cascading of flip-flops

With n cascaded flip-flops FF1 or FF3 it is possible to construct frequency dividers with a dividend of 2^n. When such a chain of flip-flops is used for counting, the total counting capacity amounts to 2^n as well.
By using a pulse feedback or gating principle it is possible to skip a given number of counts, so that with n flip-flops any dividend up to 2^n can be obtained. When a dividend of N is required, the minimum number of flip-flops (n) can be derived from:

$$2^{n-1} < N \leq 2^n.$$

Pulse feedback is required when $N \neq 2^n$, so that 2^n N positions are skipped. The value of $2^n - N$ gives the indication to which flip-flop in the series the feedback should be applied. In Figs. 11 to 15 a few examples of FF1 counters are given. The feedback pulse is supplied to the preceding flip-flops via a pulse gate circuit.

The value of the capacitor in this circuit is determined by the number of flip-flops to which the feedback pulse has to be supplied, viz. approximately 500 pF per flip-flop.
Care should be taken, that the maximum permissible capacitive load of the flip-flop that supplies the feedback pulse is not exceeded. The maximum capacitive loading of the FF1 is 2000 pF. For both Q terminals together when the FF1 is loaded during the negative as well as the positive transient of the pulse. If a 1500 pF series capacitor is used in the feedback path, 500 pF is left for external loading on that terminal (equivalent to another flip-flop). If more than four feedback paths are required, the signal may also be taken from one of the preceding flip-flops.
A disadvantage of this type of counter is that a spurious pulse occurs at the outputs of the flip-flops to which the feedback pulse is applied (see e.g. the output levels of the DC1 as given in the corresponding Data Sheet). If the occurrence of this pulse is not wanted an intermediate gate can be used as indicated in Fig.15.
In Fig. 16b a similar type of decade counter is given, but now equipped with flip-flop FF3. With this FF3 however the intermediate gate has been built in the unit itself. The gate condition derived from the 4th flip-flop is connected to the extended gate terminal of the 2nd FF3 via a diode.

Shift registers

The flip-flops FF2 and FF4 are in principle equivalent to the FF1 and FF3 circuits respectively, with the exception that the built-in input pulse gates can be controlled externally. In this way the switching of the unit, upon reception of a positive going voltage step on its A input is determined by the d.c. levels applied to its G inputs. Thus the binary information presented to the G inputs can be shifted into the flip-flops by the voltage step on A.
The pulse gates are opened by a "negative low" level and closed by a "negative high" level on the corresponding G input.
It is to be noted that for proper working the G_1 and G_2 terminals may not be at a "negative low" level simultaneously.
The units 2.PL1 and 2.PL2 (Dual Pulse Logic) contain the input gate circuitry of the normal flip-flop FF1 and FF2, and FF3 and FF4 respectively. In this way it is possible by connecting these units to an FF1 and FF3 respectively to obtain a second A input on this unit. In combination with FF2's and FF4's respectively bi-directional shift registers can be made.
In the figures 28 and 29 examples are given of a uni- and a bi-directional shift register.

GATES

General

As mentioned before, it is immaterial which binary level is denoted by the logic value "0" or by "1", since it has no influence whatsoever on the logic design of a circuit. However, confusion may arise when gate circuits are discussed. Many designers use the words AND and OR for the basic logic functions as well as for the electronic circuits that perform these specific logic operations. The notations AND and OR should, however, be restricted to logic operations, since one gate circuit can perform both the AND and OR operation, dependent on the designation of "0" and "1" to the voltage levels used.
For the above reasons the circuit blocks comprising gate circuits are denoted by "NEGATIVE GATE" and "POSITIVE GATE". The negative gate performs the AND operation on "negative high" signals and the OR operation on "negative low" signals, whilst the positive gate performs the OR operation on a "negative high" signal and the AND operation on a "negative low" signal (see Table below).

Signal value "1" assigned to:	Logic operation performed by	
	Positive gate	Negative gate
"Negative high" level	OR	AND
"Negative low" level	AND	OR

Gate Sequence: Always negative gate - positive gate

Technically it is only possible to drive a positive (P) gate by a negative (N) gate. In the system where the "negative high" signal corresponds to binary "1", the AND-OR sequence is therefore allowed only. This means that every OR-AND combination in the logic diagram should be converted into an AND-OR combination. An example of such a conversion was already given on page A12. It may be convenient to remember that an AND-gate is an OR-gate for the signal of opposite polarity and vice versa. At the outputs of a flip-flop a signal and its complement are simultaneously present, so that no inverter need be used when the signal is taken from a flip-flop.

Cascading of gates: no more than two

Cascading of more than two gates must generally be avoided. This is due to a large increase of the load on the driving unit when gates are connected in cascade, so that the signal level shift (signal loss) may amount to impracticable values.
An N-N or P-P gate sequence is generally not allowed; such a sequence can, however, always be replaced by one multiple N or P gate respectively.

After a signal has passed an N-gate or an N-P gate sequence, it must be restored by an inverter amplifier IA2, an emitter-follower EF2 or a pulse shaper PS1.

Gates with multiple inputs

In many cases gates with more than three inputs may be required. Such a gate may be composed of any number of 2- or 3-input gates. The following rules should then be observed:

1. Interconnect the Q-outputs.
2. Connect the negative supply N only once for the whole gate, leaving the other terminals N_1 or N_2 floating.
3. If the newly composed gate would have more inputs than actually necessary leave the unused inputs floating.
4. A P-gate driven by an N-gate may have 25 inputs at maximum.
5. When part of the number of inputs of an N-gate are at "0" level and the other inputs at "1" level, the supply of the leakage currents of the diodes that are cut-off is distributed over the inputs at zero level. (The maximum of this leakage current is 40 μA for every input in the "1" position.) This may give rise to a considerable increase of the load at these inputs. (See also the corresponding Data Sheets.)

Examples of multiple-input gates are given in Figs. 18 to 22.

Positive gates

The rules given above under 1, 2 and 3 for N-gates also apply to P-gates. It must be noted, however, that, unlike the N-gate, the P-gate may load the driving stage at both binary levels.
The terminals P_1 or P_2 of the P-gate may be left floating when the following stage is already equipped with a resistor from the input to the positive supply voltage. This is the case with the inverter-amplifiers IA1 and IA2.
When a P-gate is driven by an N-gate, the number of P-gate inputs may not exceed 25. On the other hand, an N-gate may be loaded by only one P-gate.

More than one gate driven by more than one flip-flop

The Loading Table indicates the number of gates with which the other circuit blocks may be loaded. It should be remembered, however, that an N-gate only presents a "load" if it produces a "negative low" signal at its output. When several gate inputs carry a "negative low" signal simultaneously, the load is divided among the driving sources. When a number of gates is driven by a number of flip-flops, it may therefore be allowed to connect each flip-flop to a number of gates greatly exceeding that given in the Loading Table. That is because the

effective loading may be far less than the actual number of gates. This must be checked carefully for every possible state of the circuit.
The same applies, as a matter of course, for other driving sources.

Voltage levels in gate circuits

Due to the voltage drop across the diodes of the gates, a voltage level shift will occur in every gate, so that the signal, after having passed one or more gates, is no longer in agreement with the level standards of the input signals. In the Loading Table this effect has already been taken into account. When a combination of gates that is not covered by the Loading Table must be used, the following information should be borne in mind:

1. A germanium diode in an N-gate causes a level shift of −0.1 V to −0.5 V [1].
2. A silicon diode in a P-gate causes a level shift of +0.4 V to +1.0 V [1].
3. A common emitter stage needs −0.2 V to −0.4 V on its base for the conducting state and approximately +0.2 V for its cut-off state [1].
4. The collector-voltage level of a conducting common emitter stage ("0" output) has to be taken as −0.05 V to −0.2 V [1].

Current in gate circuits

Since the forward resistance of a conducting diode and the input impedance of a common emitter transistor, when driven into the conducting state, is very low, a strong gate current may occur, which may overload or damage the circuit elements.
On the other hand, the generator impedance of an "open" gate is high, resulting sometimes in too low an available driving current for a given stage. When applying other combinations, such as given in the examples below or in the Loading Table, these points have therefore to be investigated.

ONE-SHOT MULTIVIBRATORS OS1 AND OS2

The one-shot multivibrator OS1 is intended to produce a pulse of definite length for providing a time delay. Both a positive- and a negative-going pulse are available at the outputs. It should be noted that at the Q_2 terminal the maximum permissible load current is appreciably lower than that at the Q_1 terminal, whilst the rise time of the pulse at the Q_2 terminal is higher than that at the Q_1 terminal.

[1]) Related to the type of semiconductor as used in the circuit blocks and dependent on the current flowing through the diodes. In calculations on the levels the most unfavourable limit of the values given has to be applied.

It is not recommended to use the OS1 for delays that exceed the values given in the graph (see Data Sheets), i.e. longer than 1 ms, since in this case the OS1 is more sensitive to spurious signals induced on the supply line. Moreover, the use of electrolytic capacitors would be required, which are less stable during life and may show a considerable leakage current. For long delays it is therefore recommended to use a frequency divider fed from a fixed frequency, such as the a.c. mains.
When the OS1 is used for long delays the negative supply line should be bypassed close to the unit by a large capacitor.
The one-shot multivibrator OS2 has considerable advantages above the OS1 in particular with respect to the maximum permissible load current on both Q-terminals whilst the rise time of the pulses derived from Q_1- and Q_2-terminal are equal (see Data Sheets).

TRANSIENTS AND DELAY TIMES

Although all circuit blocks function properly in any permitted sequence at frequencies up to 100 kHz, practical considerations may cause a reduction of this speed. This may happen when the total delay in a chain of cascaded circuits is too long for the specific application. It must be examined on the basis of the switching times and delay times as given in the Data Sheets.

As a typical example an 8-stage binary counter with flip-flops FF1 will be considered. From the Data Sheet it follows, that in this counter a total delay of $8.(t_{rd} + t_r) = 8.8\ \mu s$ occurs. If the output signal of the 8^{th} flip-flop should coincide with the input pulse of the counter for at least 2 μs, it is required for this input pulse to have a duration of minimum $8.8\ \mu s + 2\ \mu s = 10.8 \mu s$. This requirement reduces the maximum operational frequency in the application at issue to approximately 46 kHz.

The transients in a loaded switching circuit can be calculated from the output data given in the Data Sheets.
The intrinsic switching times given in these data always apply to the unloaded condition. Generally they remain unaffected under conditions of resistive loading, whereas a capacitive load increases the switching times.

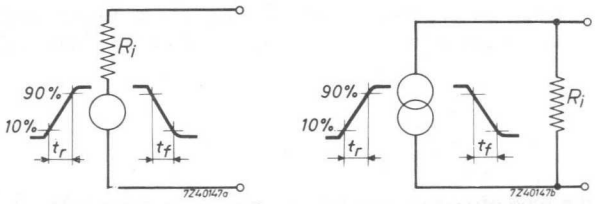


Fig. 58 Equivalent diagrams of active circuit blocks

The actual switching time of a loaded circuit can easily be calculated from the equivalent diagrams shown in Fig. 58. The unit can be represented by a step voltage or current source in combination with the internal (output) impedance of the unit. The value of this output impedance is given in the Data Sheet of the unit under consideration. The total rise time and fall time of the output voltage are approximately equal to:

$$t_{r\ tot} = \sqrt{t_r^2 + (2.2\ \tau)^2} \text{ and } t_{f\ tot} = \sqrt{t_f^2 + (2.2\ \tau)^2}$$

in which:

t_r = the intrinsic rise time of the unit,
t_f = the intrinsic fall time of the unit,
τ = the time constant of the load and internal resistance of the unit.

When the load consists of the parallel circuit of a resistive part R_1 and a capacitive part C_1 (which will mostly be the case):

$$\tau_1 = \frac{R_1 \cdot R_i}{R_1 + R_i} \cdot C_1,$$

in which R_i is the internal resistance of the unit.

ELECTRICAL INTERFERENCE AND APPROPRIATE COUNTER-MEASURES

Introduction

In industrial applications of transistorized electronic equipment sometimes troubles are encountered caused by interfering signals.
In designing equipment in which circuit blocks containing transistorized circuits are applied it is very important to pay due attention to the various possible sources of interference.
Interfering signals, mostly present during a short interval, can temporarily disturb the regular signals. In sequential circuits e.g. a one-shot multivibrator or flip-flop circuit (with a memory function), the interfering signal may be stored as a piece of information. In industrial equipment with transistor circuits interference is often produced by the switching of electro-magnetic loads, such as: relays, clutches, electro-magnetic valves, motors, transformers, welding apparatus, etc..
In almost all cases, however, these interference problems can be fully overcome by observing a number of simple design rules.
Most of these rules refer to the circuit lay-out, the wiring etc., so that they can only be applied efficiently and in the most effective way, when they have been duly accounted for at the outset of the development. Any correction afterwards is costly, time consuming and often even impossible.

Transistors versus Tubes and Relays in Control Equipment with respect to Interference

Relay systems which operate at a very high power level are by nature very insensitive to interference.
In electronic control circuits a much lower signal power level is applied which consequently can be easily upset by interfering signals that are caused by external stray fields. In such cases special precautions are required.
It is not generally recognised that thermionic tube and transistor equipment behave quite differently in this respect.
In tube circuitry with higher voltage levels mostly higher interference levels are allowed. Because of the rather high impedance of the signal lines most interference is of capacitive nature, a capacitive screening of the signal lines is in many cases sufficient.
Transistor circuitry mostly operates at a much lower voltage level and has a lower impedance. Here a relatively higher sensitivity to magnetic stray interferences can be found. In these circuits a simple capacitive screening only solves a small part of the problems.

The sections below contain a survey of various kinds of interference and indications as to their elimination or reduction.

Essentially there are two principal rules to be borne in mind:

A. eliminate the sources of interference or reduce their effect

B. make the circuit itself insensitive to the remaining interference signals to the highest possible degree.

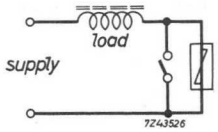
The latter rule is most important because:

- during design and development the future working circumstances are often not known,
- a complete suppression of interference is mostly not possible.

A. SUMMARY OF POSSIBLE INTERFERENCE SOURCES AND COUNTER-MEASURES

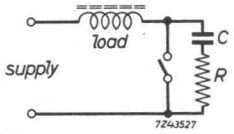
1. Spark extinction at switch contacts of motors and peak voltage suppression at inductive loads.

1.1 Bridging the contacts by means of a voltage-dependent resistor (VDR).



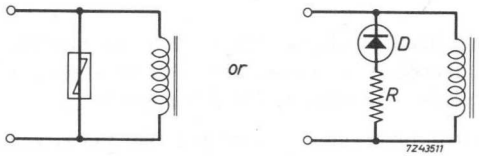
The peak voltage and the resulting arcing between the contacts will be reduced.

1.2 Bridging the contacts by means of a capacitor/resistor combination.



The capacitor reduces the voltage when the contact is opened. The resistor reduces the discharge current of the capacitor, when the contact is closed.

1.3 Bridging the load itself by a voltage dependent resistor or diode-resistor combination.



2. Dust on (or contamination of) the electro-magnetic power contacts.

A proper dust sealing solves this problem.

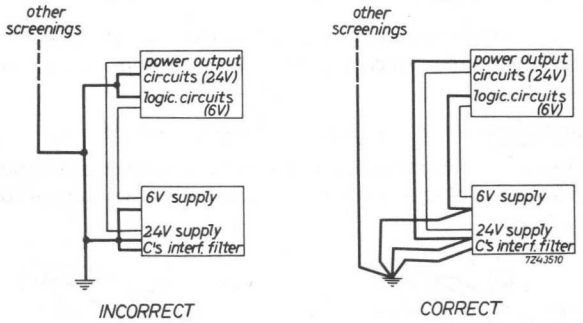
3. Incorrect positioning of possible interference sources.

Keep components and/or units which can act as interference sources, separated from the circuits that are sensitive to interference. Further improvements can be obtained by placing a metal shielding between these parts of the equipment.

4. Interference caused by improper wiring.

4.1 Wiring of earth lines

The principle is that the earth lines of the two supplies should be kept as far apart as possible. This holds in particular for the earth line of power transistors. The drive currents of these transistors, which are also sent through the earth lines, are rather high and can cause voltage differences.

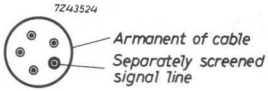


To reduce the chance of interference it is preferable to keep the length of earth lines as short as possible and to use wire of adequate diameter.
All earth lines must be connected separately to one common earth point on which also the chassis and other screenings are earthed.

4.2 Wiring that forms the connection to electro-magnetic loads, and leads that carry large currents, must be kept separated from the signal leads, which may transfer the interfering signals to the circuits that are sensitive to interference.

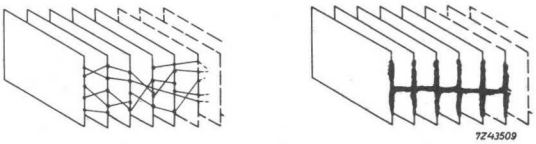
4.3 Signal carrying lines should be kept as short as possible and loops avoided. As screening material of these lines iron or steel must be used, a steel-armoured cable is very suitable for this purpose.

Furthermore it is preferable to screen signal lines, which are connected to triggered circuits, from other lines in this cable.



The earthing of the steel sheath as well as that of the separate line screening must be done at the common earth point of the chassis.

4.4 Decrease the wiring area
Example: wiring of a bank of printed-wiring connectors.

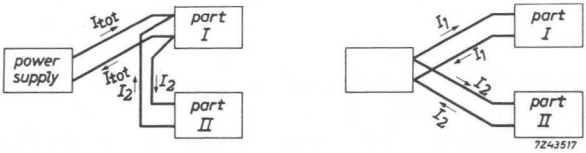


INCORRECT CORRECT

However, the wiring connected to inductive loads (drive lines for relays etc. or generally high pulse current lines) must be kept apart, with their own earth return.

5. Common impedance of two or more parts of an equipment.

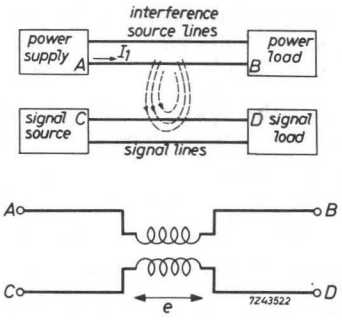
If, for instance, two parts of an equipment are connected to the same power supply, a reduction of the common impedance can be obtained by using separate supply lines.



INCORRECT CORRECT

Further reduction can be achieved by using:
- a stabilised power supply (low internal impedance)
- separate power supplies for each part of the equipment.

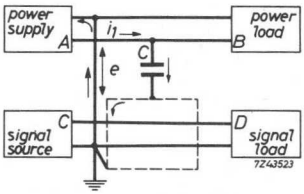
6. Electro-magnetic coupling between signal and/or supply lines.



$$e = M \frac{di}{dt}$$

This coupling can be reduced by the following measures:
- reduce the magnetic field by twisting the interference source lines;
- cancel the induced voltage by twisting the signal lines;
- reduce the coupling magnetic field by increasing the distance between interference source lines A-B and signal C-D;
- reduce the coupled magnetic field by a shield of a ferromagnetic material;
- reduce the coupled magnetic field by decreasing the length of the interfering lines;
- choose circuit parameters in order to:
  decrease signal load impedance
  decrease magnitude and frequency of interfering currents;
- cancel the induced voltage by crossing the wires at right angles.

7. Electro-static coupling



$$i = C \frac{de}{dt}$$

This coupling can be reduced by the following measures:
- use an electrically conductive shield as shown in the figure. The capacitance C short-circuits the leakage current to earth, by-passing lead CD;
- increase the distance between the wires;
- decrease the dielectric constant of medium between wires;
- decrease the diameter of the conductors;
- decrease the length of the wires.

B. MEASURES TO REDUCE OR ELIMINATE INDUCED INTERFERENCES

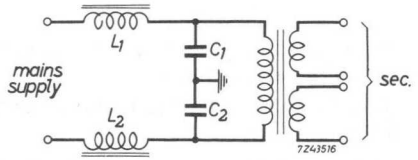
It should be noticed that induced interfering pulses may upset the functioning of systems by entering the logic circuits via:

1 the mains supply
2 induction on the low-voltage supply lines to the circuitry (included earth lines)
3 induction on lines which transmit the driving signals.

Generally, it is of great importance to place the transistor circuitry in a well-earthed metal case or frame. Metal sheet with a thickness of 1 mm will serve the purpose. The material must have a proper permeability to ensure sufficient magnetic screening, e.g. iron or steel (not aluminium).

Interference, which is introduced via the ways 1, 2 or 3 can be suppressed by:

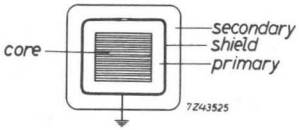
1.1 A filter in the primary of the mains transformer.



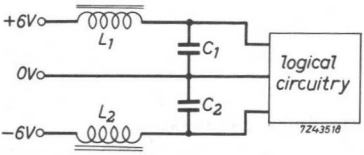
$L_1 = L_2 = 10$ mH
$C_1 = C_2 = 12$ kpf/700 V

When this is still inconclusive, a third capacitor can be connected in parallel with the primary of the transformer.

1.2 An electrostatic shield between primary and secondary of the mains transformer. This shield consists of a layer of copper foil which is connected to earth.



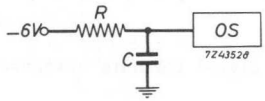
2.1 A filter in the low voltage supply lines of the logical circuitry.



$L_1 = L_2 = 510$ μH/0.5 Ω
$C_1 = C_2 = 100$ μF

Care should be taken that only the low-level logical circuits are supplied via this filter, as otherwise the current variations will become excessive.

2.2 It is sometimes necessary to use an extra filter in the −6 V supply line close to the circuits, that are sensitive to interference, e.g. the one-shot multivibrator OS.

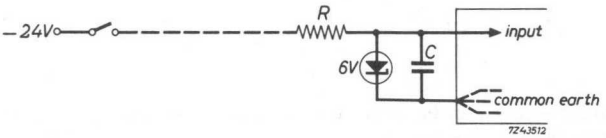


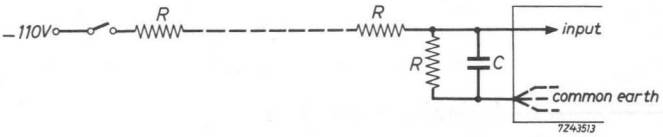
R = 47 Ω
C = 100 μF

3. If signals are to be transmitted from one part of the equipment to another the following rules must be observed:
   - improve the signal-to-noise (interference) level on the line by raising the voltage level of the signal;
   - apply low-pass filters at all equipment inputs, cutting off signals of a frequency higher than the maximum signal frequency;
   - prefer "level" (d.c.) signal transmission to pulse transmission (interference is often intermittent and of short duration).

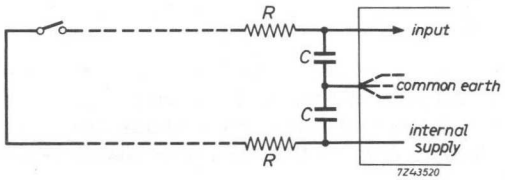
   A few circuits are given below:

3.1 Electro-mechanical contact, external supply:



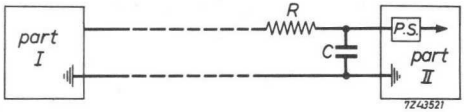


3.2 External contact, supply from the equipment:



Note: apply this filtering particularly when the supply, common to the transistor circuits, is used for the line as well. Choose the resistors such that overloading the power supply or transistorized circuitry at short-circuit conditions of the line is avoided.

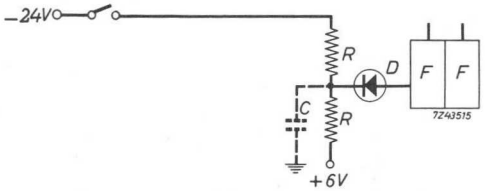
3.3 Transmission of lower-speed timing signals between equipment parts:



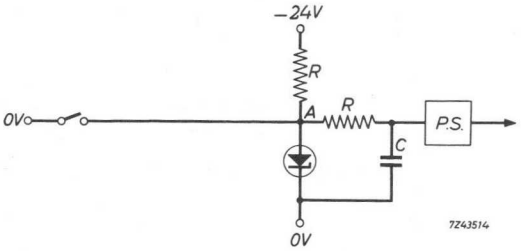
After the RC-network has been passed, the signal form is restored by a pulse shaper.
Note the delay in pulse transmission caused by the RC-network.

3.4 Remote setting of a flip-flop from a negative voltage source.

When the switch is open, the diode is non-conducting, because of the +6 V threshold voltage.
The diode remains blocked for positive interference pulses, whereas for negative pulses to become effective the amplitude must be at least comparable with the threshold voltage.

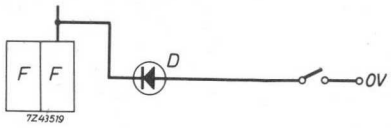


3.5 An almost similar effect can be obtained with the following circuit, intended for driving pulse shapers or inverters.



The voltage at point A will be −6 V when the switch is open. Negative interference pulses will not influence the state of the pulse shaper; positive pulses are short-circuited by the conducting Zener diode. When the switch is closed, point A will become 0 V, so that the pulse shaper is caused to change its state.

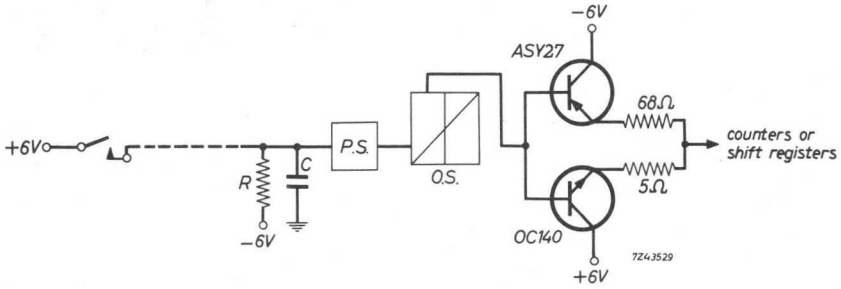
3.6 Remote setting of a flip-flop from a voltage of 0 V.



By closing the switch, the flip-flop is forced to change its state. This method has the advantage, that switch and line are not connected to the sensitive, high-impedance base input.

3.7 Avoidance of contact bouncing

When a shift register or counter must be operated by an electro-mechanical contact, it is essential that the contact bouncing should be avoided. This can be done by means of a one-shot multivibrator of which the pulse has the required characteristics.
To reduce the time in which interference can be induced (switch open) a break contact is used. The one-shot multivibrator operates every time the switch is opened.



LOADING TABLE

If not indicated separately the N and P terminal(s) of each unit are connected to V_N respectively V_P. (V_N = −6 V ±5 %, V_P = +6 V ±5 %.)

preceding unit or preceding chain of units		driving unit		via	maximum number of driven units							
					FF1		FF2			FF3		
		type	out-put		W	A	W	A	G	W	A1 or A2	A1 + A2
		FF1	Q		1[1]	4[9]	1[1]	4[9]	2[10]	1[1]	2[10]	2[10]
		FF2	Q		1[1]	1[10]	1[1]	1[10]	2[10]	1[1]	1[10]	1[10]
		FF3	Q		1[1]	5[9]	1[1]	5[9]	2[10]	1[1]	3[10]	3[10]
		FF4	Q		1[1]	5[9]	1[1]	5[9]	2[10]	1[1]	3[10]	3[10]
	IA1	N1	Q		0	4[4])[3]	0	4[4])[3]	0	0	2[3]	1[3]
	FF1[10] OS1[b]				0	4[4]	0	4[4]	0	0	2	1
PS1	IA2											
	FF2[10]				0	1[4]	0	1[4]	0	0	1	1
	PS1				0	2[4]	0	2[4]	0	0	1	0
	FF3[10] FF4[10]				0	5[4]	0	5[4]	0	0	3	2
	OS2[d]				0	6	0	6	0	0	6	5
	OS2[e]				0	5	0	5	0	0	5	3
	N1	P1	Q		0	0	0	0	0	0	0	0
		EF1	Q		4[1]		4[1]		0	3[1]	0	0
			T		1[6]		1[6]		0	1[6]	0	0
		IA1	Q		2[1]	4[3]	2[1]	4[3]	3	2[1]	2[3] 3[3])[7]	2[3] 3[3])[7]
	N1	EF2	Q	ASY27[c]	2[1]	4	2[1]	4	3	1[1]	2	2
N1	P1			ASY27[c]	2[1]	4	2[1]	4	3	1[1]	2	2
	N1		R		1	0	1	0	0	1	0	0
N1	P1											
	N1[5]	IA2	Q		2[1]	0	2[1]	0	0	2[1]	0	0
N1	P1[8]											
	IA1 IA2				2[1]	4	2[1]	4	3	2[1]	4 5[7]	4 5[7]
	PS1				2[1]	4	2[1]	4	3	2[1]	2 3[7]	2 3[7]
	OS2[d]											
	N1[5]	IA2[a]	Q		0	0	0	0	1	0	0	0
N1	P1[8]											
		PS1	Q		0	2	0	2	2	0	1	1
		OS1	Q1		2[1]	4	2[1]	4	3	2[1]	2	1
			Q2		1[1]	0	1[1]	0		0	0	0
		OS2	Q1		1[1]	6	1[1]	6	6	1[1]	6	5
			Q2		0	5	0	5	2	0	5	3
		PD1	Q		0	20	0	20	0	0	22	20
		GI1	Q		0	1	0	1	6	0	2	2
	GI1	GI1[f]	Q		0	4[13]	0	4[13]	19	0	6	6
AND-AND AND-OR	GI1	GI1	Q		0	4[13]	0	4[13]	11	0	5	5

maximum number of driven units														
FF4			N1	EF1	IA1	EF2	IA2	PS1	OS1	OS2	PA1	PD1		GI1
W	A	G	W	W	W	W	W	W	A2	A	W	A	G	G
1[1]	2[10]	2[10]	5	1	1	2	0	6[9] 2[2]	4[9]	2[10]	1	1[10]	1[10]	2[10]
1[1]	1[10]	2[10]	5	1	1	2	0	2[10] 2[2]	1[10]	2[10]	1	1[10]	1[10]	2[10]
1[1]	3[10]	3[10]	12	1	1	2	0	7[9] 2[2]	5[9]	4[10]	2	3[10]	3[10]	4[10]
1[1]	3[10]	3[10]	12	1	1	2	0	7[9] 2[2]	5[9]	4[10]	2	3[10]	3[10]	4[10]
0	1[3]	0	0	0	0	1	1[5]	1	4[4] 3[3]	1[3]	0	1[3]	0	
0	1	0	0	0	0	1	1[5]	1	4[4]	2	0	2	0	
0	1	0	0	0	0	1	1[5]	1	1[4]	1	0	1	0	
0	0	0	0	0	0	1	1[5]	1	2[4]	0	0	0	0	
0	2	0	0	0	0	1	1[5]	1	5[4]	3	0	3	0	
0	5	0	0	0	0	1	1[5]	1	8	12	0	10	0	
0	3	0	0	0	0	1	1[5]	1	6	4	0	3	0	
0	0	0	0	0	0	1	1[8]	1	0	0	0	0	0	0
3[1]	0	0	4		4		0	18[2]		0	0	0	0	0
1[6]	0	0			0		1	0		0	0	0	0	0
2[1]	2[3] 3[3] 7[3]	2	7 16[7]	2	2	5	1	8[2]	4[3]	4[3] 7[3] 7[3]	1	2[3]	2	
1[1]	2	10	50	2	2	5	1	8[2]	4	4	1	4	6	
1[1]	2	10	27	2	2	5	1	8[2]	4	4	1	4	6	
1	0	0	0	0	0	0	0	0	0	0	0	0	0	
2[1]	0	0	0	2	2	5	1	8[2]	0	0	0	0	0	
2[1]	4 5[7]	10	60	2	2	5	1	8[2]	6	7 9[7]	10	7 9[7]	8	
2[1]	2 3[7]	10	60	2	2	5	1	8[2]	4	3 6[7]	6	3 6[7]	4	
0	0	2	6 9[7]	1	1	1	1	4[2]	0	0	1	0	2 3[7]	
0	1	1	2	1	1	2	1	6[2]	2	1	0	1	1	1
2[1]	1	1	3	2	2	5	0	8[2]	4	1	0	1	1	2
0	0	0	0	1	1	2	0	3[2]	0	0	0	0	0	0
1[1]	5	10	12	1	1	2	1	6[2]	6	13	7	10	10	8
0	3	3	4	1	0	1	0	3[2]	5	4	2	3	3	6
0	20	0	10 75[11]	0	25[12]	0	0	0	20	50	0	38	0	30
0	2	5	6					4[2]	1	6	6	6	7	3
0	6	19	19					7[2]	4[13]	19	16	18	19	9
0	5	11	11					7[2]	4[13]	11	10	11	11	7

Notes:

P1 Unless specified otherwise a P1 may be interposed between two units without great influence upon the loadibility. AC inputs of FF1, FF2, FF3, FF4, OS1 and OS2 cannot be driven from it.

2PL1 The 2PL1 is normally used in conjunction with FF1 or FF2. In this case the input data are equivalent to those of the similar FF2 inputs. The output terminals are directly connected to the d.c. input terminals of the FF1 or FF2.

2PL2 Ditto for FF3 and FF4.

a) IA2 with only terminals N1 or N2 connected to V_N.
b) OS1 Q1 output only.
c) ASY27 common emitter stage with 1 kΩ collector resistor.
d) OS2 Q1 output only.
e) OS2 Q2 output only.
f) Used as NON-INVERTING AMPLIFIER.

////// not recommended.

1. Each via a 4.7 kΩ ±5 % resistor in series with a separating diode OA200, anode to driven unit.
2. Each via a 12 kΩ ±5 % resistor, bypassed by a 330 pF capacitor.
3. Only if the chain of units indicated is driven by a FF1, FF2, FF3, FF4, PS1 or the Q1 terminal of an OS1 or OS2.
4. The maximum speed of operation is
$$\frac{30 \text{ kHz}}{\text{number of units driven by the N1 gate}}$$
5. Via a diode OA200, cathode to N1, anode to IA2, and bypassed by a 1500 pF capacitor.
6. Via a separating diode OA85, cathode to driven unit.
7. Only if the N-terminals of the driving unit are floating.
8. The P-terminal of the P1 gate is floating.
9. Total number for both Q-outputs together.
10. Total number per Q-output.
11. Only with a 390 Ω ±5 % resistance between the terminals Q and N of the driving unit PD1.
12. For each a resistance of 2.7 kΩ ±5 % between the terminals Q and N of the driving unit PD1.
13. Only with a 1.3 kΩ ±5 % resistance between the terminals Q and N of the driving unit.

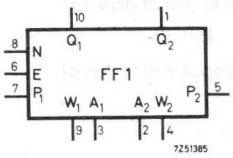
FLIP-FLOP

Colour: red

The unit FF1 contains a transistor bi-stable multivibrator circuit. The transistors are medium-speed switching types.

The circuit constitutes a memory function when driven by means of a d.c. level or a positive-going voltage step (a.c. input signal), and it can also be used as a binary scale-of-two with a positive-going input signal.

Pulse repetition frequency range:	0–100 kHz
Ambient temperature range:	−20 to +60 °C
Weight:	approx. 20 g

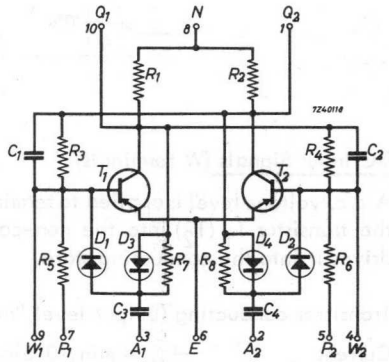


Drawing symbol

CIRCUIT DATA

Terminal

1 = Q_2 = output 2
2 = A_2 = a.c. input 2
3 = A_1 = a.c. input 1
4 = W_2 = d.c. input 2
5 = P_2 = supply +6V(2)
6 = E = common supply 0V
7 = P_1 = supply +6V(1)
8 = N = supply −6V
9 = W_1 = d.c. input 1
10 = Q_1 = output 1



Power Supply

Terminal 5:	V_{P2} = +6V ± 10%, I_{P2} = 0.15 mA [1]	Nominal value of the current
6:	V_E = 0V common	
7:	V_{P1} = +6V ± 10%, I_{P1} = 0.15 mA [1]	
8:	V_N = −6V ± 10%, $-I_N$ = 7 mA [1]	

[1]) The sign is positive when the current flows towards the circuit.

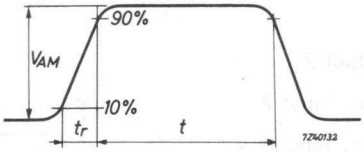
INPUT DATA

Input Signal Requirements [2])

AC Input Signal (A terminals)

A positive-going voltage step is applied to terminal A_1 or A_2, or to both terminals interconnected in the case of binary scale-of-two applications. This voltage step drives the transistor T_1 (T_2) into the non-conducting state.

Voltage	V_{AM}	= min. $-0.66V_N$
		= max. $-V_N$
Rise time	t_r	= max. 0.4 µs
Length of driving pulse	t	= min. 0.5 µs
Input noise level		= max. 1 V peak to peak



DC Input Signals (W terminals)

A d.c. voltage level is applied to terminal W_1 or W_2. A positive voltage drives the transistor T_1 (T_2) into the non-conducting state and a negative voltage drives it into the conducting state.

Transistor conducting (output level "negative low")

Current	$-I_W$	= min. 0.5 mA [1]) ($-V_W$ = max. 0.35 V)
limiting value		= max. 10 mA [1])

[1]) The sign is positive when the current flows towards the circuit

[2]) These data apply to the most adverse working condition for a combination of units, namely to supply voltages V_N = -5.4 V and V_P = +6.6 V. Unless differently specified all the voltage and current figures quoted represent absolute maximum values.

Transistor non-conducting (output level "negative high")

Voltage	V_W	= min. 0.2V
limiting value		= max. 10V
Current	I_W	= min. 1mA [1])
	(I_W	= appr. 1.1mA [1]) at V_W = 6V)

Input Impedance

Equivalent to a capacitance of approximately 500 pF (A_1, A_2 terminal or both terminals interconnected).

OUTPUT DATA

Output Signal Characteristics [2])

Transistor conducting (output level "negative low")

Voltage	$-V_Q$	= max. 0.2V
Load current	$-I_Q$	= max. 2.5mA [1])

Transistor non-conducting (output level "negative high")

Voltage	$-V_Q$	= min. -0.7V_N
Load current	I_Q	= max. 0.7mA [1])

Load currents of equal sign, up to the values given as maxima can be drawn from the two output terminals simultaneously. In the case of simultaneous load currents of opposite sign, the maximum load currents given are not guaranteed.

Maximum Capacitive Load (2000 pF for both Q-outputs together)

When the maximum capacitive and resistive loads are applied in parallel, the maximum pulse repetition frequency is not guaranteed.

Output Impedance

Equivalent to a resistance of approx.

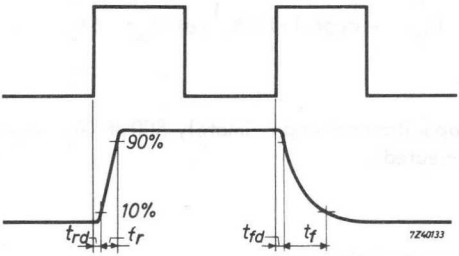
R_i = 50Ω for positive-going output voltage

R_i = 1000Ω for negative-going output voltage

1) See note 1 on previous page
2) See note 2 on previous page

Switching and Delay Times (for orientation only)

A square wave input signal (A terminals) is assumed with an amplitude of min. $-0.7V_N$.



Unit Unloaded

Rise delay	t_{rd}	= max. 0.8 µs
Rise time	t_r	= max. 0.3 µs
Fall delay	t_{fd}	= max. 0.6 µs
Fall time	t_f	= max. 2 µs

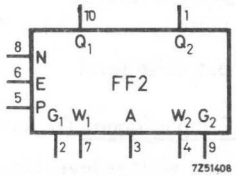
FLIP-FLOP

Colour: red

The unit FF2 contains a transistor bi-stable multivibrator circuit. The transistors are medium-speed switching types.

The circuit constitutes a memory function when driven by means of a d.c. level or a positive-going voltage step (a.c. input signal). In the case of a.c. drive, the switching of the flip-flop can be controlled by a d.c. level supplied to the built-in gate circuits (e.g. in shift registers).

Pulse repetition frequency range:	0–100 kHz
Ambient temperature range:	-20 to +60 °C
Weight:	approx. 20 g

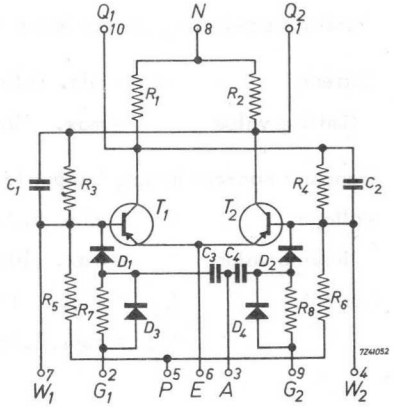


Drawing symbol

CIRCUIT DATA

Terminal

1 = Q_2 = output 2
2 = G_1 = gate input 1
3 = A = a.c. input
4 = W_2 = d.c. input 2
5 = P = supply +6 V
6 = E = common supply 0 V
7 = W_1 = d.c. input 1
8 = N = supply -6 V
9 = G_2 = gate input 2
10 = Q_1 = output 1



Power Supply

Terminal 5: V_P = +6 V ± 10%, I_P = 0.3 mA [1])
6: V_E = 0 V common
8: V_N = -6 V ± 10%, $-I_N$ = 7 mA [1])

} Nominal value of the current

[1]) The sign is positive when the current flows towards the circuit.

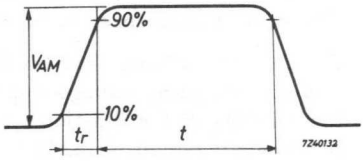
INPUT DATA

Input Signal Requirements [2])

AC Input Signal (A terminal)

A positive-going voltage step is applied to terminal A. This voltage step drives the transistor T_1 (T_2) into the non-conducting state if the corresponding gate has been opened by a proper d.c. gate input signal on terminal G_1 (G_2)

Voltage	V_{AM}	= min.	$-0.66 V_N$
		= max.	$- V_N$
Rise time	t_r	= max.	0.4 µs
Length of driving pulse	t	= min.	0.5 µs
Input noise level		= max.	1 V peak to peak



DC Input Signal (W terminals)

A d.c. voltage level is applied to terminal W_1 or W_2. A positive voltage drives the transistor T_1 (T_2) into the non-conducting state and a negative voltage drives it into the conducting state.

Transistor conducting (output level "negative low")

Current	$-I_W$	= min.	0.5 mA [1]) ($-V_W$ = max. 0.35 V)
limiting value		= max.	10 mA [1])

Transistor non-conducting (output level "negative high")

Voltage	V_W	= min.	0.2 V
limiting value		= max.	10 V
Current	I_W	= min.	1 mA [1])
	(I_W	= appr.	1.1 mA [1]) at V_W = 6 V)

[1]) The sign is positive when the current flows towards the circuit

[2]) These data apply to the most adverse working condition for a combination of units, namely to supply voltages V_N = -5.4 V and V_P = +6.6 V. Unless differently specified, all the voltage and current figures represent absolute maximum values.

Gate Input Signal (G terminals)

A d.c. voltage level is applied to terminal G_1 (G_2). Transistor T_1 (T_2) is driven into the non-conducting state by the a.c. input signal (A terminal) if the corresponding gate input G_1 (G_2) is at "negative low" level (i.e. gate open).

Note 1. The G_1 and G_2 input levels should not be "negative low" simultaneously.

2. The G_1 and G_2 input levels have to be present 8 µs before the arrival of the a.c. input signal

Gate Open (input level "negative low")

Voltage $-V_G$ = max. 0.2V
= min. 0V

Gate closed (input level "negative high")

Voltage $-V_G$ = min. V_{AM} (V_{AM} = amplitude of a.c. input signal)
= max. $-V_N$

Input Impedance

Equivalent to a capacitance of approx. 500 pF (A terminal)

OUTPUT DATA

Output Signal Characteristics [2])

Transistor conducting (output level "negative low")

Voltage $-V_Q$ = max. 0.2V
Load current $-I_Q$ = max. 2.5mA [1])

Transistor non-conducting (output level "negative high")

Voltage $-V_Q$ = min. $-0.7V_N$
Load current I_Q = max. 0.7mA [1])

Load currents of equal sign, up to the values given as maxima, can be drawn from the two output terminals simultaneously. In the case of simultaneous load currents of opposite sign, the maximum load currents given are not guaranteed.

[1]) See note 1 on previous page

[2]) See note 2 on previous page

Maximum Capacitive Load (500 pF for each Q-output)

When the maximum capacitive and resistive loads are applied in parallel, the given maximum pulse repetition frequency is not guaranteed.

Output Impedance

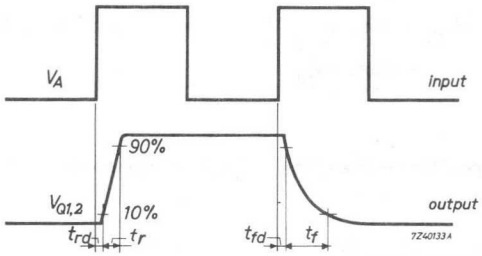
Equivalent to a resistance of approx.

R_i = 50 Ω for positive-going output voltage

R_i = 1000 Ω for negative-going output voltage

Switching and Delay Times (for orientation only)

A square wave input signal (A terminals) is assumed with an amplitude of min. $-0.7V_N$.



Unit Unloaded

Rise delay	t_{rd}	= max. 0.8 µs
Rise time	t_r	= max. 0.3 µs
Fall delay	t_{fd}	= max. 0.6 µs
Fall time	t_f	= max. 2 µs

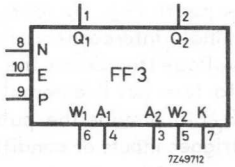
FLIP-FLOP

Colour: red

The unit FF3 contains a transistor bi-stable multivibrator circuit. The transistors are medium-speed switching types.

The circuit constitutes a memory function when driven by means of a d.c. level or a positive-going trigger signal, and it can also be used as a binary scale-of-two when the trigger inputs are interconnected.

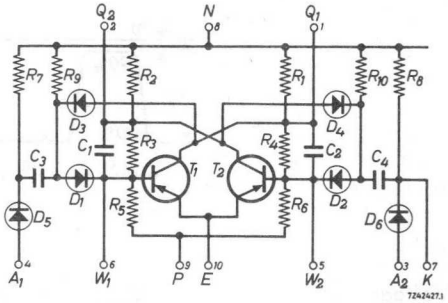
Frequency range	:	0 - 100 kHz
Ambient temperature range:		-20 to +60 °C
Weight	:	approx. 20 g



Drawing symbol

CIRCUIT DATA

Terminal



1 = Q_1 = output 1

2 = Q_2 = output 2

3 = A_2 = trigger input 2

4 = A_1 = trigger input 1

5 = W_2 = d.c. input 2

6 = W_1 = d.c. input 1

7 = K = terminal for external trigger input

8 = N = supply -6 V

9 = P = supply +6 V

10 = E = common supply 0 V

Power Supply

Terminal 8 : V_N = -6 V ± 5 %, $-I_N$ = 8.8 mA } Nominal value

9 : V_P = 6 V ± 5 %, I_P = 0.6 mA } of the current

10 : V_E = 0 V common

Notes

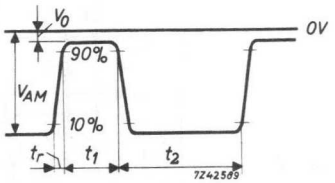
- The data given apply to the most adverse supply voltages for a combination of units, namely V_N=-5.7 V and V_P=6.3 V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input Signal Requirements

Trigger Input Signal (A terminals)

A positive-going voltage step is applied to terminal A_1 or A_2, or to both terminals interconnected in the case of binary scale-of-two applications. This voltage step drives the transistor T_1 (T_2) into the non-conducting state.
To terminal K external diodes can be connected (in the same sense as diode D_6) to provide the pulse-gate, corresponding with terminal A_2, with extra trigger inputs or condition inputs.



Voltage	V_{AM}	= min.	-0.7	V_N
		= max.	-	V_N
	$-V_o$	= min.	0	V
		= max.	0.2	V

		A_1 or A_2	A_1 and A_2 interconnected
Required direct current	I_{AD}	= min. 0.88 mA	min. 1.75 mA
Required current during the transient averaged over: 0.4 µs	I_{AT}	= min. 5 mA	min. 6 mA
0.7 µs		= min. 4 mA	min. 4.5 mA

Rise time	t_r	=	max.	0.7 µs
Pulse duration	t_1	=	min.	1 µs
	t_2	=	min.	8 µs
Input noise level	V_n	=	max.	1 V peak to peak

DC Input Signal (W terminals)

A d.c. voltage level is applied to terminal W_1 or W_2. A positive voltage drives the transistor T_1 (T_2) into the non-conducting state and a negative voltage drives it into the conducting state

Transistor conducting				
Current	$-I_W$	=	min.	0.6 mA ($-V_W$ = max. 0.4 V)
limiting value		=	max.	15 mA
Transistor non-conducting				
Voltage	V_W	=	min.	0.2 V
limiting value		=	max.	10 V
Current	I_W	=	min.	0.9 mA

OUTPUT DATA

Voltages and currents

Transistor conducting

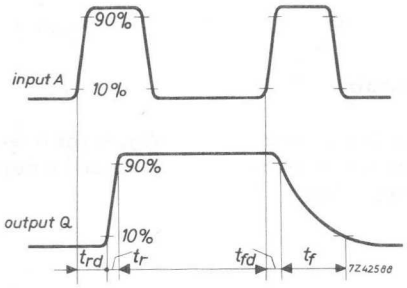
Voltage	$-V_Q$	=	max.	0.2 V
Available direct current	$-I_{QD}$	=	max.	6 mA
Available current during the transient				
averaged over: 0.4 µs	$-I_{QT}$	=	max.	11 mA
0.7 µs		=	max.	14 mA

Transistor non-conducting

Voltage	$-V_Q$	=	min.	-0.7 V_N
Available direct current	I_{QD}	=	max.	0.7 mA

Switching and delay times

These data are for orientation only and refer to an input signal as specified under INPUT DATA.



	Unit unloaded	Unit max. loaded
Rise delay	t_{rd} = max. 1.0 µs	max. 1.1 µs
Rise time	t_{r} = max. 0.3 µs	max. 0.7 µs
Fall delay	t_{fd} = max. 0.8 µs	max. 0.8 µs
Fall time	t_{f} = max. 1.7 µs	max. 1.7 µs

FLIP-FLOP

Colour: red

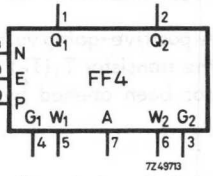
The unit FF4 contains a transistor bi-stable multivibrator circuit. The transistors are medium-speed switching types.

The circuit constitutes a memory function when driven by means of a d.c. level or a positive-going trigger signal. In the case of trigger drive, the switching of the flip-flop can be controlled by a d.c. level applied to the built-in gate circuits (e.g. in shift registers).

Frequency range : see INPUT DATA

Ambient temperature range : -20 to +60 °C

Weight : approx. 20 g

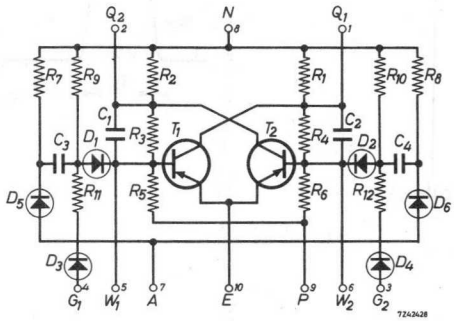


Drawing symbol

CIRCUIT DATA

Terminal

1 = Q_1 = output 1
2 = Q_2 = output 2
3 = G_2 = gate input 2
4 = G_1 = gate input 1
5 = W_1 = d.c. input 1
6 = W_2 = d.c. input 2
7 = A = trigger input
8 = N = supply -6 V
9 = P = supply +6 V
10 = E = common supply 0 V



Power Supply

Terminal 8 : V_N = -6 V ± 5 %, $-I_N$ = 8.8 mA } Nominal value
9 : V_P = +6 V ± 5 %, I_P = 0.6 mA } of the current
10 : V_E = 0 V common

Notes

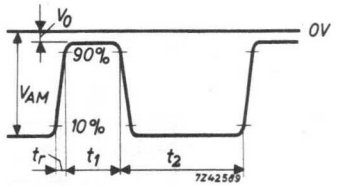
- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N = -5.7$ V and $V_p = 6.3$ V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input Signal Requirements

Trigger Input Signal (A terminal)

A positive-going voltage step is applied to terminal A. This voltage step drives the transistor $T_1(T_2)$ into the non-conducting state if the corresponding gate has been opened by an appropriate gate input signal on terminal $G_1(G_2)$.



Voltage	V_{AM}	= min.	-0.7	V_N
		max.	-	V_N
	$-V_o$	= min.	0	V
		max.	0.2	V
Required direct current	I_{AD}	= min.	1.75	mA
Required current during the transient				
averaged over: 0.4 µs	I_{AT}	= min.	6	mA
0.7 µs		min.	4.5	mA
Rise time	t_r	= max.	0.7	µs
Pulse duration	t_1	= min.	3	µs
	t_2	= min.	11	µs
Input noise level	V_n	= max.	1 V peak to peak	

DC Input signal (W terminals)

A d.c. voltage level is applied to terminal W_1 or W_2. A positive voltage drives the transistor $T_1(T_2)$ into the non-conducting state and a negative voltage drives it into the conducting state.

Transistor conducting		
Current	$-I_W$ = min. 0.6 mA	($-V_W$ = max. 0.4 V)
limiting value	= max. 15 mA	
Transistor non-conducting		
Voltage	V_W = min. 0.2 V	
limiting value	= max. 10 V	
Current	I_W = min. 0.9 mA	

Gate Input Signal (G terminals)

A d.c. voltage level is applied to terminal $G_1(G_2)$. Transistor $T_1(T_2)$ is driven into the non-conducting state by the trigger input signal (A terminal) if the corresponding gate is opened by an appropriate gate input signal.

		gate open	gate closed
Voltage	$-V_G$	= min. 0 V	min. V_{AM}
		max. 0.2 V	max. - V_N
Required gate current caused by negative transient of V_{AM}	I_{GD}	= min. 1.75 mA	min. 1.2 mA

		to open gate	to close gate
Required average current during the positive transient of V_G	I_{GT}	= min. 1.6 mA	–
Gate setting time			
when the gate input level changes at random:	t_{GS}	= min. 17 µs	min. 25 µs
when the gate input level changes within 2 µs after the positive going edge of the trigger signal:	t_{GS}	= min. 11 µs	min. 11 µs

Note: The latter applies to a shift register configuration so that the max. shift frequency is approximately 70 kHz.

During triggering the G levels should not be at zero voltage level simultaneously.

The gate setting time is the required waiting time between the last G level change and the potitive going edge of the trigger pulse.

OUTPUT DATA

Voltages and currents

Transistor conducting

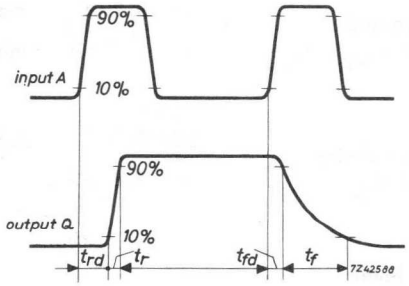
Voltage	$-V_Q$	= max.	0.2	V
Available direct current	$-I_{QD}$	= max.	6	mA
Available current during the transient				
averaged over: 0.4 µs	$-I_{QT}$	= max.	11	mA
0.7 µs		= max.	14	mA

Transistor non-conducting

Voltage	$-V_Q$	= min.	-0.7	V_N
Available direct current	I_{QD}	= max.	0.7	mA

Switching and delay times

These data are for orientation only and refer to an input signal as specified under INPUT DATA.



		Unit unloaded		Unit max. loaded	
Rise delay	t_{rd}	= max. 1.0	µs	max. 1.1	µs
Rise time	t_r	= max. 0.3	µs	max. 0.7	µs
Fall delay	t_{fd}	= max. 0.8	µs	max. 0.8	µs
Fall time	t_f	= max. 1.7	µs	max. 1.7	µs

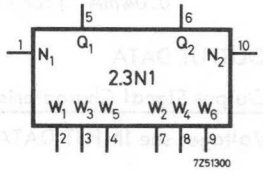
DUAL NEGATIVE GATE

Colour: orange

The unit 2.3N1 contains two three-input germanium-diode gates, that perform an AND logical operation on negative input-voltage signals.

The two gate circuits are identical and can be used separately or combined into a multiple-input gate by interconnecting the output terminals Q_1 and Q_2. In this latter case only one negative supply terminal should be used.

Pulse repetition frequency range:	0–100 kHz
Ambient temperature range:	−20 to +60 °C
Weight:	approx. 20 g

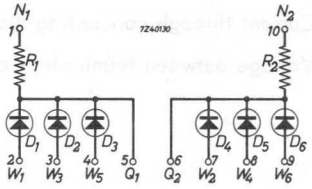


Drawing symbol

CIRCUIT DATA

Terminal

1 = N_1 = supply −6 V (1)
2 = W_1 = input 1
3 = W_3 = input 3
4 = W_5 = input 5
5 = Q_1 = output 1
6 = Q_2 = output 2
7 = W_2 = input 2
8 = W_4 = input 4
9 = W_6 = input 6
10 = N_2 = supply −6 V (2)



Power Supply

Terminal 1: $V_{N1} = -6V \pm 10\%$, $-I_{N1} = 0\text{–}0.5mA$ [1]) } Nominal value of the current
10: $V_{N2} = -6V \pm 10\%$, $-I_{N2} = 0\text{–}0.5mA$ [1]) }

INPUT DATA

Input Signal Requirements [2])

Voltage: Under all circumstances normally encountered when the unit is used in conjunction with other circuit blocks: $V_{Wn} = 0.1$ to $0.5V$ more positive than V_Q dependent on the input current I_{Wn}.

Current: To be supplied to terminal W_n having the least negative voltage level. For V_{Wn} [1]) = 0 volt and $I_Q = 0mA$: I_{Wn} = max. 0.48mA [1]) + max. 0.04mA [1]) for every W terminal at a negative voltage level.

OUTPUT DATA

Output Signal Characteristics [2])

Voltage: see INPUT DATA

Load current I_Q = max. $\frac{-V_N + V_Q}{13}$ mA [1])

Output Impedance

When V_Q is positive-going, the output impedance approximates the output impedance of the driving circuit. When V_Q is negative-going, the output impedance is max. 13kΩ.

LIMITING VALUES

Current through conducting diode I_{Wc} = max. 10mA

Voltage between terminals N and W = max. 30V

[1]) The sign is positive when the current flows towards the circuit.

[2]) These data apply to the most adverse working condition for a combination of units, namely to a supply voltage $V_N = -5.4V$. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

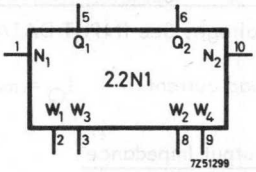
DUAL NEGATIVE GATE

Colour: orange

The unit 2.2N 1 contains two two-input germanium-diode gates that perform an AND logical operation on negative input voltage signals.

The two gate circuits are identical and can be used separately or combined into a multiple-input gate by interconnecting the output terminals Q_1 and Q_2. In this latter case, only one negative supply terminal should be used.

Pulse repetition frequency range:	0-100 kHz
Ambient temperature range:	-20 to +60 °C
Weight:	approx. 20 g

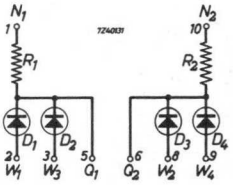


Drawing symbol

CIRCUIT DATA

Terminal

1 = N_1 = supply -6V (1)
2 = W_1 = input 1
3 = W_3 = input 3
4 = not connected
5 = Q_1 = output 1
6 = Q_2 = output 2
7 = not connected
8 = W_2 = input 2
9 = W_4 = input 4
10 = N_2 = supply -6V (2)



Power Supply

Terminal 1: $V_{N1} = -6V \pm 10\%$, $-I_{N1} = 0\text{-}0.5mA$ [1]) } Nominal value of the current

10: $V_{N2} = -6V \pm 10\%$, $-I_{N2} = 0\text{-}0,5mA$ [1]) } Nominal value of the current

[1]) The sign is positive when the current flows towards the circuit.

INPUT DATA

Input Signal Requirements [2])

Voltage: Under all circumstances normally encountered when the unit is used in conjunction with other circuit blocks: V_{Wn} = 0.1 to 0.5 V more positive than V_Q dependent on the input current I_{Wn}.

Current: To be supplied to terminal W_n having the least negative voltage level. For V_{Wn} = 0 volt and I_Q = 0 mA: I_{Wn} = max. 0.48 mA [1]) + max. 0.04 mA [1]) for every W terminal at a negative voltage level.

OUTPUT DATA

Output Signal Characteristics [2])

Voltage: See INPUT DATA

Load current $I_Q = \text{max.} \frac{-V_N + V_Q}{13}$ mA [1])

Output Impedance

When V_Q is positive-going, the output impedance approximates the output impedance of the driving circuit. When V_Q is negative-going, the output impedance is max. 13 kΩ.

LIMITING VALUES

Current through conducting diode I_{Wc} = max. 10 mA

Voltage between terminals N and W = max. 30 V

[1]) The sign is positive when the current flows towards the circuit

[2]) These data apply to the most adverse working condition for a combination of units, namely to a supply voltage V_N = -5.4 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

DUAL POSITIVE GATE

Colour: orange

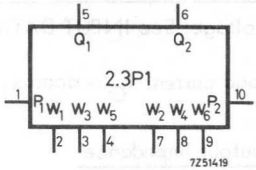
The unit 2.3P1 contains two three-input silicon-diode gates, that perform an OR logical operation on negative input-voltage signals.

The two gate circuits are identical and can be used separately or combined into a multiple-input gate by interconnecting the output terminals Q_1 and Q_2. In this latter case, only one positive supply terminal should be used.

Pulse repetition frequency range: 0–100 kHz

Ambient temperature range: −20 to +60 °C

Weight: approx. 20 g

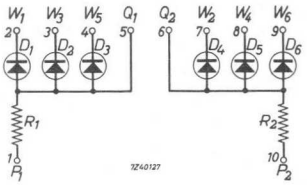


Drawing symbol

CIRCUIT DATA

Terminal

1 = P_1 = supply +6 V (1)
2 = W_1 = input 1
3 = W_3 = input 3
4 = W_5 = input 5
5 = Q_1 = output 1
6 = Q_2 = output 2
7 = W_2 = input 2
8 = W_4 = input 4
9 = W_6 = input 6
10 = P_2 = supply + 6 V (2)



Power Supply

Terminal 1: V_{P1} = 6 V ± 10%, I_{P1} = 0.05–0.1 mA [1)] } Nominal value of the current

10: V_{P2} = 6 V ± 10%, I_{P2} = 0.05–0.1 mA [1)] } Nominal value of the current

[1]) The sign is positive when the current flows towards the circuit.

INPUT DATA

Input Signal Requirements [2])

Voltage: Under all circumstances normally encountered when the unit is used in conjunction with other circuit blocks: V_{Wn} = 0.4 to 1 V more negative than V_Q dependent on the input current I_{Wn}.

Current : To be supplied to terminal W_n having the most negative voltage level. $-I_{Wn}$ = approx. I_Q + max. 0.07 mA at $-V_Q$ = 1 V.

OUTPUT DATA

Output Signal Characteristics [2])

Voltage: See INPUT DATA

Load current I_Q = approx. $-I_{Wn}$ - max. 0.07 mA [1]) at $-V_Q$ = 1 V

Output Impedance

When V_Q is negative-going, the output impedance approximates the output impedance of the driving circuit. When V_Q is positive-going, the output impedance is max. 130 kΩ.

LIMITING VALUES

Current through conducting diode I_{Wc} = max. 10 mA

Voltage between terminals P and W = max. 30 V

[1]) The sign is positive when the current flows towards the circuit

[2]) These data apply to the most adverse working conditions for a combination of units, namely to a supply voltage V_P = +6.6 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

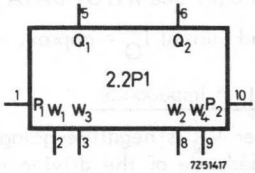
DUAL POSITIVE GATE

Colour: orange

The unit 2.2P1 contains two two-input silicon-diode gates, that perform an OR logical operation on negative input-voltage signals.

The two gate circuits are identical and can be used separately or combined into a multiple-input gate by interconnecting the output terminals Q_1 and Q_2. In this latter case, only one positive supply terminal should be used.

Pulse repetition frequency range:	0–100 kHz
Ambient temperature range:	−20 to +60 °C
Weight:	approx. 20 g

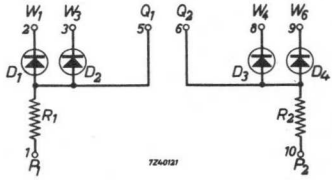


Drawing symbol

CIRCUIT DATA

Terminal

1 = P_1 = supply +6 V (1)
2 = W_1 = input 1
3 = W_3 = input 3
4 = not connected
5 = Q_1 = output 1
6 = Q_2 = output 2
7 = not connected
8 = W_2 = input 2
9 = W_4 = input 4
10 = P_2 = supply +6 V (2)



Power Supply

Terminal 1: $V_{P1} = 6\,V \pm 10\%$, $I_{P1} = 0.05\text{–}0.1\,mA$ [1])
10: $V_{P2} = 6\,V \pm 10\%$, $I_{P2} = 0.05\text{–}0.1\,mA$ [1])

} Nominal value of the current

[1]) The sign is positive when the current flows towards the circuit

INPUT DATA

Input Signal Requirements [2])

Voltage: Under all circumstances normally encountered when the unit is used in conjunction with other circuit blocks: V_{Wn} = 0.4 to 1 V more negative than V_Q dependent on the input current I_{Wn}.

Current: To be supplied to terminal W_n having the most negative voltage level. $-I_{Wn}$ = approx. I_Q + max. 0.07 mA at $-V_Q$ = 1 V

OUTPUT DATA

Output Signal Characteristics [2])

Voltage: See INPUT DATA

Load current I_Q = approx. $-I_{Wn}$ -max. 0.07 mA [1]) at $-V_Q$ = 1 V

Output Impedance

When V_Q is negative-going, the output impedance approximates the output impedance of the driving circuit. When V_Q is positive-going, the output impedance is max. 130 kΩ.

LIMITING VALUES

Current through conducting diode: I_{Wc} = max. 10 mA

Voltage between terminals P and W = max. 30 V

[1]) The sign is positive when the current flows towards the circuit

[2]) These data apply to the most adverse working conditions for a combination of units, namely to a supply voltage V_P = +6.6 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

DUAL PULSE LOGIC

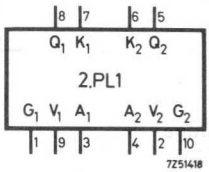
Colour: orange

The unit 2.PL1 contains two identical germanium diode pulse gates which are controlled by a d.c. voltage level.

The circuits are normally used in conjunction with flip-flop circuits. With the dual pulse logic a second pair of a.c. inputs are formed for a flip-flop FF1, or in combination with flip-flops FF2 a bi-directional shift register can be made. In these applications the twin pulse logic output terminals are to be connected directly to the flip-flop d.c. input terminals.

In each circuit a silicon diode is incorporated for reset purposes of the connected flip-flop.

Pulse repetition frequency range:	0–100 kHz
Ambient temperature range:	−20 to +60 °C
Weight:	approx. 20 g

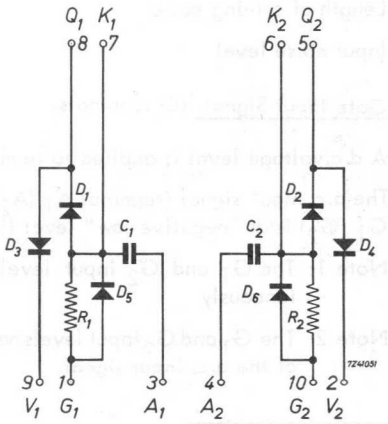


Drawing symbol

CIRCUIT DATA

Terminal

1 = G_1 = gate input 1
2 = V_2 = reset input 2
3 = A_1 = a.c. input 1
4 = A_2 = a.c. input 2
5 = Q_2 = output 2
6 = K_2 = normally not used
7 = K_1 = normally not used
8 = Q_1 = output 1
9 = V_1 = reset input 1
10 = G_2 = gate input 2



Power Supply

The unit is not connected to any supply voltage

INPUT DATA

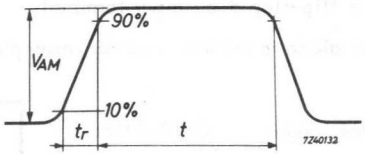
These data are dependent on the driven circuit, the values given apply to use of the dual pulse logic in conjunction with flip-flop circuits FF1 or FF2.

Input Signal Requirements [1])

AC Input Signal (A terminals)

A positive-going voltage step is applied to terminal A_1 or A_2 or to both terminals interconnected.

This voltage step passes the pulse gate if it has been opened by a proper d.c. gate input signal on terminal G_1 (G_2)



Voltage	V_{AM}	= min.	$-0.66\ V_N$
		= max.	- V_N
Rise time	t_r	= max.	0.4 µs
Length of driving pulse	t	= min.	0.5 µs
Input noise level		= max.	1 V peak to peak

Gate Input Signal (G terminals)

A d.c. voltage level is applied to terminal G_1 (G_2)

The a.c. input signal (terminal A_1 (A_2)) passes if the corresponding gate input G_1 (G_2) is at "negative low" level (i.e. gate open).

Note 1: The G_1 and G_2 input levels should not be "negative low" simultaneously

Note 2: The G_1 and G_2 input levels have to be present 8 µs before the arrival of the a.c. input signal

[1]) These data apply to the most adverse working condition for a combination of units, namely to supply voltages V_N = -5.4V and V_P = +6.6 V. Unless differently specified, all the voltage and current figures represent absolute maximum values.

Gate Open (input level "negative low")

Voltage $-V_G$ = max. 0.2V

= min. 0V

Gate Closed (input level "negative high")

Voltage $-V_G$ = min. V_{AM} (V_{AM} = amplitude of a.c. input signal)

= max. $-V_N$

Reset Input Signal (V terminals)

A negative reset signal can be applied to terminal V_1 or V_2

Current $-I_V$ = min. 0.5mA [1]) ($-V_V$ = max. 1V)

limiting value = max. 10mA [1])

OUTPUT DATA

When used in conjunction with flip-flop circuits FF1 or FF2, the output terminals (Q_1 and Q_2) are directly connected to the flip-flop d.c. input terminals (W_1 and W_2)

Input Impedance

Equivalent to a capacitance of approx. 500pF. (A_1, A_2 terminal or both terminals interconnected).

[1]) The sign is positive when the current flows towards the circuit

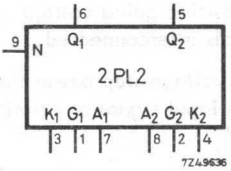
DUAL PULSE LOGIC

Colour: orange

The unit 2.PL2 contains two identical pulse gates which are controlled by a d.c. voltage level.

The circuits are normally used in conjunction with flip-flop circuits. With the dual pulse logic a second pair of a.c. inputs are formed for a flip-flop FF3, or in combination with flip-flops FF4 a bi-directional shift register can be made. In these applications the 2.PL2 output terminals are to be connected directly to the flip-flop d.c. input terminals.

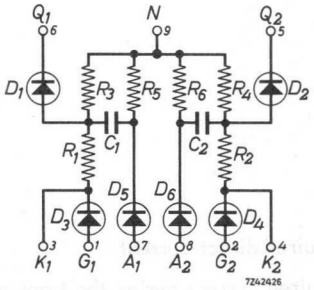
Frequency range	:	see INPUT DATA
Ambient temperature range	:	-20 to +60 °C
Weight	:	approx. 20 g



Drawing symbol

CIRCUIT DATA

Terminal 1 = G_1 = gate input 1
2 = G_2 = gate input 2
3 = K_1 = terminal for external gate input
4 = K_2 = terminal for external gate input
5 = Q_2 = output 2
6 = Q_1 = output 1
7 = A_1 = trigger input 1
8 = A_2 = trigger input 2
9 = N = supply -6 V
10 = not connected



Power Supply

Terminal 9 : V_N = -6 V ± 5 %, $-I_N$ = 0-2.5 mA Nominal value of the current

Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely V_N=-5.7 V and V_P=6.3 V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

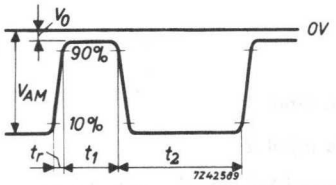
These data are dependent on the driven circuit, the values given apply to use of the dual pulse logic in conjunction with flip-flops FF3 or FF4.

Input Signal Requirements

Trigger Input Signal (A terminals)

A positive going voltage step is applied to terminal A_1 or A_2 or to both terminals interconnected.

This voltage step passes the pulse gate if it has been opened by an appropriate gate input signal on terminal G_1(G_2).



		A_1 or A_2	A_1 and A_2 interconnected
Voltage	V_{AM} = min.	-0.7 V_N	
	= max.	- V_N	
	$-V_o$ = min.	0 V	
	= max.	0.2 V	
Required direct current	I_{AD} = min.	0.88 mA	min. 1.75 mA
Required current during the transient averaged over: 0.4 µs	I_{AT} = min.	5 mA	min. 6 mA
0.7 µs	= min.	4 mA	min. 4.5 mA

Rise time	t_r = max.	0.7	µs
Pulse duration	t_1 = min.	3	µs
	t_2 = min.	11	µs
Input noise level	V_n = max.	1	V peak to peak

Gate Input Signal (G terminals)

A d.c. voltage level is applied to terminal G_1 (G_2).

The trigger input signal (terminal A_1(A_2) passes if the corresponding gate is opened by an appropriate gate input signal.

To terminal K_1(K_2) external diodes can be connected (in the same sense as diode D_3(D_4)), to provide the corresponding pulse gate with extra condition inputs.

		gate open		gate closed	
Voltage	$-V_G$ = min.	0	V	min.	V_{AM}
	= max.	0.2	V	max. -	V_N
Required gate current caused by negative transient of V_{AM}	I_{GT} = min.	1.75	mA	min. 1.2	mA

		to open gate		to close gate	
Required average current during the positive transient of V_G	I_{GT} = min.	1.6	mA		
Gate setting time					
when the gate input level changes at random	t_{GS} = min.	17.	µs	min. 25	µs
when the gate input level changes within 2 µs after the positive going edge of the trigger signal	t_{GS} = min.	11	µs	min. 11	µs

Note: The latter applies to a shift register configuration so that the max. shift frequency is approximately 70 kHz

During triggering the G levels should not be at zero voltage level simultaneously.

The gate setting time is the required waiting time between the last G level change and the positive going edge of the trigger pulse.

OUTPUT DATA

When used in conjunction with flip-flops FF3 and FF4, the output terminals (Q_1 and Q_2) are directly connected to the flip-flop d.c. input terminals (W_1 and W_2).

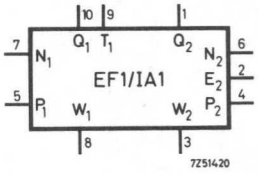
EMITTER FOLLOWER/INVERTER AMPLIFIER

Colour: yellow

The unit EF1/IA1 contains a transistor emitter-follower circuit and a transistor inverter circuit. The transistors are medium-speed switching types.

The two circuits, i.e. the standard circuits EF1 and IA1, can be used either independently or in combination.

Pulse repetition frequency range:	0–100 kHz
Ambient temperature range:	−20 to +60 °C
Weight:	approx. 20 g

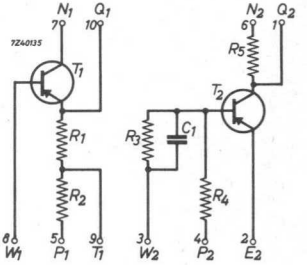


Drawing symbol

CIRCUIT DATA

Terminal

1 = Q_2 = output 2
2 = E_2 = common supply 0V
3 = W_2 = input 2
4 = P_2 = supply +6V
5 = P_1 = supply +6V
6 = N_2 = supply −6V
7 = N_1 = supply −6V
8 = W_1 = input 1
9 = T_1 = tapped output 1
10 = Q_1 = output 1



EF1 terminals with index 1
IA1 terminals with index 2

Power Supply

Terminal 2:	V_{E2}	= 0V common	
4:	V_{P2}	= +6V ± 10%, I_{P2} = 0.16mA [1]	Nominal value of the current
5:	V_{P1}	= +6V ± 10%, I_{P1} = 3.3–6.6mA [1]	
6:	V_{N2}	= −6V ± 10%, $-I_{N2}$ = 0–6mA [1]	
7:	V_{N1}	= −6V ± 10%, $-I_{N1}$ = 3.3–25mA [1]	

For input and output data see 2.IA1 and 2.EF1 specifications.

[1]) The sign is positive when the current flows towards the circuit

DUAL EMITTER FOLLOWER

Colour: yellow

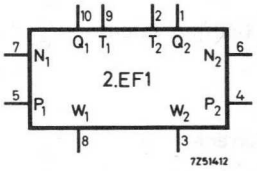
The unit 2.EF1 contains two identical transistor emitter-follower circuits that constitute a non-inverting buffer-amplifier function with a low output impedance. The transistors are medium-speed switching types.

The unit is equipped with a tap on the output resistor for cases in which a level shift towards the positive supply line is required.

Pulse repetition frequency range: 0-100 kHz

Ambient temperature range: -20 to +60 °C

Weight: approx. 20 g



Drawing symbol

CIRCUIT DATA

Terminal

1 = Q_2 = output 2

2 = T_2 = tap output 2

3 = W_2 = input 2

4 = P_2 = supply +6 V (2)

5 = P_1 = supply +6 V (1)

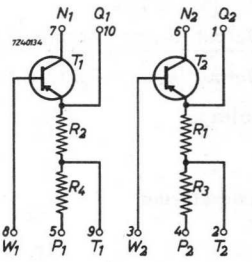
6 = N_2 = supply -6 V (2)

7 = N_1 = supply -6 V (1)

8 = W_1 = input 1

9 = T_1 = tap output 1

10 = Q_1 = output 1



Power Supply

Terminal 4:	V_{P2}	= +6 V ± 10%, I_{P2} = 3.3-6.6 mA [1]	Nominal value of the current
5:	V_{P1}	= +6 V ± 10%, I_{P1} = 3.3-6.6 mA [1]	
6:	V_{N2}	= -6 V ± 10%, $-I_{N2}$ = 3.3-25 mA [1]	
7:	V_{N1}	= -6 V ± 10%, $-I_{N1}$ = 3.3-25 mA [1]	

[1]) The sign is positive when the current flows towards the circuit

INPUT DATA

Input Signal Requirements [2])

A d.c. voltage level is applied to terminal W_1 (W_2)

Input level "negative low"

Voltage V_W = max. 0.3V more negative than V_Q

limiting value = max. 10V

Current $-I_W$ = min. 0.12mA [1]) (unit unloaded)

I_W = max. 0.12mA [1]) ($-I_Q$ at max. value)

Input level "negative high"

Voltage V_W = max. 0.3V more negative than V_Q

limiting value $-V_W$ = max. $-V_N$

= min. $-0.7V_N$

Current $-I_W = \text{min.} \frac{I_Q + 6}{34}$ mA [1])

$-I_W = \text{min.} \frac{I_T + 5.1}{34}$ mA [1])

Input Impedance

Equivalent to a capacitance of approx. 20 pF

OUTPUT DATA

Output Signal Characteristics [2])

Output level "negative low"

Voltage V_Q = max. 0.3V more positive than V_W

V_T = min. 0.2V

Load current $-I_Q$ = max. 2.2mA [1])

$-I_T$ = max. 1.8mA [1]) at V_T = 0.2V

Output level "negative high"

Voltage V_Q = max. 0.3V more positive than V_W

[1]) The sign is positive when the current flows towards the circuit

[2]) These data are derived from the most adverse working condition for a combination of units, namely to supply voltages V_N = -5.4V and V_P = +6.6V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

Load current I_Q and I_T

V_W	$I_{Q\,max}$	$I_{T\,max}$ at $V_T = -0.5\,V$	$I_{T\,max}$ at $V_T = -1\,V$
$0.7\,V_N$	2 mA	4.5 mA	3 mA
$0.8\,V_N$	4 mA	6 mA	4.5 mA
$0.9\,V_N$	11 mA	7.5 mA	6 mA
$0.95\,V_N$	17 mA	9 mA	7.5 mA

Output Impedance

Equivalent to a resistance of approx.

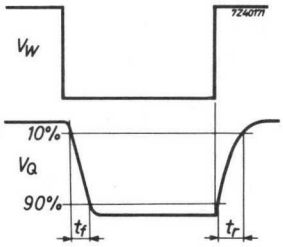
$R_i = 2000\,\Omega$ for a non-conducting transistor

$R_i = 0.03\,Z_o$ for a conducting transistor

(Z_o being the output impedance of the unit driving the W terminal)

Switching and Delay Times (for orientation only)

A square wave input signal (W terminal) is assumed with an amplitude of min. $-0.7\,V_N$.



Unit Unloaded

Fall time t_f = max. 0.1 µs

Rise time t_r = max. 0.1 µs

DUAL INVERTER AMPLIFIER

Colour: yellow

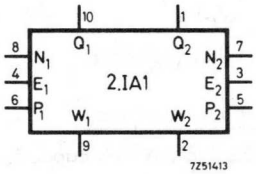
The unit 2.IA1 contains two identical transistor inverter circuits. The transistors are medium-speed switching types.

The circuits constitute an inverting (NOT) function when driven by a signal on the W terminal.

Pulse repetition frequency range: 0-100 kHz

Ambient temperature range: -20 to + 60 °C

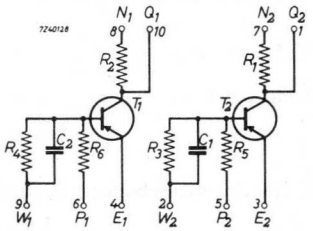
Weight: approx. 20 g



Drawing symbol

CIRCUIT DATA

Terminal
1 = Q_2 = output 2
2 = W_2 = input 2
3 = E_2 = common supply 0V (2)
4 = E_1 = common supply 0V (1)
5 = P_2 = supply +6V (2)
6 = P_1 = supply +6V (1)
7 = N_2 = supply -6V (2)
8 = N_1 = supply -6V (1)
9 = W_1 = input 1
10 = Q_1 = output 1



Power Supply

Terminal 3:	V_{E2}	= 0V common	
4:	V_{E1}	= 0V common	
5:	V_{P2}	= +6V ± 10%, I_{P2} = 0.16mA [1])	Nominal value of the current
6:	V_{P1}	= +6V ± 10%, I_{P1} = 0.16mA [1])	
7:	V_{N2}	= -6V ± 10%, $-I_{N2}$ = 0-6mA [1])	
8:	V_{N1}	= -6V ± 10%, $-I_{N1}$ = 0-6mA [1])	

[1]) The sign is positive when the current flows towards the circuit

INPUT DATA

Input Signal Requirements [2])

Transistor conducting (output level "negative low")

Voltage	$-V_W$ = min.	$-0.7V_N$
limiting value	= max.	$-V_N$
Current	$-I_W$ = min.	0.6mA [1])

Transistor non-conducting (output level "negative high")

Voltage	$-V_W$ = max.	0.3V
limiting value	V_W = max.	10V

Input Impedance

Equivalent to a capacitance of approx. 400 pF.

OUTPUT DATA

Output Signal Characteristics [2])

Transistor conducting (output level "negative low")

Voltage	$-V_Q$ = max.	0.2V	
Load current	$-I_Q$ = max.	4.3mA [1])	terminal N_1 (N_2) connected to V_N
	= max.	10mA [1])	terminal N_1 (N_2) floating

Transistor non-conducting (output level "negative high")

Voltage	$-V_Q$ = min.	$-0.7V_N$	
	I_Q = max.	1.5mA [1])	terminal N_1 (N_2) connected to V_N
	=	0mA [1])	terminal N_1 (N_2) floating

---

[1]) The sign is positive when the current flows towards the circuit

[2]) These data apply to the most adverse working conditions for a combination of units, namely to supply voltages V_N = -5.4V and V_P = +6.6V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

Output Impedance

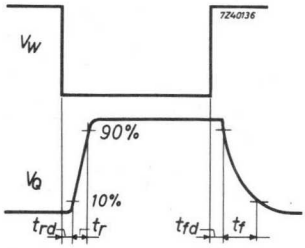
Equivalent to a resistance of approx.

R_i = 50 Ω for positive-going output voltage

R_i = 1000 Ω for negative-going output voltage

Switching and Delay Times (for orientation only)

A square wave input signal is assumed with an amplitude of min. $-0.7V_N$.



Unit Unloaded

Rise delay	t_{rd}	= max. 0.1 µs
Rise time	t_r	= max. 0.3 µs
Fall delay	t_{fd}	= max. 0.6 µs
Fall time	t_f	= max. 0.2 µs

DUAL EMITTER FOLLOWER

Colour: yellow

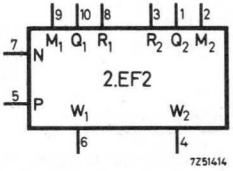
The unit 2.EF2 contains two identical EF2 transistor emitter follower circuits that constitute a buffer amplifier function. The unit has especially been designed to amplify the weak output signals originating from a diode gate circuit.

The unit drives a grounded emitter transistor directly at the base. By connecting the built-in anti-bottoming diode (D_1 or D_2) via the M terminal to the collector of the driven grounded emitter stage, hole-storage effects in this stage are avoided. In this way short transients are maintained.

The output signal is normally taken from the Q terminal. When a flip-flop is to be set or reset by an EF2, normally the R output is used, the memory property of the flip-flop then being maintained.

The transistors used are medium-speed switching types.

Pulse repetition frequency range:	0-100 kHz
Ambient temperature range:	-20 to +60 °C
Weight:	approx. 20 g

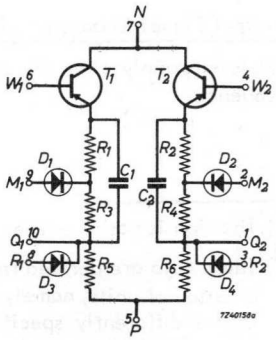


Drawing symbol

CIRCUIT DATA

Terminal

1 = Q_2 = output 2
2 = M_2 = clamp diode 2
3 = R_2 = diode output 2
4 = W_2 = input 2
5 = P = supply +6 V
6 = W_1 = input 1
7 = N = supply -6 V
8 = R_1 = diode output 1
9 = M_1 = clamp diode 1
10 = Q_1 = output 1



Power Supply

Terminal 5: V_P = +6 V ± 10%, I_P = 3.5-4 mA [1]) Nominal value
7: V_N = -6 V ± 10%, $-I_N$ = 4-12 mA [1]) of the current

INPUT DATA

Input Signal Requirements [2]

Input level "negative low"

Current $-I_W$ = max. 0.07 mA [1]) (unit unloaded)
I_W = max. 0.12 mA [1]) ($-I_Q$ at maximum value)

Input level "negative high"

Current $-I_W$ = min. 0.3 mA [1])

The unit can be driven from an N1 gate [3]) or from an N1-P1 gate [3]) sequence.

Limiting Values

Voltage $-V_W$ = max. $-V_N$
V_W = max. 10 V

Input Impedance

Equivalent to a capacitance of approx. 50 pF

OUTPUT DATA

Output Signal Characteristics [2]

These data apply to the EF2 driven from an N1 gate [3]) or from an N1-P1 gate [3]) sequence.

---

[1]) The sign is positive when the current flows towards the circuit

[2]) These data are derived from the most adverse working condition for a combination of units, namely to supply voltages V_N = -5.4 V and V_P = +6.6 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

[3]) The standard N1 gate is incorporated in the gate units 2.3N1 and 2.2N1, the standard P1 gate is incorporated in the units 2.3P1 and 2.2P1.

EF2 driven from N1 gate [3])

Gate input level "negative low"

Load current $-I_Q$ = max. 0.07 mA [1]) at V_Q = 0.2 V

Gate input level "negative high"

Load current I_Q = max. 2.9 mA [1]) at $-V_Q$ = 0.5 V
I_R = max. 1.9 mA [1]) at $-V_R$ = 0.5 V

EF2 driven from N1-P1 gate [3]) sequence

Gate input level "negative low"

Load current $-I_Q$ = max. 0.12 mA [1]) at V_Q = 0.2 V

Gate input level "negative high"

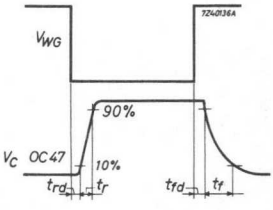
Load current I_Q = max. 0.95 mA [1]) at $-V_Q$ = 0.4 V
I_R = max. 0.5 mA [1]) at $-V_R$ = 0.35 V

Switching and Delay Times (for orientation only)

These data apply to the EF2 driven from an N1-P1 gate [3]) sequence, the EF2 is driving a grounded emitter OC 47 stage from its Q output terminal, the data are given for two values of the OC 47 collector current.

A square wave input signal with an amplitude of min. $-0.7V_N$ is applied to the gate input terminal.

Collector current OC 47		= 6 mA	= 20 mA
Rise delay	t_{rd}	= max. 0.3 µs	max. 0.6 µs
Rise time	t_r	= max. 0.3 µs	max. 1.5 µs
Fall delay	t_{fd}	= max. 2 µs	max. 3.5 µs
Fall time	t_f	= max. 0.5 µs	max. 1.2 µs



[1]) See note 1 on previous page

[2]) See note 2 on previous page

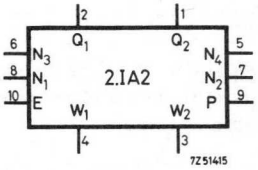
[3]) See note 3 on previous page

DUAL INVERTER AMPLIFIER

Colour: yellow

The unit 2.IA2 contains two identical inverter amplifier circuits, that constitute an inverting function with an appreciable power amplification between input and output. The unit has especially been designed to amplify the weak output signals originating from a diode gate circuit, whilst it can also be used as a driver for power stages. The transistors used, are medium-speed switching types.

Pulse repetition frequency range:	0–100 kHz
Ambient temperature range:	−20 to +60 °C
Weight:	approx. 20 g

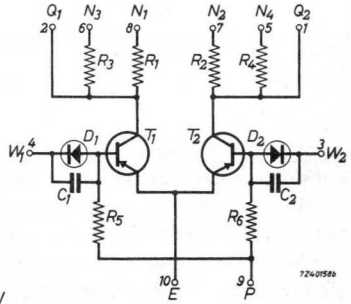


Drawing symbol

CIRCUIT DATA

Terminal

1 = Q_2 = output 2
2 = Q_1 = output 1
3 = W_2 = input 2
4 = W_1 = input 1
5 = N_4 = supply −6 V (2) [1])
6 = N_3 = supply −6 V (1) [1])
7 = N_2 = supply −6 V (2) [1])
8 = N_1 = supply −6 V (1) [1])
9 = P = supply +6 V
10 = E = common supply 0 V



[1]) Use dependent on application

Power Supply

Terminal 5:	V_{N4}	$= -6\,V \pm 10\%$, $-I_{N4} = 0\text{-}4\,mA$ [1]	Nominal value of the current
6:	V_{N3}	$= -6\,V \pm 10\%$, $-I_{N3} = 0\text{-}4\,mA$ [1]	
7:	V_{N2}	$= -6\,V \pm 10\%$, $-I_{N2} = 0\text{-}2\,mA$ [1]	
8:	V_{N1}	$= -6\,V \pm 10\%$, $-I_{N1} = 0\text{-}2\,mA$ [1]	
9:	V_P	$= +6\,V \pm 10\%$, $I_P = 0.2\,mA$ [1]	
10:	V_E	$= 0\,V$ common	

INPUT DATA

Input Signal Requirements [2]

Application 1 (use as gate amplifier): IA2 driven by a standard negative (N1) gate [3], or standard negative (N1) gate followed by a standard positive (P1) gate [3] circuit.

In the latter case the P supply terminal of the P1 gate is left floating.

Transistor conducting (output level "negative low")

Current $-I_W = \text{min. } 0.3\,mA$ [2] $(-V_W = \text{min. } 1V)$

Transistor non-conducting (output level "negative high")

Voltage $-V_W = \text{max. } 0.2\,V$

Application 2 (use as power amplifier): IA2 driven by a grounded emitter stage with a collector resistance of 1 kΩ connected to the -6 V supply terminal. This driving stage can be a standard IA1 circuit (incorporated in the units EF1/IA1 and 2.IA1) or another IA2 circuit with both corresponding −6 V supply terminals connected to the negative supply line. In both cases the collector (Q terminal) of the driving stage is connected directly to the W terminal of the IA2.

---

[1] The sign is positive when the current flows towards the circuit.

[2] These data apply to the most adverse working conditions for a combination of units, namely to supply voltages $V_N = -5.4\,V$ and $V_P = +6.6\,V$. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

[3] The standard N1 gate is incorporated in the gate units 2.3N1 and 2.2N1, the standard P1 gate is incorporated in the units 2.3P1 and 2.2P1.

Transistor conducting (output level "negative low")

Current $-I_W$ = min. 3.7mA [1]) ($-V_W$ = max. 1.3V)

Transistor non-conducting (output level "negative high")

Voltage $-V_W$ = max. 0.2V

Limiting Values

Voltage V_W = max. 10V

Current $-I_W$ = max. 10mA [1])

OUTPUT DATA

Output Signal Characteristics [2])

Application 1 (see above)

Transistor conducting (output level "negative low")

Voltage $-V_Q$ = max. 0.2V

Load current $-I_Q$ = max. 5.5mA [1]) [3])
= max. 3.6mA [1]) [4])
= max. 0.07mA [1]) [5])

Transistor non-conducting (output level "negative high")

Voltage $-V_Q$ = min. $-0.7V_N$

Load current I_Q = max. 0mA [1]) [3])
= max. 0.5mA [1]) [4])
= max. 1.5mA [1]) [5])

[1]) See note [1]) on previous page

[2]) See note [2]) on previous page

[3]) With all N terminals floating

[4]) With terminals N1 or N2 connected to the -6V supply

[5]) With terminals N1 and N3 or N2 and N4 connected to the -6V supply

Application 2 (see above)

Transistor conducting (output level "negative low")

Voltage	$-V_Q$ = max. 0.2 V	= max. 0.25 V	= max. 0.3 V
Load current	$-I_Q$ = max. 31 mA [1,3]	= max. 41 mA [1,3]	= max. 70 mA [1,3]
	= max. 25 mA [1,5]	= max. 35 mA [1,5]	= max. 64 mA [1,5]

Transistor non-conducting (output level "negative high")

Voltage	$-V_Q$ = min. $-0.7V_N$	
Load current	I_Q = 0 mA [1,3]	
	= max. 1.5 mA [1,5]	

Output Impedance

Equivalent to a resistance of approx.

R_i = 50 Ω for positive-going output voltage

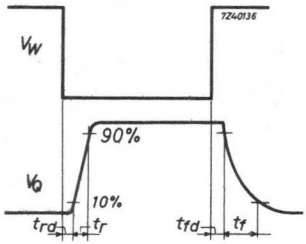
R_i = 1000 Ω for negative-going output voltage [5]

Switching and Delay Times (for orientation only)

A square wave signal with an amplitude of min. $-0.7V_N$ is fed via a standard negative (N1) gate [2] followed by a standard positive (P1) gate [2], to the W1 (W2) input terminal of the IA2.

Unit Unloaded

Rise delay	t_{rd}	= max. 0.5 µs
Rise time	t_r	= max. 2.2 µs
Fall delay	t_{fd}	= max. 1.2 µs
Fall time	t_f	= max. 2.5 µs



[2]) See note 3 on page A104

[1],[3],[5]) See corresponding notes on previous page

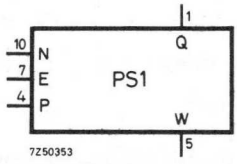
PULSE SHAPER

Colour: green

The unit PS1 contains a transistor squaring-amplifier followed by an inverter circuit. The transistors are medium-speed switching types.

A d.c. input signal of a magnitude exceeding the input tripping level of the unit, is re-shaped and inverted into the standard d.c. level at the output. The output voltage transients are very short and can be used for driving other circuit blocks, multivibrator circuits included.

Pulse repetition frequency range:	0-100 kHz
Ambient temperature range:	-20 to +60 °C
Weight:	approx. 20 g

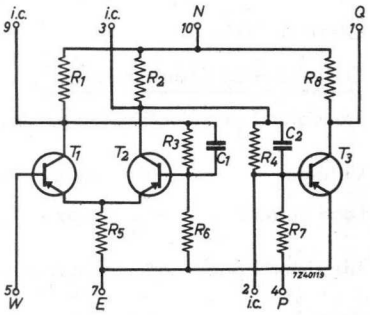


Drawing symbol

CIRCUIT DATA

Terminal

1 = Q = output
2 = internally connected
3 = internally connected
4 = P = supply +6V
5 = W = input
6 = internally not connected
7 = E = common supply 0V
8 = internally not connected
9 = internally connected
10 = N = supply -6V



Power Supply

Terminal 4:	V_P	= +6V ± 10%, I_P = 0.48 mA [1]	Nominal value of the current
7:	V_E	= 0V common	
10:	V_N	= -6V ± 10%, $-I_N$ = 3.3-6.2 mA [1]	

[1]) The sign is positive when the current flows towards the circuit.

INPUT DATA

Input Signal Requirements [2])

A d.c. voltage level is applied to terminal W.

Transistor T_3 conducting (output level "negative low")

Voltage	$-V_W$ = min.	$-0.4V_N$
Current	$-I_W$ = min.	0.1 mA [1])
limiting value	= max.	10 mA [1])

Transistor T_3 non-conducting (output level "negative high")

Voltage	$-V_W$ = max.	1 V
limiting value	V_W = max.	10 V
Current	I_W = min.	0.07 mA [1])

Hysteresis (difference between on and off tripping level)

Voltage	ΔV_W = min.	0.2 V

Input Impedance

Equivalent to a capacitance of approx. 330 pF

OUTPUT DATA

Output Signal Characteristics [2])

Transistor T_3 conducting (output level "negative low")

Voltage	$-V_Q$ = max.	0.2 V
Load current	$-I_Q$ = max.	1.2 mA [1])

Transistor T_3 non-conducting (output level "negative high")

Voltage	$-V_Q$ = min.	$-0.7V_N$
Load current	I_Q = max.	0.6 mA [1])

[1]) The sign is positive when the current flows towards the circuit.

[2]) These data apply to the most adverse working conditions for a combination of units, namely to supply voltages V_N = -5.4 V and V_P = +6.6 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

Output Impedance

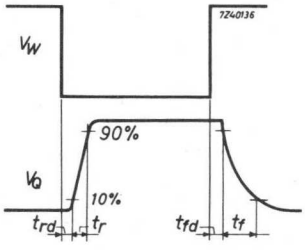
Equivalent to a resistance of approx.

R_i = 100 Ω for positive-going output voltage

R_i = 2200 Ω for negative-going output voltage

Switching and Delay Times (for orientation only)

A square wave input signal is assumed with an amplitude of min. -0.7 V_N.



Unit Unloaded

Rise delay	t_{rd}	= max. 0.1 µs
Rise time	t_r	= max. 0.2 µs
Fall delay	t_{fd}	= a function of driving current
Fall time	t_f	= max. 0.2 µs

PULSE SHAPER

Colour : green

This unit contains a Schmitt trigger followed by an inverter amplifier. An input signal of a magnitude exceeding the thresholds (tripping levels) of the unit, is re-shaped and inverted into the standard d.c. level at the output. The output voltage transients are short and suitable for driving other circuit blocks at their trigger inputs (A).

The terminals A, W, X_1 and X_2 are provided in order to be able to use the PS 2 for the following purposes:

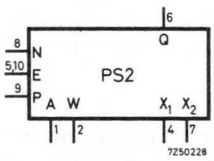
- as a pulse shaper, driven by an external source
- as a relaxation oscillator
- as a crystal controlled oscillator
- as a pulse shaper, driven by circuit blocks of the 100 kHz or 1-Series.

In the last application the number of inputs can be increased by connecting diodes type AAY 21/OA 85/OA 95 to the externally interconnected terminals A and W. The maximum number of diodes is 10.

Pulse repetition frequency range : 0 to 100 kHz

Ambient temperature range : −20 to +60 °C

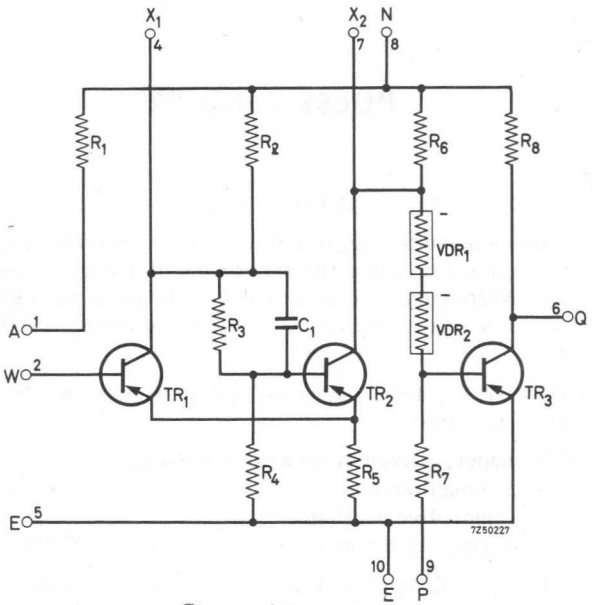
Weight : approx. 20 g



drawing symbol

CIRCUIT DATA

Terminal 1 = A = to be interconnected with terminal 2 for internal driving purposes
2 = W = input
3 = not connected
4 = X_1 = internally connected
5 = E = common supply 0 V (interconnected with terminal 10)
6 = Q = output
7 = X_2 = internally connected
8 = N = supply −6 V
9 = P = supply +6 V
10 = E = common supply 0 V



Circuit diagram

Power supply

Terminal 8 = V_N = −6 V ±5 %, $-I_N$ = 3.2 - 7.5 mA } nominal value
9 = V_P = +6 V ±5 %, I_P = 0.19 mA } of the current
10 = V_E = 0 V common

Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely V_N = −5.7 V and V_P = +6.3 V.
- The temperatures −20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Unit driven by a non-standard circuit (external souree)

Internal resistance (R_i) of the driving circuit

R_i = max. 12 kΩ (T_{amb} = min. 0 °C)
R_i = max. 8 kΩ (T_{amb} = min. −20 °C)

Input voltage to be applied to terminal W:

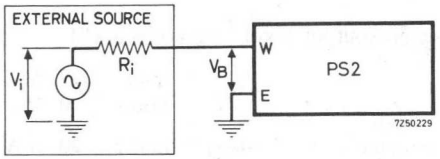
ON threshold (transistor TR_3 conducting)

	operating	limiting value
Voltage	$-V_W$ = min. −0.4 V_N	= −7.5 V
Current	$-I_W$ = max. 0.1 mA	= 15 mA

OFF threshold (transistor TR_3 non-conducting)

	operating	limiting value
Voltage	$-V_W$ = max. −0.17 V_N	= −10 V
Current	I_W = max. 0.05 mA (at $-V_W$ = 0.2 V)	
	= max. 0.1 mA (at V_W = 10 V)	

Hysteresis (difference between ON and OFF tripping levels)

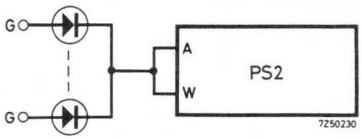


The hysteresis is affected by the internal resistance (R_i) of the driving circuit (external source). The relation is given by the following formula:

T_{amb} = min. 0 °C	T_{amb} = min. −20 °C
ΔV_i = min. (0.07 V_N − 0.033 R_i)	ΔV_i = min. 0.07 V_N − 0.05 R_i)
$\Delta V_B = \frac{\Delta V_i}{1 + 0.057\ R_i}$	$\Delta V_B = \frac{\Delta V_i}{1 + 0.071\ R_i}$

(R_i in kΩ and V in volt)

Unit driven by circuit blocks of the 1-Series



For this operation terminal A has to be connected to terminal W and the input voltage V_G has to be applied via a diode, type AAY 21/OA 85/OA 95. The maximum number of parallel diodes is 10.

Transistor TR_3 conducting (output level "negative low")

Voltage	$-V_G$	= max.	$-V_N$
		= min.	$-0.7\ V_N$

Transistor TR_3 non-conducting (output level "negative high")

Voltage	$-V_G$	= min.	0 V
		= max.	0.2 V
Required direct current	I_{GD}	= max.	0.7 mA
Required transient current			
averaged over 0.4 μs	I_{GT}	= max.	1.1 mA
averaged over 0.7 μs		= max.	0.75 mA

OUTPUT DATA

Transistor TR_3 conducting (output level "negative low")

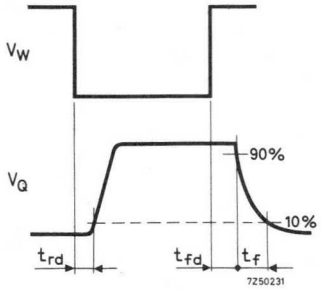
Voltage	$-V_Q$	= max.	0.2 V
		= min.	0 V
Available direct current	$-I_{QD}$	= max.	20 mA
Available transient current			
averaged over 0.4 μs	$-I_{QT}$	= max.	8 mA
averaged over 0.7 μs		= max.	13.7 mA

Transistor TR_3 non-conducting (output level "negative high")

Voltage	V_Q	= max. V_N
Current	I_{QD}	= max. 0.65 mA (at $V_Q = 0.7\ V_N$)

Switching and delay times (when unit is used in combination with 1-Series circuit blocks)

A square wave input signal is assumed with an amplitude of min. $-0.7\ V_N$



Unit fully loaded

Rise delay	t_{rd} = max. 0.7 μs
Fall delay	t_{fd} = max. 1.2 μs
Fall time	t_f = max. 0.7 μs

Note

- If for a particular application a capacitor is required between terminal W (2) and earth, use should be made of terminal 5 in order to avoid noise on the common earth point which could disturb the proper operation of the unit.

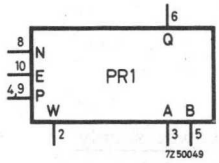
POSITIVE RESET UNIT

Colour: blue

This unit is intended for resetting purposes of flip-flops FF 1, FF 2, FF 3 and FF 4. When a "negative low" level is applied to the input terminal (W), the unit produces a positive reset signal at its output terminal (Q). The time, that the reset level will be present, is determined by the driving circuit.
In general a reset time of maximum 2 μs per flip-flop is required when a chain of flip-flops is to be reset.
Up to 15 flip-flops can be reset without external interconnections. By interconnecting the terminals A and P the maximum number of flip-flops that can be reset is 30; by interconnecting the terminals B and P maximum 40 flip-flops can be reset simultaneously.

To reset a flip-flop the output terminal (Q) of the PR1 has to be connected to an input terminal (W) of a flip-flop via a diode OA 85 or OA 95 (anode to Q).

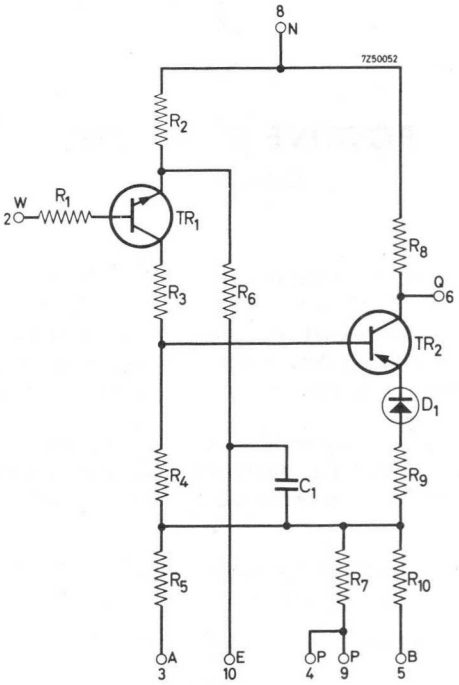
Ambient-temperature range	−20 to +60 °C
Weight	approx. 20 g



Drawing symbol

CIRCUIT DATA

Terminal
1 = not connected
2 = W = input
3 = A = to be interconnected with terminal 4 for resetting maximum 30 flip-flops
4 = P = supply + 6 V (internally connected to terminal 9)
5 = B = to be interconnected with terminal 4 for resetting maximum 40 flip-flops
6 = Q = output
7 = not connected
8 = N = supply −6 V
9 = P = supply +6 V
10 = E = common supply 0 V



Circuit diagram

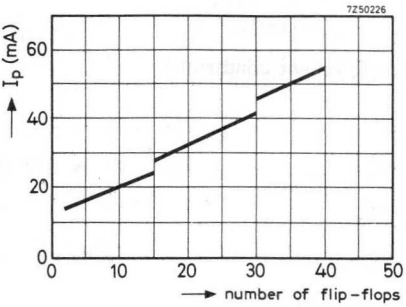
Power supply

Voltages

Terminal 8 : V_N = −6 V ± 5%
9 : V_P = +6 V ± 5%
10 : V_E = 0 V common

Currents (at nominal voltage)

	I_N	I_P
W-input at "1" level	−3.5 mA	1.1 mA
W-input at "0" level	−7.5 mA	see diagram on next page.



Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N = -5.7$ V and $V_P = +6.3$ V.
- The temperatures −20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input signal (W-terminal)

A "negative low" level applied to the input terminal (W) produces a positive reset signal at the output terminal (Q).

Transistor TR2 conducting (reset condition)

Voltage	$-V_W$	= min. 0	V
		= max. 0.2	V
limiting value	V_W	= max. 6.5	V
Required direct current	I_{WD}	= min. 0.1	mA
Required transient current averaged over 0.7 μs	I_{WT}	= min. 0.08	mA

Transistor TR2 non-conducting

Voltage	$-V_W$	= min. 0.7	V_N
		= max.	V_N

OUTPUT DATA

Transistor TR_2 conducting (reset condition)

Voltage	V_Q	= min. 1.0 V
Available direct current	I_{QD}	= min. 15 mA
A and P interconnected		= min. 30 mA
B and P interconnected		= min. 40 mA

Transistor TR_2 non-conducting

Voltage	$-V_Q$	= min. 0.5 V = max. V_N

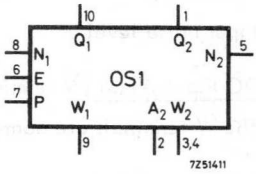
ONE-SHOT MULTIVIBRATOR

Colour: green

The unit OS1 contains a transistor monostable multivibrator circuit. The transistors are medium-speed switching types.

When a positive-going voltage step is applied to terminal A_2 the circuit generates a pulse on the Q-terminals. The length of the output pulse is determined by the value of the external capacitance C between the terminals 4 and 10.

Pulse repetition frequency range:	0-100 kHz
Ambient temperature range:	-20 to +60 °C
Weight:	approx. 20 g

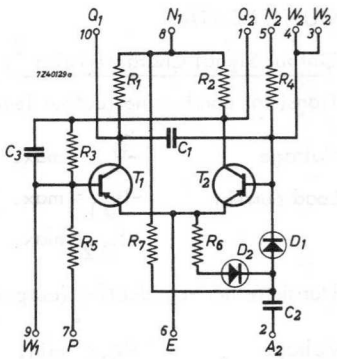


Drawing symbol

CIRCUIT DATA

Terminal

1 = Q_2 = output 2
2 = A_2 = a.c. input 2
3 = W_2 } = d.c. input 2
4 = W_2 }
5 = N_2 = supply -6V
6 = E = common supply 0
7 = P = supply +6V
8 = N_1 = supply -6V
9 = W_1 = d.c. input 1
10 = Q_1 = output 1



Power Supply

Terminal 6:	V_E	= 0V
7:	V_P	= +6V ± 10%, I_P = 0.15 mA [1]) Nominal value
8:	V_N	= -6V ± 10%, $-I_N$ = 6-7 mA [1]) of the current

[1]) The sign is positive when the current flows towards the circuit.

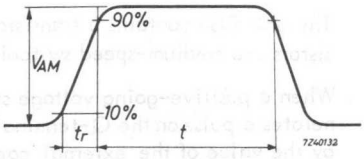
INPUT DATA

Input Signal Requirements [2]

AC Input signal (A_2 terminal)

A positive-going voltage step is applied to terminal A_2. This voltage step drives the transistor T_2 into the non-conducting state.

Voltage	V_{AM}	= min.	$-0.66V_N$
		= max.	V_N
Rise time	t_r	= max.	0.4 µs
Length of driving pulse	t	= min.	0.5 µs
Input noise level		= max.	1 V peak to peak



DC Input signal (W terminals)

The W terminals are normally not used.

Input Impedance

Equivalent to a capacitance of approx. 500 pF (A_2 terminal)

OUTPUT DATA

Output Signal Characteristics [2]

Transistor conducting (output level "negative low")

Voltage	$-V_Q$	= max.	0.2V
Load current	$-I_{Q1}$	= max.	2.2mA [1]
	$-I_{Q2}$	= max.	0.5mA [1]

Transistor non-conducting (output level "negative "high")

Voltage	$-V_Q$	= min.	$-0.7V_N$
Load current	I_{Q1}	= max.	1.5mA [1]
	I_{Q2}	= max.	0.7mA [1]

[1]) The sign is positive when the current flows towards the circuit

[2]) These data apply to the most adverse working conditions for a combination of units, namely to supply voltages $V_N = -5.4V$ and $V_P = +6.6V$. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

Load currents of equal sign, up to the values given as maxima, can be drawn from the two output terminals simultaneously. In the case of simultaneous load currents of opposite sign, the maximum load currents given are not guaranteed.

Maximum Capacitive Load (2000 pF)

When the maximum capacitive and resistive loads are applied in parallel, the given maximum pulse repetition frequency is not guaranteed.

Output Impedance

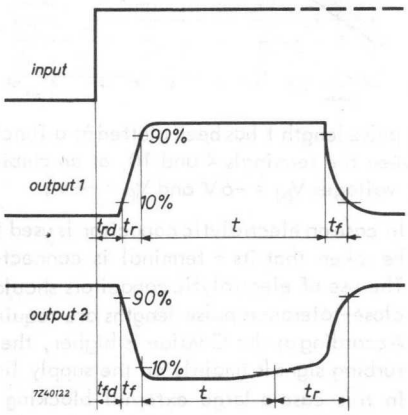
Equivalent to a resistance of approx.

R_i = 50 Ω for positive-going output voltage

R_i = 1000 Ω for negative-going output voltage

Switching and Delay Times (for orientation only)

A square wave input signal (A_2 terminal) is assumed with an amplitude of min. $-0.7V_N$.



Unit Unloaded

Output 1 (Q_1 terminal)

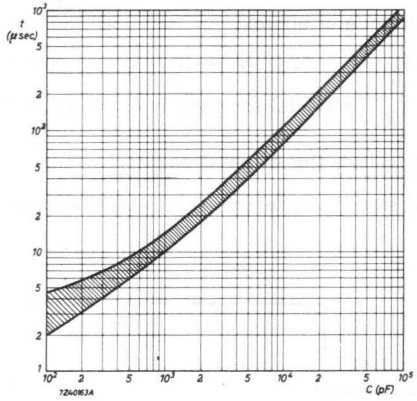
Rise delay	t_{rd}	= max. 0.8 μs
Rise time	t_r	= max. 0.3 μs
Fall time	t_f	= dependent on the external capacitance between the terminals 4 and 10

Output 2 (Q_2 terminal)

Fall delay	t_{fd}	= max. 0.2 µs	
Fall time	t_f	= max. 1.8 µs	
Rise time	t_r	= max. 1 µs	(without external capacitance)

Length of the output pulse

When the unit is unloaded, and without external capacitance t = 1.5–4.0 µs



In this diagram, the pulse length t has been plotted as a function of the external capacitance C between the terminals 4 and 10, at an ambient temperature of 25 °C and at supply voltages V_N = -6 V and V_p = +6 V.

Note 1 In case an electrolytic capacitor is used for C, care should be taken that its + terminal is connected to terminal 4. The use of electrolytic capacitors should be avoided when close-tolerance pulse lengths are required.
According as the C value is higher, the sensitivity to disturbing signals (mainly on the supply line -6 V) increases. In this case a large external blocking capacitor may be required between the -6 V supply and 0 V common, to be mounted close to the unit.

Note 2 The length of the output pulse is affected by capacitively loading the Q_2 terminal. In general, it will be within 0 to 25 % of the values given above.

Stability of Pulse Length

An increase in supply voltage V_N of 5 % reduces the pulse length by less than 1 %. Any variation of the supply voltage V_p has practically no influence. An increase in ambient temperature of 1 °C reduces the pulse length by less than 0.5 %.

ONE-SHOT MULTIVIBRATOR

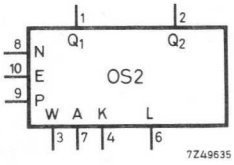
Colour : green

The unit OS2 contains a monostable multivibrator circuit equipped with medium-speed switching type transistors.

When a positive-going voltage step is applied to terminal A, the circuit generates a pulse at the Q-terminals.
The duration of the output pulse is determined by the value of:

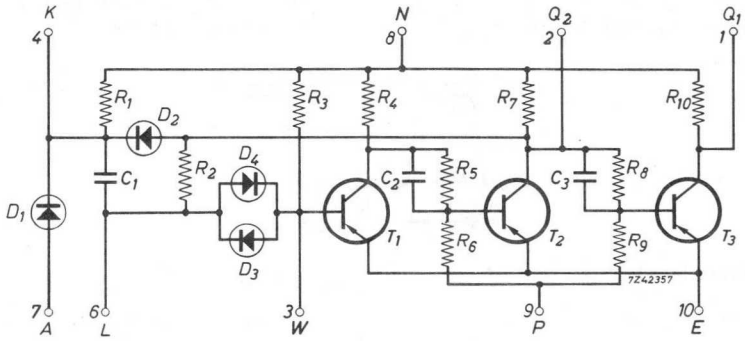
(a) the external capacitance parallel to C_1 between the terminals K and L (for pulses longer than the intrinsic value);
(b) the external resistance between the terminals Q_1 and W (for pulses shorter than the intrinsic value).

Frequency range	0 - 100 kHz
Permissible ambient temperature	-20 to +60 °C
Weight	approx. 20 g



Drawing symbol

CIRCUIT DATA



Terminals

1 = Q_1	= output 1	6 = L	= for external capacitor
2 = Q_2	= output 2	7 = A	= trigger input
3 = W	= d.c. input	8 = N	= supply (-6 V)
4 = K	= for external capacitor	9 = P	= supply (+6 V)
5 = not connected		10 = E	= common of supply (0 V)

Power supply

8 : V_N = -6 V ± 5 %, $-I_N$ = 8.8 mA

9 : V_P = +6 V ± 5 %, I_P = 0.4 mA

nominal value

10 : V_E = 0 V common

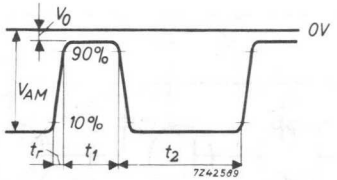
Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely V_N = -5.7 V and V_P = 6.3 V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT REQUIREMENTS

Trigger input signal (A terminal)

A positive-going voltage pulse is applied to terminal A. The leading edge of this voltage pulse drives by means of the transistor T_1 the transistor T_2 into the conducting, and the transistor T_3 into the non-conducting state.



Voltage levels

V_{AM} = min. -0.7 V_N

= max. $-V_N$

$-V_o$ = min. 0 V

= max. 0.2 V

Required current during the transient				
averaged over: 0.4 µs	I_{AT}	= min.	2.4	mA
0.7 µs	I_{AT}	= min.	1.4	mA
Required direct current 1)	I_{AD}	= min.	1.3	mA
Rise time				
without external capacitor	t_r	= max.	0.4	µs
with a capacitor of min. 200 pF between terminals K and L	t_r	= max.	0.7	µs
Duration of driving pulse	t_1	= min.	1	µs
Recovery time	t_2	= min.	6	µs 2)
when the duration of the output pulse (t_o) exceeds 7.5 µs	t_2	= min.	0.8	t_o 2)
Input noise level	V_n	= max.	1	V peak to peak

OUTPUT DATA

Voltages and currents

Transistor conducting		Output Q_1	Output Q_2
Voltage	$-V_Q$	= max. 0.2 V	max. 0.2 V
Available direct current	$-I_{QD}$	= max. 18 mA	max. 6 mA
Available current during the transient			
averaged over: 0.4 µs	$-I_{QT}$	= max. 19 mA	max. 15 mA
0.7 µs		= max. 25 mA	max. 21 mA

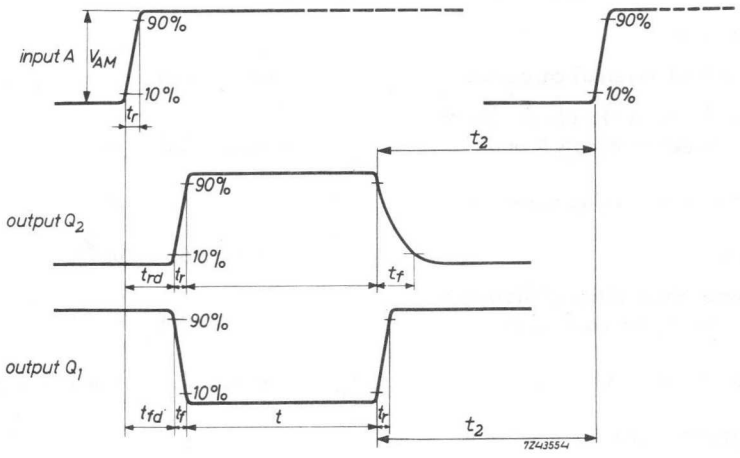
Transistor non-conducting		Output Q_1	Output Q_2
Voltage	$-V_Q$	= min. $-0.7\ V_N$	min. $-0.7\ V_N$
Available direct current	I_{QD}	= max. 0.7 mA	max. 0.25 mA

1) This is the current flowing to the input of the OS2 during the input pulse after decay of the output pulse, if the duration of the input pulse is longer.

2) The recovery time t_2 is starting at the trailing edge ot V_A when $t_1 > t_o$ and at the trailing edge of V_{Q2} when $t_o > t_1$

Switching and delay times

These data refer to an input signal as specified under "Input Data".



Unit unloaded		Output Q_1	Output Q_2
Rise delay	t_{rd} =	-	t_{rA} + max. 0.4 µs
Rise time	t_r =	max. 0.2 µs	max. 0.2 µs
Fall delay	t_{fd} =	t_{rA} + max. 0.5 µs	-
Fall time	t_f =	max. 0.4 µs	max. 3 µs

Duration of the output pulse

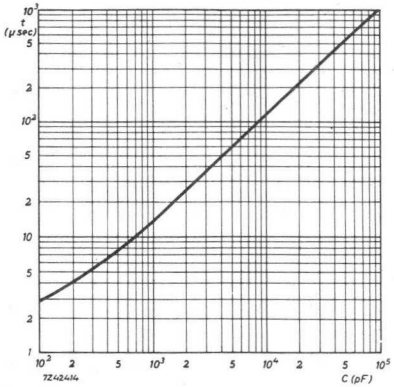
Unit unloaded

Intrinsic value	t_o = max. 4 µs
With resistor of 12 kΩ [1] between terminals Q_1 and W	t_o = max. 2 µs

With a capacitor between terminals K and L, at an ambient temperature of 25 °C and supply voltages V_N = -6 V and V_P = +6 V, see figure given below.

For larger capacitances log t is proportionate to log C.

[1]) minimum permissible value



Stability of pulse duration

A variation of the supply voltage V_N of 5 % varies the pulse duration by less than 1 % in the same direction.

The influence of a variation of the supply voltage Vp of 5 % is negligible.

An increase in ambient temperature by 1 °C gives a reduction of the pulse duration of less than 0.5 % and vice versa.

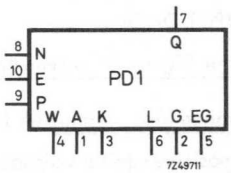
Note. In case an electrolytic capacitor is used for C_{ext} care should be taken that its + terminal is connected to terminal 6.

PULSE DRIVER

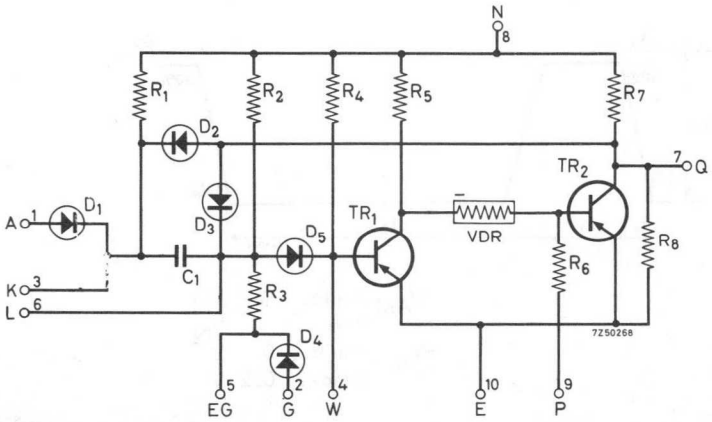
Colour: green

The unit PD1 contains a monostable multivibrator with a built-in trigger gate. It is mainly intended as a clock source, delivering trigger pulses for a great number of flip-flops FF1, FF2, FF3, and FF4 or as a counter driver.
The trigger gate can be controlled by a d.c. voltage level applied to terminal G.
The number of condition inputs can be extended with the aid of external diodes OA85/OA95 at the extension input E.G.
When a positive-going voltage step is applied to terminal A, the unit generates a pulse at the output (Q)-terminal, provided the gate is open.
The duration of the output pulse can be increased by means of an external capacitor between the terminals K and L (for pulses longer than the intrinsic value, e.g. necessary when driving a FF4 or 2PL2).
For mounting in the chassis 4322 026 38240 a printed-wiring board PDA 1, catalogue number 4322 026 34710, is available. On this standard printed-wiring board up to four PD 1's can be mounted (see section "ACCESSORIES FOR CIRCUIT BLOCKS 100 kHz SERIES").

Frequency range	: see INPUT DATA
Permissible ambient temperature	: -20 to +60 °C
Weight	: approx. 20 g



Drawing symbol



CIRCUIT DATA

Terminal
1 = A = trigger input
2 = G = gate input
3 = K = for external capacitor
4 = W = d.c. input
5 = EG = extension gate input
6 = L = for external capacitor
7 = Q = output
8 = N = supply -6 V
9 = P = supply +6 V
10 = E = common supply 0 V

Power supply

Terminal 8: V_N = -6 V ± 5 %, $-I_N$ = 26 mA (T_1 conducting)
= 51 mA (T_2 conducting)
9: V_P = +6 V ± 5 %, I_P = 0.4 mA
10: V_E = 0 V common

Notes

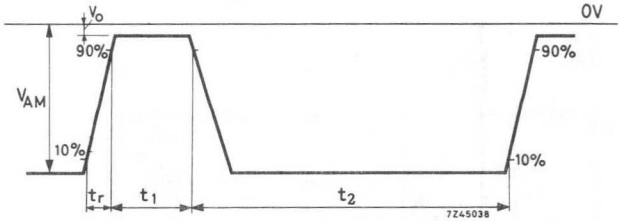
- The data given apply to the most adverse supply voltages for a combination of units, namely V_N = -5.7 V and V_P = 6.3 V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input Signal Requirements

Trigger Input Signal (A terminal)

A positive-going voltage step is applied to input terminal A. This voltage step generates a pulse at the output Q if the gate has been opened by an appropriate gate input signal on terminal G.



Voltage

V_{AM} = min. -0.7 V_N
= max. - V_N
$-V_o$ = min. 0 V
= max. 0.2 V

Required direct current	I_{AD} = min. 1.7 mA
Required average current during the transient	I_{AT} = min. 1.5 mA (practically independent of rise time)
Rise time	t_r = max. 0.7 µs
Pulse duration	t_1 = min. 1 µs
Recovery time	t_2 = min. 6 µs (without external capacitor)
	t_2 = min. 11 µs (with C_{EXT} = 1000 pF between terminals K and L)
Note	Type of diodes and maximum number to be connected in parallel at terminal K: 6 x OA85/OA95.

Input Impedance:

Equivalent to a capacitance of 500 pF.

Gate Input Signals (G-terminals)

A d.c. voltage level is applied to terminal G. A **"negative low" voltage opens** the gate.

		Gate open	Gate closed
Voltage	$-V_G$	= min. 0 V	min. - 0.7 V_N
		max. 0.2 V	max. - V_N
Required gate current caused by negative transient of V_A	I_{GD}	= min. 1.75 mA	min. 0.5 mA
Required average current during the positive transient of V_G	I_{GT}	= min. 1.2 mA	

Gate Setting Times:

When the gate changes at random:		to open gate	to close gate
Without external capacitor	t_{gs}	= min. 8.5 µs	min. 25 µs
With an external capacitor of 1000 pF between K and L		= min. 24 µs	75 µs

When the gate level changes within 1 µs after the positive going edge of the trigger signal:		to open gate	to close gate
Without external capacitor	t_{gs}	= min. 6 µs	0
With external capacitor of 1000 pF between K and L		= min. 11 µs	0

Notes

- The gate setting time is the time the gate (G)-signal shall be present in advance to open the gate for the trigger (A) -signal.
- The absolute maximum value of the external capacitor is 1000 pF.
- Type of diodes and maximum number to be connected in parallel at terminal EG: 6 x OA85/OA95.

W-terminal (base connection transistor T1):

Transistor T_1 non-conducting:

Voltage limiting value

V_W = min. 0.2 V
V_W = max. 2.5 V

These voltages may be applied for max. 5 µs and a max.freq. of 100 kHz

Transistor T_1 conducting:

Current (limiting value)

$-I_W$ = max. 2 mA
(at $-V_W$ = max. 0.5 V)

Up to max.6 output-Q terminals of pulse logic units 2.PL2 may be connected to the W-input terminal of the PD 1 each via a resistor of 560 Ω ± 5%.

OUTPUT DATA

Voltages and Currents

Transistor conducting:

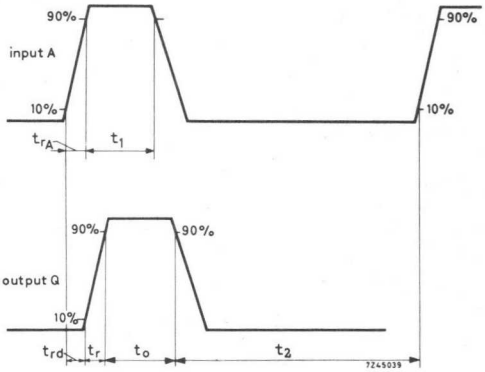
Voltage	$-V_Q$	= max. 0.2 V
Available direct current	$-I_{QD}$	= max. 65 mA
Available current during the transient: averaged over 0.7 µs	$-I_{QT}$	= max. 90 mA

Transistor non-conducting:

Voltage	$-V_Q$	= min. - 0.7 V_N
		= max. - 0.84 V_N

Switching and Delay Times:

These data are for orientation only and refer to an input signal as specified under INPUT DATA.



$t_{rd} = t_{rA} + 0.2$ µs
(fully loaded)

Unit max. loaded with:	$t_r + t_o$:	ext. capacitor between terminals K and L:
20 x FF1 or FF2	max. 1.5 µs	none
5 x FF3	min. 1.2 µs	none
20 x FF3	max. 2 µs	none
20 x FF4 (at 70 kHz)	max. 4 µs	C_{ext} = 1000 pF ± 5% (absolute max. value of C_{ext}).

The recovery time t_2 is starting at the trailing edge of V_A when $t_1 > t_o$ and at the trailing edge of V_Q when $t_o > t_1$ (t_1 = duration of input pulse V_A).

The typical output pulse duration of an unloaded pulse driver PD 1, triggered via a PL 2 unit (at 70 kHz): $t_r + t_o = 3.2$ µs.

POWER AMPLIFIER

The PA1 consists of an n-p-n/p-n-p transistor amplifier circuit, designed to be used as a power amplifier in the range of circuit blocks. The amplifier is non-inverting, and can be driven directly by the circuit blocks FF1,FF2,FF3, FF4, GI1, IA1, IA2 and OS2

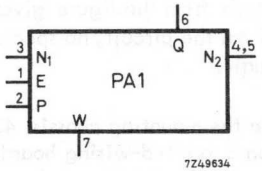
The output loadability is 600 mA at 60 V (abs. max. values). The built-in diode across the output terminals protects the output transistor against voltage transients which occur when the unit is driving an inductive load.

The circuit is mounted on an epoxy-paper printed-wiring board, the output transistor is provided with an aluminium heat sink.

Frequency range : 0-100 Hz

Ambient temperature range: -20 to +60 °C

Weight : approx. 60 g



CIRCUIT DATA

Terminal: 1 = E = common supply 0 V

2 = P = supply +6 V

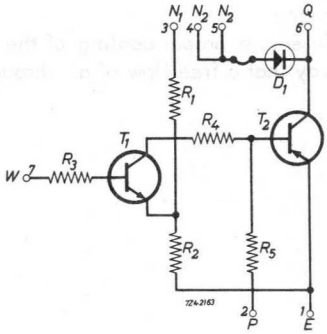
3 = N1 = supply -6 V

4 = N2) = supply abs. max. 60 V

5 = N2)

6 = Q = output

7 = W = input



Power Supply

Terminal: 1: V_E = 0 V common

2: V_P = 6 V ± 10 %, I_P = max. 20 mA 1) 2)

3: V_{N1} = -6 V ± 10 %, $-I_{N1}$ = max. 70 mA (T_2 non-conducting)
= max. 110 mA (T_2 conducting)

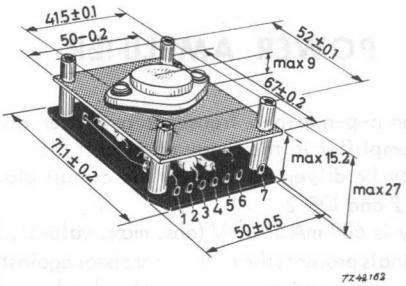
4) 5) $-V_{N2}$ = max. 60 V, $-I_{N2}$ = max. 600 mA 1) 2)

---

1) The sign is positive when the current flows towards the unit.

2) When $-V_{N2}$ is applied to the unit, care must be taken that Vp is present as well, otherwise transistor T2 may be damaged.

MECHANICAL CONSTRUCTION



The dimensions (approx. 71 mm x 50 mm x 27 mm) and terminal location can be seen from the figure given above. Since the aluminium heat sink is insulated from the circuit, no special measures need be taken as regards mounting of the unit.

In the mounting chassis 4322 026 38240 the PA 1 is to be mounted directly on a printed-wiring board. On such a standard printed-wiring board PAA 1 up to four PA 1's can be mounted, the next position in the chassis being left empty.
To ensure proper cooling of the unit, the PA 1 has to be mounted in such a way that a free flow of air through it is guaranteed.

INPUT DATA

Input Signal Requirements 2)

A d.c. voltage level is applied to terminal W.

Output-transistor conducting

Voltage	$-V_w$	=	max. 0.2 V min. 0 V
Current	I_w	=	min. 2.5 mA 1)

Output-transistor non-conducting

Voltage	$-V_w$	=	min. 4.25 V
Limiting value		=	max. 13.2 V
Current	$-I_w$	=	min. 0.1 mA 1)

OUTPUT DATA

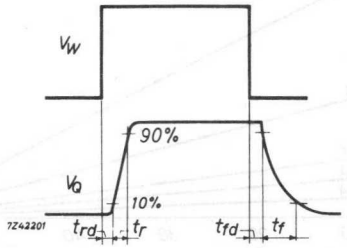
Output Signal Characteristics 2)

Output transistor conducting

Voltage	$-V_Q$	=	max. 0.75 V
Load current	$-I_Q$	=	max. 600 mA 1)

Output transistor non-conducting

Voltage	$-V_Q$	=	max. 60 V (dependent on the value of V_{N2} which is abs. max. 60 V.)
Leakage current	$-I_Q$	=	max. 14.5 mA 1)



1) The sign is positive when the current flows towards the unit.

2) These data apply to the most adverse working conditions for a combination of units, namely to supply voltages $V_N = -5.4$ V and $V_p = +6.6$ V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

Switching and Delay Times (for orientation only)

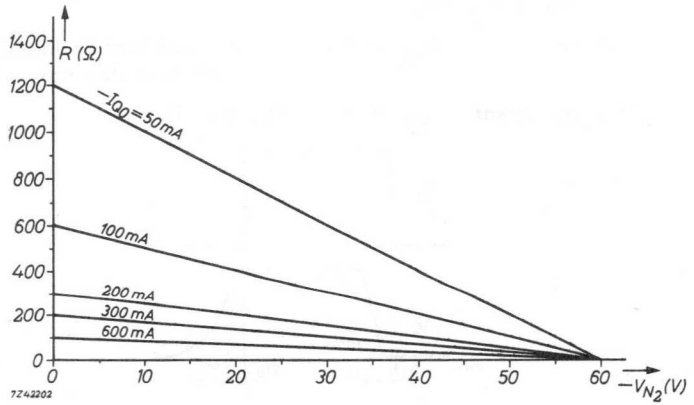
A square wave input signal is applied with an amplitude of 4.25 V, a rise time of max. 2.2 µs and a fall time of max. 2.5 µs

Unit loaded with a resistor of 100 Ω

Rise delay	t_{rd}	= max.	15 µs
Rise time	t_r	= max.	120 µs
fall delay	t_{fd}	= max.	70 µs
fall time	t_f	= max.	60 µs

Unit loaded with an inductive load

The unit is provided with a built-in diode to protect the output transistor against voltage transients which occur when an inductive load is switched. This protection is realised at the expense of a very long fall delay time of the current in this load. At supply voltages below 60 V, however, a wire jumper in series with this diode can be interchanged with a resistor to decrease this delay time.
The maximum permissible value of this resistor is given in the figure below, with the current flowing through the load at the moment of switching-off as parameter.



DECADE COUNTER

The unit DC1 consists of four flip-flops type FF1 mounted on a printed wiring board, the flip-flops are connected as a counter.

The counter is provided with pulse feed-back to achieve that six of the sixteen possible positions are skipped. The flip-flops can be reset by means of a common positive signal.

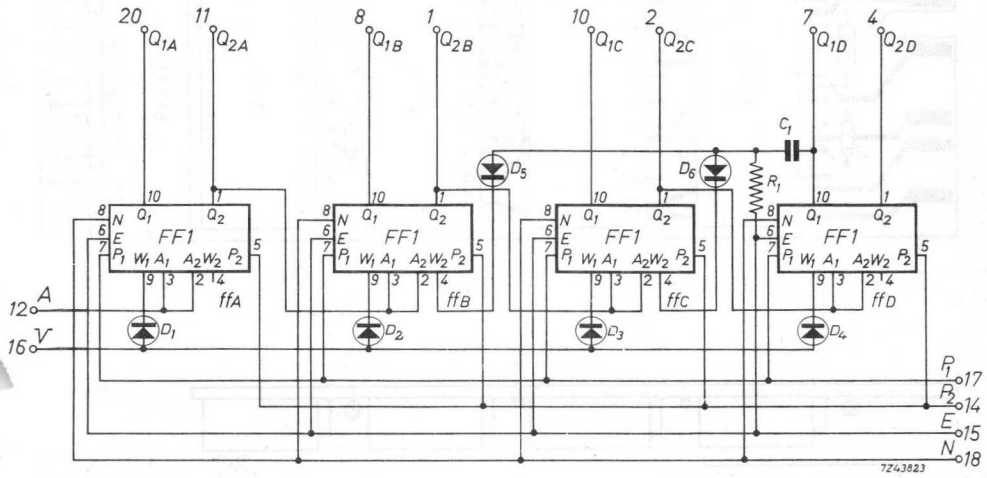
The reset diodes D_1, D_2, D_3, D_4 and the feed-back network D_5, D_6, R_1 and C_1 are mounted on the printed wiring board.

The printed wiring board 4322 026 33620 is provided with plated-through holes, double sided printed wiring and double sided gold-plated contacts.

The mating connector type 2422 020 51491 is normally not supplied with the counter.

Pulse repetition frequency range	: 0 - 100 kHz
Ambient temperature range	: -20 to + 60 °C
Weight	: approx. 100 g

CIRCUIT DATA



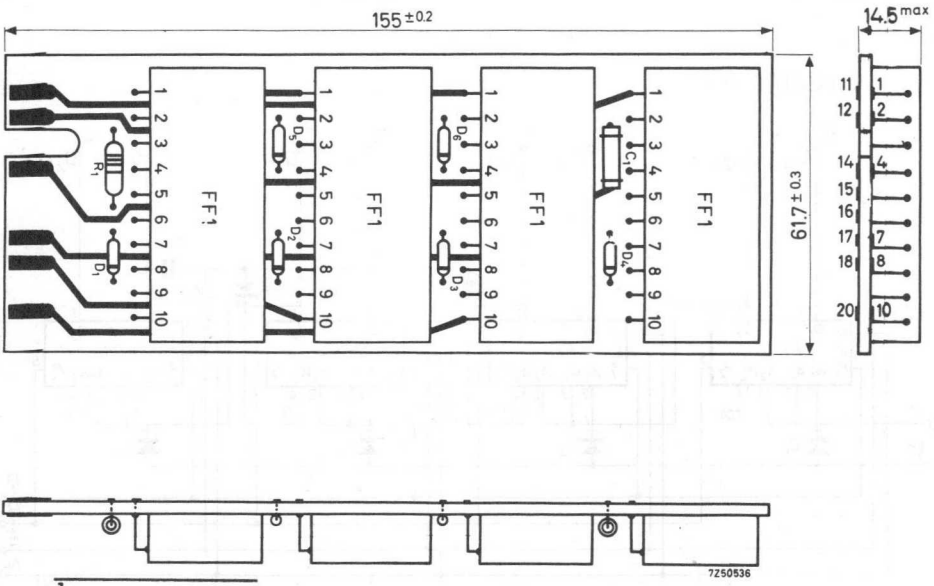
Terminal:

1 = Q_{2B} = output 2 flip-flop B	12 = A = a.c. input
2 = Q_{2C} = output 2 flip-flop C	14 = P_2 = supply +6V (2)
4 = Q_{2D} = output 2 flip-flop D	15 = E = common supply 0V
7 = Q_{1D} = output 1 flip-flop D	16 = V = reset input
8 = Q_{1B} = output 1 flip-flop B	17 = P_1 = supply +6V (1)
10 = Q_{1C} = output 1 flip-flop C	18 = N = supply -6V
11 = Q_{2A} = output 2 flip-flop A	20 = Q_{1A} = output 1 flip-flop A

Power Supply

Terminal 14:	$V_{P2} = +6V \pm 10\%$, $I_{P2} = 0.6mA$ [1]	Nominal value of the current
15:	V_E = 0V common	
17:	$V_{P1} = +6V \pm 10\%$, $I_{P1} = 0.6mA$ [1]	
18:	$V_N = -6V \pm 10\%$, $-I_N = 28mA$ [1]	

DIMENSIONS AND TERMINAL LOCATION



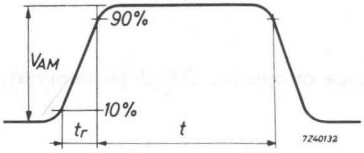
[1]) The sign is positive when the current flows towards the circuit

INPUT DATA

Input Signal Requirements [2])

AC Input Signal (A terminal)

A positive-going voltage step is applied to terminal A. This voltage step advances the counter one position.



Voltage	V_{AM}	= min.	$-0.66\ V_N$
		= max.	$-\ V_N$
Rise time	t_r	= max.	0.4 µs
Length of driving pulse	t	= min.	0.5 µs
Input noise level		= max.	1 V peak to peak

Reset Input Signal (V terminal)

For resetting the counter a positive d.c. voltage is applied to terminal V. This signal causes all Q_1 terminals to reach "negative high" and all Q_2 terminals to reach "negative low" level.

Input level during reset

Voltage	V_V	= min.	1 V
limiting value		= max.	10 V
Current	I_V	= min.	4 mA [1])
		(I_V = approx. 4.4 mA [1]) at V_V = 6 V)	

---

[1]) The sign is positive when the current flows towards the circuit

[2]) These data apply to the most adverse working condition for a combination of units, namely to supply voltages V_N = -5.4 V and V_P = +6.6 V. Unless differently specified, all the voltage and current figures represent absolute maximum values.

Input level during counting

During counting terminal V should be left floating or be returned to a voltage level:

Voltage $-V_V$ = min. 0.4 V

limiting value = max. 30 V

Input Impedance

Equivalent to a capacitance of approx. 500 pF (A terminal)

OUTPUT DATA

These data apply to each individual flip-flop stage.

Output Signal Characteristics [2])

Transistor conducting (output level "negative low")

Voltage $-V_Q$ = max. 0.2 V

Load current $-I_Q$ = max. 2.5 mA [1])

Transistor non-conducting (output level "negative high")

Voltage $-V_Q$ = min. $-0.7V_N$

Load current I_Q = max. 0.7 mA [1])

Load currents of equal sign, up to the values given as maxima, can be drawn from two corresponding output terminals simultaneously. In the case of simultaneous load currents of opposite sign, the maximum load currents given are not guaranteed.

Maximum Capacitive Load

1. If loaded during positive as well as negative-going pulses (e.g. FF1, FF2, OS1):

500 pF for terminals Q_{1D} and Q_{2D} together

1500 pF for terminals Q_{1A} and Q_{2A} together,

Q_{1B} and Q_{2B} together,

Q_{1C} and Q_{2C} together

[1]) See note 1 on previous page

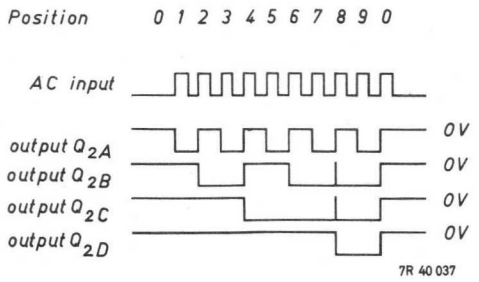
[2]) See note 2 on previous page

2. If loaded only during positive-going pulses (e.g. FF3, FF4, OS2):

500 pF for terminal Q_{1D}
1500 pF for each terminal Q_{2A}, Q_{2B}, Q_{2C}
2000 pF for each terminal Q_{1A}, Q_{1B}, Q_{1C}, Q_{2D}

When the maximum capacitive and resistive loads are applied in parallel, the given maximum pulse repetition frequency is not guaranteed.

Output levels during counting



The output levels at the Q_2 terminals can be taken from the above figure. Note that when a Q_2 output is at "negative low" level the corresponding Q_1 terminal is at "negative high" level and vice-versa.

DUAL DECADE COUNTER

The unit 2.DCA 2 contains two identical decade counter units, mounted on a printed wiring board. Each counter consists of four flip-flops FF3, connected to operate in the 1-2-4-8 code. To achieve this operation, it is provided with a gate-diode with the result that six of the sixteen possible positions are skipped. The flip-flops can be reset by means of a common positive signal.

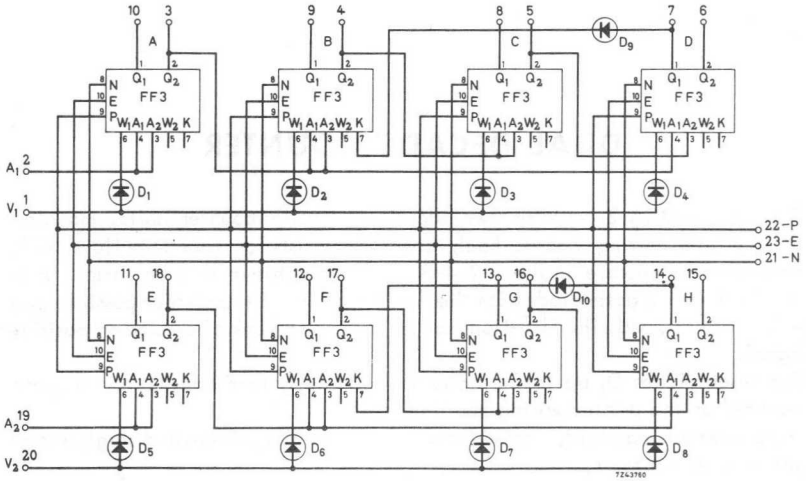
The reset diodes D_1 up to D_8 inclusive and the gate-diodes D_9 and D_{10} are mounted on the printed wiring board as well.

The printed wiring board is provided with plated-through holes and single-sided gold-plated contacts.

With the mating connector, 2422 020 52592, not supplied with the dual decade counter, the printed wiring board of standard dimensions (121.8mm x x 180.3mm x 1.6mm) can be used directly in the standard mounting chassis, catalog number 4322 026 38240.

The fixation of the circuit blocks FF3 to the p.w. board is secured by means of locking tags, catalog number 4322 026 33690.

Pulse repetition frequency range:	0 - 100 kHz
Ambient temperature range:	-20 to +60 °C
Weight:	approx. 210 g



Terminal

1 = V_1 = reset input counter 1
2 = A_1 = a.c. input counter 1
3 = Q_{2A} = output 2 flip-flop A
4 = Q_{2B} = output 2 flip-flop B
5 = Q_{2C} = output 2 flip-flop C
6 = Q_{2D} = output 2 flip-flop D
7 = Q_{1D} = output 1 flip-flop D
8 = Q_{1C} = output 1 flip-flop C
9 = Q_{1B} = output 1 flip-flop B
10 = Q_{1A} = output 1 flip-flop A
11 = Q_{1E} = output 1 flip-flop E
12 = Q_{1F} = output 1 flip-flop F
13 = Q_{1G} = output 1 flip-flop G
14 = Q_{1H} = output 1 flip-flop H
15 = Q_{2H} = output 2 flip-flop H
16 = Q_{2G} = output 2 flip-flop G
17 = Q_{2F} = output 2 flip-flop F
18 = Q_{2E} = output 2 flip-flop E
19 = A_2 = a.c. input counter 2
20 = V_2 = reset input counter 2
21 = N = common negative supply $-6V$
22 = P = common positive supply $+6V$
23 = E = common supply 0V

Power Supply

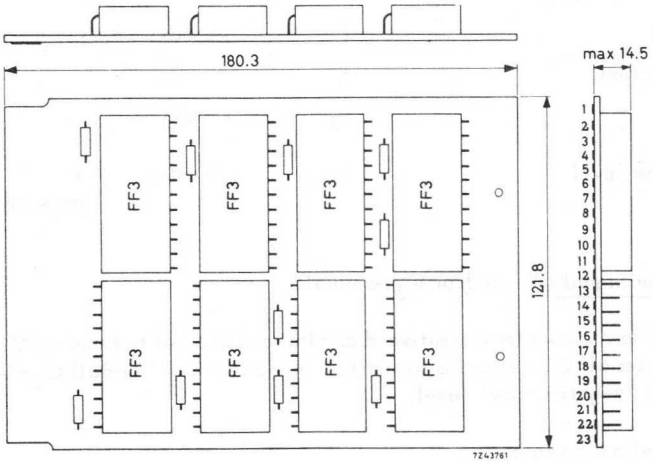
Terminal 21: $V_N = -6V \pm 5\%$, $-I_N = 70mA$
22: $V_P = +6V \pm 5\%$, $I_P = 4.8mA$
23: $V_E = 0V$

} Nominal value of the current

Notes:

- When a current is flowing towards the unit, the positive sign is used
- The data given apply to the most adverse supply voltages for a combination of units, namely
  $V_N = -5.7V$ and $V_P = +6.3V$
- The temperatures $-20\,^{\circ}C$ and $+60\,^{\circ}C$, and the tolerances on the supply voltages are absolute limiting values.

Dimensions and Terminal Location

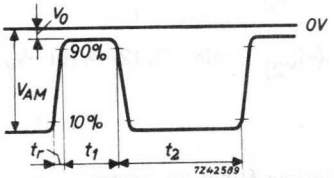


INPUT DATA

Input Signal Requirements

Trigger Input Signal (A_1 and/or A_2 terminals)

A positive-going voltage step is applied to terminal A. This voltage step advances the counter one position.



Voltage	V_{AM}	= min.	$-0.7V_N$
		= max.	$-V_N$
	$-V_0$	= min.	0V
		= max.	0.2V
Required direct current	$I_{A1D}(I_{A2D})$	= min.	1.75mA
Required current during the transient averaged over 0.4µs	I_{A1T} (I_{A2T})	= min.	6mA
0.7µs		= min.	4.5mA
Rise time	t_r	= max.	0.7µs
Pulse duration	t_1	= min.	1µs
	t_2	= min.	8µs
Input noise level	V_n	= max.	1V peak to peak

Reset Input Signal (V_1 and/or V_2 terminals)

For resetting the counter a positive d.c.voltage is applied to terminal V. This signal causes all Q_1-terminals to reach a "negative-high" and all Q_2-terminals to reach a "negative-low" level.

Input level during reset

Voltage	$V_{v1}(V_{v2})$	= min.	1V
		= max.	10V
Current	I_{v1} (I_{v2})	= min.	3.6 mA

During counting it is recommended that terminal V_1 and/or V_2 are connected to a voltage level.

Voltage	$-V_{v1}$ ($-V_{v2}$)	= min.	0.4V
		= max.	15V
Current	$-I_{v1}$ ($-I_{v2}$)	= min.	0.12mA (at $-V_{v1}$ ($-V_{v2}$) = 0.4V)

OUTPUT DATA

These data apply to the various flip-flop stages.

Output Signal Characteristics

Transistor non-conducting

Voltage: $-V_Q$ = min. $-0.7V_N$

Available direct current I_{QD} = max. 0.7 mA

Transistor conducting

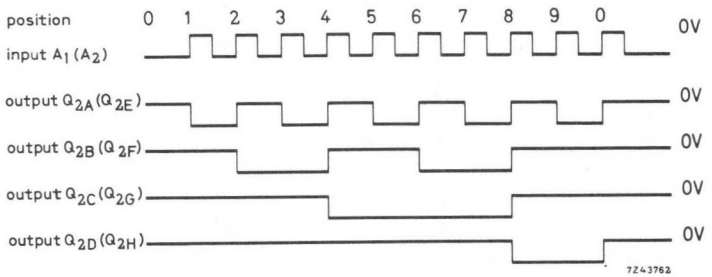
Voltage $-V_Q$ = max. 0.2 V
= min. 0 V

		output Q_1		output Q_2			
		Flip-Flop A-B-C E-F-G-	Flip-Flop D-H	Flip-Flop A-E	Flip-Flop B-F	Flip-Flop C-G	Flip-Flop D-H
max. available current during transient $-I_{QT}$	averaged over 0.4 µs	11 mA	11 mA	4 mA	5 mA	6 mA	11 mA
	averaged over 0.7 µs	14 mA	14 mA	9 mA	9.5 mA	10 mA	14 mA
maximum available direct current $-I_{QD}$		6 mA	5.1 mA	3.4 mA	4.25 mA	5.1 mA	6 mA

Maximum Speed:

For all loads within the limits mentioned above, also applied simultaneously, the maximum counting speed of 100 kHz is guaranteed.

Output levels during counting



The output levels at the Q_2-terminals are shown in the figure above.
Note that when a Q_2 output is at "negative-low" level the corresponding Q_1 output is at "negative-high" level and vice versa.
After 10 positive-going voltage steps at the input terminal A_1 (A_2), the output terminal Q_{2D} (Q_{2H}) delivers one positive-going voltage step, whilst the decade counter has resumed its initial position, namely all Q_2-terminals being at 0 V level.

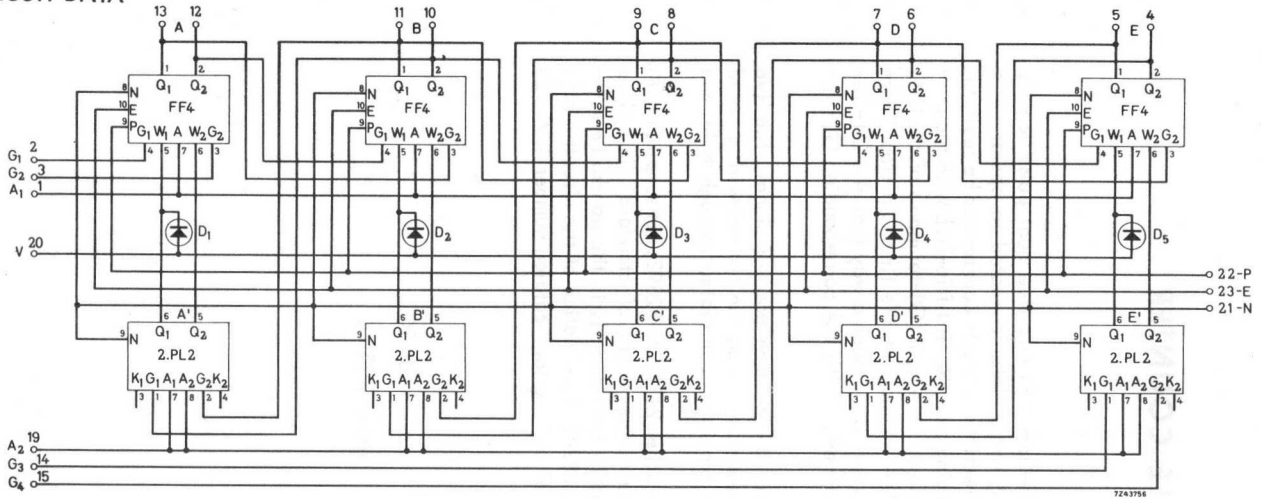
REVERSIBLE COUNTER

The unit BCA 1 consists of five flip-flops FF4 and five dual pulse logic's 2.PL2, mounted on a printed-wiring board, interconnected to operate as a bi-directional shift register. A bi-directional decade counter can be realised by interconnecting the gate (G)-terminals of the first flip-flop with the output (Q)-terminals of the fifth flip-flop and the gate (G)-terminals of the fifth dual pulse logic with the output (Q)-terminals of the first flip-flop. These interconnections have to be made externally in such a way that the Q1- respectively Q2-terminal has to be connected with the corresponding G_1- respectively G_2-terminal.

The flip-flops can be reset by means of a common positive signal. The five reset diodes D_1 up to D_5 inclusive are mounted on the printed-wiring board as well. The printed-wiring board is provided with plated through holes and single sided gold plated contacts.
With the mating connector catalog number 2422 020 52592, not supplied with the reversible counter, this printed-wiring board of standard dimensions (121.8 mm x 180.3 mm x 1.6 mm) can be used directly in the standard mounting chassis catalog number 4322 026 38240. The fixation of the circuit blocks FF4 and 2.PL2 is secured by means of locking tags catalog number 4322 026 33690.

Pulse repetition frequency range:	0 - 70 kHz
Ambient temperature range:	−20 to +60 °C
Weight:	approx. 250 g

CIRCUIT DATA



Terminal

1 = A_1	= a.c. input forward direction	9 = Q_{1C}	= output 1 flip-flop C	16 = not connected	
2 = G_1	= gate input (G_1) flip-flop A	10 = Q_{2B}	= output 2 flip-flop B	17 = not connected	
3 = G_2	= gate input (G_2) flip-flop A	11 = Q_{1B}	= output 1 flip-flop B	18 = not connected	
4 = Q_{2E}	= output 2 flip-flop E	12 = Q_{2A}	= output 2 flip-flop A	19 = A_2	= a.c. input reverse direction
5 = Q_{1E}	= output 1 flip-flop E	13 = Q_{1A}	= output 1 flip-flop A	20 = V	= reset input
6 = Q_{2D}	= output 2 flip-flop D	14 = G_3	= gate input (G_1) dual pulse logic E'	21 = N	= common negative supply −6 V
7 = Q_{1D}	= output 1 flip-flop D			22 = P	= common positive supply +6 V
8 = Q_{2C}	= output 2 flip-flop C	15 = G_4	= gate input (G_2) dual pulse logic E'	23 = E	= common supply 0 V

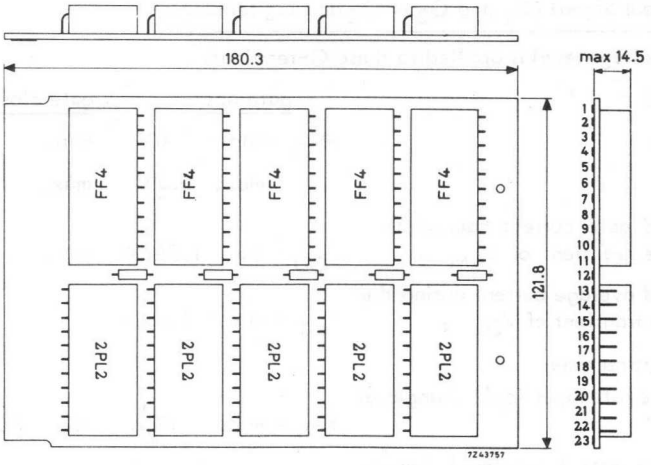
Power Supply

Terminal 21: $V_N = -6V \pm 5\%$, $-I_N = 55mA$
22: $V_P = +6V \pm 5\%$, $I_P = 3mA$
Nominal value of the current
23: $V_E = 0V$

Notes

- When a current is flowing towards the unit, the positive sign is used
- The data given apply to the most adverse supply voltages for a combination of units, namely
  $V_N = -5.7V$ and $V_P = +6.3V$
- The temperatures $-20\,^{\circ}C$ and $+60\,^{\circ}C$ and the tolerances on the supply voltages are absolute limiting values

Dimensions and terminal location



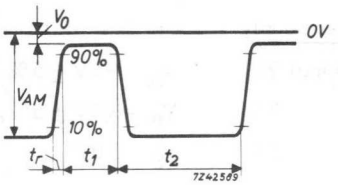
INPUT DATA

Input Signal Requirements

Trigger Input Signal (A_1 or A_2 terminal)

A positive-going voltage step is applied to terminal A. When this voltage step is applied to terminal A_1 the counter advances one position, when it is applied to terminal A_2 the counter reverses one position.

Voltage V_{AM} = min. $-0.7V_N$
= max. $-V_N$
$-V_0$ = min. 0V
= max. 0.2V



Required direct current I_{A1D} (I_{A2D}) = min. 8.8mA

Required current during the transient:
averaged over 0.4 µs I_{A1T} (I_{A2T}) = min. 30mA
0.7 µs = min. 22.5mA

Rise time t_r = max. 0.7 µs

Pulse duration t_1 = min. 3 µs
t_2 = min. 11 µs

Input noise level V_n = max. 1V p-p

Gate Input Signal (G_1 and G_2 or G_3 and G_4 terminals)

A d.c. voltage level is applied to these G-terminals

		gate open	gate closed
Voltage	$-V_G$ = min.	0V	min. V_{AM}
	= max.	0.2V	max. $-V_N$
Required gate current caused by negative transient of V_{AM}	I_{GD} = min.	1.75mA	min. 1.2 mA
Required average current during the positive transient of V_G	I_{GT} = min.	1.6mA	
Gate setting time			
when the gate input level changes at random	t_{GS} = min.	17 µs	min. 25 µs
when the gate input level changes within 2 µs after the positive going edge of the trigger signal	t_{GS} = min.	11 µs	min. 11 µs

Notes
- The latter applies to the shift register configuration so that the max. shift frequency is approximately 70 kHz
- During triggering the G levels should not be at zero voltage level simultaneously
- The gate setting time is the required waiting time between the last G level change and the positive-going edge of the trigger pulse

Reset Input Signal (V-terminal)

For resetting the counter a positive d.c. voltage is applied to terminal V. This signal causes all Q_1-terminals to reach a "negative high" and all Q_2-terminals to reach a "negative low" level.

Input Level during Reset

Voltage V_v = min. 1 V
= max. 10 V

Current I_v = min. 4.5 mA

During shifting it is recommended that terminal V is connected to a voltage level:

Voltage $-V_v$ = min. 0.4 V
= max. 15 V

Current $-I_v$ = min. 0.15 mA
(at $-V_v$ = 0.4 V)

OUTPUT DATA

These data apply to the various flip-flop stages:

Output Signal Characteristics

Transistor non-conducting

Voltage $-V_Q$ = min. $-0.7 V_N$

Available direct current I_{QD} = max. 0.7 mA

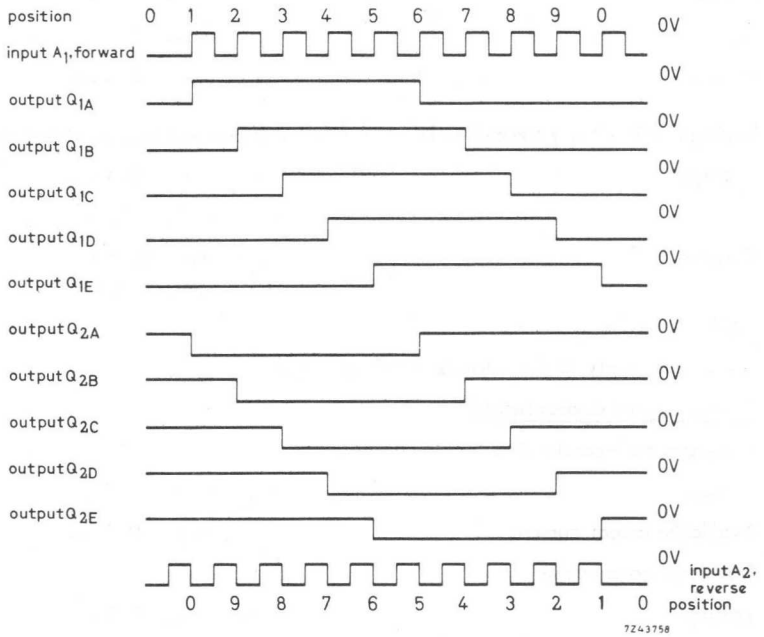
Transistor conducting

Voltage $-V_Q$ = max. 0.2 V
= min. 0 V

		flip-flops B-C-D	flip-flops A-E
available current during the transient $-I_{QT}$	averaged over 0.4 µs	max. 8 mA	max. 9.4 mA
	averaged over 0.7 µs	max. 11 mA	max. 12.4 mA
available direct current $-I_{QD}$		max. 3.75 mA	max. 4.25 mA

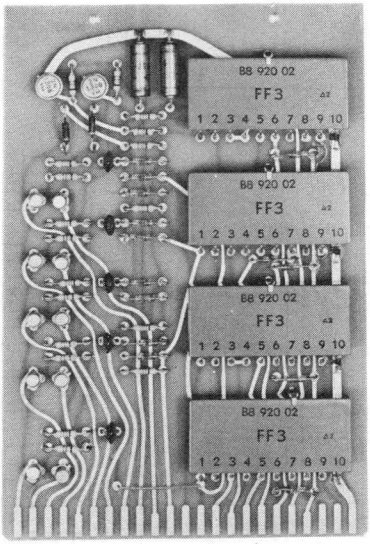
These current data apply to the unit, operating as a bi-directional shift register. When the unit is interconnected to form a bi-directional decade counter the lowest current values of $-I_{QT}$ and $-I_{QD}$ are valid for all flip-flops.

Output levels during counting, when the unit is externally interconnected to form a bi-directional decade counter. To this end terminals 2 and 5, 3 and 4, 12 and 15, 13 and 14 have to be connected.
The output levels at the Q-terminals can be taken from the figure below.



Note that after 10 positive-going voltage steps at the input terminal A_1 (A_2), the output terminal Q_{2E} (Q_{2A}) delivers one positive-going voltage step, whilst the decade counter has retaken its initial position, namely all Q_2-terminals being at 0V level.

DECADE COUNTER AND NUMERICAL INDICATOR TUBE DRIVER ASSEMBLY



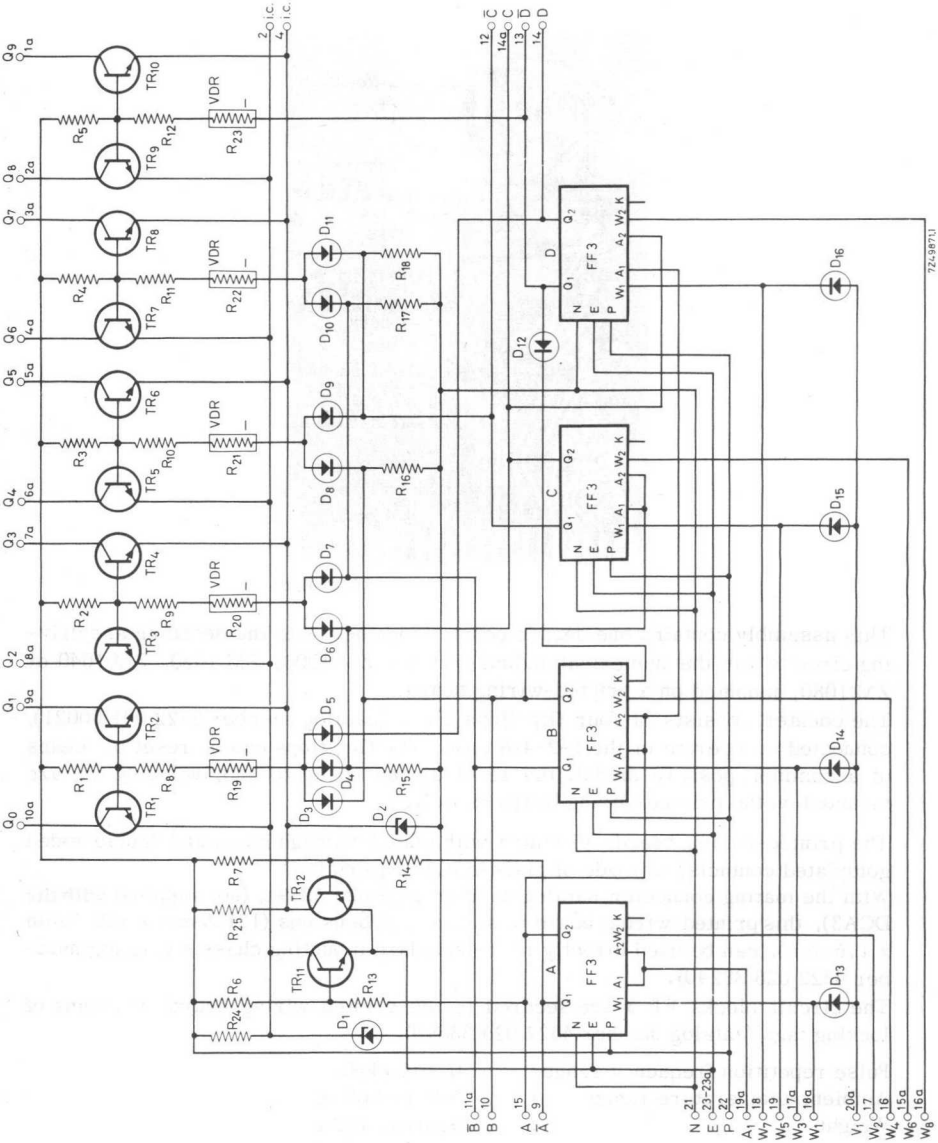
RZ 22603-6

This assembly contains one decade counter together with the decoding and driving circuits for the numerical indicator tubes ZM 1000, ZM 1020, ZM 1040 or ZM 1080, mounted on a printed-wiring board.
The counter consists of four flip-flops FF 3 (catalog number 2722 001 00021), connected to operate in the 1-2-4-8 code. The flip-flops can be reset by means of a common positive signal; the reset diodes D_1 up to and including D_4 are mounted on the printed-wiring board as well.

The printed-wiring board, provided with plated-through holes and double-sided goldplated contacts, is made of glass-epoxy material.
With the mating connector, catalog number 2422 020 52591, (not supplied with the DCA3), this printed-wiring board of standard dimensions (121.8 mm x 180.3 mm x 1.6 mm), can be used directly in the standard mounting chassis (catalog number 4322 026 38240).
The circuit blocks FF 3 are secured to the printed-wiring board by means of locking tags (catalog number 4322 026 33690).

Pulse repetition frequency range	:	0 - 100 kHz
Ambient-temperature range	:	−20 to +60 °C
Weight	:	approx. 150 g

CIRCUIT DATA



Terminals

1 = not connected
2 = internal connection
3 = not connected
4 = internal connection
5 = not connected
6 = not connected
7 = not connected
8 = not connected
9 = $\overline{A}$ = Q_{1A} = output 1 flip-flop A
10 = B = Q_{2B} = output 2 flip-flop B
11 = not connected
12 = $\overline{C}$ = Q_{1C} = output 1 flip-flop C
13 = $\overline{D}$ = Q_{1D} = output 1 flip-flop D
14 = D = Q_{2D} = output 2 flip-flop D
15 = A = Q_{2A} = output 2 flip-flop A
16 = W_4 = W_2 of flip-flop B
17 = W_2 = W_2 of flip-flop A
18 = W_7 = W_1 of flip-flop D
19 = W_5 = W_1 of flip-flop C
20 = not connected
21 = N = common negative supply −6 V
22 = P = common positive supply +6 V
23 = E = common supply 0 V

1a = Q_9 = digit number 9
2a = Q_8 = digit number 8
3a = Q_7 = digit number 7
4a = Q_6 = digit number 6
5a = Q_5 = digit number 5
6a = Q_4 = digit number 4
7a = Q_3 = digit number 3
8a = Q_2 = digit number 2
9a = Q_1 = digit number 1
10a = Q_o = digit number 0
11a = $\overline{B}$ = Q_{1B} = output 1 flip-flop B
12a = not connected
13a = not connected
14a = C = Q_{2C} = output 2 flip-flop C
15a = W_6 = W_2 of flip-flop C
16a = W_8 = W_2 of flip-flop D
17a = W_3 = W_1 of flip-flop B
18a = W_1 = W_1 of flip-flop A
19a = A_1 = a.c. input counter
20a = V_1 = reset input counter
21a = not connected
22a = not connected
23a = E = common supply 0 V

Power supply

Terminal 21 : $V_N = -6\ V \pm 5\ \%$, $-I_N = 42\ mA$ } nominal value
22 : $V_P = +6\ V \pm 5\ \%$, $I_P = 8.8\ mA$ } of the current
23 = 23A : $V_E = 0\ V$

Notes

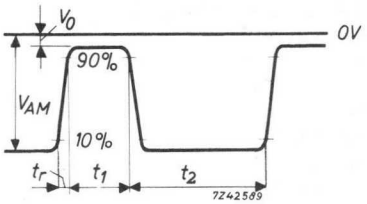
- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N = -5.7\ V$ and $V_P = +5.7\ V$.
- The temperatures $-20\ ^oC$ and $+60\ ^oC$ and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input signal requirements

Trigger input signal (terminal A_1)

A positive-going voltage step is applied to terminal A_1. This voltage step advances the counter one position.



Voltage	V_{AM}	= min.	$-0.7\ V_N$
		= max.	$-\ V_N$
	$-V_0$	= min.	$0\ V$
		= max.	$0.2\ V$
Required direct current	I_{A_1D}	= min.	$1.75\ mA$
Required current during the transient averaged over $0.4\ \mu s$	I_{A_1T}	= min.	$6\ mA$
over $0.7\ \mu s$		= min.	$4.5\ mA$
Rise time	t_r	= max.	$0.7\ \mu s$
Pulse duration	t_1	= min.	$1\ \mu s$
	t_2	= min.	$8\ \mu s$

Reset input signal (terminal V_1)

For resetting the counter a positive d.c. voltage is applied to terminal V_1. This signal causes all terminals Q_1 to reach a "negative high" and all terminals Q_2 to reach a "negative low" level.

Input level during reset

Voltage	V_{V_1}	= min.	1 V
		= max.	10 V
Current	I_{V_1}	= min.	3.6 mA

During counting it is recommended that terminal V_1 is connected to a voltage level.

Voltage	$-V_{V_1}$	= min.	0.4 V
		= max.	10 V
Current	$-I_{V_1}$	= min.	0.12 mA (at $-V_{V_1}$ = 0.4 V)

D.C. input (terminals W)

A d.c. voltage level is applied to terminals W_1 up to and including W_8. A positive voltage drives the corresponding transistor into the non-conducting state and a negative voltage drives the transistor into the conducting state.

Transistor conducting

Current	$-I_W$	= min.	0.6 mA ($-V_W$ = max. 0.4 V)
		= max.	15 mA

Transistor non-conducting

Voltage	V_W	= min.	0.2 V
		= max.	10 V
Current	I_W	= min.	0.9 mA

OUTPUT DATA

Decade counter section

The outputs of the counter (A, $\overline{A}$, B, $\overline{B}$, etc.) may furthermore be loaded with two gate invertors GI or two negative AND-gates. Output D of the last flip-flop is then still capable to drive a next decade.
A, B, C and D are the outputs of the flip-flops which are at 0 V level, when the decade is set on digit number 0.

Output transistor conducting

Voltage $-V_Q$ = min. 0 V, max. 0.2 V

		A	$\overline{A}$	B	$\overline{B}$	C	$\overline{C}$	D	$\overline{D}$
Available direct current (in mA)	$-I_{QD}$ =	3.4	6	2.15	3.9	3	3.9	6	5.1
Available transient current averaged over 0.7 μs (in mA)	$-I_{QT}$ =	9	14	8.4	12.9	8.9	12.9	14	14

Output transistor non-conducting

Voltage $-V_Q$ = min. 0.7 V_N, = max. V_N

		A	$\overline{A}$	B	$\overline{B}$	C	$\overline{C}$	D	$\overline{D}$
Available direct current (in mA)	I_{QD} =	0.1	0.13	0.1	0.1	0.1	0.1	0.13	0.1

Numerical indicator tube driver

The outputs Q_0 (terminal 10a) up to and including Q_9 (terminal 1a) have to be connected to the pins k_0 up to and including k_9 of the numerical indicator tube ZM 1000, ZM 1020, ZM 1040 or ZM 1080.
The anode of these tubes has to be connected via a resistor R_a to the high voltage power supply V_b.

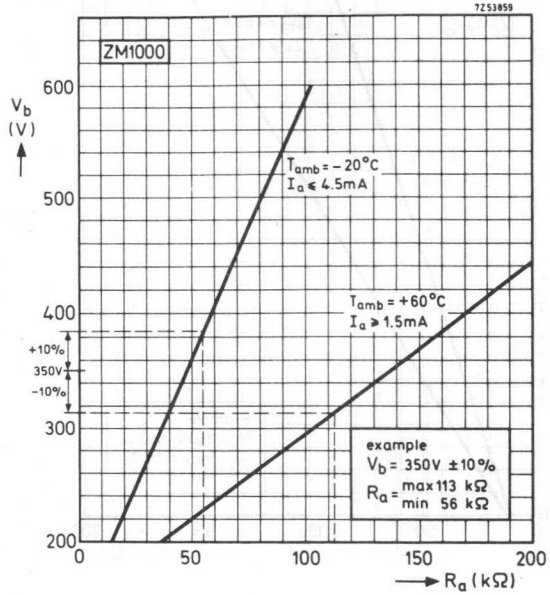
Output transistor conducting

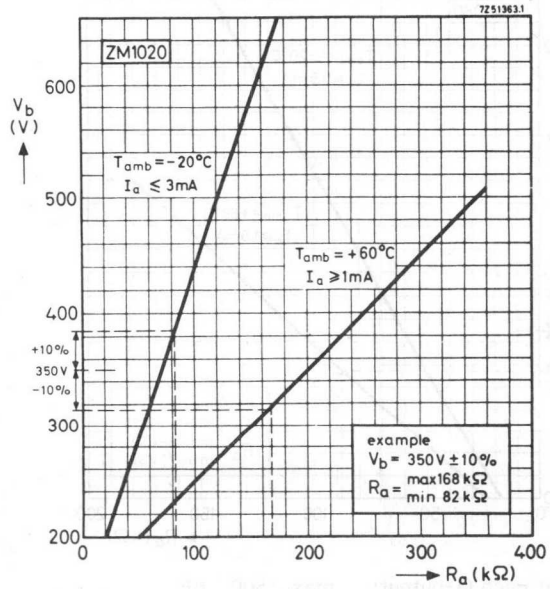
Voltage V_Q = max. 3.2 V

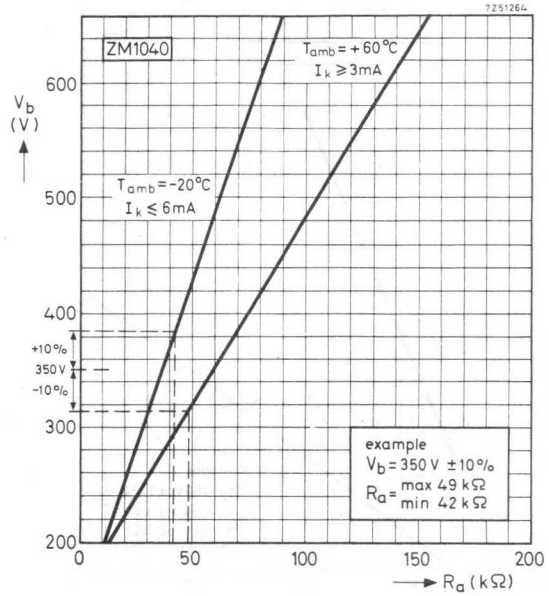
Current I_Q = max. 6 mA

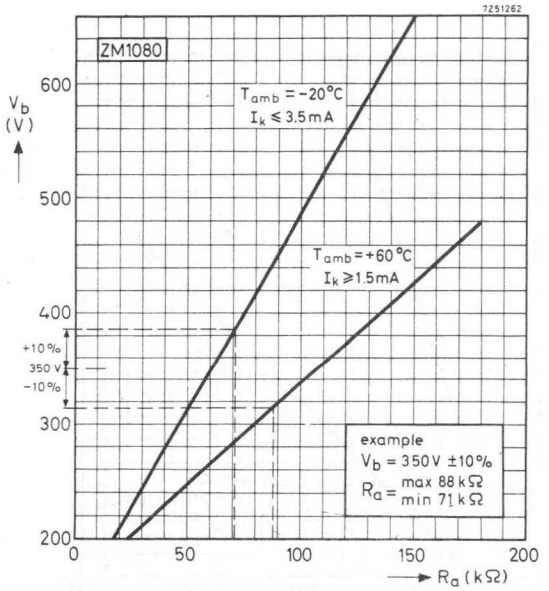
The available output current (I_Q) of the ten numerical outputs Q_0 up to and including Q_9 is sufficient to deliver the required current for the numerical indicator tube ZM 1000, ZM 1020, ZM 1040 or ZM 1080.

The relation between the permitted value and tolerances of the high voltage supply V_b and the corresponding anode series resistor R_a for the various indicator tubes over the whole temperature range is given in the following graphs.


7Z53859
ZM1000
V_b (V)
600
500
400
300
200
+10%
350V
-10%
$T_{amb} = -20°C$
$I_a \leq 4.5mA$
$T_{amb} = +60°C$
$I_a \geq 1.5mA$
example
V_b = 350V ±10%
R_a = max 113 kΩ
min 56 kΩ
0
50
100
150
200
R_a (kΩ)

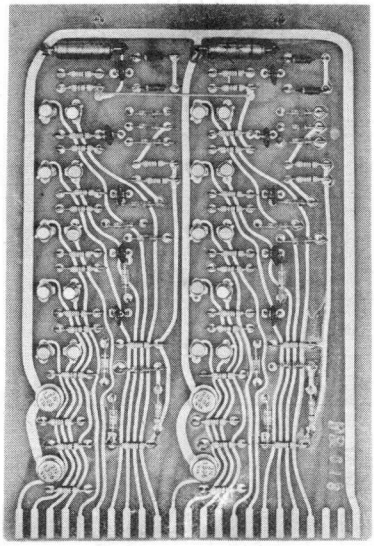

7Z51363.1
ZM1020
V_b (V)
600
500
400
300
200
+10%
350V
-10%
$T_{amb} = -20°C$
$I_a \leq 3mA$
$T_{amb} = +60°C$
$I_a \geq 1mA$
example
V_b = 350V ±10%
R_a = max 168 kΩ
min 82 kΩ
0
100
200
300
400
R_a (kΩ)





Wiring capacitance at each Q-output: max. 500 pF

DUAL NUMERICAL INDICATOR TUBE DRIVER ASSEMBLY



RZ 22603-8

This assembly contains two BCD-to-decimal decoding and driving circuits for the numerical indicator tubes ZM 1000, ZM 1020, ZM 1040 or ZM 1080, mounted on a printed-wiring board.

The 2.ID 1 has been designed to operate in conjunction with decade counters in the 1-2-4-2 (jump at 8) or 1-2-4-8 code, e.g. the dual decade counter assembly 2.DCA 2 (catalog number 2722 009 00011).

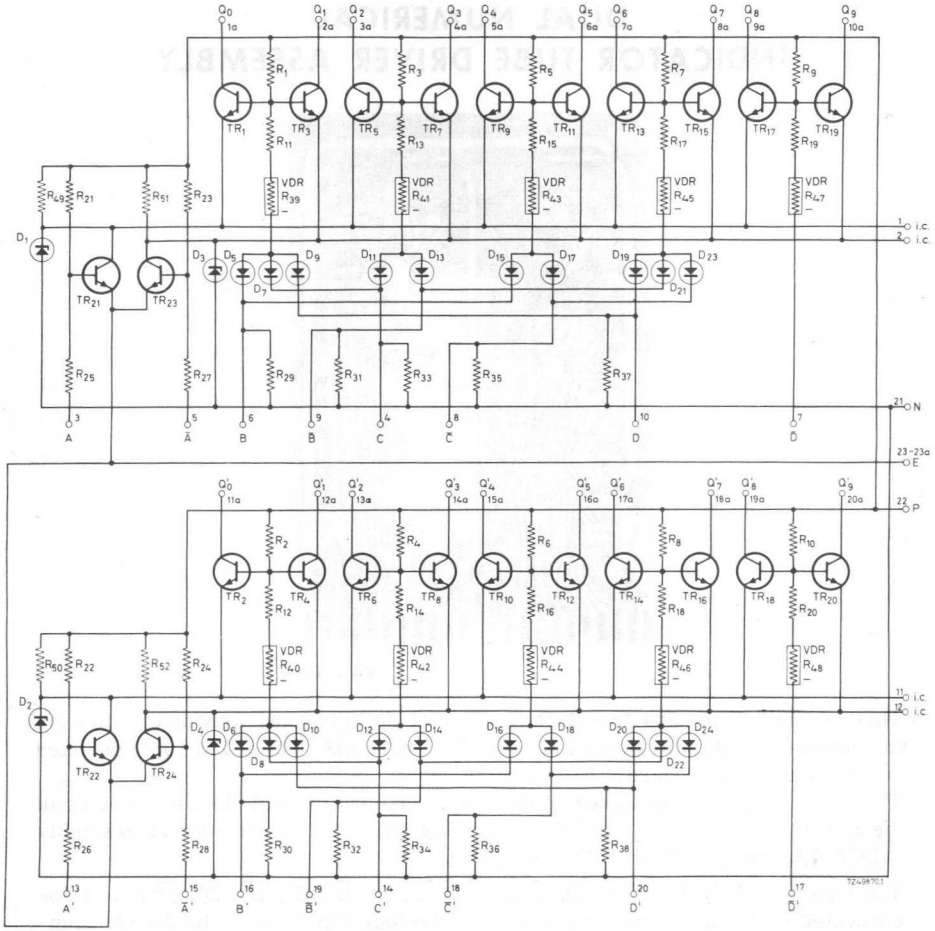
The inputs A, $\overline{A}$, B, $\overline{B}$, C, $\overline{C}$, D, $\overline{D}$ and A', $\overline{A'}$, B', $\overline{B'}$, C', $\overline{C'}$, D', $\overline{D'}$ have to be connected to the corresponding outputs of the four flip-flops of the decade counter.

The inputs A, B, C, D and A', B', C', D' have to be at the "0" level for the digit number 0 to be indicated.

The printed-wiring board, provided with plated-through holes and double-sided goldplated contacts, is made of glass-epoxy material. With the mating connector (catalog number 2422 020 52591), not supplied with the 2.ID 1, this printed-wiring board of standard dimensions (121.8 mm x 180.3 mm x 1.6 mm) can be used directly in the standard mounting chassis (catalog number 4322 026 38240).

Ambient-temperature range:	−20 to +60 °C
Weight	approx. 100 g

CIRCUIT DATA



Terminals

1 = internal connection
2 = internal connection
3 = A = to be connected to output Q of first flip-flop
4 = C = to be connected to output Q of third flip-flop
5 = $\overline{A}$ = to be connected to output $\overline{Q}$ of first flip-flop
6 = B = to be connected to output Q of second flip-flop
7 = $\overline{D}$ = to be connected to output $\overline{Q}$ of fourth flip-flop
8 = $\overline{C}$ = to be connected to output $\overline{Q}$ of third flip flop
9 = $\overline{B}$ = to be connected to output $\overline{Q}$ of second flip-flop
10 = D = to be connected to output Q of fourth flip-flop

} decade counter 1

11 = internal connection
12 = internal connection
13 = A' = to be connected to output Q of first flip-flop
14 = C' = to be connected to output Q of third flip-flop
15 = $\overline{A'}$ = to be connected to output $\overline{Q}$ of first flip-flop
16 = B' = to be connected to output Q of second flip-flop
17 = $\overline{D'}$ = to be connected to output $\overline{Q}$ of fourth flip-flop
18 = $\overline{C'}$ = to be connected to output $\overline{Q}$ of third flip-flop
19 = $\overline{B'}$ = to be connected to output $\overline{Q}$ of second flip-flop
20 = D' = to be connected to output Q of fourth flip-flop
} decade counter 2
21 = N = common negative supply −6 V
22 = P = common positive supply +6 V
23 = 23a = E = common supply 0 V

1a up to and including 10a = numerical outputs Q_0 up to and including Q_9 to drive numerical indicator tube 1

11a up to and including 20a = numerical outputs Q'_0 up to and including Q'_9 to drive numerical indicator tube 2

Power supply

Terminal 21 : $V_N = -6\ V \pm 5\%$, $-I_N = 8.5$ mA
22 : $V_P = +6\ V \pm 5\%$, $I_P = 7$ mA
} nominal value of the current required for one ID 1
23 : $V_E = 0$ V common

Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely: $V_N = -5.7$ V and $V_P = +6.3$ V
- The temperatures −20 °C and +60 °C and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input signal requirements (terminals A, $\overline{A}$, A', $\overline{A'}$, etc.)

Input at "0" level

Voltage $-V_I$ = min. 0 V
= max. 0.2 V

		A, A', $\overline{A}$, $\overline{A'}$	B, B', $\overline{B}$, $\overline{B'}$, C, C', $\overline{C}$, $\overline{C'}$, D, D'	$\overline{D}$, $\overline{D'}$
Required direct current	I_I	0 mA	2.1 mA	0 mA
Required transient current	I_{QT}	0 mA	1.1 mA	0 mA

Input at negative high level

Voltage $-V_I$ = min. 0.7 V_N
= max. V_N

		A, A', $\overline{A}$, $\overline{A'}$	B, B', $\overline{B}$, $\overline{B'}$, C, C', $\overline{C}$, $\overline{C'}$, D, D' $\overline{D}$, $\overline{D'}$
Required direct current	$-I_I$	0.57 mA	0.6 mA

Input impedance equivalent to a capacitance of approx. 150 pF

Operational data

- When an ID 1 is driven from a decade counter with flip-flops operating in the 1-2-4-8 code, these flip-flops may be additionally loaded with two negative AND-gates, or with two GI's if the decade counter is equipped with FF 3 flip-flops, or with one GI if the decade counter is equipped with FF 1 flip-flops. Output D of the last flip-flop is capable of driving a following decade counter.
- A, B, C, D and A', B', C', D' must be connected to the outputs of the flip-flops which are at "0" level, when the decade counter is set on digit number 0.

OUTPUT DATA

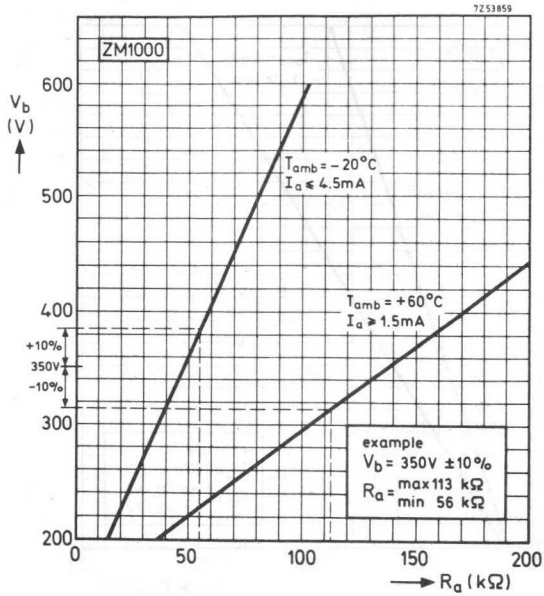
The outputs Q_0 up to and including Q_9 and Q'_0 up to and including Q'_9 have to be connected to the pins k_0 up to and including k_9 of the numerical indicator tube ZM 1000, ZM 1020, ZM 1040 or ZM 1080.
The anode of these tubes has to be connected via a resistor R_a to the high voltage power supply V_b.

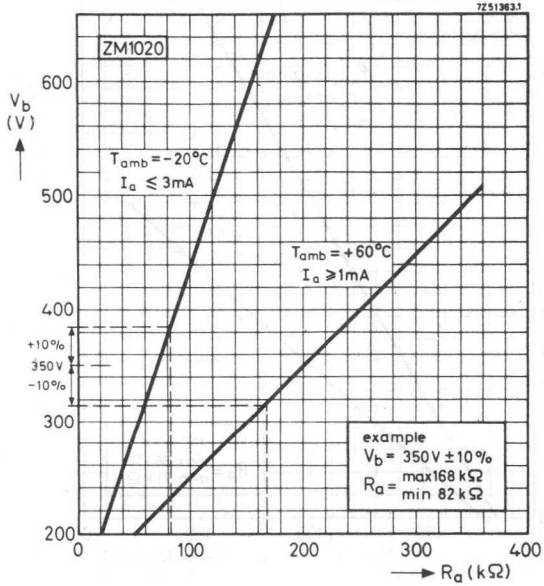
Output transistor conducting

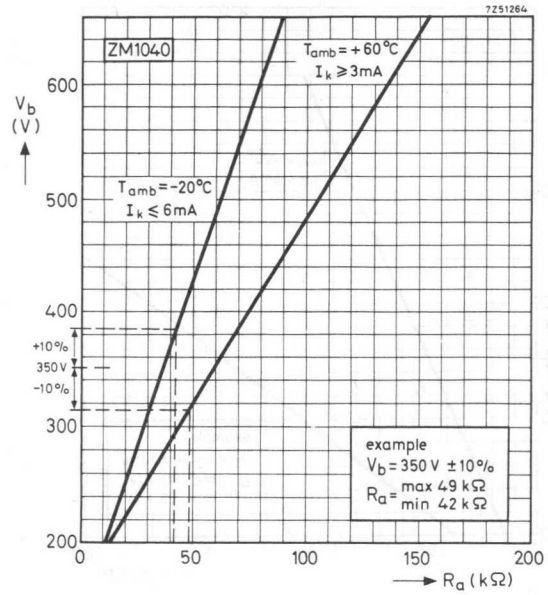
Voltage V_Q = max. 3.2 V

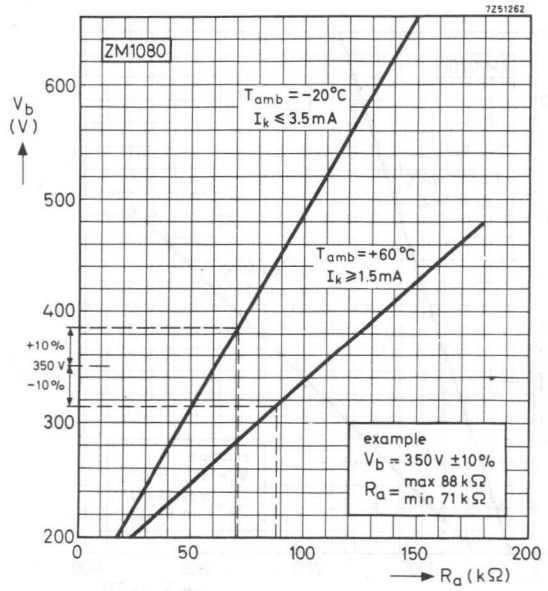
Current I_Q = max. 6 mA

The available output current (I_Q) of the ten numerical outputs Q_0 (terminal 1a and 11a) up to and including Q_9 (terminal 10a and 20a) is sufficient to deliver the required current for the numerical indicator tube ZM 1000, ZM 1020, ZM 1040 or ZM 1080.
The relation between the permitted value and tolerances of the high voltage supply V_b and the corresponding anode series resistor R_a for the various indicator tubes over the whole temperature range is given in the following graphs.


7Z53859
ZM1000
V_b (V)
600
500
400
300
200
+10%
350V
-10%
T_{amb} = -20°C
$I_a \leq$ 4.5mA
T_{amb} = +60°C
$I_a \geq$ 1.5mA
example
V_b = 350V ±10%
R_a = max 113 kΩ
min 56 kΩ
0
50
100
150
200
R_a (kΩ)


7Z51363.1
ZM1020
V_b (V)
600
500
400
300
200
+10%
350V
-10%
T_{amb} = -20°C
$I_a \leq$ 3mA
T_{amb} = +60°C
$I_a \geq$ 1mA
example
V_b = 350V ±10%
R_a = max 168 kΩ
min 82 kΩ
0
100
200
300
400
R_a (kΩ)

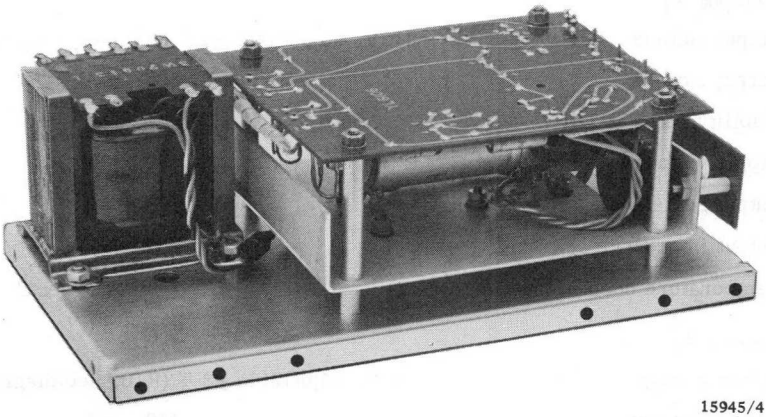




Wiring capacitance at each Q-output: max. 500 pF

ACCESSORIES FOR CIRCUIT BLOCKS
100 kHz SERIES

POWER SUPPLY UNIT



15945/4

Input voltage	220 V_{ac} and 235 V_{ac}
Output voltage	+6 V_{dc} and −6 V_{dc}

APPLICATION

This power supply unit has been designed for use with the circuit blocks of the 100 kHz- and the 1-series. However, it is also suitable as a supply for other transistorised circuits.

CONSTRUCTION

The unit is dimensioned for mounting in the standardized 19" chassis. The power supply unit fits in chassis 4322 026 38240; the base plate of the unit then replaces a side plate of the chassis. The supply unit occupies the same space as four printed-wiring boards.

Dimensions	215 x 125 x 70 mm
Weight	1.5 kg

TECHNICAL PERFORMANCE

Input voltage	220 V_{ac} +10 %, −15 %	
	235 V_{ac} +10 %, −15 %	
Frequency	50 to 60	Hz
Fusing	1 A fuse in the 220 V winding only	

−6 V output [1])

Output voltage	6 V, adjustable ±3 % (R5, see diagram)	
Output current	600	mA
Stability ratio at 220 V	450:1	
Ripple voltage	50	mV_{rms}
Output resistance	0.3	Ω
Output impedance at 10 kHz	0.2	Ω
Temperature coefficient	−3	mV/deg C

+6 V output [1])

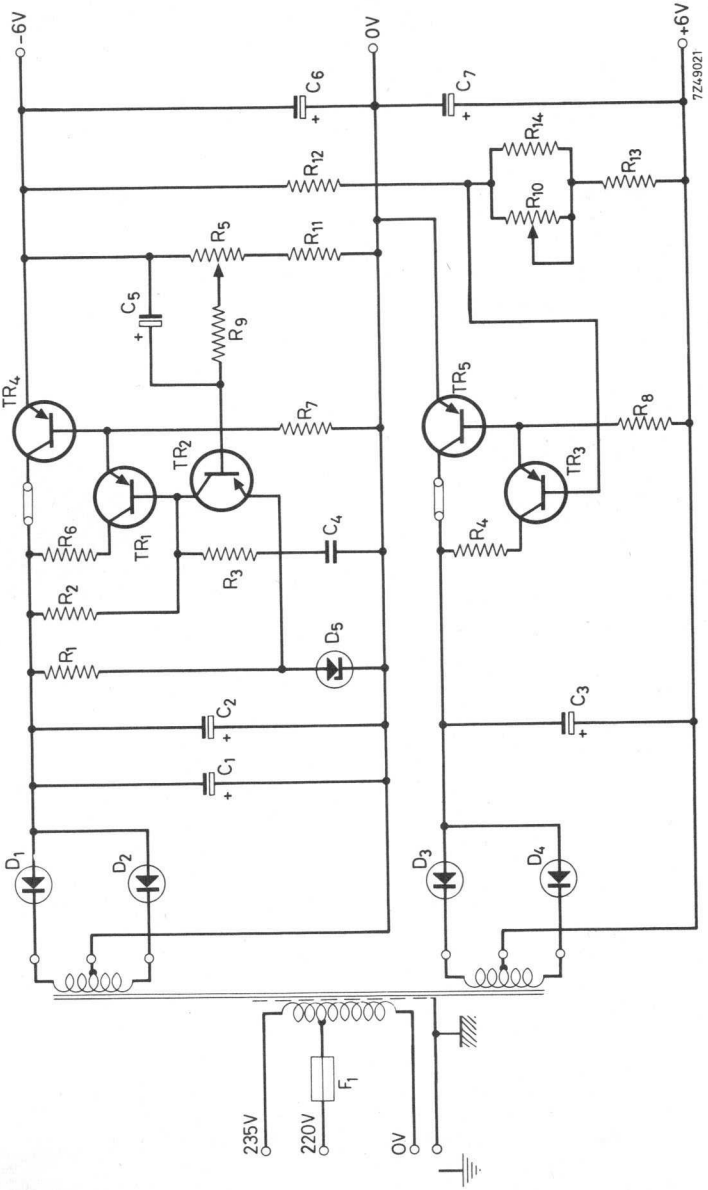
Output voltage	6 V, adjustable ±3 % (R10, see diagram)	
Output current	150	mA
Stability ratio at 220 V	360:1	
Ripple voltage	50	mV_{rms}
Output resistance	1.5	Ω
Output impedance at 10 kHz	0.5	Ω
Temperature coefficient	+6	mV/deg C

Operating-temperature range	−20 to +60	°C
Storage-temperature range	−20 to +75	°C

In systems requiring more than one power supply unit, the earth tags (marked "0 V") may be interconnected, the positive tags (marked "+6 V") and the negative tags (marked "−6 V") must remain strictly separated.

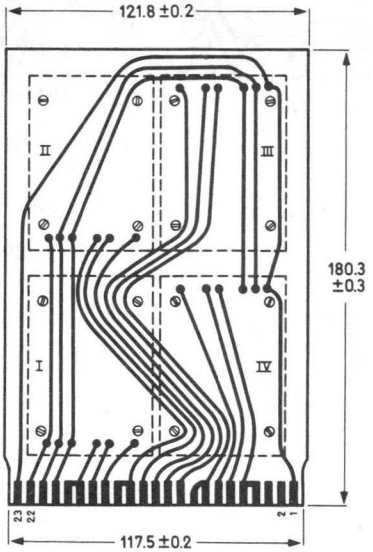
When a system is put into operation for the first time, the output voltages of the power supply units have to be adjusted to 6 V under nominal system load.

1) All values are given for full load.


-6V
0V
+6V
7249021
C6
C7
R14
R12
R10
R13
R5
R11
C5
R9
TR4
R7
TR5
R8
TR2
TR3
TR1
R6
C4
R4
R3
R2
D5
R1
C2
C3
C1
D1
D2
D3
D4
235V
220V
F1
0V

PRINTED-WIRING BOARD FOR FOUR UNITS PA 1

This printed-wiring board fits the mounting chassis 4322 026 38240. It can be used directly with the aid of the mating connector 2422 020 52592. On this board up to four PA 1's can be mounted, the next position in the chassis being left empty.



Terminal location:

1 = E = common supply 0 V (interconnected to terminal 1)

2 = not connected

3 = not connected

4 = N_2, 5 = N_2 } supply max. 60 V — unit nr. IV

6 = Q = output PA 1 — unit nr. IV

7 = W = input PA 1 — unit nr. IV

8 = N_2, 9 = N_2 } supply max. 60 V — unit nr. III

10 = Q = output PA 1 — unit nr. III

11 = W = input PA 1 — unit nr. III

12 = W = input PA 1 — unit nr. II

13 = Q = output PA 1 — unit nr. II

14 = N_2, 15 = N_2 } supply max. 60 V — unit nr. II

16 = W = input PA 1 — unit nr. I

17 = Q = output PA 1 — unit nr. I

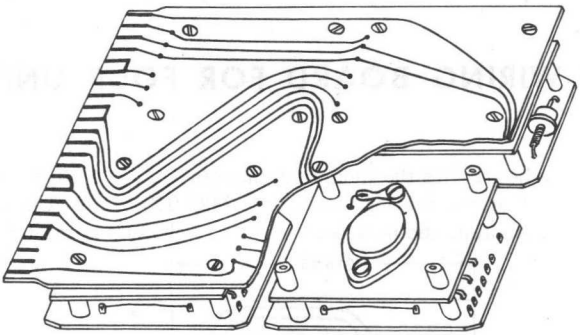
18 = N_2, 19 = N_2 } supply max. 60 V — unit nr. I

20 = N_1 = common supply −6 V

21 = P = common supply +6 V

22 = E = common supply 0 V

23 = E = common supply 0 V



7Z43648

Material	glass epoxy with plated-through holes
Hole diameter	1.2 mm
Contacts	1 x 23, gold plated, pitch 0.2 inch

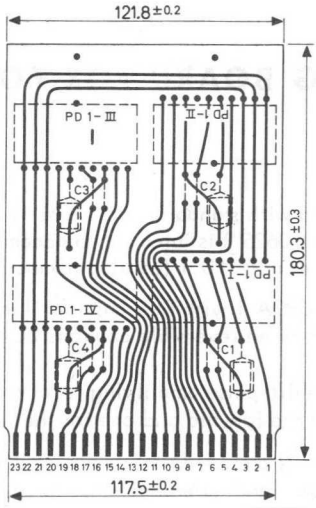
PRINTED-WIRING BOARD FOR FOUR UNITS PD 1

This printed-wiring board with standard dimensions 121.8 mm x 180.3 mm x 1.6 mm (4.8" x 7.1" x 0.0625") is intended to accomplish the mounting of maximum four pulse driver units PD 1 (catalog number 2722 001 13011).

One printed-wiring board PDA 1 with four units PD 1 mounted on it, can be used in conjunction with three reversible counters BCA 1 (catalog number 2722 009 00021).
Two units PD 1 perform shift-pulse amplifying functions between two reversible counters BCA 1, one for the forward and one for the reverse direction.

The printed-wiring board is provided with two wire jumpers for each PD 1. In case the number of trigger- and gate-inputs has to be extended, these wire jumpers can be replaced by diodes, type OA 95. The required connections with the EG- and K-terminals of the PD 1 have already been made in the print pattern.
Furthermore the printed-wiring board is provided with two plated-through holes for each unit PD 1. In case the output-pulse duration of the PD 1 has to be increased, these holes can be used for mounting the required capacitor. The terminals of this capacitor are then directly connected to the K- and L-terminals of the concerning PD 1.

Holes are provided to secure the PD 1 rigidly to the board by means of the locking tag 4322 026 33690.
With the mating connector 2422 020 52592 the printed-wiring board can be used directly in the mounting chassis 4322 026 38240.



Terminal location:

1 = Q_1 = output PD 1-I
2 = EG_1 = extension gate input PD 1-I
3 = K_1 = extension trigger input PD 1-I
4 = G_1 = gate input PD 1-I
5 = A_1 = trigger input PD 1-I
6 = Q_2 = output PD 1-II
7 = EG_2 = extension gate input PD 1-II
8 = K_2 = extension trigger input PD 1-II
9 = G_2 = gate input PD 1-II
10 = A_2 = trigger input PD 1-II
11 = A_3 = trigger input PD 1-III
12 = G_3 = gate input PD 1-III
13 = K_3 = extension trigger input PD 1-III
14 = EG_3 = extension gate input PD 1-III
15 = Q_3 = output PD 1-III
16 = A_4 = trigger input PD 1-IV
17 = G_4 = gate input PD 1-IV
18 = K_4 = extension trigger input PD 1-IV
19 = EG_4 = extension gate input PD 1-IV
20 = Q_4 = output PD 1-IV
21 = N = common supply −6 V
22 = P = common supply +6 V
23 = E = common supply 0 V

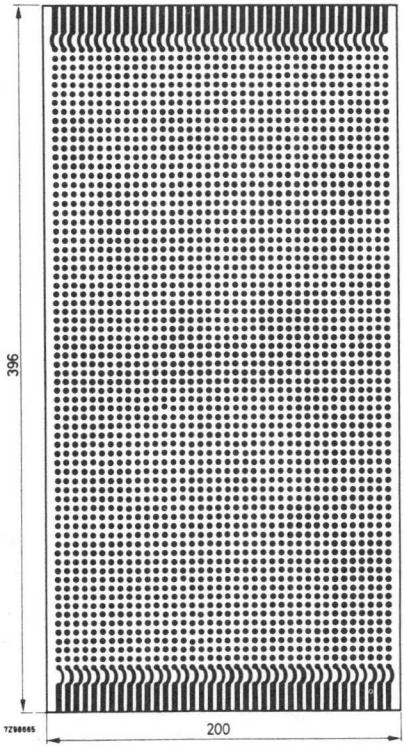
Material	glass epoxy with plated-through holes
Hole diameter	1.2 mm
Contacts	1 x 23, gold plated, pitch 0.2 inch

INPUT AND OUTPUT DATA

See specification of pulse driver unit PD 1 (catalog number 2722 001 13011)

EXPERIMENTERS' PRINTED–WIRING BOARDS

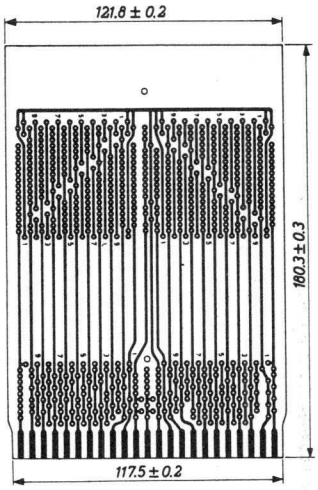
These experimenters' printed-wiring boards are very suitable for circuit blocks of the 100 kHz- and 1-Series.



Material	copper-clad phenolic resin bonded paper	
Grid pitch	5.08 mm (0.2 inch)	
Contacts	gold plated, pitch 0.2 inch	
	single sided 2 x 38	double sided 4 x 38
Holes	with holes	–
Catalogue number	4322 026 34900	4322 026 34910

PRINTED-WIRING BOARD

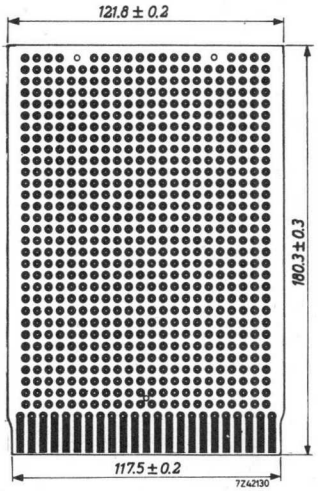
This printed-wiring board is intended for mounting circuit blocks of the 100 kHz- and 1-Series.
It fits the mounting chassis 4322 026 38240.



Material	copper-clad phenolic resin bonded paper with punched holes
Hole diameter	1.3 mm
Contacts	1 x 23, gold plated, pitch 0.2 inch

EXPERIMENTERS' PRINTED—WIRING BOARD

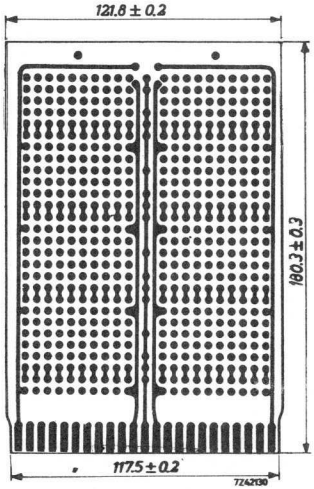
This experimenters' printed-wiring board is very suitable for circuit blocks of the 100 kHz- and 1-Series.
It fits the mounting chassis 4322 026 38240.



Material	copper-clad phenolic resin bonded paper with punched holes
Grid pitch	5.08 mm (0.2 inch)
Hole diameter	1.3 mm
Contacts	1 x 23, gold plated, pitch 0.2 inch

PRINTED—WIRING BOARD

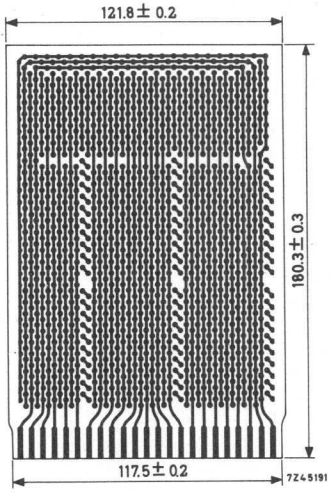
This printed-wiring board for 100 kHz- and 1-Series circuit blocks can accommodate 8 horizontally mounted blocks. Combination of circuit blocks with discrete components is easily possible on this board.
It fits the mounting chassis 4322 026 38240.



Material	copper-clad phenolic resin bonded paper with plated-through holes
Hole diameter	1.2 mm
Contacts	1 x 23, gold plated, pitch 0.2 inch

PRINTED-WIRING BOARD

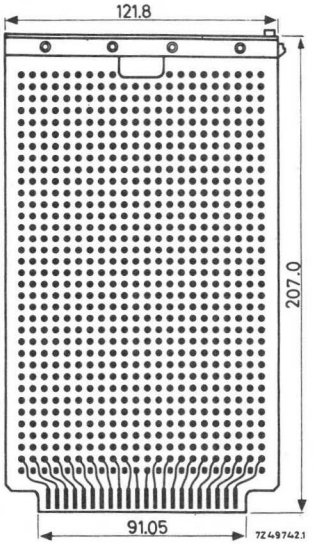
This printed-wiring board is intended for mounting circuit blocks of the 100 kHz- and 1-Series. It fits the mounting chassis 4322 026 38240.



Material	copper-clad phenolic resin bonded paper with plated-through holes
Hole diameter	1.2 mm
Contacts	1 x 23, gold plated, pitch 0.2 inch

EXPERIMENTERS' PRINTED–WIRING BOARD

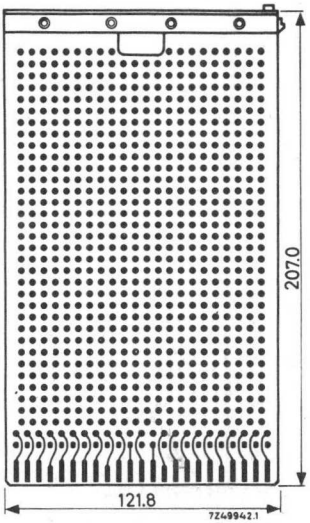
This experimenters' printed-wiring board (with extractor) is very suitable for circuit blocks of the 100 kHz- and 1-Series.
It fits the mounting chassis 4322 026 38230.



Material	phenolic resin bonded paper with holes; on both sides are copper lands around each hole
Grid pitch	5.08 mm (0.2 inch)
Hole diameter	1.3 mm
Contacts	2 x 22, gold plated, pitch 0.156 inch

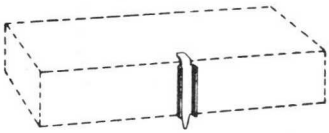
EXPERIMENTERS' PRINTED-WIRING BOARDS

These experimenters' printed-wiring boards (with extractor) are very suitable for circuit blocks of the 100 kHz- and 1-Series.
They fit the mounting chassis 4322 026 38240.



Catalogue number	4322 026 38630	4322 026 38690
Material	phenolic resin bonded paper	glass epoxy
Grid pitch	5.08 mm (0.2 inch)	
Holes	diameter 1.3 mm; on both sides of the board are copper lands around each hole	
Contacts	2 x 23, gold plated, pitch 0.2 inch	

LOCKING TAG



Circuit blocks of the 100 kHz- and 1-Series mounted parallel to the printed-wiring board can be secured rigidly by means of this small tag, which permits soldering in a standard 1.3 mm diameter hole. The minimum supply quantity is 1000 pieces.

STICKERS

These are drawing symbols of circuit blocks printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings. The drawing symbols are as shown on the data sheets of the relevant circuit blocks.
The stickers are available in rolls, each containing 1000 drawing symbols of the same type of circuit block. Each sticker can be separately detached from the roll, without cutting.

for circuit block of type	catalog number of a roll with 1000 stickers
FF 1	4322 026 35780
FF 2	4322 026 35790
FF 3	4322 026 35800
FF 4	4322 026 35810
2.3.N 1	4322 026 35820
2.2.N 1	4322 026 35830
2.3.P 1	4322 026 35840
2.2.P 1	4322 026 35850
2.PL 1	4322 026 35860
2.PL 2	4322 026 35880
EF 1/IA 1	4322 026 35890
2.EF 1	4322 026 35900
2.IA 1	4322 026 35910
2.EF 2	4322 026 35920
2.IA 2	4322 026 35930
2.GI 1	4322 026 34620
PS 1	4322 026 35950
PS 2	4322 026 36820
PR 1	4322 026 36830
OS 1	4322 026 35960
OS 2	4322 026 35980
PD 1	4322 026 30710
PA 1	4322 026 07760

Circuit blocks

1-Series

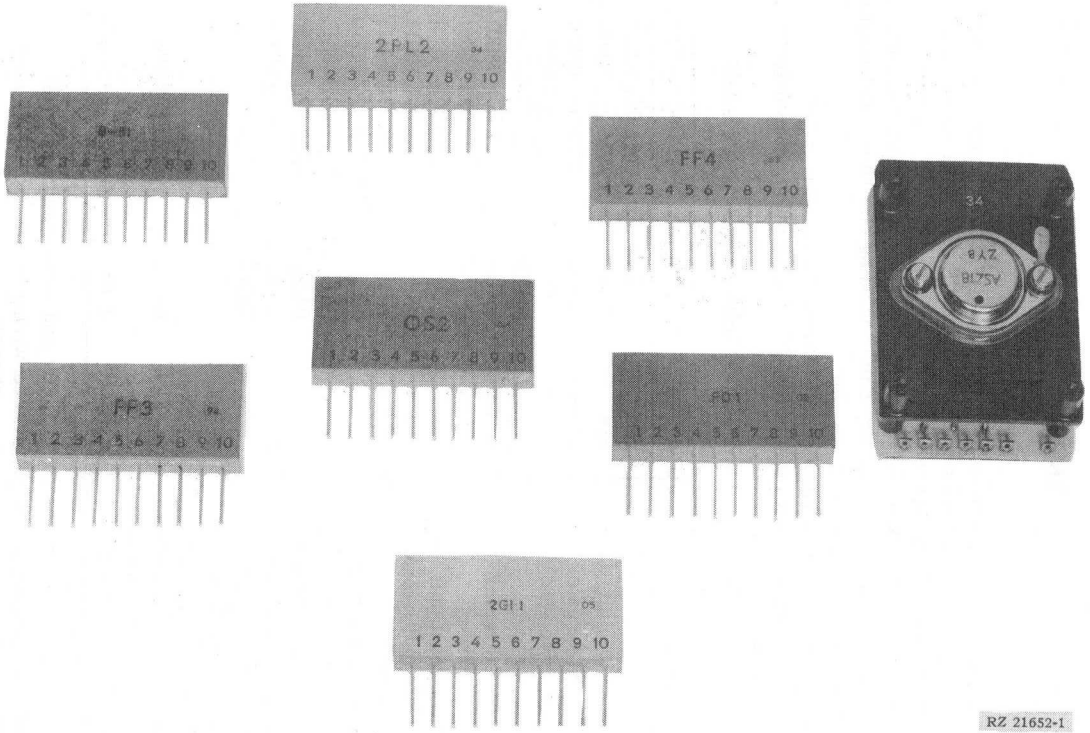
INTRODUCTION

The 1-Series of circuit blocks presents a range of logic circuits to be applied in general purpose and special purpose data handling systems as well as for industrial measuring and instrumentation.
The 1-Series offers a complete range consisting of various logic elements together with all necessary auxiliary units including one-shot multivibrator, input and output devices, pulse shapers, etc.
Frequently occurring functions such as counters, shift registers, numerical indicator tube drivers, etc. can be supplied ready made, assembled on printed-wiring boards.
In this series the following units and assembled panels are available:

description	colour	abbreviation	catalog number	page
Flip-flop	red	FF3	2722 001 00021	B15
Flip-flop	red	FF4	2722 001 00031	B19
Dual negative gate	orange	2.3N1	2722 001 01001	B23
Dual negative gate	orange	2.2N1	2722 001 01011	B25
Dual pulse logic	orange	2.PL2	2722 001 03011	B27
Dual gate inverter	yellow	2.GI1	2722 001 08001	B31
Pulse shaper	green	PS2	2722 001 11011	B49
Positive reset unit	blue	PR1	2722 001 22001	B55
One-shot multivibrator	green	OS2	2722 001 10011	B59
Pulse driver	green	PD1	2722 001 13011	B65
Printed-wiring board		PDA1	4322 026 34710	B109
Power amplifier		PA1	2722 032 00011	B71
Printed-wiring board		PAA1	4322 026 33630	B107
Dual decade counter		2.DCA2	2722 009 00011	B75
Reversible counter		BCA1	2722 009 00021	B81
Decade counter and numerical indicator tube driver assembly		DCA3	2722 009 00031	B87
Dual numerical indicator tube driver assembly		2.ID1	2722 009 05001	B95

Moreover all accessories for a quick and easy construction of equipment are available e.g. power supplies, printed-wiring boards, etc., see section "ACCESSORIES FOR CIRCUIT BLOCKS 1-SERIES".

In conjunction with 1-Series circuit blocks a number of static input and output devices can be used, see "INPUT/OUTPUT DEVICES".


2PL2
1 2 3 4 5 6 7 8 9 10
FF4
1 2 3 4 5 6 7 8 9 10
34
FF3
1 2 3 4 5 6 7 8 9 10
OS2
1 2 3 4 5 6 7 8 9 10
FD1
1 2 3 4 5 6 7 8 9 10
2GI1
1 2 3 4 5 6 7 8 9 10

RZ 21652-1

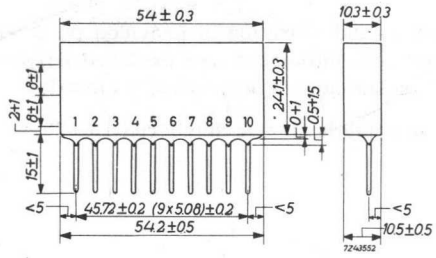
Easy-to-use loading table and simple loading rules, particularly for mixed loads, enables the system design to be completed quickly. Due to the fact that driven blocks only represent a load in the conducting state of the driving transistor, the required input d.c.- and transient currents of driven blocks are additive.

All circuits are compatible with little circuit diversity permitting simple and direct interconnections of the blocks within the range.

Input- and output currents of the blocks are designed in a way that external components are unnecessary with the exception of diodes.

The uniformity of the terminal location reduces the time for interwiring the blocks and facilitates the design of printed-wiring boards.

CONSTRUCTION

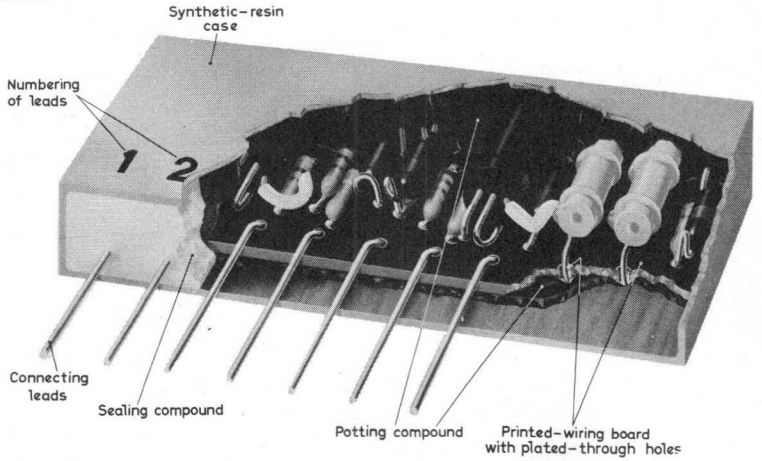


Weight:
approximately 20 g

Dimensional drawing of the circuit block

The dimensions of all 1-Series circuit blocks are approximately 54 mm x 24 mm x 11 mm. Out of one side of 54 mm x 11 mm emerge ten wire terminals of 0.7 mm diameter and 15 mm length. The distances between the wires are 5.08 mm (0.2 in) in accordance with the I.E.C. standard hole grid for printed-wiring boards.

The blocks are colour-coded, a different colour being used for each group of functions.



Cut-away view of a circuit block

The construction of a 1-Series circuit block can easily be seen in the cut-away view.

The electronic components, of which the circuit is made up (transistors, diodes, resistors, capacitors) are mounted on a printed-wiring board. This board is provided with plated-through holes to ensure reliable joints due to the large contact area of soldered contacts. The connecting leads are also mounted on the printed-wiring board.

Protection against mechanical shock and vibration is provided by the resilient potting compound, whilst atmospheric influences are excluded by the sealing compound, by which the synthetic resin case is hermetically closed.

For the sake of reference the connecting leads are numbered 1 to 10.

CHARACTERISTICS

For all circuit blocks the following temperature range is specified:

Operating	−20 to +60 °C
Storage	−25 to +75 °C

The maximum pulse repetition frequency is 100 kHz for triggered logic applications.

The standard power supply voltages are

$+6\ V \pm 5\ \% (V_p)$ and $-6\ V \pm 5\ \% (V_N)$

The power dissipation of the blocks is 20 to 100 mW.

Logic levels:

binary "1"	max.	V_N
	min.	$0.7\ V_N$
binary "0"	max.	−0.2 V
	min.	0 V

The general logic functions AND, OR, NOT and MEMORY can be performed with the two basic units of the range, viz. the gate inverter and the flip-flop respectively.

TEST SPECIFICATIONS

Before and during manufacture samples of circuit blocks are regularly subjected to the following tests.

(1) Shock test and vibration test according to method 202A and 201A of MIL-STD-202, terminals tested on strength, tests on mounting, soldering, lacquer and coding.

(2) Corrosion test (salt haze), according to method 101A of MIL-STD-202 (condition B, 48 hours).

(3) Temperature cycling test, according to method 102A of MIL-STD-202 (5 cycles from $-25\ ^{o}C$ to $+65\ ^{o}C$).

(4) Dip test, according to method 104A of MIL-STD-202 (2 cycles $65\ ^{o}C/20\ ^{o}C$, condition B, NaCl).

(5) Accelerated humidity test, according to method 106A of MIL-STD-202 (10 cycles $65\ ^{o}C$).

(6) Long-term humidity test (units not operating), according to I.E.C. 68, C IV ($40\ ^{o}C$, relative humidity 90% to 95%, duration longer than 2000 hours, functional marginal measurements after 250, 1000 etc. hours).

(7) As item 6, but units operating under the most unfavourable electrical conditions.

(8) Long-term test at maximum temperature ($60\ ^{o}C$), units operating under the most unfavourable electrical conditions. Duration and measurements as item 6.

INPUT AND OUTPUT DATA

INPUT DATA

unit	terminal	note	d.c. current (mA)	transient load (mA)
FF3	A_1 or A_2		0.88	4.0
	A_1 + A_2		1.75	4.5
	W	see note a	0.9	
FF4	G_1 or G_2	to open gate gate open	 1.75	1.6
	A	one gate closed both gates closed	1.75 1.75	4.5 1.0
	W	see note a	0.9	
2.PL2	G_1 or G_2	to open gate gate open	 1.75	1.6
	A_1 or A_2	gate open gate closed	0.88 0.88	4.0 0.5
2.GI1	EG	via diode OA95	1.0	3.0
2.2N1/ 2.3N1	W	see note b	0.52	0.37
OS2	A		1.3	1.4
PD1	A		1.7	1.5
	G	to open gate gate open	 1.75	1.2
PR1	W		0.1	0.08
PS2	W		0.7	0.75
PA1	W		2.5	1.3

Notes

a. Only to be driven by PR 1 via a diode OA 85/OA 95.

b. The input requirements also hold for the preset switches 1248 N (catalog number 4311 027 82221) and 1242 N (catalog number 4311 027 82211).

OUTPUT DATA

unit	terminal	note		d.c. current (mA)	transient load (mA)
FF3, FF4	Q			6	14
GI 1	Q	preceded by	AND	15	9
			AND - AND	8	4.5
			AND - OR	8	4.5
GI 1 - GI 1	Q	preceded by	AND - AND	25	22.5
			AND - OR	25	22.5
		connected as	set-reset FF	9	9
			non-inverting ampl.	40	27
			relay driver	65	
OS2	Q_1			18	25
	Q_2			6	21
PD1	Q			65	90
PS2	Q			20	13.7
PR1	Q			15	
		terminals 3 and 4 interconnected		30	
		terminals 5 and 4 interconnected		40	
PA1	Q			600	

Note

For driving the numerical indicator tubes ZM 1000, ZM 1020, ZM 1040 or ZM 1080 two assembled printed-wiring boards, 2.ID 1 and DCA 3, are available. The input requirements are specified in the individual sheets.

LOADING RULES

1. Verify that the sum of the required d.c. input currents of the driven units does not exceed the available d.c. output current of the driving unit.
2. When however, A-inputs are incorporated in the driven units, the transient loads must also be verified.
3. The verifications mentioned above hold for operations at the worst combination of supply voltage tolerances (6 V ±5 %) and ambient temperature between −20 °C and +60 °C.
4. W-inputs of FF3 and FF4 are to be used as extension inputs for the 2.PL2 and for positive-reset. For the latter purpose the positive reset unit PR1, designed for various loadings and driver circuits can be used.

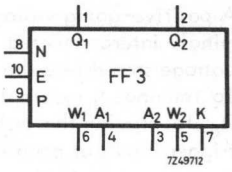
FLIP-FLOP

Colour: red

The unit FF3 contains a transistor bi-stable multivibrator circuit. The transistors are medium-speed switching types.

The circuit constitutes a memory function when driven by means of a d.c. level or a positive-going trigger signal, and it can also be used as a binary scale-of-two when the trigger inputs are interconnected.

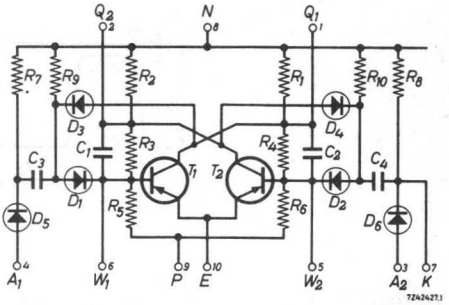
Frequency range	:	0 - 100 kHz
Ambient temperature range:		-20 to +60 °C
Weight	:	approx. 20 g



Drawing symbol

CIRCUIT DATA

Terminal



1 = Q_1 = output 1
2 = Q_2 = output 2
3 = A_2 = trigger input 2
4 = A_1 = trigger input 1
5 = W_2 = d.c. input 2
6 = W_1 = d.c. input 1
7 = K = terminal for external trigger input
8 = N = supply -6 V
9 = P = supply +6 V
10 = E = common supply 0 V

Power Supply

Terminal 8 : V_N = -6 V ± 5 %, $-I_N$ = 8.8 mA
9 : V_P = 6 V ± 5 %, I_P = 0.6 mA
} Nominal value of the current
10 : V_E = 0 V common

Notes

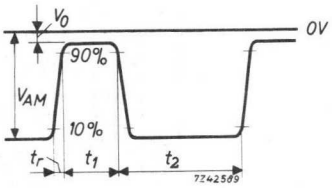
- The data given apply to the most adverse supply voltages for a combination of units, namely V_N=-5.7V and V_P=6.3V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input Signal Requirements

Trigger Input Signal (A terminals)

A positive-going voltage step is applied to terminal A_1 or A_2, or to both terminals interconnected in the case of binary scale-of-two applications. This voltage step drives the transistor T_1 (T_2) into the non-conducting state.
To terminal K external diodes can be connected (in the same sense as diode D_6) to provide the pulse-gate, corresponding with terminal A_2, with extra trigger inputs or condition inputs.



Voltage

V_{AM}	=	min.	-0.7	V_N
	=	max.	-	V_N
$-V_o$	=	min.	0	V
	=	max.	0.2	V

	A_1 or A_2	A_1 and A_2 interconnected
Required direct current	I_{AD} = min. 0.88 mA	min. 1.75 mA
Required current during the transient averaged over: 0.4 µs	I_{AT} = min. 5 mA	min. 6 mA
0.7 µs	= min. 4 mA	min. 4.5 mA

Rise time	t_r	=	max.	0.7 µs
Pulse duration	t_1	=	min.	1 µs
	t_2	=	min.	8 µs
Input noise level	V_n	=	max.	1 V peak to peak

DC Input Signal (W terminals)

A d.c. voltage level is applied to terminal W_1 or W_2. A positive voltage drives the transistor T_1 (T_2) into the non-conducting state and a negative voltage drives it into the conducting state

Transistor conducting				
Current	$-I_W$	=	min.	0.6 mA ($-V_W$ = max. 0.4 V)
limiting value		=	max.	15 mA
Transistor non-conducting				
Voltage	V_W	=	min.	0.2 V
limiting value		=	max.	10 V
Current	I_W	=	min.	0.9 mA

OUTPUT DATA

Voltages and currents

Transistor conducting

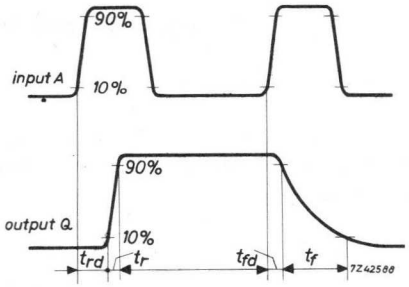
Voltage	$-V_Q$	=	max.	0.2 V
Available direct current	$-I_{QD}$	=	max.	6 mA
Available current during the transient				
averaged over: 0.4 µs	$-I_{QT}$	=	max.	11 mA
0.7 µs		=	max.	14 mA

Transistor non-conducting

Voltage	$-V_Q$	=	min.	$-0.7 \cdot V_N$
Available direct current	I_{QD}	=	max.	0.7 mA

Switching and delay times

These data are for orientation only and refer to an input signal as specified under INPUT DATA.



		Unit unloaded	Unit max. loaded
Rise delay	t_{rd}	= max. 1.0 µs	max. 1.1 µs
Rise time	t_r	= max. 0.3 µs	max. 0.7 µs
Fall delay	t_{fd}	= max. 0.8 µs	max. 0.8 µs
Fall time	t_f	= max. 1.7 µs	max. 1.7 µs

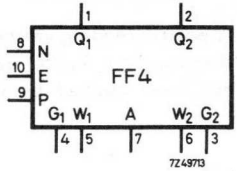
FLIP-FLOP

Colour: red

The unit FF4 contains a transistor bi-stable multivibrator circuit. The transistors are medium-speed switching types.

The circuit constitutes a memory function when driven by means of a d.c. level or a positive-going trigger signal. In the case of trigger drive, the switching of the flip-flop can be controlled by a d.c. level applied to the built-in gate circuits (e.g. in shift registers).

Frequency range	: see INPUT DATA
Ambient temperature range	: -20 to +60 °C
Weight	: approx. 20 g

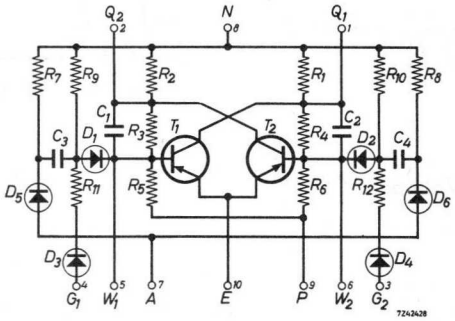


Drawing symbol

CIRCUIT DATA

Terminal

1 = Q_1 = output 1
2 = Q_2 = output 2
3 = G_2 = gate input 2
4 = G_1 = gate input 1
5 = W_1 = d.c. input 1
6 = W_2 = d.c. input 2
7 = A = trigger input
8 = N = supply -6 V
9 = P = supply +6 V
10 = E = common supply 0 V



Power Supply

Terminal 8 : V_N = -6 V ± 5 %, $-I_N$ = 8.8 mA } Nominal value
9 : V_P = +6 V ± 5 %, I_P = 0.6 mA } of the current
10 : V_E = 0 V common

Notes

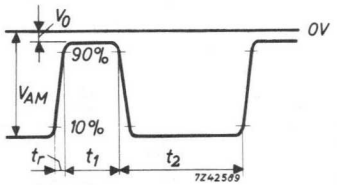
- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N = -5.7$ V and $V_P = 6.3$ V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input Signal Requirements

Trigger Input Signal (A terminal)

A positive-going voltage step is applied to terminal A. This voltage step drives the transistor $T_1(T_2)$ into the non-conducting state if the corresponding gate has been opened by an appropriate gate input signal on terminal $G_1(G_2)$.



Voltage	V_{AM}	= min.	-0.7	V_N
		max.	-	V_N
	$-V_o$	= min.	0	V
		max.	0.2	V
Required direct current	I_{AD}	= min.	1.75	mA
Required current during the transient				
averaged over: 0.4 µs	I_{AT}	= min.	6	mA
0.7 µs		min.	4.5	mA
Rise time	t_r	= max.	0.7	µs
Pulse duration	t_1	= min.	3	µs
	t_2	= min.	11	µs
Input noise level	V_n	= max.	1 V peak to peak	

DC Input signal (W terminals)

A d.c. voltage level is applied to terminal W_1 or W_2. A positive voltage drives the transistor $T_1(T_2)$ into the non-conducting state and a negative voltage drives it into the conducting state.

Transistor conducting	
Current	$-I_W$ = min. 0.6 mA ($-V_W$ = max. 0.4 V)
limiting value	= max. 15 mA
Transistor non-conducting	
Voltage	V_W = min. 0.2 V
limiting value	= max. 10 V
Current	I_W = min. 0.9 mA

Gate Input Signal (G terminals)

A d.c. voltage level is applied to terminal $G_1(G_2)$. Transistor $T_1(T_2)$ is driven into the non-conducting state by the trigger input signal (A terminal) if the corresponding gate is opened by an appropriate gate input signal.

		gate open	gate closed
Voltage	$-V_G$	= min. 0 V	min. V_{AM}
		max. 0.2 V	max. - V_N
Required gate current caused by negative transient of V_{AM}	I_{GD}	= min. 1.75 mA	min. 1.2 mA

		to open gate	to close gate
Required average current during the positive transient of V_G	I_{GT}	= min. 1.6 mA	–
Gate setting time			
when the gate input level changes at random:	t_{GS}	= min. 17 µs	min. 25 µs
when the gate input level changes within 2 µs after the positive going edge of the trigger signal:	t_{GS}	= min. 11 µs	min. 11 µs

Note: The latter applies to a shift register configuration so that the max. shift frequency is approximately 70 kHz.

During triggering the G levels should not be at zero voltage level simultaneously.

The gate setting time is the required waiting time between the last G level change and the positive going edge of the trigger pulse.

OUTPUT DATA

Voltages and currents

Transistor conducting

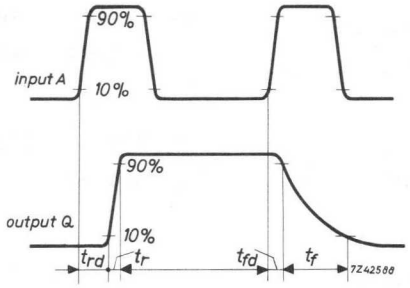
Voltage	$-V_Q$	= max.	0.2	V
Available direct current	$-I_{QD}$	= max.	6	mA
Available current during the transient				
averaged over: 0.4 µs	$-I_{QT}$	= max.	11	mA
0.7 µs		= max.	14	mA

Transistor non-conducting

Voltage	$-V_Q$	= min.	-0.7	V_N
Available direct current	I_{QD}	= max.	0.7	mA

Switching and delay times

These data are for orientation only and refer to an input signal as specified under INPUT DATA.



		Unit unloaded		Unit max. loaded	
Rise delay	t_{rd}	= max. 1.0	µs	max. 1.1	µs
Rise time	t_r	= max. 0.3	µs	max. 0.7	µs
Fall delay	t_{fd}	= max. 0.8	µs	max. 0.8	µs
Fall time	t_f	= max. 1.7	µs	max. 1.7	µs

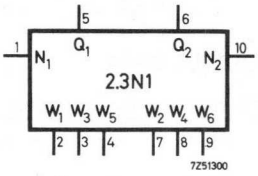
DUAL NEGATIVE GATE

Colour: orange

The unit 2.3N1 contains two three-input germanium-diode gates, that perform an AND logical operation on negative input-voltage signals.

The two gate circuits are identical and can be used separately or combined into a multiple-input gate by interconnecting the output terminals Q_1 and Q_2. In this latter case only one negative supply terminal should be used.

Pulse repetition frequency range:	0–100 kHz
Ambient temperature range:	−20 to +60 °C
Weight:	approx. 20 g

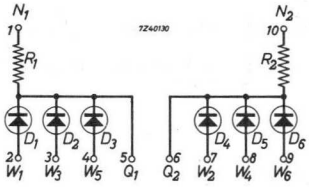


Drawing symbol

CIRCUIT DATA

Terminal

1 = N_1 = supply −6 V (1)
2 = W_1 = input 1
3 = W_3 = input 3
4 = W_5 = input 5
5 = Q_1 = output 1
6 = Q_2 = output 2
7 = W_2 = input 2
8 = W_4 = input 4
9 = W_6 = input 6
10 = N_2 = supply −6 V (2)



Power Supply

Terminal 1: $V_{N1} = -6V \pm 10\%$, $-I_{N1} = 0\text{-}0.5mA$ [1]) } Nominal value of the current
10: $V_{N2} = -6V \pm 10\%$, $-I_{N2} = 0\text{-}0.5mA$ [1]) }

INPUT DATA

Input Signal Requirements [2])

Voltage: Under all circumstances normally encountered when the unit is used in conjunction with other circuit blocks: $V_{Wn} = 0.1$ to $0.5V$ more positive than V_Q dependent on the input current I_{Wn}.

Current: To be supplied to terminal W_n having the least negative voltage level. For $V_{Wn} = 0$ volt and $I_Q = 0mA$: I_{Wn} = max. 0.48mA [1]) + max. 0.04mA [1]) for every W terminal at a negative voltage level.

OUTPUT DATA

Output Signal Characteristics [2])

Voltage: see INPUT DATA

Load current I_Q = max. $\frac{-V_N + V_Q}{13}$ mA [1])

Output Impedance

When V_Q is positive-going, the output impedance approximates the output impedance of the driving circuit. When V_Q is negative-going, the output impedance is max. 13kΩ.

LIMITING VALUES

Current through conducting diode I_{Wc} = max. 10mA

Voltage between terminals N and W = max. 30V

[1]) The sign is positive when the current flows towards the circuit.

[2]) These data apply to the most adverse working condition for a combination of units, namely to a supply voltage $V_N = -5.4V$. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

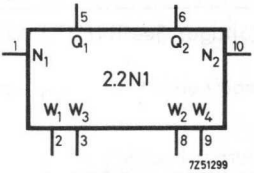
DUAL NEGATIVE GATE

Colour: orange

The unit 2.2N 1 contains two two-input germanium-diode gates that perform an AND logical operation on negative input voltage signals.

The two gate circuits are identical and can be used separately or combined into a multiple-input gate by interconnecting the output terminals Q_1 and Q_2. In this latter case, only one negative supply terminal should be used.

Pulse repetition frequency range:	0–100 kHz
Ambient temperature range:	−20 to +60 °C
Weight:	approx. 20 g

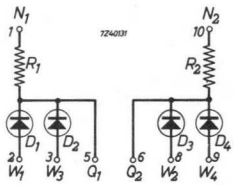


Drawing symbol

CIRCUIT DATA

Terminal

1 = N_1 = supply −6 V (1)
2 = W_1 = input 1
3 = W_3 = input 3
4 = not connected
5 = Q_1 = output 1
6 = Q_2 = output 2
7 = not connected
8 = W_2 = input 2
9 = W_4 = input 4
10 = N_2 = supply −6 V (2)



Power Supply

Terminal 1: $V_{N1} = -6\,V \pm 10\%$, $-I_{N1} = 0\text{–}0.5\,mA$ [1]) } Nominal value of the current

10: $V_{N2} = -6\,V \pm 10\%$, $-I_{N2} = 0\text{–}0{,}5\,mA$ [1]) } Nominal value of the current

[1]) The sign is positive when the current flows towards the circuit.

INPUT DATA

Input Signal Requirements [2])

Voltage: Under all circumstances normally encountered when the unit is used in conjunction with other circuit blocks: V_{Wn} = 0.1 to 0.5 V more positive than V_Q dependent on the input current I_{Wn}.

Current: To be supplied to terminal W_n having the least negative voltage level. For V_{Wn} = 0 volt and I_Q = 0 mA: I_{Wn} = max. 0.48 mA [1]) + max. 0.04 mA [1]) for every W terminal at a negative voltage level.

OUTPUT DATA

Output Signal Characteristics [2])

Voltage: See INPUT DATA

Load current $I_Q = \text{max.} \frac{-V_N + V_Q}{13}$ mA [1])

Output Impedance

When V_Q is positive-going, the output impedance approximates the output impedance of the driving circuit. When V_Q is negative-going, the output impedance is max. 13 kΩ.

LIMITING VALUES

Current through conducting diode I_{Wc} = max. 10 mA

Voltage between terminals N and W = max. 30 V

[1]) The sign is positive when the current flows towards the circuit

[2]) These data apply to the most adverse working condition for a combination of units, namely to a supply voltage V_N = -5.4 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

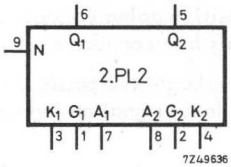
DUAL PULSE LOGIC

Colour: orange

The unit 2.PL2 contains two identical pulse gates which are controlled by a d.c. voltage level.

The circuits are normally used in conjunction with flip-flop circuits. With the dual pulse logic a second pair of a.c. inputs are formed for a flip-flop FF3, or in combination with flip-flops FF4 a bi-directional shift register can be made. In these applications the 2.PL2 output terminals are to be connected directly to the flip-flop d.c. input terminals.

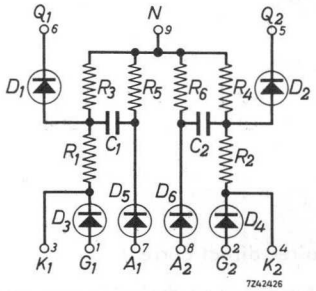
Frequency range	: see INPUT DATA
Ambient temperature range	: -20 to +60 °C
Weight	: approx. 20 g



Drawing symbol

CIRCUIT DATA

Terminal 1 = G_1 = gate input 1
2 = G_2 = gate input 2
3 = K_1 = terminal for external gate input
4 = K_2 = terminal for external gate input
5 = Q_2 = output 2
6 = Q_1 = output 1
7 = A_1 = trigger input 1
8 = A_2 = trigger input 2
9 = N = supply -6 V
10 = not connected



Power Supply

Terminal 9 : V_N = -6 V ± 5 %, $-I_N$ = 0-2.5 mA Nominal value of the current

Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely V_N=-5.7V and V_P=6.3V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

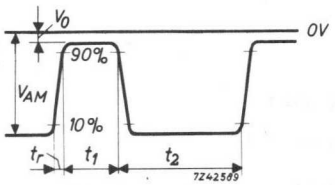
These data are dependent on the driven circuit, the values given apply to use of the dual pulse logic in conjunction with flip-flops FF3 or FF4.

Input Signal Requirements

Trigger Input Signal (A terminals)

A positive going voltage step is applied to terminal A_1 or A_2 or to both terminals interconnected.

This voltage step passes the pulse gate if it has been opened by an appropriate gate input signal on terminal G_1(G_2).



		A_1 or A_2	A_1 and A_2 interconnected
Voltage	V_{AM} = min.	-0.7 V_N	
	= max.	- V_N	
	$-V_o$ = min.	0 V	
	= max.	0.2 V	
Required direct current	I_{AD} = min.	0.88 mA	min. 1.75 mA
Required current during the transient			
averaged over: 0.4 µs	I_{AT} = min.	5 mA	min. 6 mA
0.7 µs	= min.	4 mA	min. 4.5 mA

Rise time	t_r	= max. 0.7	µs
Pulse duration	t_1	= min. 3	µs
	t_2	= min. 11	µs
Input noise level	V_n	= max. 1	V peak to peak

Gate Input Signal (G terminals)

A d.c. voltage level is applied to terminal G_1 (G_2).

The trigger input signal (terminal A_1(A_2) passes if the corresponding gate is opened by an appropriate gate input signal.

To terminal K_1(K_2) external diodes can be connected (in the same sense as diode D_3(D_4)), to provide the corresponding pulse gate with extra condition inputs.

		gate open	gate closed
Voltage	$-V_G$	= min. 0 V	min. V_{AM}
		= max. 0.2 V	max. - V_N
Required gate current caused by negative transient of V_{AM}	I_{GT}	= min. 1.75 mA	min. 1.2 mA
		to open gate	to close gate
Required average current during the positive transient of V_G	I_{GT}	= min. 1.6 mA	
Gate setting time			
when the gate input level changes at random	t_{GS}	= min. 17 µs	min. 25 µs
when the gate input level changes within 2 µs after the positive going edge of the trigger signal	t_{GS}	= min. 11 µs	min. 11 µs

Note: The latter applies to a shift register configuration so that the max. shift frequency is approximately 70 kHz

During triggering the G levels should not be at zero voltage level simultaneously.

The gate setting time is the required waiting time between the last G level change and the positive going edge of the trigger pulse.

OUTPUT DATA

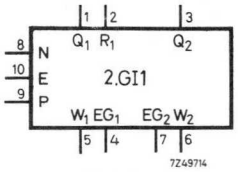
When used in conjunction with flip-flops FF3 and FF4, the output terminals (Q_1 and Q_2) are directly connected to the flip-flop d.c. input terminals (W_1 and W_2).

DUAL GATE INVERTER

The 2.GI 1 is to be considered as the back bone of the 1-Series circuit blocks with which all logic configurations can be realised. Moreover the 2.GI 1 can perform other important functions which are specified below.

The unit 2.GI 1 contains two gate inverter circuits; the terminals W and EG have normally to be interconnected externally. The gating function is obtained by connecting diodes externally to the terminal EG.
The circuit performs a NAND function on the negative high level. The terminals R_1 and Q_1 are normally interconnected.
When collector-OR logic is employed, terminal R_1 can be left floating. The logic operation is performed by connecting both collectors Q to the collector resistor of TR_2. Herewith the AND-OR operation can be obtained. Up to four collectors may be interconnected with one collector resistor.
The inverter circuits can also be preceded by a double diode logic configuration to perform the AND-AND as well as the Factored-AND operation. For these applications a VDR, asymmetric type 2322 574 90007 has to be connected externally between the terminals W and EG; the gating diodes are to be connected to terminal EG. Furthermore the following major functions can be realised as well:

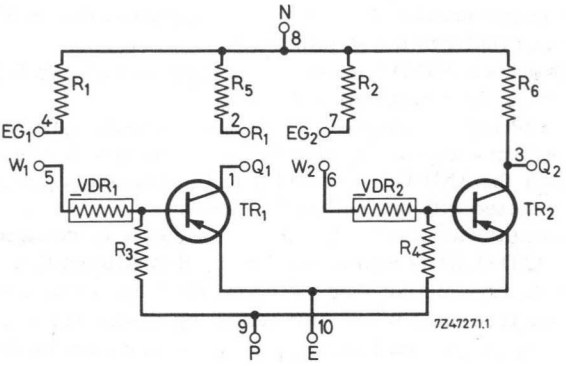
- a set-reset flip-flop by cross-connecting the inputs and outputs of both gate inverter circuits via diodes type OA85/OA95, to be mounted externally
- a non-inverting amplifier with increased output loadability
- a relay driver, by interconnecting the two inverter circuits in series.



Drawing symbol

CIRCUIT DATA

Terminal
1 = Q_1 = output 1
2 = R_1 = connection collector resistor
3 = Q_2 = output 2
4 = EG_1 = extension gate input 1
5 = W_1 = d.c. input 1
6 = W_2 = d.c. input 2
7 = EG_2 = extension gate input 2
8 = N = supply −6 V
9 = P = supply +6 V
10 = E = common supply 0 V



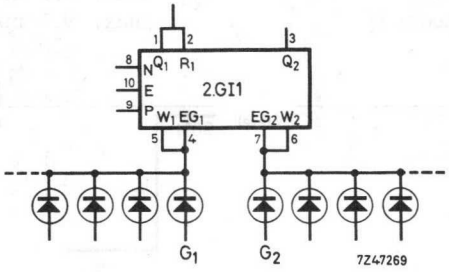
Power supply

Terminal 8 : V_N = −6 V ± 5 %
9 : V_P = +6 V ± 5 %
10 : V_E = 0 V common

$-I_N$ = 2 to 4.2 mA } nominal value
I_P = 0.22 mA } of the current

Notes
- The data given apply to the most adverse supply voltages for a combination of units, namely V_N = −5.7 V and V_P = 6.3 V.
- The temperatures −20 °C and +60 °C and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

DUAL NAND or DUAL NOR



Circuit diagram with interconnections to be made externally

Input requirements

Input at G:

Transistor conducting	(output level "negative low")	
Voltage	$-V_G$ = min.	-0.7 V_N
	max.	$-V_N$
Transistor non-conducting	(output level "negative high")	
Voltage	$-V_G$ = min.	0 V
	max.	0.2 V
Required direct current	I_{GD} = min.	1 mA
Required transient current averaged over 0.7 μs	I_{GT} = min.	3 mA

Type of diodes and maximum number connected in parallel at terminals EG: 11 x OA85/OA95.

Output data

Transistor non-conducting	(output level "negative high")	
Voltage	$-V_Q$ = approx.	V_N
Transistor conducting	(output level "negative low")	
Voltage	$-V_Q$ = min.	0 V
	max.	0.2 V

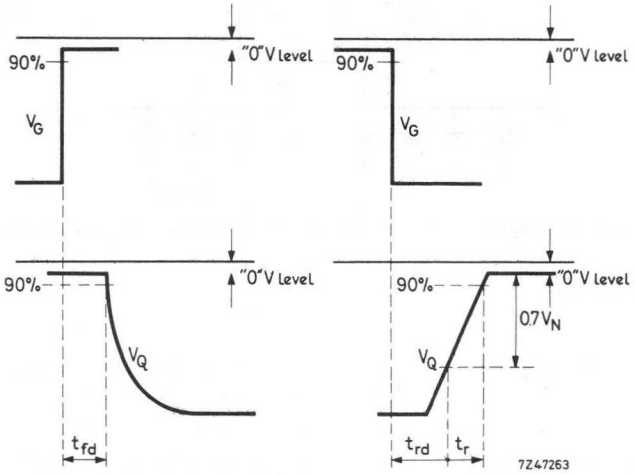
Available direct current

R connected to Q	$-I_{QD}$ = max.	15 mA
in collector-OR configuration	max.	10 mA
R not connected to Q	max.	11.3 mA

Available transient current averaged over 0.7 μs

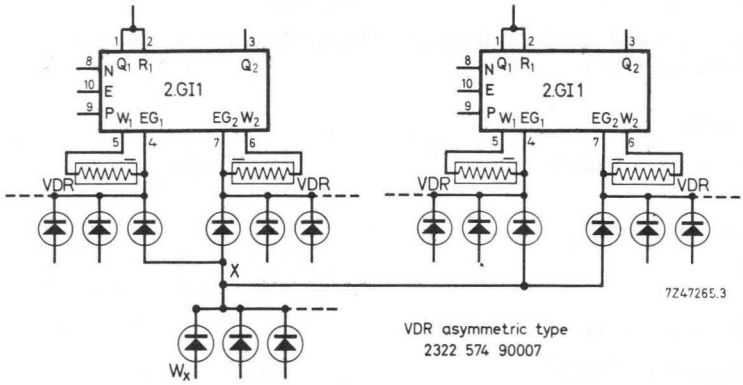
R connected to Q	$-I_{QT}$ = max.	9.0 mA
R not connected to Q	max.	9.7 mA

Time data



For further data see Table 2, page B48

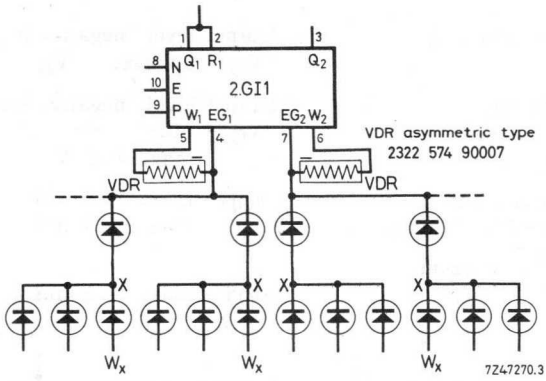
FACTORED-AND-GI



Circuit diagram with interconnections to be made externally

4 separate GI circuits, each which may have 10 input diodes in parallel, may be driven simultaneously by a gate with 10 diodes in parallel.
A gate resistor between point X and V_N decreases the rise delay time t_{rd} (see Time data under AND-AND-GI)

AND-AND-GI



Circuit diagram with interconnections to be made externally

To each EG terminal 25 parallel input diodes may be connected. Each of these input diodes may be driven by a gate with 10 input diodes in parallel.
A gate resistor between points X and V_N decreases the rise delay time t_{rd} (see Time data)

Input requirements

Input at terminals W_X:

Transistor conducting (all terminals W_X at "negative high" level)

Voltage	$-V_{WX}$ = min.	-0.7 V_N
	max.	$-V_N$

Transistor non-conducting (one of the terminals W_X at "0" V level)

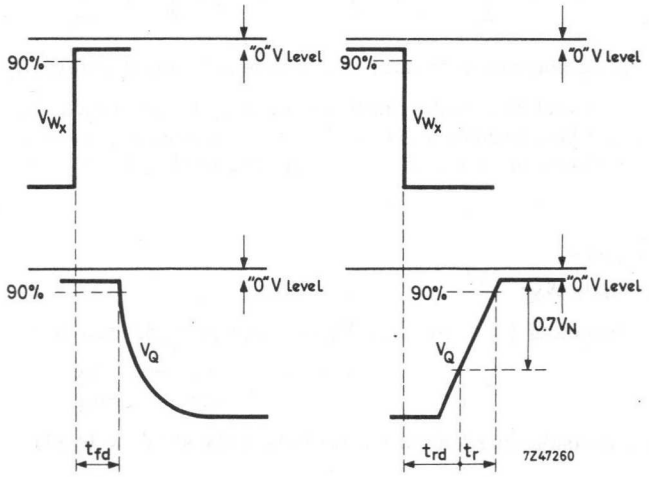
Voltage	$-V_{WX}$ = min.	0 V
	max.	0.2 V
Required direct current	Sum of GI d.c. input currents [1]	
Required transient current averaged over 0.7 μs	Sum of GI transient input currents [2]	

[1]) When a gate resistor between point X and V_N is used, the negative gate input current has to be added.

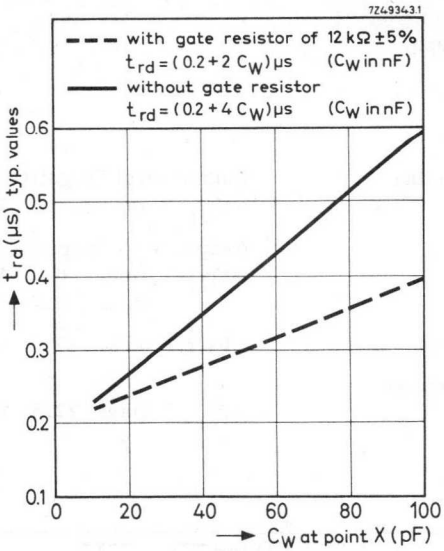
[2]) When a gate resistor is used, 0.7 x d.c. input current of the negative gate has to be added.

Output data

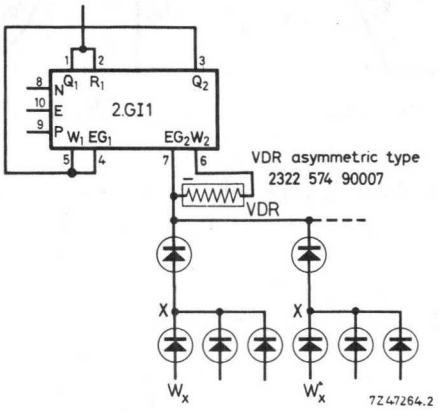
Transistor non-conducting Voltage	(output level "negative high") $-V_Q$ = approx. V_N
Transistor conducting Voltage	(output level "negative low") $-V_Q$ = min. 0 V max. 0.2 V
Available direct current in collector - OR configuration	$-I_{QD}$ = max. 8 mA max. 4.5 mA
Available transient current averaged over 0.7 μs	$-I_{QT}$ = max. 4.5 mA



For further data see Table 2, page B48.



AND-AND-GI-GI



Circuit diagram with interconnections to be made externally

When AND-AND or Factored-AND is employed and Q_2 is connected to EG_1 an increased loadability can be obtained from Q_1. The output voltage at Q_1 is not inverted with respect to the input voltage at W_X.
A gate resistor between points X and V_N decreases the fall delay time t_{fd} (see Time data).

Input requirements

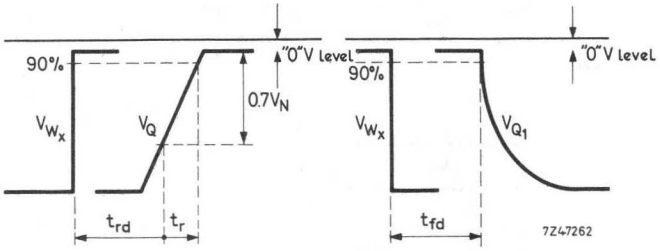
See preceding paragraph.

Output data

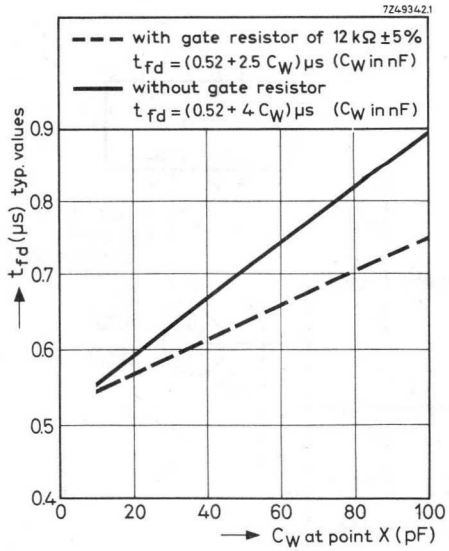
Output Q_1

Transistor non-conducting	(output level "negative high")		
Voltage	$-V_{Q_1}$ = approx.	V_N	
Transistor conducting	(output level "negative low")		
Voltage	$-V_{Q_1}$ = min.	0	V
	max.	0.2	V
Available direct current	$-I_{Q_1D}$ = max.	25	mA
Available transient current averaged over 0.7 μs	$-I_{Q_1T}$ = max.	22.5	mA

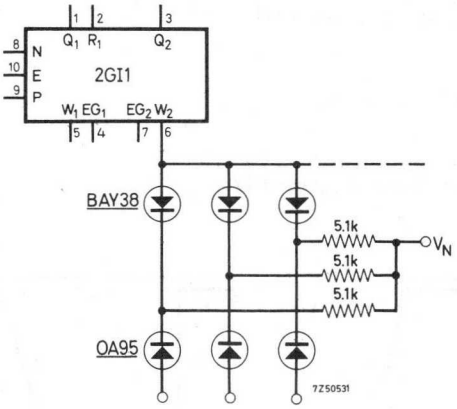
Time data



For further data see Table 2, page B48.



AND-OR-GI (1)



Used where long switching delays can be tolerated.

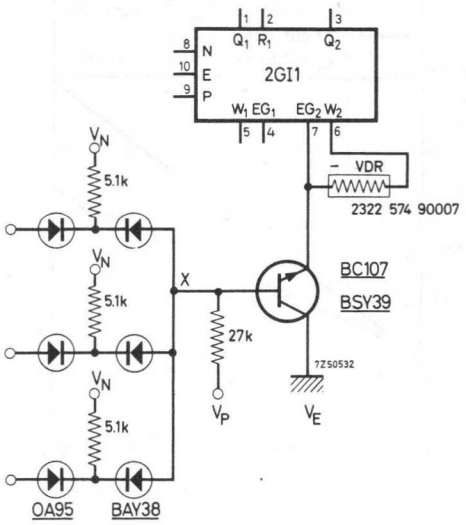
Input requirements

See DUAL NAND or DUAL NOR.

Output data

See AND-AND-GI and Table 1, page B47.
For time data see Table 2, page B48.

AND-OR-GI (2)



Used where short delays are essential.

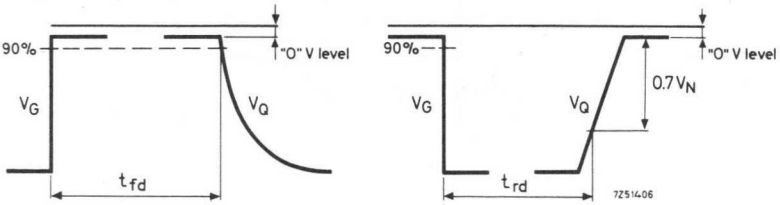
Input data

See DUAL NAND or DUAL NOR.

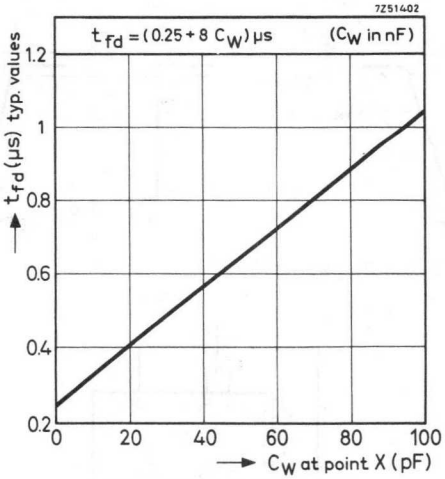
Output data

See AND-AND-GI and Table 1, page B47.

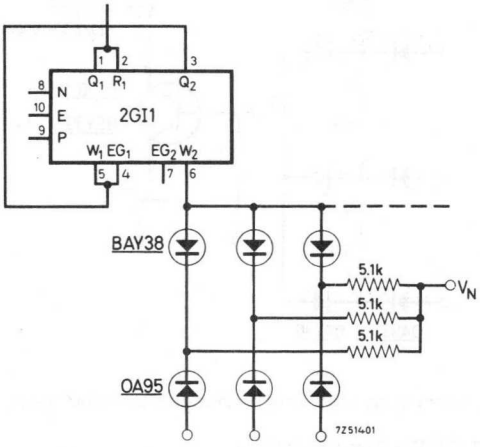
Time data



For further data see Table 2, page B48.



AND-OR-GI-GI (1)



Circuit diagram with interconnections to be made externally

Used where long switching delays are tolerated.

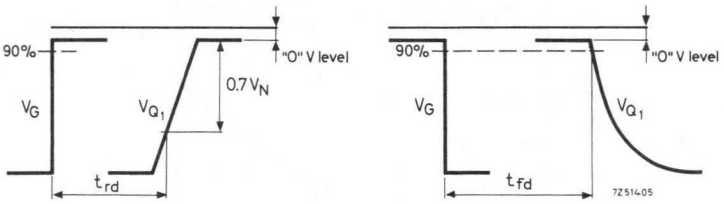
Input requirements

See DUAL NAND or DUAL NOR.

Output data

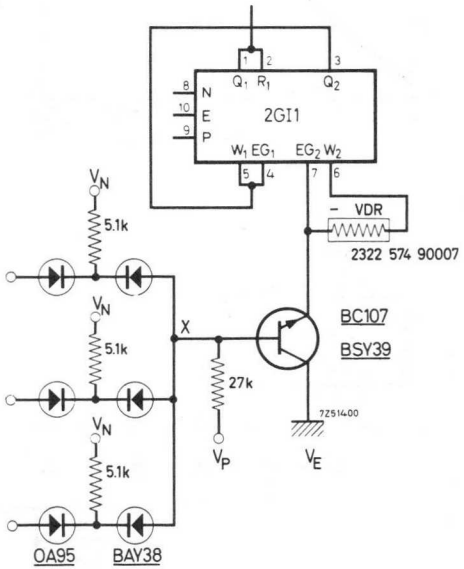
See AND-AND-GI-GI.

Time data



For further data see Table 2, page B48.

AND-OR-GI-GI (2)



Circuit diagram with interconnections to be made externally

Used where short delays are essential.

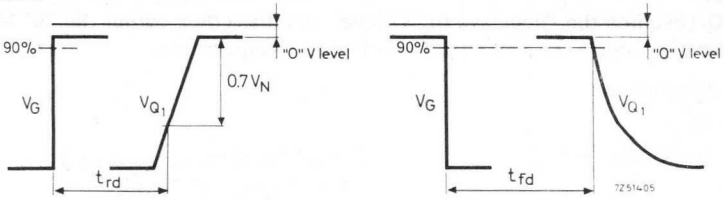
Input requirements

See DUAL NAND or DUAL NOR.

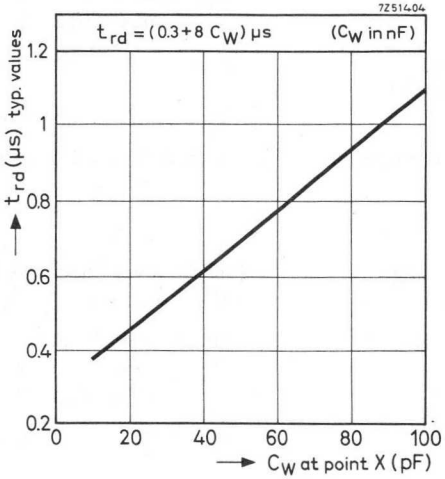
Output data

See AND-AND-GI-GI.

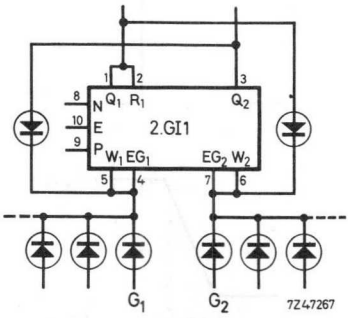
Time data



For further data see Table 2, page B48.



SET-RESET FLIP-FLOP



Circuit diagram with interconnections to be made externally

Upon application of the "0" V level to one of the diode inputs, the corresponding output Q resumes the "negative high" level, and the other output the "0" V level. The "negative high" level applied to an input is inoperative.

Input requirements

Input at G:

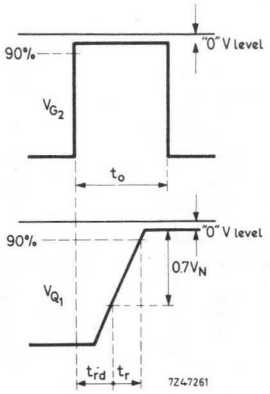
Transistor conducting	(output level "negative low")			
Voltage	$-V_G$	= min.	-0.7	V_N
		max.		$-V_N$
Transistor non-conducting	(output level "negative high")			
Voltage	$-V_G$	= min.	0	V
		max.	0.2	V
Required direct current	I_{GD}	= min.	1	mA
Required transient current averaged over 0.7 μs	I_{GT}	= min.	3	mA

Type of diodes and maximum number connected in parallel at terminal EG: 10 x OA85/OA95.

Output data

Transistor non-conducting	(output level "negative high")			
Voltage	$-V_Q$	= approx.		V_N
Transistor conducting	(output level "negative low")			
Voltage	$-V_Q$	= min.	0	V
		max.	0.2	V
Available direct current	$-I_{QD}$	= max.	9	mA
Available transient current averaged over 0.7 μs	$-I_{QT}$	= max.	9	mA

Time data



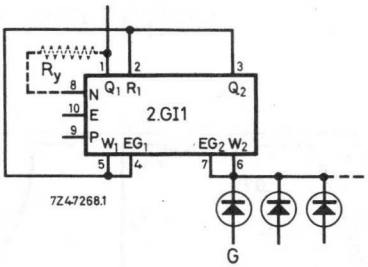
t_{rd} = typ. 0.5 μs (delay from G_2 to Q_1, or G_1 to Q_2, with a square wave input signal)

t_r = max. 0.7 μs (at maximum transient load e.g. 3 x GI1 or 2 FF3/FF4)

= max. 1.5 μs (loaded with 9 x GI1)

t_o = min. 2 μs

NON-INVERTING AMPLIFIER or RELAY DRIVER



Circuit diagram with interconnections to be made externally

When used as non-inverting amplifier an external resistor R_y = 2.2 k$\Omega \pm 2$ % is needed between Q_1 and V_N.

Input requirements

Input at G:

Output transistor non-conducting	(output level "negative high")
Voltage	$-V_G$ = min. 0.7 V_N
	max. - V_N
Transistor conducting	(output level "negative low")
Voltage	$-V_G$ = min. 0 V
	max. 0.2 V
Required direct current	I_{GD} = min. 1 mA
Required transient current averaged over 0.7 μs	I_{GT} = min. 3 mA

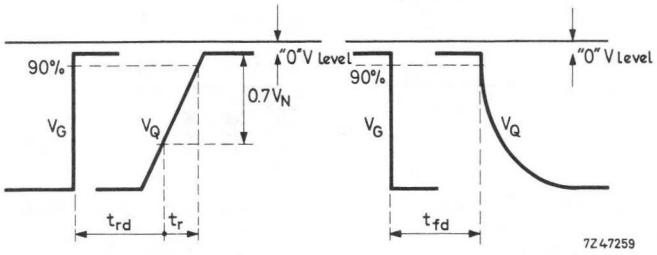
Type of diodes and maximum number connected in parallel at terminal EG: 11 x OA85/OA95.

Output data (as non-inverting amplifier)

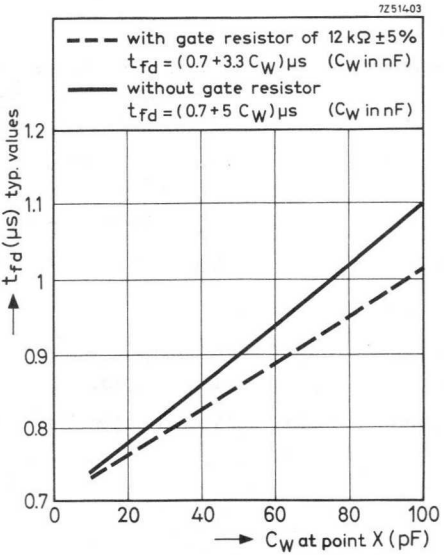
Output Q_1 :

Transistor non-conducting	(output level "negative high")			
Voltage	$-V_{Q_1}$	= approx.		V_N
Transistor conducting	(output level "negative low")			
Voltage	$-V_{Q_1}$	= min.	0	V
		max.	0.2	V
Available direct current	$-I_{Q_1D}$	= max.	40	mA
Available transient current averaged over 0.7 μs	$-I_{Q_1T}$	= max.	27	mA

Time data



For further data see Table 2, page B48.



Output data (as relay driver)

Output Q_1 :

Transistor non-conducting	(output level "negative high")
Voltage	$-V_{Q_1}$ = abs. max. 15 V
Transistor conducting	(output level "negative low")
Voltage	$-V_{Q_1}$ = min. 0 V
	max. 0.25 V
Available direct current	$-I_{Q_1D}$ = max. 65 mA

SURVEY OF OUTPUT DATA

Table 1

applied configuration	preceded by			
	AND		AND-AND Factored-AND AND-OR (1) AND-OR (2)	
	$-I_{QD}$ (mA)	$-I_{QT}$ (mA)	$-I_{QD}$ (mA)	$-I_{QT}$ (mA)
GI	15	9	8	4.5
GI-collector-OR	10	9	4.5	4.5
GI-GI	25	22.5	25	22.5
non-inverting amplifier	40	27	40	27

Table 2 SURVEY OF TIME DATA

applied configuration	preceded by	t_{fd}, typical values (μs)	t_{rd}, typical values (μs)	t_r max (μs)	
				at maximum d.c. load	at maximum transient load
GI	AND	0.3	0.2	1.5	1.5
	AND-AND Factored-AND	0.3	with gate resistor (0.2+2 C_w)	1.5	1.5
			without gate resistor (0.2+4 C_w)		
	AND-OR (1)	(2.5+0.4 n)	0.2	1.5	1.5
	AND-OR (2)	(0.25+8 C_w)	0.3	1.5	1.5
GI-collector-OR	AND	0.3	0.2	1.5	1.5
	AND-AND Factored-AND	0.3	with gate resistor (0.2+2 C_w)	1.5	1.5
			without gate resistor (0.2+4 C_w)		
GI-GI	AND	0.5	0.4	1.5	1.5
	AND-AND Factored-AND	with gate resistor (0.52+2.5 C_w)	0.3	1.5	1.5
		without gate resistor (0.52+4 C_w)			
	AND-OR (1)	0.5	(3+0.4 n)	1.5	1.5
	AND-OR (2)	0.7	(0.3+8 C_w)	1.5	1.5
non-inverting amplifier	AND	0.5	0.3	1.5	1.5
	AND-AND Factored-AND	with gate resistor (0.7+3.3 C_w)	0.3	1.5	1.5
		without gate resistor (0.7+5 C_w)			
	AND-OR (1)	0.6	(3+0.4 n)	1.5	1.5
	AND-OR (2)	0.7	(0.3+8 C_w)	1.5	1.5

Note n = number of inputs, switching from "1" to "0" level simultaneously. C_w in nF.

PULSE SHAPER

Colour : green

This unit contains a Schmitt trigger followed by an inverter amplifier. An input signal of a magnitude exceeding the thresholds (tripping levels) of the unit, is re-shaped and inverted into the standard d.c. level at the output. The output voltage transients are short and suitable for driving other circuit blocks at their trigger inputs (A).

The terminals A, W, X_1 and X_2 are provided in order to be able to use the PS 2 for the following purposes:

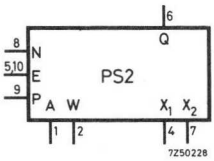
- as a pulse shaper, driven by an external source
- as a relaxation oscillator
- as a crystal controlled oscillator
- as a pulse shaper, driven by circuit blocks of the 100 kHz or 1-Series.

In the last application the number of inputs can be increased by connecting diodes type AAY 21/OA 85/OA 95 to the externally interconnected terminals A and W. The maximum number of diodes is 10.

Pulse repetition frequency range : 0 to 100 kHz

Ambient temperature range : −20 to +60 °C

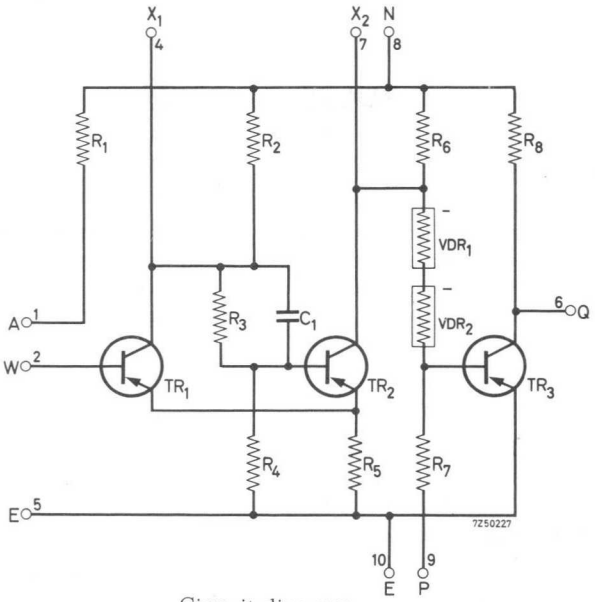
Weight : approx. 20 g



drawing symbol

CIRCUIT DATA

Terminal 1 = A = to be interconnected with terminal 2 for internal driving purposes
2 = W = input
3 = not connected
4 = X_1 = internally connected
5 = E = common supply 0 V (interconnected with terminal 10)
6 = Q = output
7 = X_2 = internally connected
8 = N = supply −6 V
9 = P = supply +6 V
10 = E = common supply 0 V



Circuit diagram

Power supply

Terminal 8 = V_N = −6 V ±5 %, $-I_N$ = 3.2 - 7.5 mA } nominal value
9 = V_P = +6 V ±5 %, I_P = 0.19 mA } of the current
10 = V_E = 0 V common

Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely V_N = −5.7 V and V_P = +6.3 V.
- The temperatures −20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Unit driven by a non-standard circuit (external source)

Internal resistance (R_i) of the driving circuit

R_i = max. 12 kΩ (T_{amb} = min. 0 °C)
R_i = max. 8 kΩ (T_{amb} = min. −20 °C)

Input voltage to be applied to terminal W:

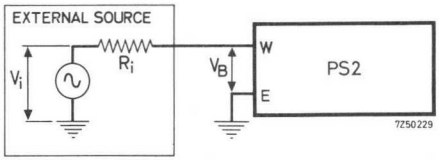
ON threshold (transistor TR_3 conducting)

	operating	limiting value
Voltage	$-V_W$ = min. −0.4 V_N	= −7.5 V
Current	$-I_W$ = max. 0.1 mA	= 15 mA

OFF threshold (transistor TR_3 non-conducting)

	operating	limiting value
Voltage	$-V_W$ = max. −0.17 V_N	= −10 V
Current	I_W = max. 0.05 mA (at $-V_W$ = 0.2 V)	
	= max. 0.1 mA (at V_W = 10 V)	

Hysteresis (difference between ON and OFF tripping levels)

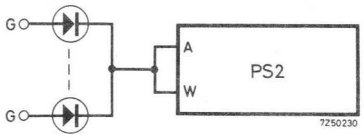


The hysteresis is affected by the internal resistance (R_i) of the driving circuit (external source). The relation is given by the following formula:

T_{amb} = min. 0 °C	T_{amb} = min. −20 °C
ΔV_i = min. (0.07 V_N − 0.033 R_i)	ΔV_i = min. 0.07 V_N − 0.05 R_i)
$\Delta V_B = \frac{\Delta V_i}{1 + 0.057\ R_i}$	$\Delta V_B = \frac{\Delta V_i}{1 + 0.071\ R_i}$

(R_i in kΩ and V in volt)

Unit driven by circuit blocks of the 1-Series



For this operation terminal A has to be connected to terminal W and the input voltage V_G has to be applied via a diode, type AAY 21/OA 85/OA 95. The maximum number of parallel diodes is 10.

Transistor TR_3 conducting (output level "negative low")

Voltage	$-V_G$	= max. $-V_N$ = min. $-0.7\ V_N$

Transistor TR_3 non-conducting (output level "negative high")

Voltage	$-V_G$	= min. 0 V = max. 0.2 V
Required direct current	I_{GD}	= max. 0.7 mA
Required transient current averaged over 0.4 μs averaged over 0.7 μs	I_{GT}	= max. 1.1 mA = max. 0.75 mA

OUTPUT DATA

Transistor TR_3 conducting (output level "negative low")

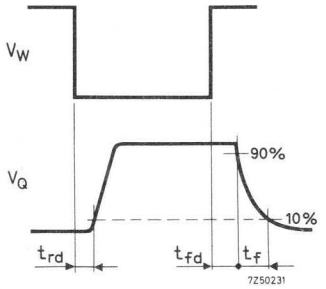
Voltage	$-V_Q$	= max. 0.2 V = min. 0 V
Available direct current	$-I_{QD}$	= max. 20 mA
Available transient current averaged over 0.4 μs averaged over 0.7 μs	$-I_{QT}$	= max. 8 mA = max. 13.7 mA

Transistor TR_3 non-conducting (output level "negative high")

Voltage	V_Q	= max. V_N
Current	I_{QD}	= max. 0.65 mA (at $V_Q = 0.7\ V_N$)

Switching and delay times (when unit is used in combination with 1-Series circuit blocks)

A square wave input signal is assumed with an amplitude of min. $-0.7\ V_N$



Unit fully loaded

Rise delay	t_{rd} = max. 0.7 μs
Fall delay	t_{fd} = max. 1.2 μs
Fall time	t_f = max. 0.7 μs

Note

- If for a particular application a capacitor is required between terminal W (2) and earth, use should be made of terminal 5 in order to avoid noise on the common earth point which could disturb the proper operation of the unit.

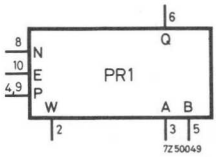
POSITIVE RESET UNIT

Colour: blue

This unit is intended for resetting purposes of flip-flops FF 1, FF 2, FF 3 and FF 4. When a "negative low" level is applied to the input terminal (W), the unit produces a positive reset signal at its output terminal (Q). The time, that the reset level will be present, is determined by the driving circuit.
In general a reset time of maximum 2 μs per flip-flop is required when a chain of flip-flops is to be reset.
Up to 15 flip-flops can be reset without external interconnections. By interconnecting the terminals A and P the maximum number of flip-flops that can be reset is 30; by interconnecting the terminals B and P maximum 40 flip-flops can be reset simultaneously.

To reset a flip-flop the output terminal (Q) of the PR1 has to be connected to an input terminal (W) of a flip-flop via a diode OA 85 or OA 95 (anode to Q).

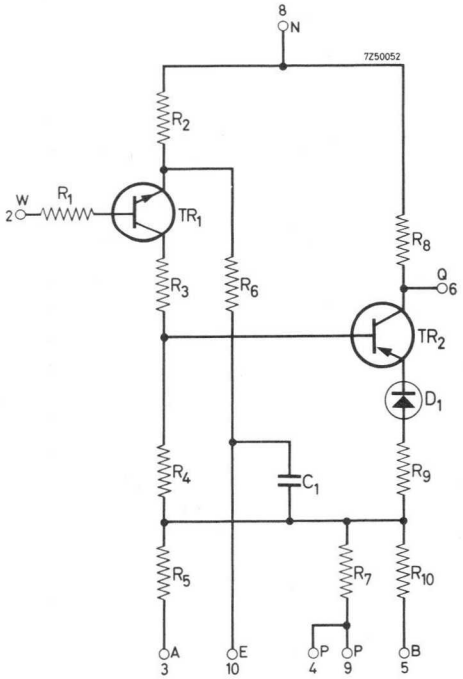
Ambient-temperature range	−20 to +60 °C
Weight	approx. 20 g



Drawing symbol

CIRCUIT DATA

Terminal 1 = not connected
2 = W = input
3 = A = to be interconnected with terminal 4 for resetting maximum 30 flip-flops
4 = P = supply + 6 V (internally connected to terminal 9)
5 = B = to be interconnected with terminal 4 for resetting maximum 40 flip-flops
6 = Q = output
7 = not connected
8 = N = supply −6 V
9 = P = supply +6 V
10 = E = common supply 0 V



Circuit diagram

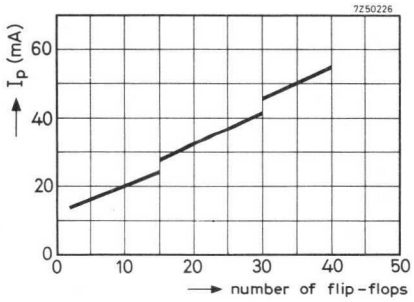
Power supply

Voltages

Terminal 8 : V_N = −6 V ± 5%
9 : V_P = +6 V ± 5%
10 : V_E = 0 V common

Currents (at nominal voltage)

	I_N	I_P
W-input at "1" level	−3.5 mA	1.1 mA
W-input at "0" level	−7.5 mA	see diagram on next page.



Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N = -5.7$ V and $V_P = +6.3$ V.
- The temperatures -20 °C and $+60$ °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input signal (W-terminal)

A "negative low" level applied to the input terminal (W) produces a positive reset signal at the output terminal (Q).

Transistor TR2 conducting (reset condition)

Voltage	$-V_W$	= min. 0	V
		= max. 0.2	V
limiting value	V_W	= max. 6.5	V
Required direct current	I_{WD}	= min. 0.1	mA
Required transient current averaged over 0.7 μs	I_{WT}	= min. 0.08	mA

Transistor TR2 non-conducting

Voltage	$-V_W$	= min. 0.7	V_N
		= max.	V_N

OUTPUT DATA

Transistor TR2 conducting (reset condition)

Voltage	V_Q	= min. 1.0	V
Available direct current	I_{QD}	= min. 15	mA
A and P interconnected		= min. 30	mA
B and P interconnected		= min. 40	mA

Transistor TR2 non-conducting

Voltage	$-V_Q$	= min. 0.5	V
		= max.	V_N

ONE-SHOT MULTIVIBRATOR

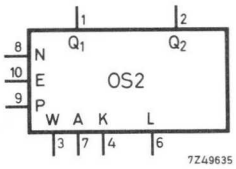
Colour : green

The unit OS2 contains a monostable multivibrator circuit equipped with medium-speed switching type transistors.

When a positive-going voltage step is applied to terminal A, the circuit generates a pulse at the Q-terminals.
The duration of the output pulse is determined by the value of:

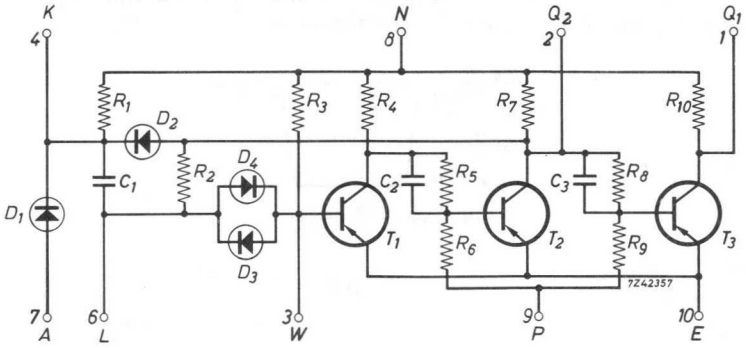
(a) the external capacitance parallel to C_1 between the terminals K and L (for pulses longer than the intrinsic value);
(b) the external resistance between the terminals Q_1 and W (for pulses shorter than the intrinsic value).

Frequency range	0 - 100 kHz
Permissible ambient temperature	-20 to +60 °C
Weight	approx. 20 g



Drawing symbol

CIRCUIT DATA



Terminals

1 = Q_1	= output 1	6 = L	= for external capacitor
2 = Q_2	= output 2	7 = A	= trigger input
3 = W	= d.c. input	8 = N	= supply (-6 V)
4 = K	= for external capacitor	9 = P	= supply (+6 V)
5 = not connected		10 = E	= common of supply (0 V)

Power supply

8 : V_N	= -6 V ± 5 %,	$-I_N$ = 8.8 mA	nominal value
9 : V_P	= +6 V ± 5 %,	I_P = 0.4 mA	
10 : V_E	= 0 V common		

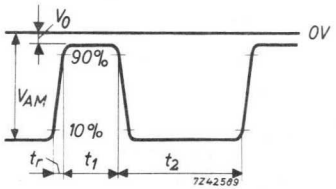
Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely V_N = -5.7 V and V_P = 6.3 V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT REQUIREMENTS

Trigger input signal (A terminal)

A positive-going voltage pulse is applied to terminal A. The leading edge of this voltage pulse drives by means of the transistor T_1 the transistor T_2 into the conducting, and the transistor T_3 into the non-conducting state.



Voltage levels

V_{AM}	= min.	-0.7	V_N
	= max.		$-V_N$
$-V_o$	= min.	0	V
	= max.	0.2	V

Required current during the transient				
averaged over: 0.4 µs	I_{AT}	= min.	2.4	mA
0.7 µs		= min.	1.4	mA
Required direct current 1)	I_{AD}	= min.	1.3	mA
Rise time				
without external capacitor	t_r	= max.	0.4	µs
with a capacitor of min. 200 pF between terminals K and L	t_r	= max.	0.7	µs
Duration of driving pulse	t_1	= min.	1	µs
Recovery time	t_2	= min.	6	µs 2)
when the duration of the output pulse (t_o) exceeds 7.5 µs	t_2	= min.	0.8	t_o 2)
Input noise level	V_n	= max.	1	V peak to peak

OUTPUT DATA

Voltages and currents

Transistor conducting		Output Q_1	Output Q_2
Voltage	$-V_Q$	= max. 0.2 V	max. 0.2 V
Available direct current	$-I_{QD}$	= max. 18 mA	max. 6 mA
Available current during the transient			
averaged over: 0.4 µs	$-I_{QT}$	= max. 19 mA	max. 15 mA
0.7 µs		= max. 25 mA	max. 21 mA

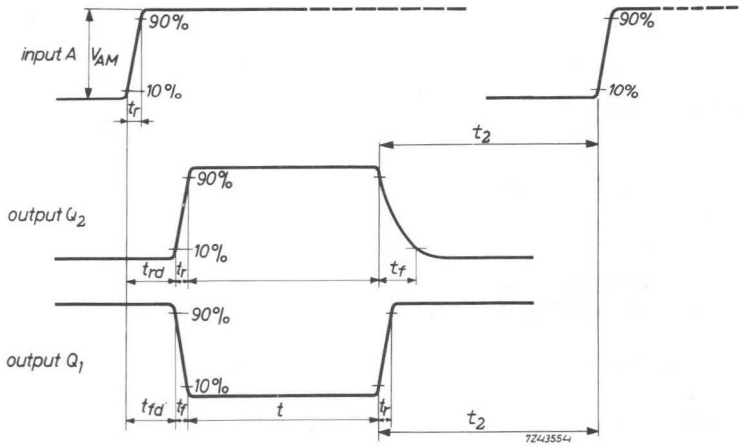
Transistor non-conducting		Output Q_1	Output Q_2
Voltage	$-V_Q$	= min. $-0.7\ V_N$	min. $-0.7\ V_N$
Available direct current	I_{QD}	= max. 0.7 mA	max. 0.25 mA

1) This is the current flowing to the input of the OS2 during the input pulse after decay of the output pulse, if the duration of the input pulse is longer.

2) The recovery time t_2 is starting at the trailing edge of V_A when $t_1 > t_o$ and at the trailing edge of V_{Q2} when $t_o > t_1$

Switching and delay times

These data refer to an input signal as specified under "Input Data".



Unit unloaded		Output Q_1	Output Q_2
Rise delay	t_{rd} =	-	t_{rA} + max. 0.4 µs
Rise time	t_r =	max. 0.2 µs	max. 0.2 µs
Fall delay	t_{fd} =	t_{rA} + max. 0.5 µs	-
Fall time	t_f =	max. 0.4 µs	max. 3 µs

Duration of the output pulse

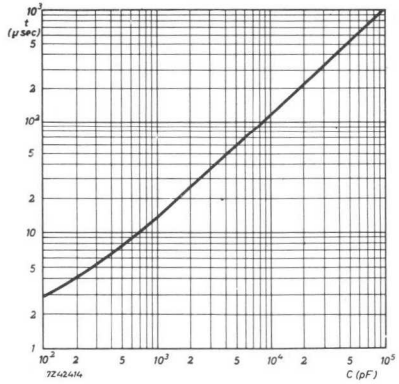
Unit unloaded

Intrinsic value	t_o = max. 4 µs
With resistor of 12 kΩ [1] between terminals Q_1 and W	t_o = max. 2 µs

With a capacitor between terminals K and L, at an ambient temperature of 25 °C and supply voltages V_N = -6 V and V_P = +6 V, see figure given below.

For larger capacitances log t is proportionate to log C.

[1]) minimum permissible value



Stability of pulse duration

A variation of the supply voltage V_N of 5 % varies the pulse duration by less than 1 % in the same direction.

The influence of a variation of the supply voltage Vp of 5 % is negligible.

An increase in ambient temperature by 1 °C gives a reduction of the pulse duration of less than 0.5 % and vice versa.

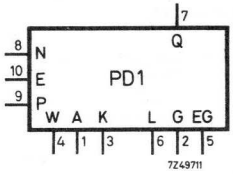
Note. In case an electrolytic capacitor is used for C_{ext} care should be taken that its + terminal is connected to terminal 6.

PULSE DRIVER

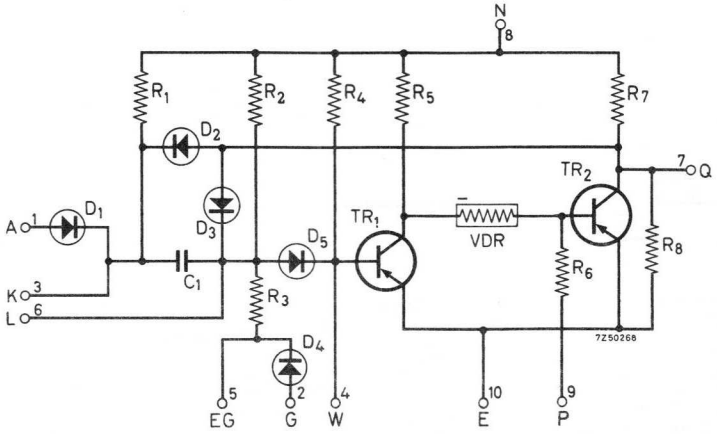
Colour: green

The unit PD1 contains a monostable multivibrator with a built-in trigger gate. It is mainly intended as a clock source, delivering trigger pulses for a great number of flip-flops FF1, FF2, FF3, and FF4 or as a counter driver.
The trigger gate can be controlled by a d.c. voltage level applied to terminal G.
The number of condition inputs can be extended with the aid of external diodes OA85/OA95 at the extension input E.G.
When a positive-going voltage step is applied to terminal A, the unit generates a pulse at the output (Q)-terminal, provided the gate is open.
The duration of the output pulse can be increased by means of an external capacitor between the terminals K and L (for pulses longer than the intrinsic value, e.g. necessary when driving a FF4 or 2PL2).
For mounting in the chassis 4322 026 38240 a printed-wiring board PDA 1, catalogue number 4322 026 34710, is available. On this standard printed-wiring board up to four PD 1's can be mounted (see section "ACCESSORIES FOR CIRCUIT BLOCKS 1-SERIES").

Frequency range	: see INPUT DATA
Permissible ambient temperature	: -20 to +60 °C
Weight	: approx. 20 g



Drawing symbol



CIRCUIT DATA

Terminal 1 = A = trigger input
2 = G = gate input
3 = K = for external capacitor
4 = W = d.c. input
5 = EG = extension gate input
6 = L = for external capacitor
7 = Q = output
8 = N = supply -6 V
9 = P = supply +6 V
10 = E = common supply 0 V

Power supply

Terminal 8: $V_N = -6\ V \pm 5\ \%$, $-I_N = 26\ mA$ (T_1 conducting)
$= 51\ mA$ (T_2 conducting)
9: $V_P = +6\ V \pm 5\ \%$, $I_P = 0.4\ mA$
10: $V_E = 0\ V$ common

Notes

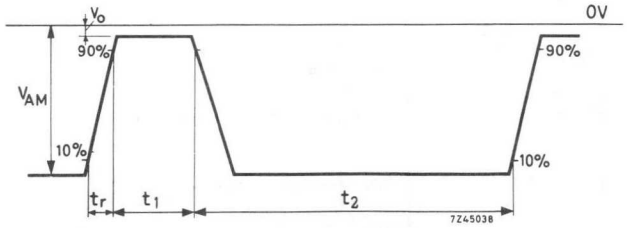
- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N = -5.7\ V$ and $V_P = 6.3\ V$.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input Signal Requirements

Trigger Input Signal (A terminal)

A positive-going voltage step is applied to input terminal A. This voltage step generates a pulse at the output Q if the gate has been opened by an appropriate gate input signal on terminal G.



Voltage

V_{AM} = min. -0.7 V_N
= max. - V_N
$-V_o$ = min. 0 V
= max. 0.2 V

Required direct current	I_{AD} = min. 1.7 mA
Required average current during the transient	I_{AT} = min. 1.5 mA (practically independent of rise time)
Rise time	t_r = max. 0.7 µs
Pulse duration	t_1 = min. 1 µs
Recovery time	t_2 = min. 6 µs (without external capacitor)
	t_2 = min. 11 µs (with C_{EXT} = 1000 pF between terminals K and L)
Note	Type of diodes and maximum number to be connected in parallel at terminal K: 6 x OA85/OA95.

Input Impedance:

Equivalent to a capacitance of 500 pF.

Gate Input Signals (G-terminals)

A d.c. voltage level is applied to terminal G. A "negative low" voltage opens the gate.

		Gate open	Gate closed
Voltage	$-V_G$	= min. 0 V	min. - 0.7 V_N
		max. 0.2 V	max. - V_N
Required gate current caused by negative transient of V_A	I_{GD}	= min. 1.75 mA	min. 0.5 mA
Required average current during the positive transient of V_G	I_{GT}	= min. 1.2 mA	

Gate Setting Times:

When the gate changes at random:		to open gate	to close gate
Without external capacitor	t_{gs}	= min. 8.5 µs	min. 25 µs
With an external capacitor of 1000 pF between K and L		= min. 24 µs	75 µs

		to open gate	to close gate
When the gate level changes within 1 µs after the positive going edge of the trigger signal:			
Without external capacitor	t_{gs}	= min. 6 µs	0
With external capacitor of 1000 pF between K and L		= min. 11 µs	0

Notes

- The gate setting time is the time the gate (G)-signal shall be present in advance to open the gate for the trigger (A) -signal.
- The absolute maximum value of the external capacitor is 1000 pF.
- Type of diodes and maximum number to be connected in parallel at terminal EG: 6 x OA85/OA95.

W-terminal (base connection transistor T1):

Transistor T_1 non-conducting:

Voltage limiting value

V_W = min. 0.2 V
V_W = max. 2.5 V

These voltages may be applied for max. 5 µs and a max.freq. of 100 kHz

Transistor T_1 conducting:

Current (limiting value)

$-I_W$ = max. 2 mA
(at $-V_W$ = max. 0.5 V)

Up to max.6 output-Q terminals of pulse logic units 2.PL2 may be connected to the W-input terminal of the PD 1 each via a resistor of 560 Ω ± 5%.

OUTPUT DATA

Voltages and Currents

Transistor conducting:

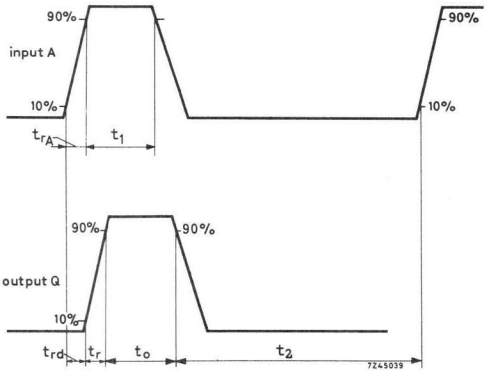
Voltage	$-V_Q$	= max. 0.2 V
Available direct current	$-I_{QD}$	= max. 65 mA
Available current during the transient: averaged over 0.7 µs	$-I_{QT}$	= max. 90 mA

Transistor non-conducting:

Voltage	$-V_Q$	= min. - 0.7 V_N = max. - 0.84 V_N

Switching and Delay Times:

These data are for orientation only and refer to an input signal as specified under INPUT DATA.



$t_{rd} = t_{rA} + 0.2$ µs
(fully loaded)

Unit max. loaded with:	$t_r + t_o$:	ext. capacitor between terminals K and L:
20 x FF1 or FF2	max. 1.5 µs	none
5 x FF3	min. 1.2 µs	none
20 x FF3	max. 2 µs	none
20 x FF4 (at 70 kHz)	max. 4 µs	C_{ext} = 1000 pF ± 5% (absolute max. value of C_{ext}).

The recovery time t_2 is starting at the trailing edge of V_A when $t_1 > t_o$ and at the trailing edge of V_Q when $t_o > t_1$ (t_1 = duration of input pulse V_A).

The typical output pulse duration of an unloaded pulse driver PD 1, triggered via a PL 2 unit (at 70 kHz): $t_r + t_o = 3.2$ µs.

POWER AMPLIFIER

The PA1 consists of an n-p-n/p-n-p transistor amplifier circuit, designed to be used as a power amplifier in the range of circuit blocks. The amplifier is non-inverting, and can be driven directly by the circuit blocks FF1,FF2,FF3, FF4, GI1, IA1, IA2 and OS2

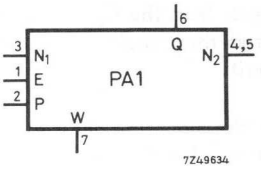
The output loadability is 600 mA at 60 V (abs. max. values). The built-in diode across the output terminals protects the output transistor against voltage transients which occur when the unit is driving an inductive load.

The circuit is mounted on an epoxy-paper printed-wiring board, the output transistor is provided with an aluminium heat sink.

Frequency range : 0-100 Hz

Ambient temperature range: -20 to +60 °C

Weight : approx. 60 g



CIRCUIT DATA

Terminal: 1 = E = common supply 0 V

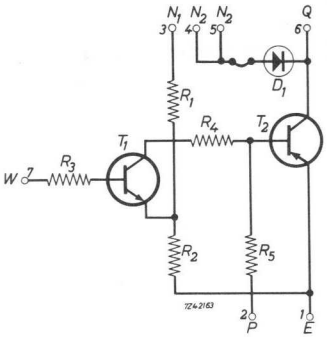
2 = P = supply +6 V

3 = N1 = supply -6 V

4 = N2, 5 = N2 = supply abs. max. 60 V

6 = Q = output

7 = W = input



Power Supply

Terminal: 1: V_E = 0 V common

2: V_P = 6 V ± 10 %, I_P = max. 20 mA 1) 2)

3: V_{N1} = -6 V ± 10 %, $-I_{N1}$ = max. 70 mA (T_2 non-conducting)
= max. 110 mA (T_2 conducting)

4), 5) $-V_{N2}$ = max. 60 V, $-I_{N2}$ = max. 600 mA 1) 2)

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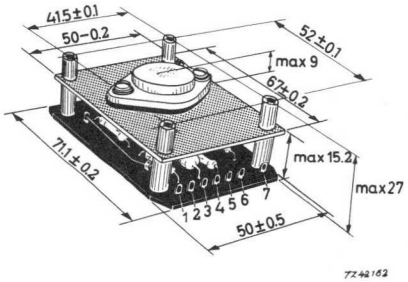
1) The sign is positive when the current flows towards the unit.

2) When $-V_{N2}$ is applied to the unit, care must be taken that Vp is present as well, otherwise transistor T2 may be damaged.

MECHANICAL CONSTRUCTION



The dimensions (approx. 71 mm x 50 mm x 27 mm) and terminal location can be seen from the figure given above. Since the aluminium heat sink is insulated from the circuit, no special measures need be taken as regards mounting of the unit.

In the mounting chassis 4322 026 38240 the PA 1 is to be mounted directly on a printed-wiring board. On such a standard printed-wiring board PAA 1 up to four PA 1's can be mounted, the next position in the chassis being left empty.
To ensure proper cooling of the unit, the PA 1 has to be mounted in such a way that a free flow of air through it is guaranteed.

INPUT DATA

Input Signal Requirements 2)

A d.c. voltage level is applied to terminal W.

Output-transistor conducting

Voltage	$-V_w$	=	max. 0.2 V min. 0 V
Current	I_w	=	min. 2.5 mA 1)

Output-transistor non-conducting

Voltage	$-V_w$	=	min. 4.25 V
Limiting value		=	max. 13.2 V
Current	$-I_w$	=	min. 0.1 mA 1)

OUTPUT DATA

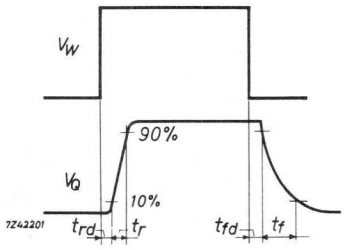
Output Signal Characteristics 2)

Output transistor conducting

Voltage	$-V_Q$	=	max. 0.75 V
Load current	$-I_Q$	=	max. 600 mA 1)

Output transistor non-conducting

Voltage	$-V_Q$	=	max. 60 V (dependent on the value of V_{N2} which is abs. max. 60 V.)
Leakage current	$-I_Q$	=	max. 14.5 mA 1)



1) The sign is positive when the current flows towards the unit.

2) These data apply to the most adverse working conditions for a combination of units, namely to supply voltages V_N = -5.4 V and V_p = +6.6 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

Switching and Delay Times (for orientation only)

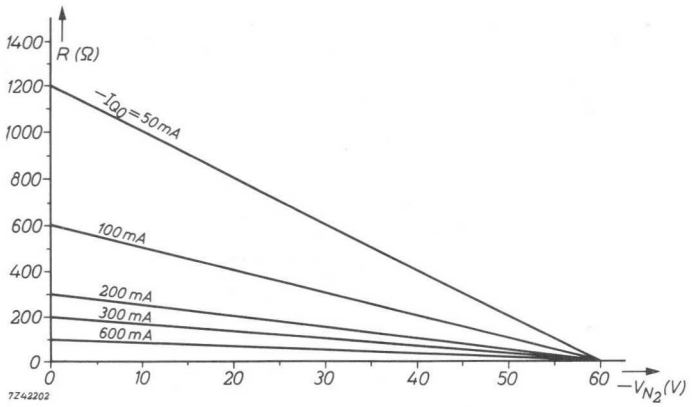
A square wave input signal is applied with an amplitude of 4.25 V, a rise time of max. 2.2 µs and a fall time of max. 2.5 µs

Unit loaded with a resistor of 100 Ω

Rise delay	t_{rd}	= max.	15 µs
Rise time	t_r	= max.	120 µs
fall delay	t_{fd}	= max.	70 µs
fall time	t_f	= max.	60 µs

Unit loaded with an inductive load

The unit is provided with a built-in diode to protect the output transistor against voltage transients which occur when an inductive load is switched. This protection is realised at the expense of a very long fall delay time of the current in this load. At supply voltages below 60 V, however, a wire jumper in series with this diode can be interchanged with a resistor to decrease this delay time.
The maximum permissible value of this resistor is given in the figure below, with the current flowing through the load at the moment of switching-off as parameter.



DUAL DECADE COUNTER

The unit 2.DCA 2 contains two identical decade counter units, mounted on a printed wiring board. Each counter consists of four flip-flops FF3, connected to operate in the 1-2-4-8 code. To achieve this operation, it is provided with a gate-diode with the result that six of the sixteen possible positions are skipped. The flip-flops can be reset by means of a common positive signal.

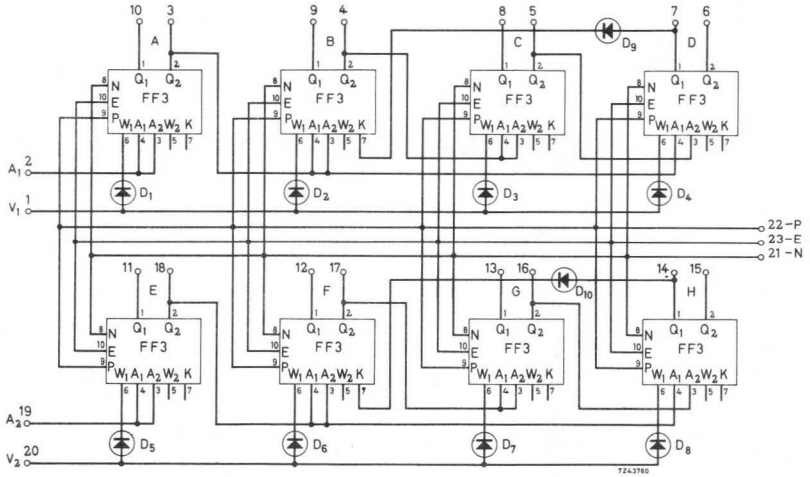
The reset diodes D_1 up to D_8 inclusive and the gate-diodes D_9 and D_{10} are mounted on the printed wiring board as well.

The printed wiring board is provided with plated-through holes and single-sided gold-plated contacts.

With the mating connector, 2422 020 52592, not supplied with the dual decade counter, the printed wiring board of standard dimensions (121.8mm x x 180.3mm x 1.6mm) can be used directly in the standard mounting chassis, catalog number 4322 026 38240.

The fixation of the circuit blocks FF3 to the p.w. board is secured by means of locking tags, catalog number 4322 026 33690.

Pulse repetition frequency range:	0 - 100 kHz
Ambient temperature range:	-20 to +60 °C
Weight:	approx. 210 g



Terminal

1 = V_1 = reset input counter 1	13 = Q_{1G} = output 1 flip-flop G
2 = A_1 = a.c. input counter 1	14 = Q_{1H} = output 1 flip-flop H
3 = Q_{2A} = output 2 flip-flop A	15 = Q_{2H} = output 2 flip-flop H
4 = Q_{2B} = output 2 flip-flop B	16 = Q_{2G} = output 2 flip-flop G
5 = Q_{2C} = output 2 flip-flop C	17 = Q_{2F} = output 2 flip-flop F
6 = Q_{2D} = output 2 flip-flop D	18 = Q_{2E} = output 2 flip-flop E
7 = Q_{1D} = output 1 flip-flop D	19 = A_2 = a.c. input counter 2
8 = Q_{1C} = output 1 flip-flop C	20 = V_2 = reset input counter 2
9 = Q_{1B} = output 1 flip-flop B	21 = N = common negative supply
10 = Q_{1A} = output 1 flip-flop A	22 = P = common positive supply $^{-6V}_{+6V}$
11 = Q_{1E} = output 1 flip-flop E	23 = E = common supply 0V
12 = Q_{1F} = output 1 flip-flop F	

Power Supply

Terminal 21: $V_N = -6V \pm 5\%$, $-I_N = 70mA$

22: $V_P = +6V \pm 5\%$, $I_P = 4.8mA$

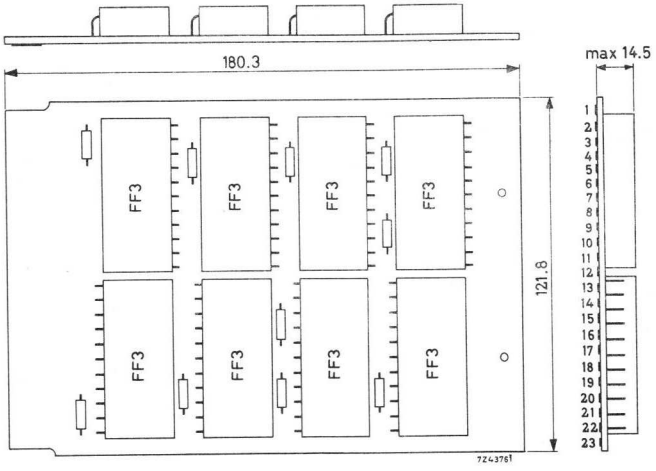
23: $V_E = 0V$

} Nominal value of the current

Notes:

- When a current is flowing towards the unit, the positive sign is used
- The data given apply to the most adverse supply voltages for a combination of units, namely
  $V_N = -5.7V$ and $V_P = +6.3V$
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.

Dimensions and Terminal Location

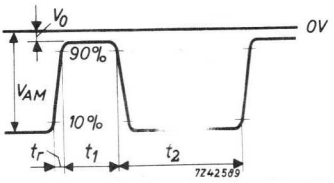


INPUT DATA

Input Signal Requirements

Trigger Input Signal (A_1 and/or A_2 terminals)

A positive-going voltage step is applied to terminal A. This voltage step advances the counter one position.



Voltage	V_{AM}	= min.	$-0.7V_N$
		= max.	$-V_N$
	$-V_0$	= min.	0V
		= max.	0.2V
Required direct current	$I_{A1D}(I_{A2D})$	= min.	1.75mA
Required current during the transient averaged over 0.4μs	I_{A1T} (I_{A2T})	= min.	6mA
0.7μs		= min.	4.5mA
Rise time	t_r	= max.	0.7μs
Pulse duration	t_1	= min.	1μs
	t_2	= min.	8μs
Input noise level	V_n	= max.	1V peak to peak

Reset Input Signal (V_1 and/or V_2 terminals)

For resetting the counter a positive d.c.voltage is applied to terminal V. This signal causes all Q_1-terminals to reach a "negative-high" and all Q_2-terminals to reach a "negative-low" level.

Input level during reset

Voltage	$V_{v1}(V_{v2})$	= min.	1V
		= max.	10V
Current	I_{v1} (I_{v2})	= min.	3.6 mA

During counting it is recommended that terminal V_1 and/or V_2 are connected to a voltage level.

Voltage	$-V_{v1}$ $(-V_{v2})$	= min.	0.4V
		= max.	15V
Current	$-I_{v1}$ $(-I_{v2})$	= min.	0.12mA (at $-V_{v1}$ $(-V_{v2})$ = 0.4V)

OUTPUT DATA

These data apply to the various flip-flop stages.

Output Signal Characteristics

Transistor non-conducting

Voltage: $-V_Q$ = min. $-0.7V_N$

Available direct current I_{QD} = max. 0.7 mA

Transistor conducting

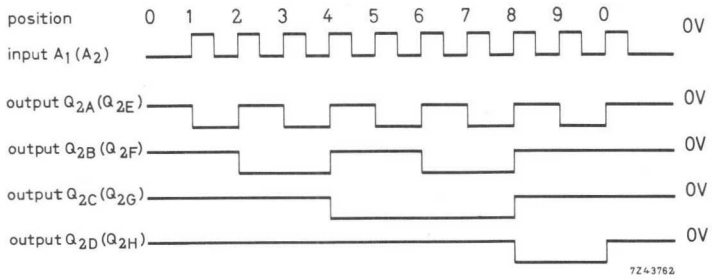
Voltage $-V_Q$ = max. 0.2 V
= min. 0 V

		output Q_1		output Q_2			
		Flip-Flop A-B-C E-F-G-	Flip-Flop D-H	Flip-Flop A-E	Flip-Flop B-F	Flip-Flop C-G	Flip-Flop D-H
max. available current during transient $-I_{QT}$	averaged over 0.4 µs	11 mA	11 mA	4 mA	5 mA	6 mA	11 mA
	averaged over 0.7 µs	14 mA	14 mA	9 mA	9.5 mA	10 mA	14 mA
maximum available direct current $-I_{QD}$		6 mA	5.1 mA	3.4 mA	4.25 mA	5.1 mA	6 mA

Maximum Speed:

For all loads within the limits mentioned above, also applied simultaneously, the maximum counting speed of 100 kHz is guaranteed.

Output levels during counting



The output levels at the Q_2-terminals are shown in the figure above.
Note that when a Q_2 output is at "negative-low" level the corresponding Q_1 output is at "negative-high" level and vice versa.
After 10 positive-going voltage steps at the input terminal A_1 (A_2), the output terminal Q_{2D} (Q_{2H}) delivers one positive-going voltage step, whilst the decade counter has resumed its initial position, namely all Q_2-terminals being at 0V level.

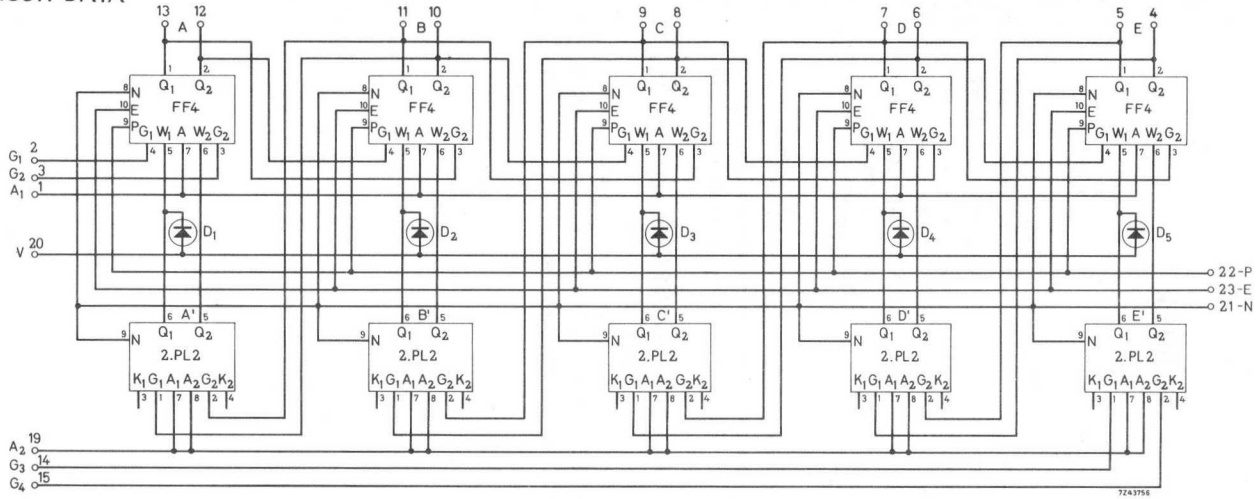
REVERSIBLE COUNTER

The unit BCA 1 consists of five flip-flops FF4 and five dual pulse logic's 2.PL2, mounted on a printed-wiring board, interconnected to operate as a bi-directional shift register. A bi-directional decade counter can be realised by interconnecting the gate (G)-terminals of the first flip-flop with the output (Q)-terminals of the fifth flip-flop and the gate (G)-terminals of the fifth dual pulse logic with the output (Q)-terminals of the first flip-flop. These interconnections have to be made externally in such a way that the Q1- respectively Q2-terminal has to be connected with the corresponding G_1- respectively G_2-terminal.

The flip-flops can be reset by means of a common positive signal. The five reset diodes D_1 up to D_5 inclusive are mounted on the printed-wiring board as well. The printed-wiring board is provided with plated through holes and single sided gold plated contacts.
With the mating connector catalog number 2422 020 52592, not supplied with the reversible counter, this printed-wiring board of standard dimensions (121.8 mm x 180.3 mm x 1.6 mm) can be used directly in the standard mounting chassis catalog number 4322 026 38240. The fixation of the circuit blocks FF4 and 2.PL2 is secured by means of locking tags catalog number 4322 026 33690.

Pulse repetition frequency range:	0 - 70 kHz
Ambient temperature range:	−20 to +60 °C
Weight:	approx. 250 g

CIRCUIT DATA



Terminal

1 = A_1	= a.c. input forward direction	9 = Q_{1C}	= output 1 flip-flop C	16 = not connected	
2 = G_1	= gate input (G_1) flip-flop A	10 = Q_{2B}	= output 2 flip-flop B	17 = not connected	
3 = G_2	= gate input (G_2) flip-flop A	11 = Q_{1B}	= output 1 flip-flop B	18 = not connected	
4 = Q_{2E}	= output 2 flip-flop E	12 = Q_{2A}	= output 2 flip-flop A	19 = A_2	= a.c. input reverse direction
5 = Q_{1E}	= output 1 flip-flop E	13 = Q_{1A}	= output 1 flip-flop A	20 = V	= reset input
6 = Q_{2D}	= output 2 flip-flop D	14 = G_3	= gate input (G_1) dual pulse logic E'	21 = N	= common negative supply -6 V
7 = Q_{1D}	= output 1 flip-flop D			22 = P	= common positive supply +6 V
8 = Q_{2C}	= output 2 flip-flop C	15 = G_4	= gate input (G_2) dual pulse logic E'	23 = E	= common supply 0 V

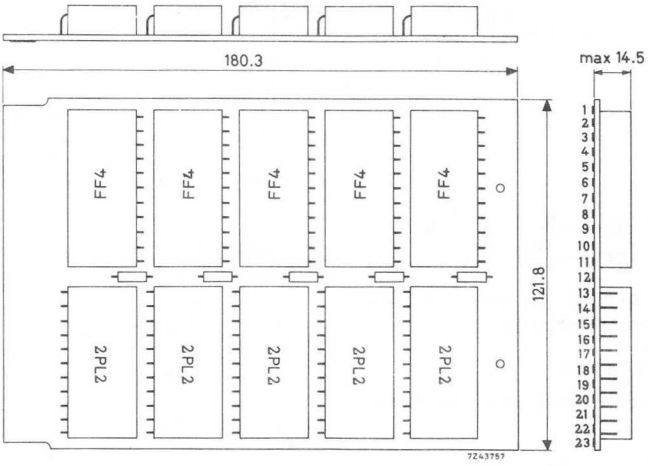
Power Supply

Terminal 21:	$V_N = -6V \pm 5\%$, $-I_N = 55mA$	Nominal value of the current
22:	$V_P = +6V \pm 5\%$, $I_P = 3mA$	
23:	$V_E = 0V$	

Notes

- When a current is flowing towards the unit, the positive sign is used
- The data given apply to the most adverse supply voltages for a combination of units, namely
  $V_N = -5.7V$ and $V_P = +6.3V$
- The temperatures $-20\,^{\circ}C$ and $+60\,^{\circ}C$ and the tolerances on the supply voltages are absolute limiting values

Dimensions and terminal location



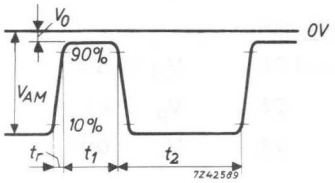
INPUT DATA

Input Signal Requirements

Trigger Input Signal (A_1 or A_2 terminal)

A positive-going voltage step is applied to terminal A. When this voltage step is applied to terminal A_1 the counter advances one position, when it is applied to terminal A_2 the counter reverses one position.

Voltage V_{AM} = min. $-0.7V_N$
= max. $-V_N$
$-V_0$ = min. 0V
= max. 0.2V



Required direct current	I_{A1D} (I_{A2D}) = min.	8.8mA
Required current during the transient: averaged over 0.4 µs	I_{A1T} (I_{A2T}) = min.	30mA
0.7 µs	= min.	22.5mA
Rise time	t_r = max.	0.7 µs
Pulse duration	t_1 = min.	3 µs
	t_2 = min.	11 µs
Input noise level	V_n = max.	1V p-p

Gate Input Signal (G_1 and G_2 or G_3 and G_4 terminals)

A d.c. voltage level is applied to these G-terminals

	gate open		gate closed	
Voltage	$-V_G$ = min.	0V	min.	V_{AM}
	= max.	0.2V	max.	$-V_N$
Required gate current caused by negative transient of V_{AM}	I_{GD} = min.	1.75mA	min.	1.2 mA
Required average current during the positive transient of V_G	I_{GT} = min.	1.6mA		
Gate setting time				
when the gate input level changes at random	t_{GS} = min.	17 µs	min.	25 µs
when the gate input level changes within 2 µs after the positive going edge of the trigger signal	t_{GS} = min.	11 µs	min.	11 µs

Notes

- The latter applies to the shift register configuration so that the max. shift frequency is approximately 70 kHz
- During triggering the G levels should not be at zero voltage level simultaneously
- The gate setting time is the required waiting time between the last G level change and the positive-going edge of the trigger pulse

Reset Input Signal (V-terminal)

For resetting the counter a positive d.c. voltage is applied to terminal V. This signal causes all Q_1-terminals to reach a "negative high" and all Q_2-terminals to reach a "negative low" level.

Input Level during Reset

Voltage V_v = min. 1 V
= max. 10 V

Current I_v = min. 4.5 mA

During shifting it is recommended that terminal V is connected to a voltage level:

Voltage $-V_v$ = min. 0.4 V
= max. 15 V

Current $-I_v$ = min. 0.15 mA
(at $-V_v$ = 0.4 V)

OUTPUT DATA

These data apply to the various flip-flop stages:

Output Signal Characteristics

Transistor non-conducting

Voltage $-V_Q$ = min. $-0.7V_N$

Available direct current I_{QD} = max. 0.7 mA

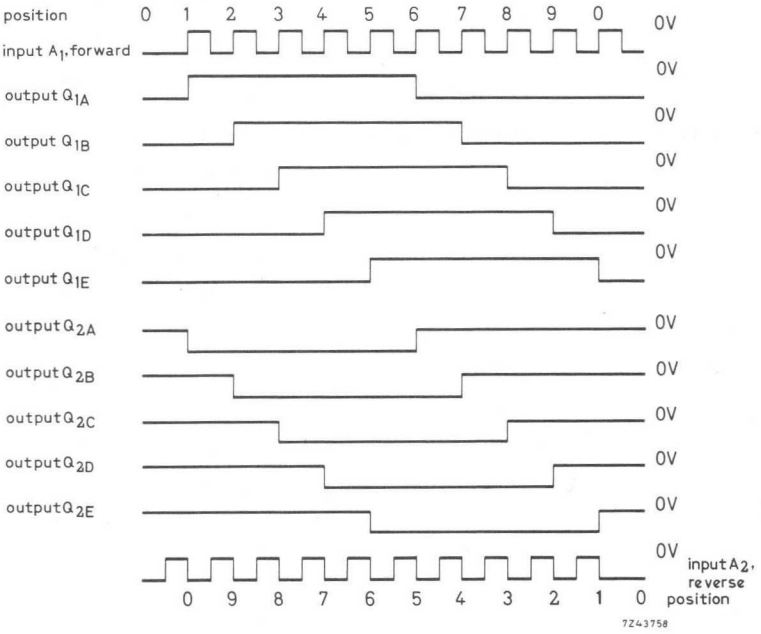
Transistor conducting

Voltage $-V_Q$ = max. 0.2 V
= min. 0 V

		flip-flops B-C-D	flip-flops A-E
available current during the transient $-I_{QT}$	averaged over 0.4 µs	max. 8 mA	max. 9.4 mA
	averaged over 0.7 µs	max. 11 mA	max. 12.4 mA
available direct current $-I_{QD}$		max. 3.75 mA	max. 4.25 mA

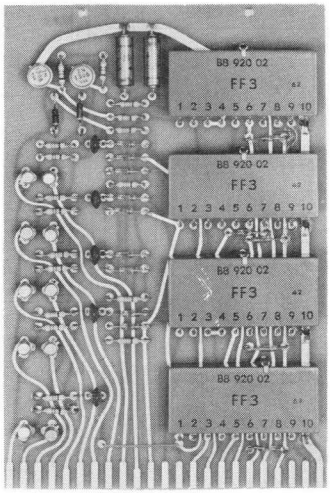
These current data apply to the unit, operating as a bi-directional shift register. When the unit is interconnected to form a bi-directional decade counter the lowest current values of $-I_{QT}$ and $-I_{QD}$ are valid for all flip-flops.

Output levels during counting, when the unit is externally interconnected to form a bi-directional decade counter. To this end terminals 2 and 5, 3 and 4, 12 and 15, 13 and 14 have to be connected.
The output levels at the Q-terminals can be taken from the figure below.



Note that after 10 positive-going voltage steps at the input terminal A_1 (A_2), the output terminal Q_{2E} (Q_{2A}) delivers one positive-going voltage step, whilst the decade counter has retaken its initial position, namely all Q_2-terminals being at 0V level.

DECADE COUNTER AND NUMERICAL INDICATOR TUBE DRIVER ASSEMBLY



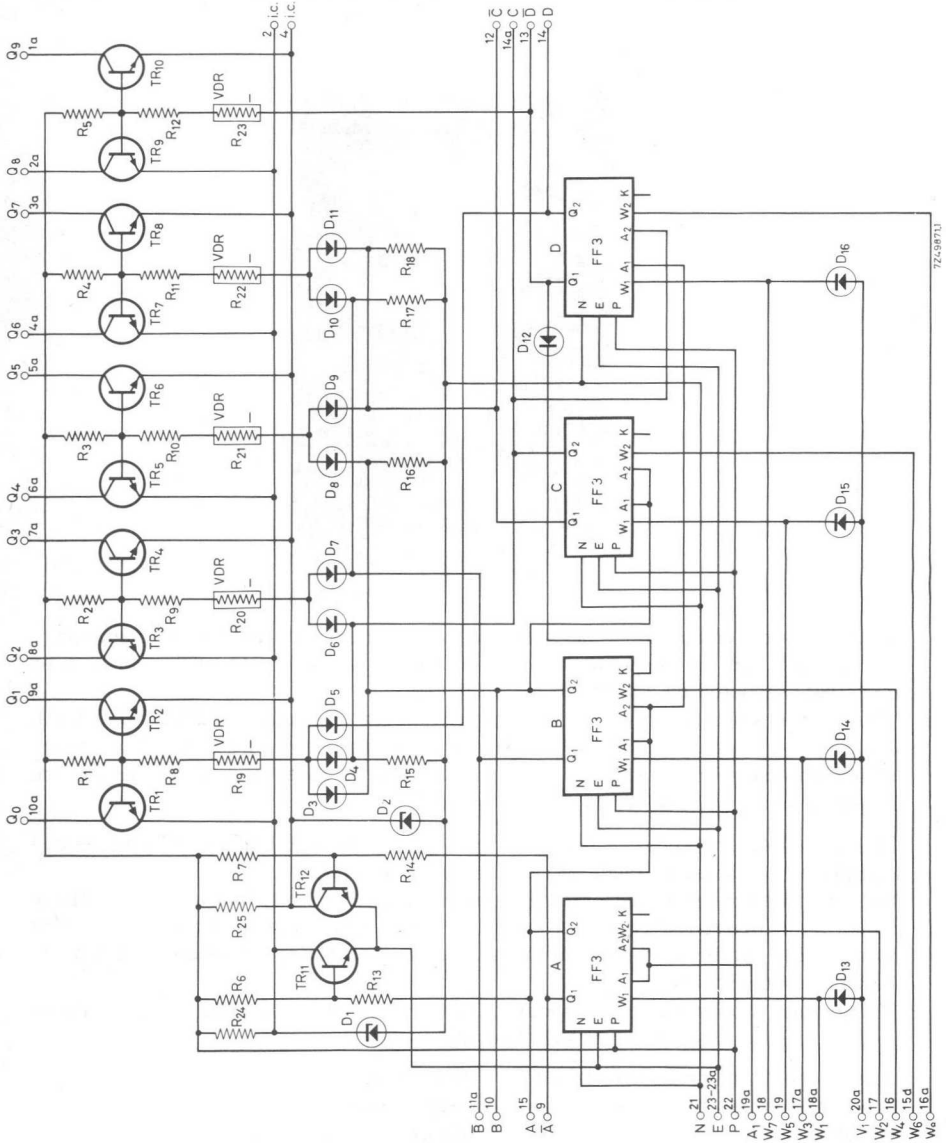
RZ 22603-6

This assembly contains one decade counter together with the decoding and driving circuits for the numerical indicator tubes ZM 1000, ZM 1020, ZM 1040 or ZM 1080, mounted on a printed-wiring board.
The counter consists of four flip-flops FF 3 (catalog number 2722 001 00021), connected to operate in the 1-2-4-8 code. The flip-flops can be reset by means of a common positive signal; the reset diodes D_1 up to and including D_4 are mounted on the printed-wiring board as well.

The printed-wiring board, provided with plated-through holes and double-sided goldplated contacts, is made of glass-epoxy material.
With the mating connector, catalog number 2422 020 52591, (not supplied with the DCA3), this printed-wiring board of standard dimensions (121.8 mm x 180.3 mm x 1.6 mm), can be used directly in the standard mounting chassis (catalog number 4322 026 38240).
The circuit blocks FF 3 are secured to the printed-wiring board by means of locking tags (catalog number 4322 026 33690).

Pulse repetition frequency range	:	0 - 100 kHz
Ambient-temperature range	:	−20 to +60 °C
Weight	:	approx. 150 g

CIRCUIT DATA



Terminals

1 = not connected
2 = internal connection
3 = not connected
4 = internal connection
5 = not connected
6 = not connected
7 = not connected
8 = not connected
9 = $\overline{A}$ = Q_{1A} = output 1 flip-flop A
10 = B = Q_{2B} = output 2 flip-flop B
11 = not connected
12 = $\overline{C}$ = Q_{1C} = output 1 flip-flop C
13 = $\overline{D}$ = Q_{1D} = output 1 flip-flop D
14 = D = Q_{2D} = output 2 flip-flop D
15 = A = Q_{2A} = output 2 flip-flop A
16 = W_4 = W_2 of flip-flop B
17 = W_2 = W_2 of flip-flop A
18 = W_7 = W_1 of flip-flop D
19 = W_5 = W_1 of flip-flop C
20 = not connected
21 = N = common negative supply −6 V
22 = P = common positive supply +6 V
23 = E = common supply 0 V

1a = Q_9 = digit number 9
2a = Q_8 = digit number 8
3a = Q_7 = digit number 7
4a = Q_6 = digit number 6
5a = Q_5 = digit number 5
6a = Q_4 = digit number 4
7a = Q_3 = digit number 3
8a = Q_2 = digit number 2
9a = Q_1 = digit number 1
10a = Q_0 = digit number 0
11a = $\overline{B}$ = Q_{1B} = output 1 flip-flop B
12a = not connected
13a = not connected
14a = C = Q_{2C} = output 2 flip-flop C
15a = W_6 = W_2 of flip-flop C
16a = W_8 = W_2 of flip-flop D
17a = W_3 = W_1 of flip-flop B
18a = W_1 = W_1 of flip-flop A
19a = A_1 = a.c. input counter
20a = V_1 = reset input counter
21a = not connected
22a = not connected
23a = E = common supply 0 V

Power supply

Terminal 21 : V_N = −6 V ±5 %, $-I_N$ = 42 mA } nominal value
22 : V_P = +6 V ±5 %, I_P = 8.8 mA } of the current
23 = 23A : V_E = 0 V

Notes

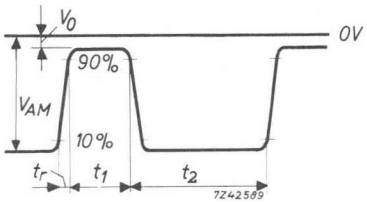
- The data given apply to the most adverse supply voltages for a combination of units, namely V_N = −5.7 V and V_P = +5.7 V.
- The temperatures −20 °C and +60 °C and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input signal requirements

Trigger input signal (terminal A_1)

A positive-going voltage step is applied to terminal A_1. This voltage step advances the counter one position.



Voltage	V_{AM}	= min.	−0.7 V_N
		= max.	− V_N
	$-V_0$	= min.	0 V
		= max.	0.2 V
Required direct current	I_{A_1D}	= min.	1.75 mA
Required current during the transient averaged over 0.4 μs	I_{A_1T}	= min.	6 mA
over 0.7 μs		= min.	4.5 mA
Rise time	t_r	= max.	0.7 μs
Pulse duration	t_1	= min.	1 μs
	t_2	= min.	8 μs

Reset input signal (terminal V_1)

For resetting the counter a positive d.c. voltage is applied to terminal V_1. This signal causes all terminals Q_1 to reach a "negative high" and all terminals Q_2 to reach a "negative low" level.

Input level during reset

Voltage	V_{V_1}	= min.	1 V
		= max.	10 V
Current	I_{V_1}	= min.	3.6 mA

During counting it is recommended that terminal V_1 is connected to a voltage level.

Voltage	$-V_{V_1}$	= min.	0.4 V
		= max.	10 V
Current	$-I_{V_1}$	= min.	0.12 mA (at $-V_{V_1}$ = 0.4 V)

D.C. input (terminals W)

A d.c. voltage level is applied to terminals W_1 up to and including W_8. A positive voltage drives the corresponding transistor into the non-conducting state and a negative voltage drives the transistor into the conducting state.

Transistor conducting

Current	$-I_W$	= min.	0.6 mA ($-V_W$ = max. 0.4 V)
		= max.	15 mA

Transistor non-conducting

Voltage	V_W	= min.	0.2 V
		= max.	10 V
Current	I_W	= min.	0.9 mA

OUTPUT DATA

Decade counter section

The outputs of the counter (A, $\overline{A}$, B, $\overline{B}$, etc.) may furthermore be loaded with two gate invertors GI or two negative AND-gates. Output D of the last flip-flop is then still capable to drive a next decade.
A, B, C and D are the outputs of the flip-flops which are at 0 V level, when the decade is set on digit number 0.

Output transistor conducting

Voltage $-V_Q$ = min. 0 V, max. 0.2 V

		A	$\overline{A}$	B	$\overline{B}$	C	$\overline{C}$	D	$\overline{D}$
Available direct current (in mA)	$-I_{QD}$ =	3.4	6	2.15	3.9	3	3.9	6	5.1
Available transient current averaged over 0.7 μs (in mA)	$-I_{QT}$ =	9	14	8.4	12.9	8.9	12.9	14	14

Output transistor non-conducting

Voltage $-V_Q$ = min. 0.7 V_N, = max. V_N

		A	$\overline{A}$	B	$\overline{B}$	C	$\overline{C}$	D	$\overline{D}$
Available direct current (in mA)	I_{QD} =	0.1	0.13	0.1	0.1	0.1	0.1	0.13	0.1

Numerical indicator tube driver

The outputs Q_0 (terminal 10a) up to and including Q_9 (terminal 1a) have to be connected to the pins k_0 up to and including k_9 of the numerical indicator tube ZM 1000, ZM 1020, ZM 1040 or ZM 1080.
The anode of these tubes has to be connected via a resistor R_a to the high voltage power supply V_b.

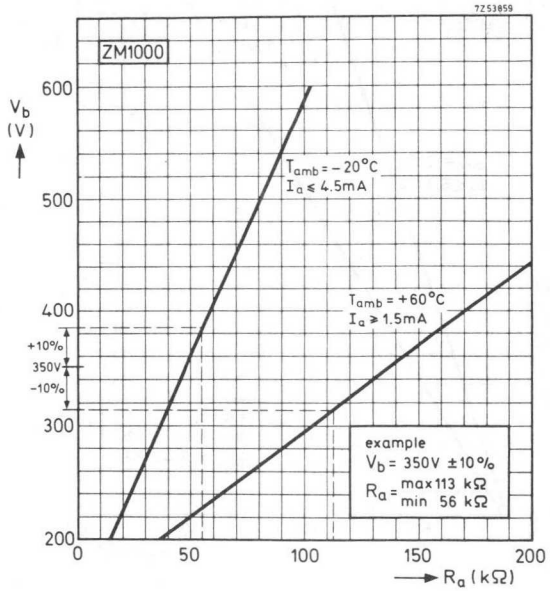
Output transistor conducting

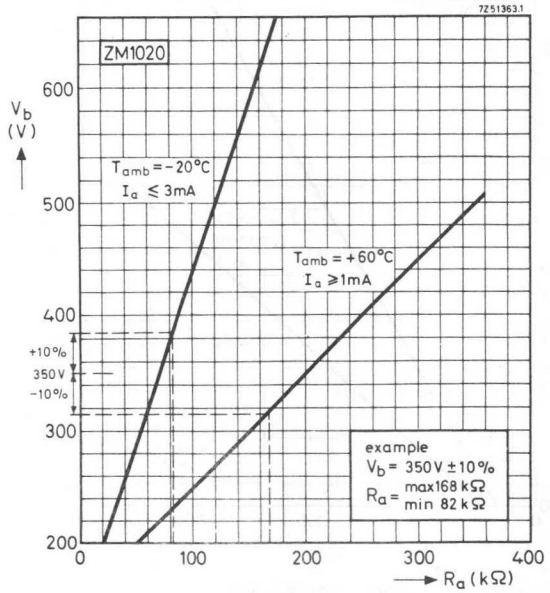
Voltage V_Q = max. 3.2 V

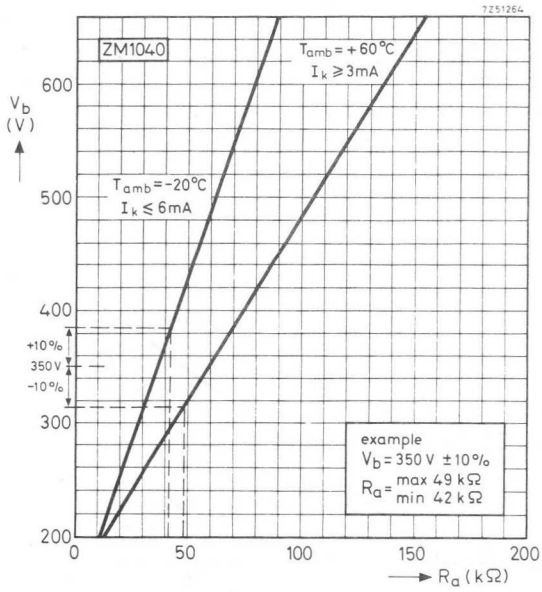
Current I_Q = max. 6 mA

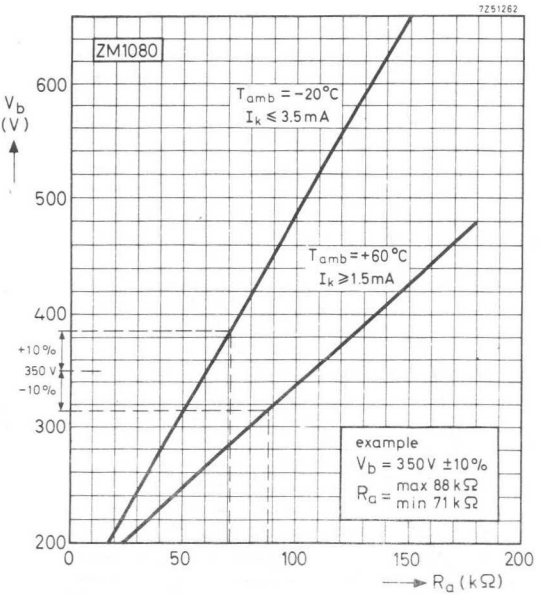
The available output current (I_Q) of the ten numerical outputs Q_0 up to and including Q_9 is sufficient to deliver the required current for the numerical indicator tube ZM 1000, ZM 1020, ZM 1040 or ZM 1080.

The relation between the permitted value and tolerances of the high voltage supply V_b and the corresponding anode series resistor R_a for the various indicator tubes over the whole temperature range is given in the following graphs.


7Z53859
ZM1000
V_b (V)
600
500
400
300
200
+10%
350V
-10%
$T_{amb} = -20°C$
$I_a \leq 4.5mA$
$T_{amb} = +60°C$
$I_a \geq 1.5mA$
example
$V_b = 350V \pm 10\%$
$R_a =$ max 113 kΩ
min 56 kΩ
0
50
100
150
200
R_a (kΩ)

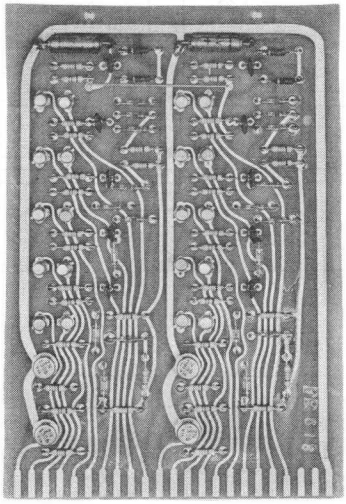

7Z51363.1
ZM1020
V_b (V)
600
500
400
300
200
+10%
350V
-10%
$T_{amb} = -20°C$
$I_a \leq 3mA$
$T_{amb} = +60°C$
$I_a \geq 1mA$
example
$V_b = 350V \pm 10\%$
$R_a =$ max 168 kΩ
min 82 kΩ
0
100
200
300
400
R_a (kΩ)





Wiring capacitance at each Q-output: max. 500 pF

DUAL NUMERICAL INDICATOR TUBE DRIVER ASSEMBLY



RZ 22603-8

This assembly contains two BCD-to-decimal decoding and driving circuits for the numerical indicator tubes ZM 1000, ZM 1020, ZM 1040 or ZM 1080, mounted on a printed-wiring board.

The 2.ID 1 has been designed to operate in conjunction with decade counters in the 1-2-4-2 (jump at 8) or 1-2-4-8 code, e.g. the dual decade counter assembly 2.DCA 2 (catalog number 2722 009 00011).

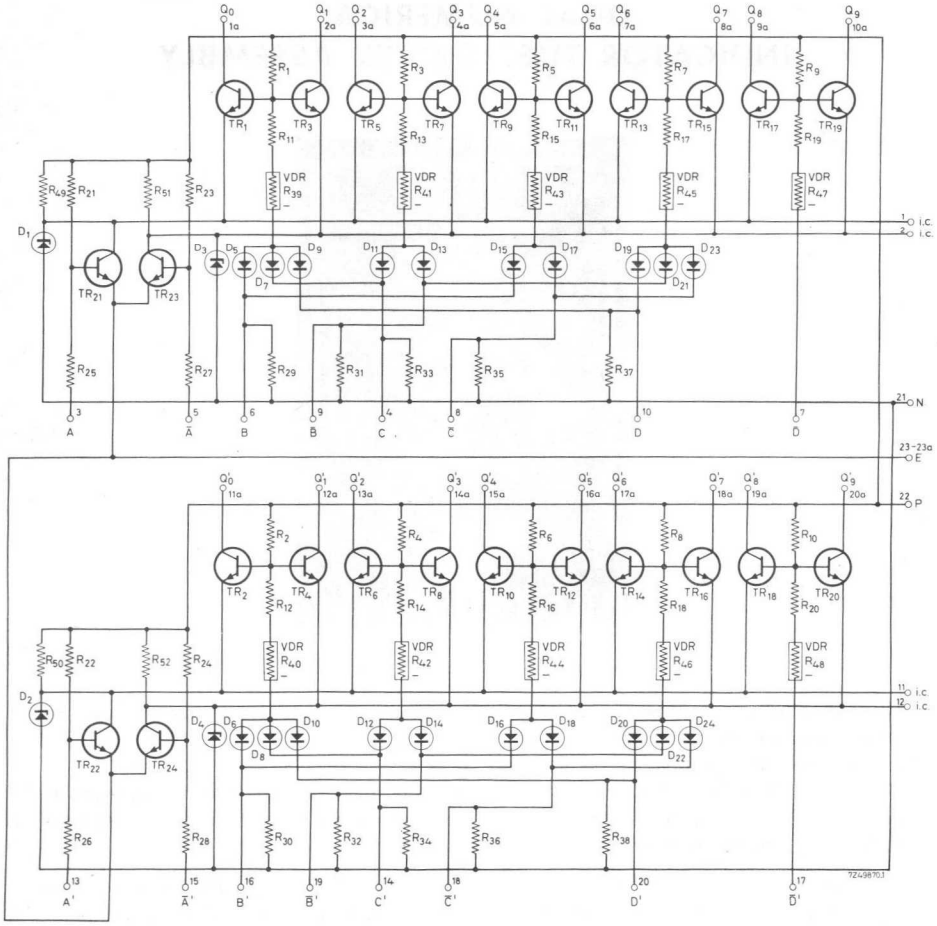
The inputs A, $\overline{A}$, B, $\overline{B}$, C, $\overline{C}$, D, $\overline{D}$ and A', $\overline{A'}$, B', $\overline{B'}$, C', $\overline{C'}$, D', $\overline{D'}$ have to be connected to the corresponding outputs of the four flip-flops of the decade counter.

The inputs A, B, C, D and A', B', C', D' have to be at the "0" level for the digit number 0 to be indicated.

The printed-wiring board, provided with plated-through holes and double-sided goldplated contacts, is made of glass-epoxy material. With the mating connector (catalog number 2422 020 52591), not supplied with the 2.ID 1, this printed-wiring board of standard dimensions (121.8 mm x 180.3 mm x 1.6 mm) can be used directly in the standard mounting chassis (catalog number 4322 026 38240).

Ambient-temperature range:	−20 to +60 °C
Weight	approx. 100 g

CIRCUIT DATA



Terminals

1 = internal connection
2 = internal connection
3 = A = to be connected to output Q of first flip-flop
4 = C = to be connected to output Q of third flip-flop
5 = $\overline{A}$ = to be connected to output $\overline{Q}$ of first flip-flop
6 = B = to be connected to output Q of second flip-flop
7 = $\overline{D}$ = to be connected to output $\overline{Q}$ of fourth flip-flop
8 = $\overline{C}$ = to be connected to output $\overline{Q}$ of third flip flop
9 = $\overline{B}$ = to be connected to output $\overline{Q}$ of second flip-flop
10 = D = to be connected to output Q of fourth flip-flop

} decade counter 1

11 = internal connection
12 = internal connection
13 = A' = to be connected to output Q of first flip-flop
14 = C' = to be connected to output Q of third flip-flop
15 = $\overline{A'}$ = to be connected to output $\overline{Q}$ of first flip-flop
16 = B' = to be connected to output Q of second flip-flop
17 = $\overline{D'}$ = to be connected to output $\overline{Q}$ of fourth flip-flop
18 = $\overline{C'}$ = to be connected to output $\overline{Q}$ of third flip-flop
19 = $\overline{B'}$ = to be connected to output $\overline{Q}$ of second flip-flop
20 = D' = to be connected to output Q of fourth flip-flop
} decade counter 2
21 = N = common negative supply −6 V
22 = P = common positive supply +6 V
23 = 23a = E = common supply 0 V

1a up to and including 10a = numerical outputs Q_0 up to and including Q_9 to drive numerical indicator tube 1

11a up to and including 20a = numerical outputs Q'_0 up to and including Q'_9 to drive numerical indicator tube 2

Power supply

Terminal 21 : $V_N = -6\ V \pm 5\%$, $-I_N = 8.5\ mA$
22 : $V_P = +6\ V \pm 5\%$, $I_P = 7\ mA$
} nominal value of the current required for one ID 1
23 : $V_E = 0\ V$ common

Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely: $V_N = -5.7\ V$ and $V_P = +6.3\ V$
- The temperatures −20 °C and +60 °C and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input signal requirements (terminals A, $\overline{A}$, A', $\overline{A'}$, etc.)

Input at "0" level

Voltage $-V_I$ = min. 0 V
= max. 0.2 V

		A, A', $\overline{A}$, $\overline{A'}$	B, B', $\overline{B}$, $\overline{B'}$, C, C', $\overline{C}$, $\overline{C'}$, D, D'	$\overline{D}$, $\overline{D'}$
Required direct current	I_I	0 mA	2.1 mA	0 mA
Required transient current	I_{QT}	0 mA	1.1 mA	0 mA

Input at negative high level

Voltage $-V_I$ = min. 0.7 V_N
= max. V_N

	A, A', $\overline{A}$, $\overline{A'}$	B, B', $\overline{B}$, $\overline{B'}$, C, C', $\overline{C}$, $\overline{C'}$, D, D' $\overline{D}$, $\overline{D'}$
Required direct current $-I_I$	0.57 mA	0.6 mA

Input impedance: equivalent to a capacitance of approx. 150 pF

Operational data

- When an ID 1 is driven from a decade counter with flip-flops operating in the 1-2-4-8 code, these flip-flops may be additionally loaded with two negative AND-gates, or with two GI's if the decade counter is equipped with FF 3 flip-flops, or with one GI if the decade counter is equipped with FF 1 flip-flops. Output D of the last flip-flop is capable of driving a following decade counter.
- A, B, C, D and A', B', C', D' must be connected to the outputs of the flip-flops which are at "0" level, when the decade counter is set on digit number 0.

OUTPUT DATA

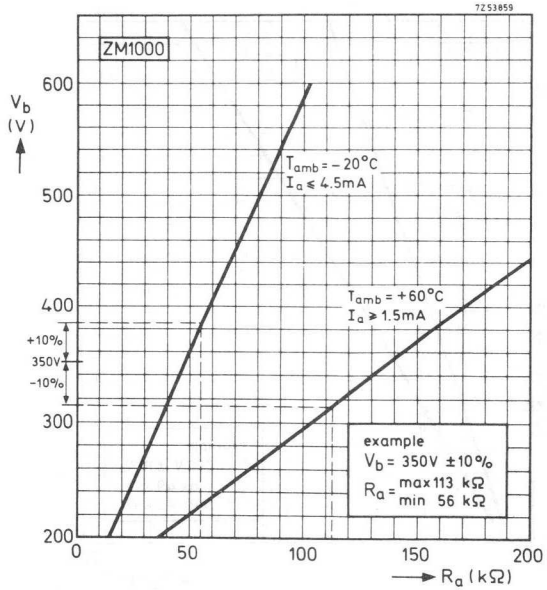
The outputs Q_o up to and including Q_9 and Q'_o up to and including Q'_9 have to be connected to the pins k_0 up to and including k_9 of the numerical indicator tube ZM 1000, ZM 1020, ZM 1040 or ZM 1080.
The anode of these tubes has to be connected via a resistor R_a to the high voltage power supply V_b.

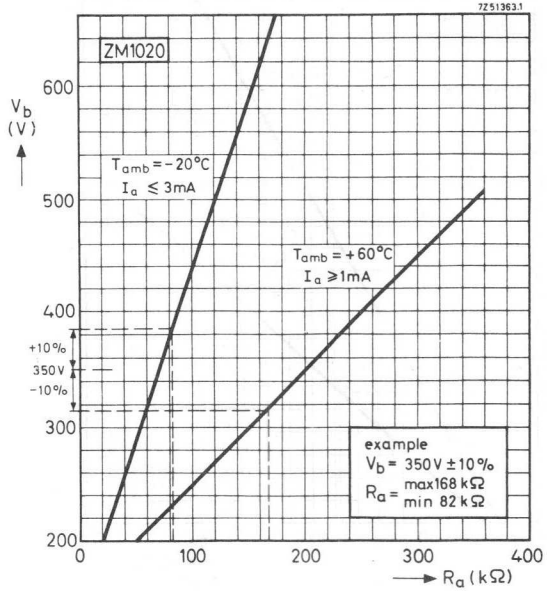
Output transistor conducting

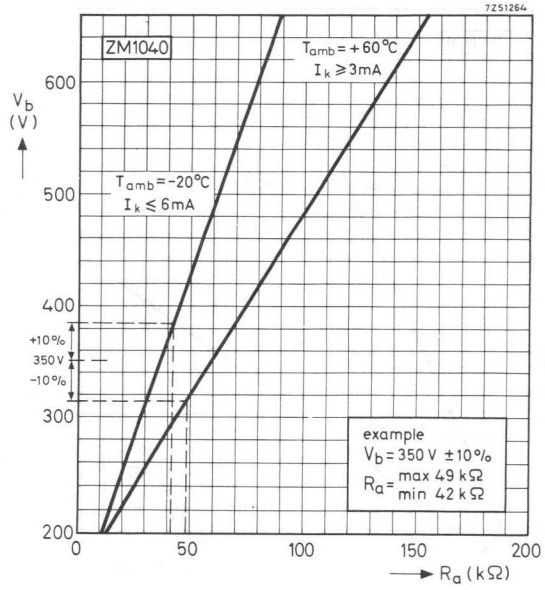
Voltage V_Q = max. 3.2 V

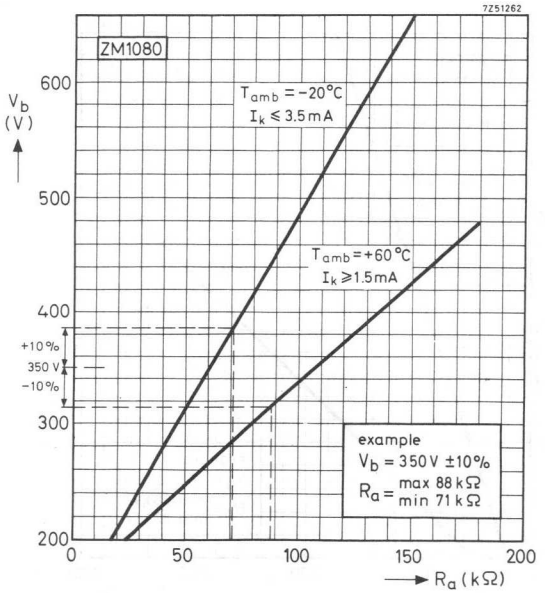
Current I_Q = max. 6 mA

The available output current (I_Q) of the ten numerical outputs Q_o (terminal 1a and 11a) up to and including Q_9 (terminal 10a and 20a) is sufficient to deliver the required current for the numerical indicator tube ZM 1000, ZM 1020, ZM 1040 or ZM 1080.
The relation between the permitted value and tolerances of the high voltage supply V_b and the corresponding anode series resistor R_a for the various indicator tubes over the whole temperature range is given in the following graphs.


7Z53859
ZM1000
V_b (V)
600
500
400
300
200
+10%
350V
-10%
$T_{amb} = -20°C$
$I_a \leq 4.5mA$
$T_{amb} = +60°C$
$I_a \geq 1.5mA$
example
$V_b = 350V \pm 10\%$
$R_a =$ max 113 kΩ min 56 kΩ
0
50
100
150
200
R_a (kΩ)


7Z51363.1
ZM1020
V_b (V)
600
500
400
300
200
+10%
350V
-10%
$T_{amb} = -20°C$
$I_a \leq 3mA$
$T_{amb} = +60°C$
$I_a \geq 1mA$
example
$V_b = 350V \pm 10\%$
$R_a =$ max 168 kΩ min 82 kΩ
0
100
200
300
400
R_a (kΩ)



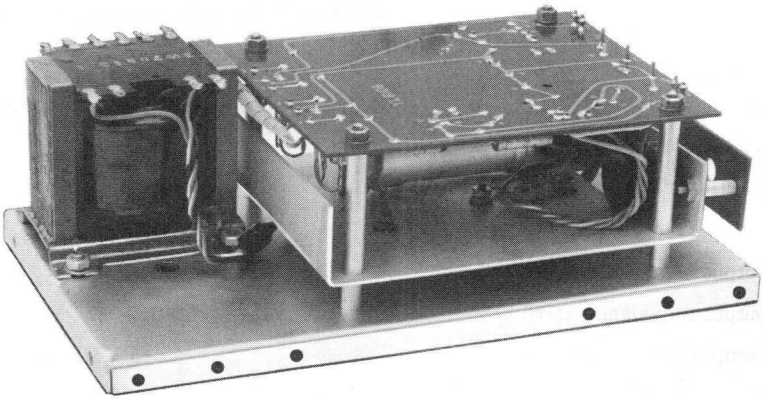


Wiring capacitance at each Q-output: max. 500 pF

ACCESSORIES FOR CIRCUIT BLOCKS

1– SERIES

POWER SUPPLY UNIT



15945/4

Input voltage	220 V_{ac} and 235 V_{ac}
Output voltage	+6 V_{dc} and −6 V_{dc}

APPLICATION

This power supply unit has been designed for use with the circuit blocks of the 100 kHz- and the 1-series. However, it is also suitable as a supply for other transistorised circuits.

CONSTRUCTION

The unit is dimensioned for mounting in the standardized 19" chassis. The power supply unit fits in chassis 4322 026 38240; the base plate of the unit then replaces a side plate of the chassis. The supply unit occupies the same space as four printed-wiring boards.

Dimensions	215 x 125 x 70 mm
Weight	1.5 kg

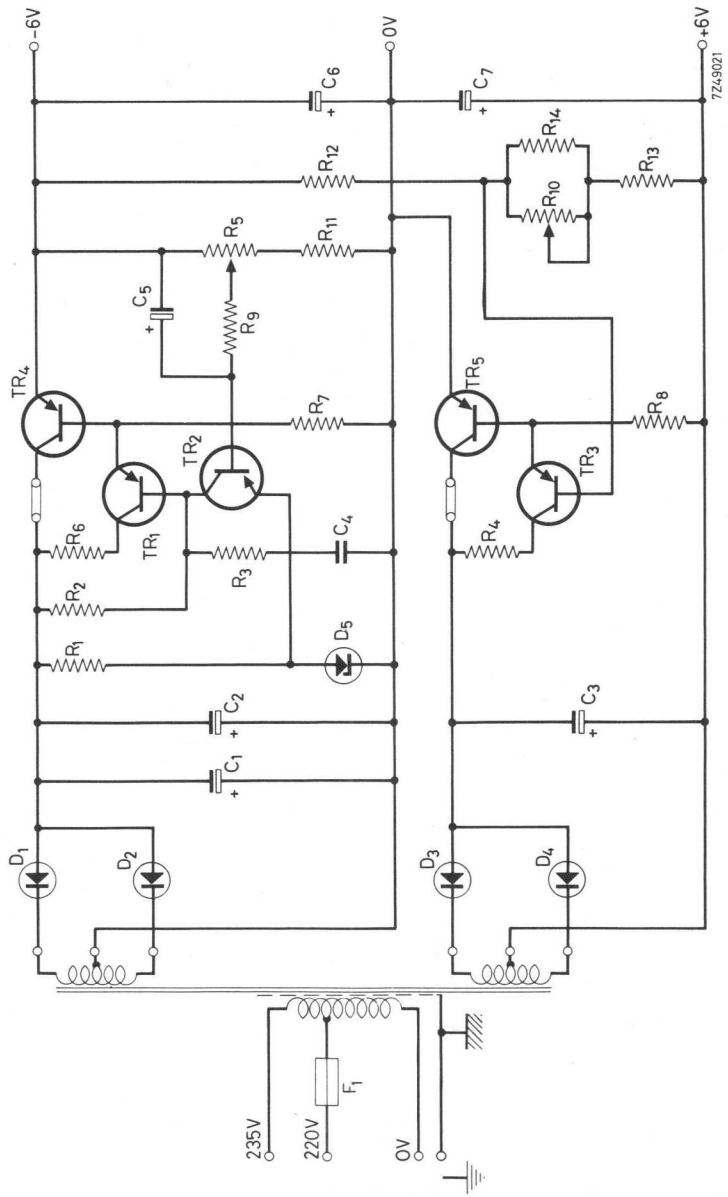
TECHNICAL PERFORMANCE

Input voltage	220 V_{ac} +10 %, −15 %	
	235 V_{ac} +10 %, −15 %	
Frequency	50 to 60	Hz
Fusing	1 A fuse in the 220 V winding only	
−6 V output [1]		
Output voltage	6 V, adjustable ±3 % (R5, see diagram)	
Output current	600	mA
Stability ratio at 220 V	450:1	
Ripple voltage	50	mV_{rms}
Output resistance	0.3	Ω
Output impedance at 10 kHz	0.2	Ω
Temperature coefficient	−3	mV/deg C
+6 V output [1]		
Output voltage	6 V, adjustable ±3 % (R10, see diagram)	
Output current	150	mA
Stability ratio at 220 V	360:1	
Ripple voltage	50	mV_{rms}
Output resistance	1.5	Ω
Output impedance at 10 kHz	0.5	Ω
Temperature coefficient	+6	mV/deg C
Operating-temperature range	−20 to +60	°C
Storage-temperature range	−20 to +75	°C

In systems requiring more than one power supply unit, the earth tags (marked "0 V") may be interconnected, the positive tags (marked "+6 V") and the negative tags (marked "−6 V") must remain strictly separated.

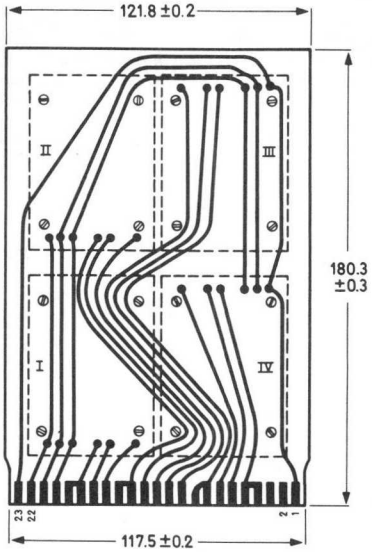
When a system is put into operation for the first time, the output voltages of the power supply units have to be adjusted to 6 V under nominal system load.

1) All values are given for full load.


-6V
0V
+6V
7249021
C6
C7
R14
R12
R13
R10
R5
R11
C5
R9
TR4
TR5
R7
R8
TR2
TR3
TR1
R6
C4
R4
R3
R2
D5
R1
C2
C3
C1
D1
D2
D3
D4
F1
235V
220V
0V

PRINTED-WIRING BOARD FOR FOUR UNITS PA 1

This printed-wiring board fits the mounting chassis 4322 026 38240. It can be used directly with the aid of the mating connector 2422 020 52592. On this board up to four PA 1's can be mounted, the next position in the chassis being left empty.



Terminal location:

1 = E = common supply 0 V (interconnected to terminal 1)

2 = not connected

3 = not connected

4 = N_2, 5 = N_2 } supply max. 60 V } unit nr. IV

6 = Q = output PA 1 } unit nr. IV

7 = W = input PA 1 } unit nr. IV

8 = N_2, 9 = N_2 } supply max. 60 V } unit nr. III

10 = Q = output PA 1 } unit nr. III

11 = W = input PA 1 } unit nr. III

12 = W = input PA 1 } unit nr. II

13 = Q = output PA 1 } unit nr. II

14 = N_2, 15 = N_2 } supply max. 60 V } unit nr. II

16 = W = input PA 1 } unit nr. I

17 = Q = output PA 1 } unit nr. I

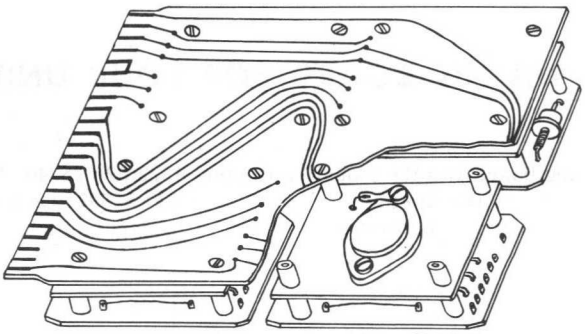
18 = N_2, 19 = N_2 } supply max. 60 V } unit nr. I

20 = N_1 = common supply −6 V

21 = P = common supply +6 V

22 = E = common supply 0 V

23 = E = common supply 0 V



7Z43648

Material	glass epoxy with plated-through holes
Hole diameter	1.2 mm
Contacts	1 x 23, gold plated, pitch 0.2 inch

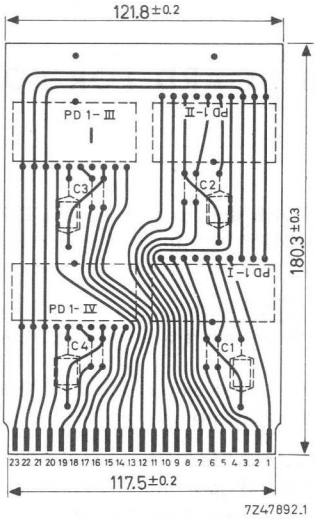
PRINTED-WIRING BOARD FOR FOUR UNITS PD 1

This printed-wiring board with standard dimensions 121.8 mm x 180.3 mm x 1.6 mm (4.8" x 7.1" x 0.0625") is intended to accomplish the mounting of maximum four pulse driver units PD 1 (catalog number 2722 001 13011).

One printed-wiring board PDA 1 with four units PD 1 mounted on it, can be used in conjunction with three reversible counters BCA 1 (catalog number 2722 009 00021).
Two units PD 1 perform shift-pulse amplifying functions between two reversible counters BCA 1, one for the forward and one for the reverse direction.

The printed-wiring board is provided with two wire jumpers for each PD 1. In case the number of trigger- and gate-inputs has to be extended, these wire jumpers can be replaced by diodes, type OA 95. The required connections with the EG- and K-terminals of the PD 1 have already been made in the print pattern.
Furthermore the printed-wiring board is provided with two plated-through holes for each unit PD 1. In case the output-pulse duration of the PD 1 has to be increased, these holes can be used for mounting the required capacitor. The terminals of this capacitor are then directly connected to the K- and L-terminals of the concerning PD 1.

Holes are provided to secure the PD 1 rigidly to the board by means of the locking tag 4322 026 33690.
With the mating connector 2422 020 52592 the printed-wiring board can be used directly in the mounting chassis 4322 026 38240.



Terminal location:

1 = Q_1 = output PD 1-I
2 = EG_1 = extension gate input PD 1-I
3 = K_1 = extension trigger input PD 1-I
4 = G_1 = gate input PD 1-I
5 = A_1 = trigger input PD 1-I
6 = Q_2 = output PD 1-II
7 = EG_2 = extension gate input PD 1-II
8 = K_2 = extension trigger input PD 1-II
9 = G_2 = gate input PD 1-II
10 = A_2 = trigger input PD 1-II
11 = A_3 = trigger input PD 1-III
12 = G_3 = gate input PD 1-III
13 = K_3 = extension trigger input PD 1-III
14 = EG_3 = extension gate input PD 1-III
15 = Q_3 = output PD 1-III
16 = A_4 = trigger input PD 1-IV
17 = G_4 = gate input PD 1-IV
18 = K_4 = extension trigger input PD 1-IV
19 = EG_4 = extension gate input PD 1-IV
20 = Q_4 = output PD 1-IV
21 = N = common supply −6 V
22 = P = common supply +6 V
23 = E = common supply 0 V

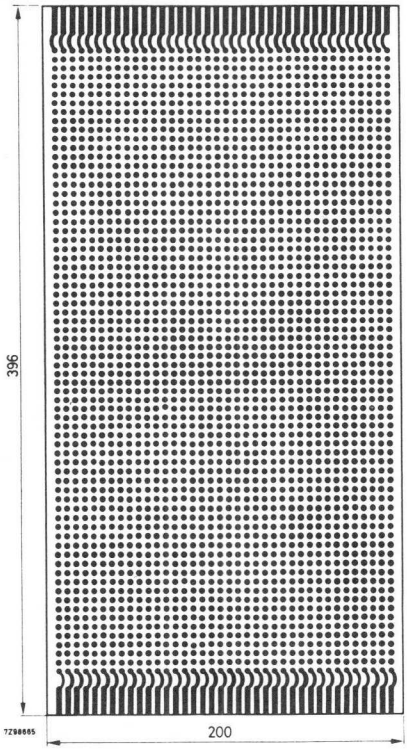
Material	glass epoxy with plated-through holes
Hole diameter	1.2 mm
Contacts	1 x 23, gold plated, pitch 0.2 inch

INPUT AND OUTPUT DATA

See specification of pulse driver unit PD 1 (catalog number 2722 001 13011)

EXPERIMENTERS' PRINTED—WIRING BOARDS

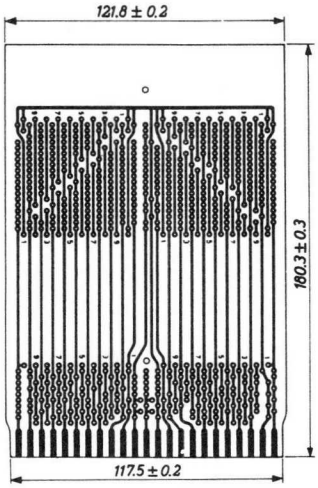
These experimenters' printed-wiring boards are very suitable for circuit blocks of the 100 kHz- and 1-Series.



Material	copper-clad phenolic resin bonded paper	
Grid pitch	5.08 mm (0.2 inch)	
Contacts	gold plated, pitch 0.2 inch	
	single sided 2 x 38	double sided 4 x 38
Holes	with holes	–
Catalogue number	4322 026 34900	4322 026 34910

PRINTED-WIRING BOARD

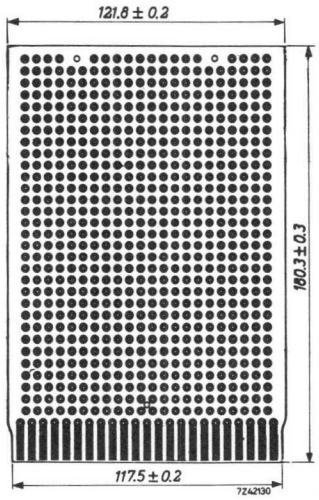
This printed-wiring board is intended for mounting circuit blocks of the 100 kHz- and 1-Series.
It fits the mounting chassis 4322 026 38240.



Material	copper-clad phenolic resin bonded paper with punched holes
Hole diameter	1.3 mm
Contacts	1 x 23, gold plated, pitch 0.2 inch

EXPERIMENTERS' PRINTED—WIRING BOARD

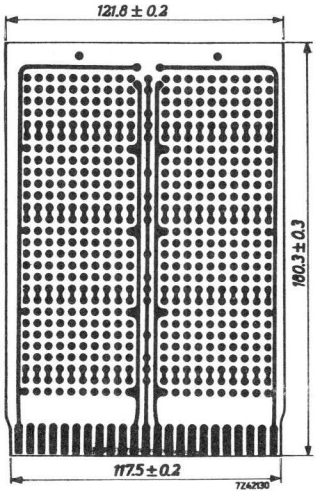
This experimenters' printed-wiring board is very suitable for circuit blocks of the 100 kHz- and 1-Series.
It fits the mounting chassis 4322 026 38240.



Material	copper-clad phenolic resin bonded paper with punched holes
Grid pitch	5.08 mm (0.2 inch)
Hole diameter	1.3 mm
Contacts	1 x 23, gold plated, pitch 0.2 inch

PRINTED—WIRING BOARD

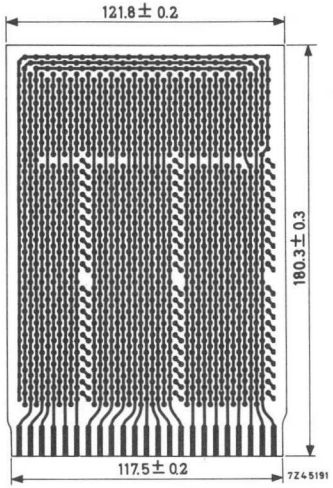
This printed-wiring board for 100 kHz- and 1-Series circuit blocks can accommodate 8 horizontally mounted blocks. Combination of circuit blocks with discrete components is easily possible on this board.
It fits the mounting chassis 4322 026 38240.



Material	copper-clad phenolic resin bonded paper with plated-through holes
Hole diameter	1.2 mm
Contacts	1 x 23, gold plated, pitch 0.2 inch

PRINTED-WIRING BOARD

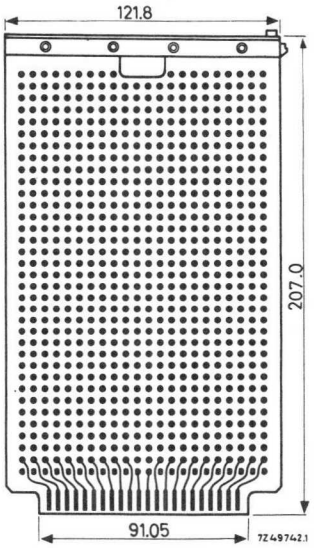
This printed-wiring board is intended for mounting circuit blocks of the 100 kHz- and 1-Series. It fits the mounting chassis 4322 026 38240.



Material	copper-clad phenolic resin bonded paper with plated-through holes
Hole diameter	1.2 mm
Contacts	1 x 23, gold plated, pitch 0.2 inch

EXPERIMENTERS' PRINTED—WIRING BOARD

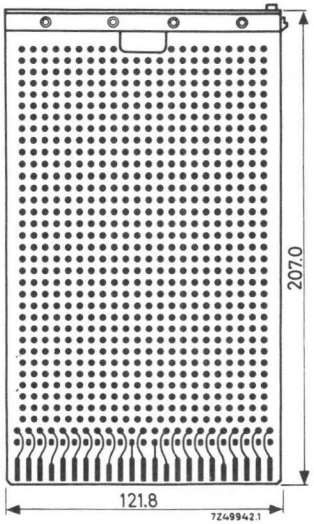
This experimenters' printed-wiring board (with extractor) is very suitable for circuit blocks of the 100 kHz- and 1-Series.
It fits the mounting chassis 4322 026 38230.



Material	phenolic resin bonded paper with holes; on both sides are copper lands around each hole
Grid pitch	5.08 mm (0.2 inch)
Hole diameter	1.3 mm
Contacts	2 x 22, gold plated, pitch 0.156 inch

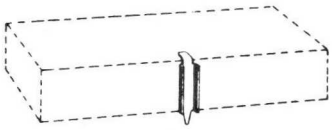
EXPERIMENTERS' PRINTED-WIRING BOARDS

These experimenters' printed-wiring boards (with extractor) are very suitable for circuit blocks of the 100 kHz- and 1-Series.
They fit the mounting chassis 4322 026 38240.



Catalogue number	4322 026 38630	4322 026 38690
Material	phenolic resin bonded paper	glass epoxy
Grid pitch	5.08 mm (0.2 inch)	
Holes	diameter 1.3 mm; on both sides of the board are copper lands around each hole	
Contacts	2 x 23, gold plated, pitch 0.2 inch	

LOCKING TAG



Circuit blocks of the 100 kHz- and 1-Series mounted parallel to the printed-wiring board can be secured rigidly by means of this small tag, which permits soldering in a standard 1.3 mm diameter hole. The minimum supply quantity is 1000 pieces.

STICKERS

These are drawing symbols of circuit blocks printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings. The drawing symbols are as shown on the data sheets of the relevant circuit blocks.
The stickers are available in rolls, each containing 1000 drawing symbols of the same type of circuit block. Each sticker can be separately detached from the roll, without cutting.

for circuit block of type	catalog number of a roll with 1000 stickers
FF 1	4322 026 35780
FF 2	4322 026 35790
FF 3	4322 026 35800
FF 4	4322 026 35810
2.3.N 1	4322 026 35820
2.2.N 1	4322 026 35830
2.3.P 1	4322 026 35840
2.2.P 1	4322 026 35850
2.PL 1	4322 026 35860
2.PL 2	4322 026 35880
EF 1/IA 1	4322 026 35890
2.EF 1	4322 026 35900
2.IA 1	4322 026 35910
2.EF 2	4322 026 35920
2.IA 2	4322 026 35930
2.GI 1	4322 026 34620
PS 1	4322 026 35950
PS 2	4322 026 36820
PR 1	4322 026 36830
OS 1	4322 026 35960
OS 2	4322 026 35980
PD 1	4322 026 30710
PA 1	4322 026 07760

Circuit blocks
for
ferrite core memory drive

INTRODUCTION

In the development and manufacture of magnetic core memories it is essential to have a profound knowledge of the specific characteristics and requirements that are imposed on the core drive circuits.
These circuits should perform their functions with accuracy, efficiency and reliability and this can be met by a proper design and care in manufacture. The different properties of the various cores as well as their responses, dependent on the number of cores per matrix plane and the number of planes per stack, make great demands on those responsible for the design of the complete system and in particular the development of the basic circuits.

The core drive units in this series have been designed especially for properly performing the specific functions in magnetic core memories, such as the sense amplifier, the selection switch, the selection gate and the pulse generator. They should be used in conjunction with 100 kHz-series circuit blocks.

The following four circuit blocks for driving and reading core memories are available:

description	abbreviation	catalog number	page
dual selection switch	2.SS1	2722 001 14001	C5
selection gate	SG1	2722 001 04001	C9
pulse generator	PG1	2722 001 12001	C11
read amplifier	RA2A	2722 001 09011	C15
	RA2B	2722 001 09021	

These circuit blocks have been developed as a part of the complete range of standard 100 kHz circuit blocks. For this reason reference is made to the section "Circuit Blocks 100 kHz Series" for CONSTRUCTION and TEST SPECIFICATION.

DUAL SELECTION SWITCH

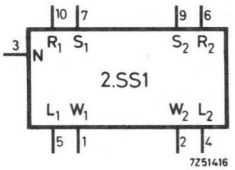
Colour: blue

The unit 2.SS1 contains two identical circuits designed to operate as current switches in series with the drive wires of a ferrite-core memory.

The switching of the n-p-n output transistor is controlled by a d.c. input level applied to a built-in pre-amplifier stage.

Frequency range : 0 - 100 kHz
Ambient temperature range:
operating 0 to 60 °C
storage -25 to 75 °C
Weight : approx. 20 g

drawing symbol



CIRCUIT DATA

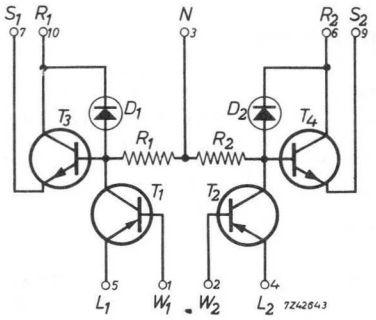


Fig 1

Terminal
1 = W_1 = control input 1
2 = W_2 = control input 2
3 = N = supply -6V
4 = L_2 = current supply T2
5 = L_1 = current supply T1
6 = R_2 = switch 2 in
7 = S_1 = switch 1 out
8 = = not connected
9 = S_2 = switch 2 out
10 = R_1 = switch 1 in

Power supply

Terminal 3 : $V_N = -6V \pm 2\%$, $-I_N = 8mA$ (nominal value)

Terminals 4 and 5 via a current stabilisation circuit (either resistor or transistor) to V_P.

$V_P = +6V \pm 2\%$, I_P = max 25 mA each terminal

Terminals 6 and 10 : I_{RS} see output data

APPLICATION DATA

The unit is normally used in combination with other standard circuit blocks for ferrite-core memory operation.

Control input (W-terminals)

The W terminals are directly connected to the output terminals of the driving selection gate SG1.

Line input (L-terminals)*

The L terminals are connected to a current source which can be common to all selection switches operating at the same side of the core matrix (Fig 2).

For the selection switches operating at the negative supply voltage side of the matrix (terminals 5 of both units 2.SS1 in Fig 2):

Required current I_L = approx. 15 mA (16 mA)**

Note - Usually a $620\Omega \pm 5\%$ ($510\Omega \pm 5\%$)** resistor is used between the inter-connected L terminals and the +6V supply.

For the selection switches operating at the positive supply voltage side of the matrix (terminals 4 of both units 2.SS1 in Fig 2):

Required current I_L = approx. 23 mA (25 mA)**

Notes - Usually a grounded base transistor (e.g. type ASY 80) with a collector resistor of $47\Omega \pm 5\%$ and an emitter resistor of approx. $270\Omega \pm 5\%$ ($220\Omega \pm 5\%$)** is used between the inter-connected L terminals and the +6V supply.

* I_L = 0 mA T_1 and T_2 non-conducting
I_L = 16 mA T_1 conducting
I_L = 25 mA T_2 conducting
I_L = 41 mA T_1 and T_2 conducting

** The values between brackets are given with respect to a switch current of 310 mA.

- For memories in which the group selection principle is applied a voltage of max. 2 V can be tolerated across the drive wire during the switching-on of the drive current.

Output (R- and S-terminals)

The output terminals are connected in series with a group of drive wires.

Selection switch conducting

Current I_{RS} = max. 250 mA (310 mA) **

Voltage V_{RS} = max. 0.8 V peak

Selection switch non-conducting

Current I_{RS} = max. 0.1 mA

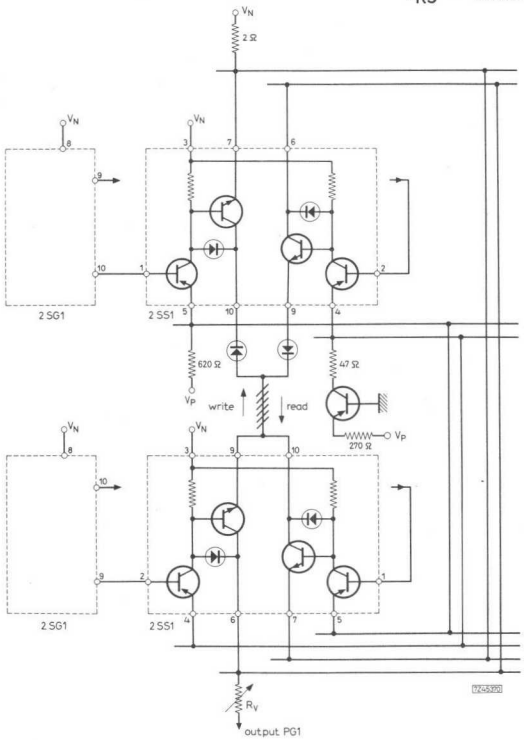


Fig.2

Notes
- When a current is flowing towards the unit, the positive sign is used.
- Unless differently specified, all voltage and current figures quoted represent absolute limiting values.

** The values between brackets are given with respect to a switch current of 310 mA.

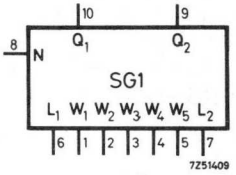
SELECTION GATE

Colour: orange

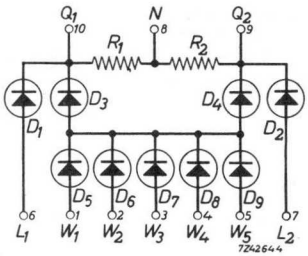
The unit SG1 is designed to perform a two-level AND operation between address register and selection switches in ferrite-core memories.
The W input AND gate which decodes the selection register information, is followed by a twin two-input AND gate to perform the Read/Write control function.

Frequency range : 0 - 100 kHz
Ambient temperature range:
operating 0 to +60 °C
storage -25 to +75 °C
Weight : approx. 20 g

drawing symbol



CIRCUIT DATA



Terminal 1 = W_1 = address - selection input 1
2 = W_2 = address - selection input 2
3 = W_3 = address - selection input 3
4 = W_4 = address - selection input 4
5 = W_5 = address - selection input 5
6 = L_1 = Read/Write control input 1
7 = L_2 = Read/Write control input 2
8 = N = supply -6V
9 = Q_2 = output 2
10 = Q_1 = output 1

Power supply

Terminal 8 : $V_N = -6V \pm 2\%$, $-I_N = 2mA$ (nominal value)

APPLICATION DATA

The unit is normally used in combination with the dual selection switch 2.SS 1 and other circuit blocks for ferrite-core memory operation.

Selection input (W-terminals)

The W terminals are connected to the flip-flops in the address selection register. Depending on the size of the memory, this connection is done directly or via adequate amplifier stages.

Voltage	$-V_W$ = max 0.2V
Required current	I_W = min 1 mA at $V_W = 0V$

Read/Write control input (L-terminals)

The L_1 and L_2 terminals are connected to opposite voltage levels, normally derived from a Read/Write control flip-flop. Depending on the memory capacity, the interconnected L_1 respectively L_2 terminals are driven directly or via a 2.IA1 - 2.IA2 amplifier chain.

Voltage	$-V_L$ = max 0.2 V
Required current	I_L = min 1 mA at $V_L = 0V$

Output (Q-terminals)

The Q terminals are directly connected to the W terminals of the driven dual selection switch (2.SS1).

Notes
- When a current is flowing towards the unit, the positive sign is used.
- Unless differently specified, all voltage and current figures quoted represent absolute limiting values.

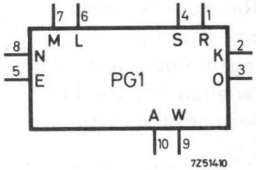
PULSE GENERATOR

Colour: green

The unit PG 1 has been designed to operate as a drive current switch for the drive (X and Y) wires and the inhibit (Z) wires of a ferrite-core memory.

The switching of the n-p-n output transistor is controlled by an input level change applied to a built-in pre-amplifier stage.

Frequency range	:	0 - 100 kHz
Ambient temperature range:		
operating		- 20 to + 60 °C
storage		- 25 to + 75 °C
Weight	:	approximately 20 g



drawing symbol

CIRCUIT DATA

Terminal 1 = R = drive current input
2 = K = to be connected to terminal 4*
3 = O = to be connected to terminal 4*
4 = S = drive current output
5 = E = common supply 0 V
6 = L = terminal for external capacitor
7 = M = supply - 6 V*
8 = N = supply - 6 V*
9 = W = d.c. input
10 = A = trigger input

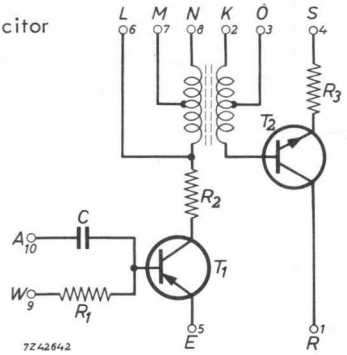


Fig 1

* Depending on the application, see Fig 4 and table "Switching and delay times".

Power supply

Terminal 5: V_E = 0V common
7 or 8: V_N = -6V ± 2%, $-I_N$ = 50mA (nominal value)

Terminal 3 and 4 or 2 and 4: see Fig 3a or b, $-I_S$
Terminal 1 : see Fig 3a or b, I_R
} see output data PG 1

APPLICATION DATA

The unit is normally used in combination with other standard circuit blocks, for ferrite-core memory operation.

Input circuit PG 1

The PG 1 is normally triggered by the Q-output of an IA 1 or IA 2 inverter amplifier by connecting this output to input terminal A. For proper functioning a diode must be connected between the terminals A and W (cathode to terminal A), see Fig 2. A positive going input signal applied to the PG 1, switches the output transistor into the conducting state.

Driving requirements of the PG 1

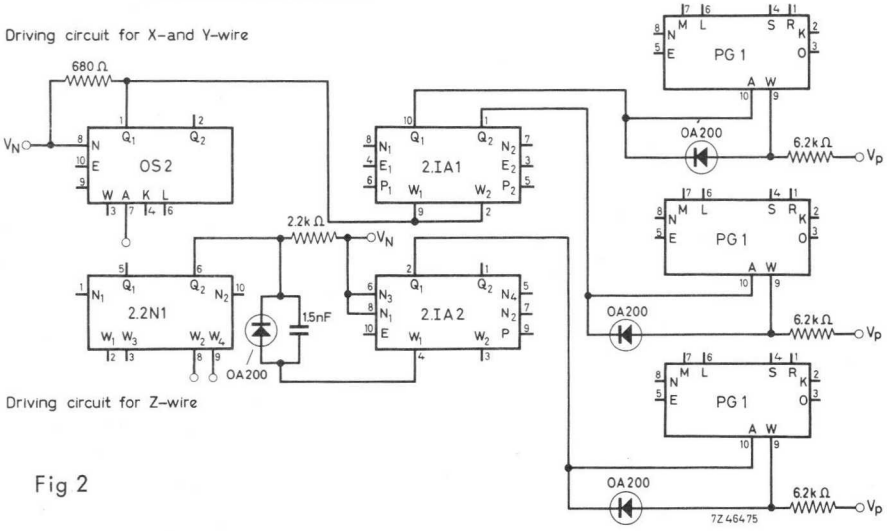


Fig 2

Output data PG 1

The output terminals R and S are connected in series with a group of X and Y wires or a Z wire.

Pulse generator conducting

	temperature	- 20 °C	0 °C	60 °C
Current	I_{RS} max	250 mA	310 mA	250 mA
Voltage	V_{RS} max	1.5 V_{peak}	1.7 V_{peak}	1.5 V_{peak}

For temperatures between - 20 ° and + 60 ° the maximum values for I_{RS} can be found by linear interpolation.

Pulse generator non-conducting

Current I_{RS} = max 2.5 mA
at V_{RS} = max 15 V_{peak}

To adapt the current I_{RS} to the drive current requirements of the X, Y and Z wires an external resistor has to be inserted in the circuit in series with the above mentioned wires. Two alternative circuits are given below.

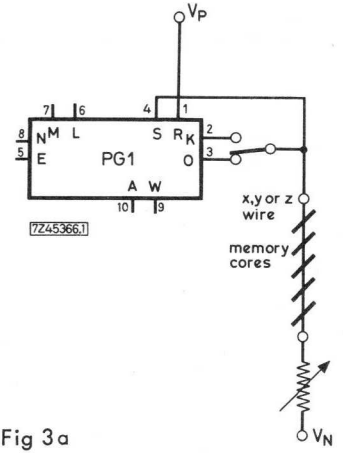


Fig 3a

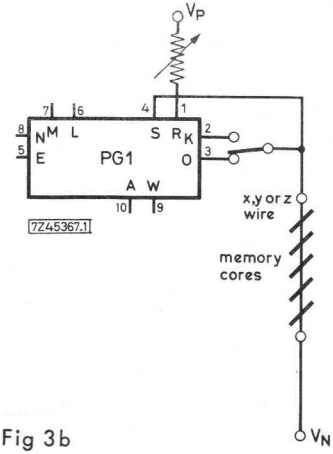


Fig 3b

Switching and delay times (for orientation only)

The duration of the output pulse depends on the duration of the input pulse. When short output pulses are required V_N has to be connected to the terminals 3, 4 and 7 (Fig. 4a) and for wider output pulses to 2, 4 and 8 (Fig. 4b).

The switching and delay times given below, apply for the driving circuits shown in Fig. 4a and 4b.

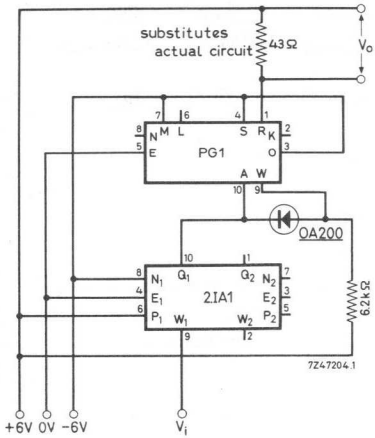
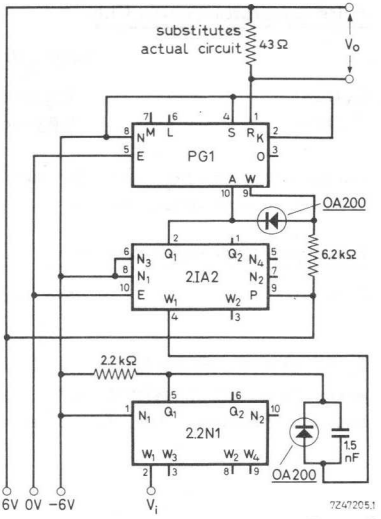
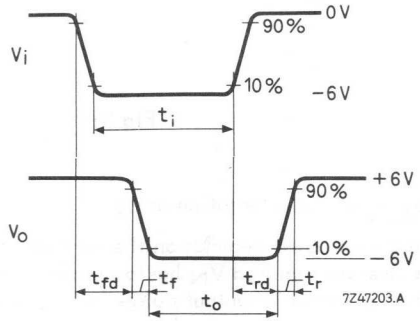


Fig. 4a DRIVING CIRCUIT FOR X-AND Y WIRE



DRIVING CIRCUIT FOR Z-WIRE Fig. 4b

		Fig. 4a	Fig. 4b	
Input pulse duration	t_i	2	4	µs
Repetition frequency	f_i	100	50	kHz
Fall delay	t_{fd} = max	0.2	0.2	µs
Fall time	t_f = max	0.1	0.1	µs
Output pulse duration	t_o = min	--	--	
Rise delay	t_{rd} = max	1	1	µs
Rise time	t_r = max	0.1	0.1	µs



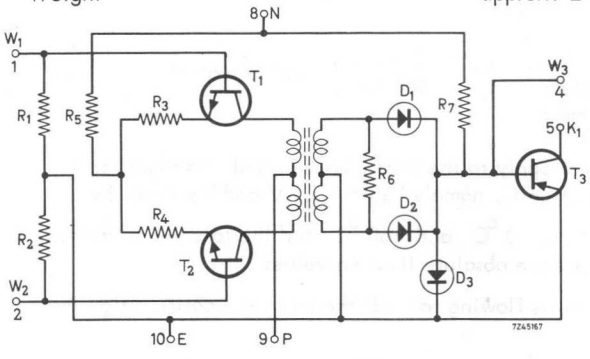
Notes
- When a current is flowing towards the unit, the positive sign is used.
- Unless differently specified, all voltage and current figures quoted represent absolute limiting values.

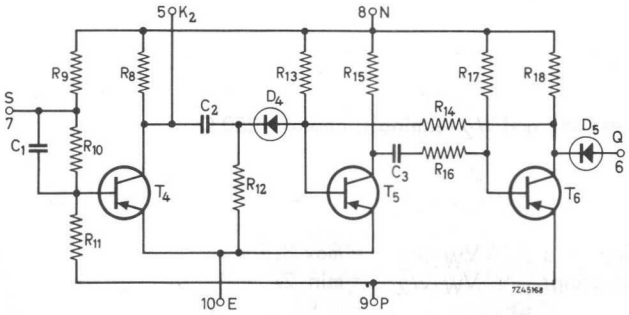
READ AMPLIFIER

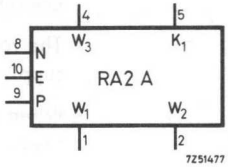
Colour : yellow

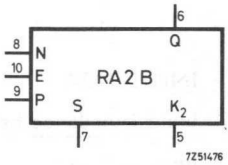
This read - or sense amplifier, consisting of two circuit blocks of standard dimensions called RA 2 A and RA 2 B, is designed to amplify the signals originating from the sense wire of ferrite-core memories.
The unit RA 2 A, to which the sense voltage is applied, contains a pre-amplifier circuit and a full wave rectifier circuit.
The input is balanced, so either positive going or negative going input signals can be applied.
Its output signal is applied to the input of the second unit RA 2 B, which contains a strobing circuit as well as a pulse stretching circuit. The output of the RA 2 B can be used directly to set a flip-flop of the 100 kHz range on its W-input terminal.
Ambient temperature range:

operating	0 to + 60 °C
storage	- 25 to + 75 °C
Weight	approx. 2 × 20 g









Drawing symbols

Terminal Location

RA 2 A:

Terminal 1 = W_1 } input
2 = W_2 }
3 = not connected
4 = W_3 = terminal for external resistor
5 = K_1 = to connect to terminal 5 of RA 2 B
6 = not connected
7 = not connected
8 = N = supply -6V
9 = P = supply +6V
10 = E = common supply 0V

RA 2 B:

Terminal 1 = not connected
2 = not connected
3 = not connected
4 = not connected
5 = K_2 = to connect to terminal 5 of RA 2 A
6 = Q = output
7 = S = input STROBE pulse
8 = N = supply -6V
9 = P = supply +6V
10 = E = common supply 0V

Power Supply

RA 2 A:

Terminal 8 = V_N = -6V ± 5%, - I_N = 12.8 mA } nominal values
9 = V_P = +6V ± 5%, I_P = 11.5 mA }
10 = V_E = 0V common

RA 2 B:

Terminal 8 = V_N = -6V ± 5%, - I_N = 15.3 mA } nominal values
9 = V_P = +6V ± 5%, I_P = 9.1 mA }
10 = V_E = 0V common

Notes
- The data given apply to the most adverse supply voltages for a combination of units, namely V_N = -5.7V and V_P = + 6.3V.
- The temperatures 0 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input impedance between W_1 and W_2 terminals: approx. 250 Ω

Input voltage:

W-terminals:

Transistor T_3 conducting : $V_{W_1W_2}$ = max 8.5 mV
Transistor T_3 non-conducting: $V_{W_1W_2}$ = min 27 mV

The sensitivity of the read amplifier RA 2 A can be adjusted with the aid of an external resistor between terminal W_3 and V_N or V_P. The resistor connected to V_N decreases the sensitivity (absolute min. value is 1.6 kΩ), whilst the resistor connected to V_P increases the sensitivity (absolute min. value is 15 kΩ). This permits a sensitivity adjustment to match the threshold level of the read amplifier (where transistor T_3 starts to conduct) to the output sense voltage of a certain memory stack.

S-terminals:

Transistor T_4 conducting : $-V_S$ = min. 3.24V, I_S = max. 100 µA
= max. $-V_N$

Transistor T_4 non-conducting: $-V_S$ = max. 0.85V
= min. 0V , I_S = max. 2.5 mA

OUTPUT DATA

When K_1 - terminal of the RA 2 A is connected to the K_2 - terminal of the RA 2 B, transistor T_6 of the latter will be in the non-conducting state, as soon as transistor T_3 of RA 2 A as wel as transistor T_4 of RA 2 B have reached their cut-off state. This situation is required for setting a FF1, FF2, FF3 or FF4 on its input W - terminal.

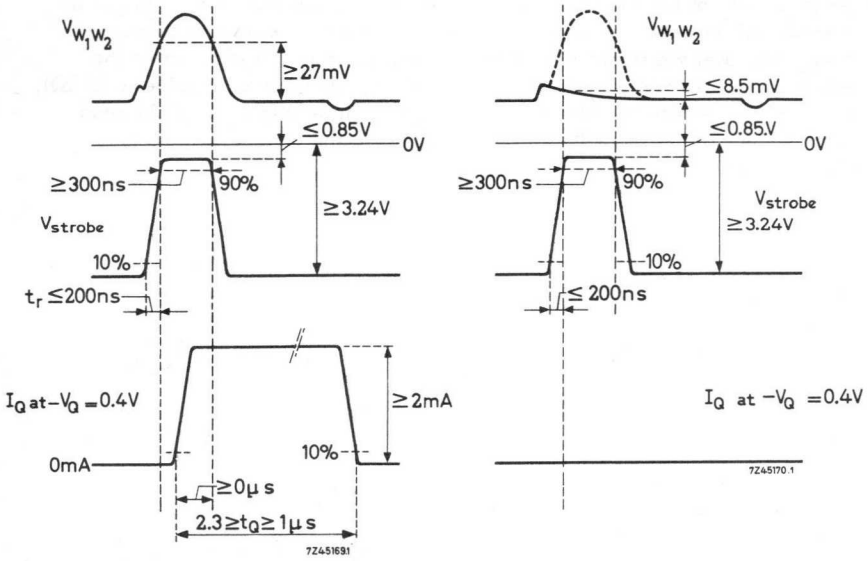
Transistor T_6 of RA 2 B non-conducting:

Voltage $-V_Q$ = min. 0.4V (at I_Q = 2 mA)
Duration of the output pulse t_Q = min. 1.0 µs
= max. 2.3 µs

Transistor T_6 of RA 2 B conducting:

Max. permissible voltage at output terminal Q is + 5V
At $-V_Q$ = 0.4V $-I_Q$ = max. 70 µA

The figure below elucidates the two situations, namely transistor T_6 of the RA 2B conducting or cut-off. Its state is determined by the fact whether the input voltage V_{W1W2} and the strobe pulse V_S meet their respective minimum requirements.

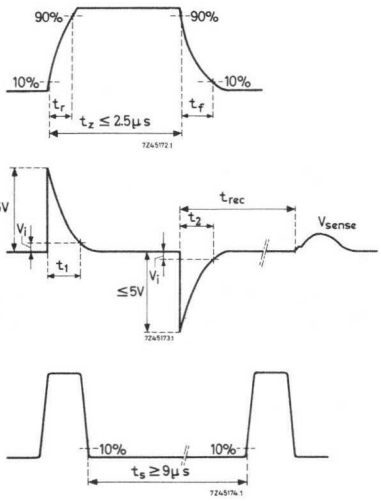


GENERAL REQUIREMENTS

Inhibit Current

1) The rise time t_r and fall time t_f of the current I_Z through the inhibit wire should have such a slope, that the induced voltage on the sense wire meets the condition:
$t_1 = t_2$ = max. 1.5 µs at V_i = 27 mV ± 1 mV

2) The minimum recovery time t_{rec} between the inhibit pulse and the read pulse has to be min. 5 µs for $t_1 = t_2$ = max. 1.5 µs at V_i = 27 mV ± 1 mV. (recovery time RA 2 A)

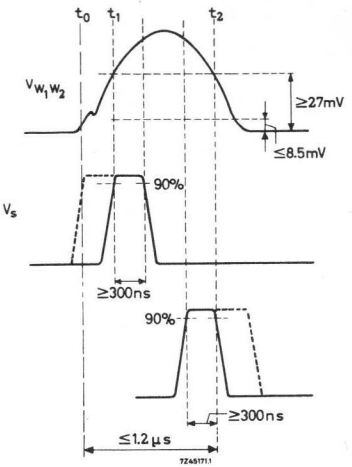


Strobe Pulse

1) The minimum time between two successive strobe pulses has to be min. 9 µs.
(recovery time RA 2 B)

2) When V_{W1W2} = min 27 mV and $-V_S$ = max 0.85 V a negative going output pulse is generated on the output terminal of the RA 2B. The coincidence of the input voltage V_{W1W2}, measured between the times t_1 and t_2, and the strobe pulse V_S, measured at the 90% level, has to be min 300 ns.
The two extreme situations are elucidated in the figure beside.

3) When however the sense wire is also carrying interference or disturbing signals, the strobe pulse V_S has to be situated very precisely with respect to the input voltage V_{W1W2}.



Circuit blocks

10-Series

INTRODUCTION

The "10-series" presents a range of circuit blocks, developed to meet the requirements of the industry for machine-control, process control, data handling, measuring- and signalling systems. With this "10-series", systems are designed and built quickly, economically and with the utmost reliability.

The "10-series" offers a complete range, consisting of various logic elements together with all necessary auxiliary units including timers, pulse shapers, input and output devices. Moreover, all accessories for a quick and easy construction of equipment are available e.g. power supplies, printed-wiring boards, etc., see section "ACCESSORIES FOR CIRCUIT BLOCKS 10-SERIES".

Types of circuit blocks

In this series the following units and assembled panels are available:

description	abbreviation	catalog number	page
Dual positive gate inverter amplifier	2.GI 10	2722 004 08001	D17
Dual positive gate inverter amplifier	2.GI 11	2722 004 08011	D21
Dual positive gate inverter amplifier	2.GI 12	2722 004 08021	D25
Flip-flop	FF 10	2722 004 00001	D29
Flip-flop	FF 11	2722 004 00011	D33
Flip-flop	FF 12	2722 004 00021	D39
Dual trigger gate	2.TG 13	2722 004 15001	D45
Dual trigger gate	2.TG 14	2722 004 15011	D49
Quadruple trigger gate	4.TG 15	2722 004 15021	D53
Timer unit	TU 10	2722 004 18001	D57
Gate amplifier	GA 11	2722 004 17001	D63
One-shot multivibrator	OS 11	2722 004 10011	D69
Pulse driver	PD 11	2722 004 13011	D75
Pulse shaper	PS 10	2722 004 11001	D81
Relay driver	RD 10	2722 004 16001	D85
Relay driver	RD 11	2722 004 16011	D89
Power amplifier	PA 10	2722 032 00021	D93
Printed-wiring board for PA 10	PAA 10	4322 026 38680	D219
Numerical indicator tube driver	ID 10	2722 004 20001	D97
Decade counter/numerical indicator tube driver assembly	DCA 10	2722 009 020..	D103
Dual decade counter/numerical indicator tube driver assembly	2.DCA 11	2722 009 020..	D123
Dual decade counter assembly	2.DCA 12	2722 009 020..	D141

description	abbreviation	catalog number	page
Reversible decade counter/numerical indicator tube driver assembly	BCA 10	2722 009 021..	D161
Dual shift register assembly	2.SRA 10	2722 009 03001	D189
Reversible shift register assembly	RSR 10	2722 009 03011	D201

A number of static input and output devices can be used in conjunction with 10-series circuit blocks, see chapter INPUT/OUTPUT DEVICES.

Economic equipment design and construction are inherent to the following features:

- all circuits are compatable with little circuit diversity permitting simple and direct interconnections of the blocks within the range
- high "fan-out" figures and built-in logic facilities reduce the total number of blocks in a system considerably. They also facilitate later additions and modifications
- easy to use loading table enables the system design to be completed quickly
- the possibility of extending gate-, trigger-, and set-inputs makes the circuit blocks particularly valuable, where flexibility in equipment design is required
- input and output currents of the blocks are designed in a way that external components are unnecessary. Only for extension of the number of inputs, diodes have to be mounted externally
- the uniformity of terminal configuration reduces the time for interwiring the blocks and facilitates the design of printed-wiring boards

Outstanding reliability has been secured by:

- "worst-case" design of all circuits, where calculations have been performed with end-of-life data of all components
- use of professional semi-conductors
- careful testing and inspection of individual components and assemblies before, during and after manufacture
- quality control on running factory production, which ensures a product of equal and high quality
- built-in threshold against interference, which render the "10-series" particularly attractive for use in industrial environments
- printed-wiring circuits with plated through holes; the encapsulation and sealing techniques give the circuit block virtual immunity from the effects of humidity, vibration and shock

For detailed design and application information the publication "Design with 10-series Circuit blocks" should be consulted.

CONSTRUCTION

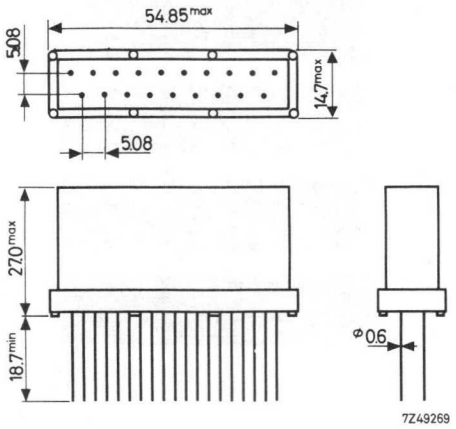
A circuit block is a small encapsulated unit containing a basic electronic circuit, designed to accept and operate upon a specific type of input signal and to produce a specific type of electrical output. A number of different blocks can be combined to form larger parts of electronic systems.

The blocks are housed in standard cases of two different heights.
The maximum overall dimensions are:

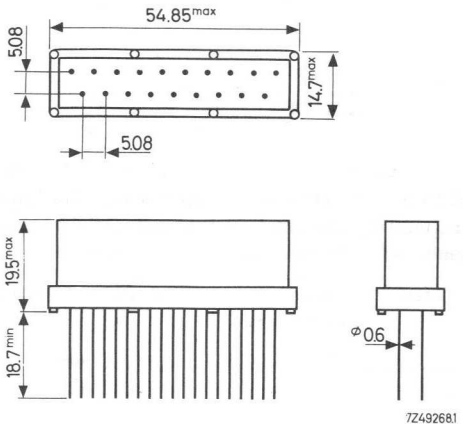
High standard case 54.85 mm x 14.70 mm x 27.00 mm
Low standard case 54.85 mm x 14.70 mm x 19.50 mm

Both cases have 19 terminals, protruding the bottom side of the cases in two rows.
The distance between the two rows is 5.08 mm ± 0.1 (0.2") and the distance between the wires in one row is 5.08 mm ± 0.1 (0.2"), in accordance with the IEC standard hole grid for printed-wiring boards.

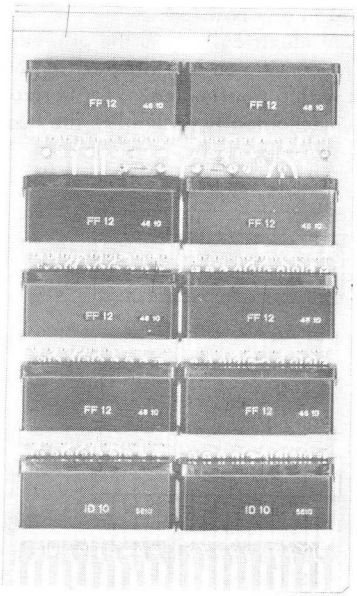
The unit can be mounted in any position.
To insulate the metal can electrically from the printed-wiring conductors for vertical and horizontal mounting on a printed-wiring board the terminal side of the unit is equipped with a plastic sleeve; for horizontal mounting the top side of the unit can be mechanically secured to the board with the aid of a special locking cap.



High standard case



Low standard case



RZ 22603-9

Assembled printed-wiring board

CHARACTERISTICS

Temperature range

Operating temperature: -25 °C to +55 °C.
For temperatures below 0 °C, derated output data are issued in the individual data sheets.
Storage temperature: -55 °C to +75 °C.

Count rate

For a.c. logic applications: approx. 30 kHz
For d.c. logic applications: approx. 65 kHz

Power supply

terminals		operating
9	V_N	-12 V ± 5%
10	V_E	0 V common
19	V_P	+12 V ± 5%

The average power dissipation of the logic blocks is 50 to 100 mW.

Logic levels

	operating		limiting values	
	maximum	minimum	diode inputs	outputs
State "1"	V_P	2/3 V_P	13V	15V
State "0"	+0.3 V	0 V	-2V	0V

TEST SPECIFICATIONS

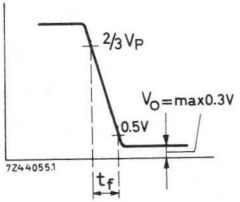
Before and during manufacture samples of circuit blocks are regularly subjected to the following tests:

1. Vibration test according to method 201A of MIL-STD-202.
   Frequency 10-55 Hz, with amplitude of 0.76 mm.
2. Shock test according to method 202A of MIL-STD-202.
   Acceleration 50 g in 3 perpendicular directions.
3. Temperature-cycling test according to method 102A of MIL-STD-202.
   Condition D, 5 cycles from - 55 °C to + 85 °C.
4. Accelerated humidity test according to method 106A of MIL-STD-202.
   10 cycles as indicated in Fig. 1 page 2 of method 106A.
5. Long-term humidity test according to MIL-STD-202, method 1034. Units not operating. Duration 56 days at 40 °C and relative humidity 95%.
   Measurements after 7, 14, 28 and 56 days.
6. As item 5, but units operating under the most unfavourable electrical conditions regarding supply voltages, output load and input characteristics.
7. Long-term test at maximum temperature according to method 108 of MIL-STD-202.
   Test condition E, 55 °C during 1500 hours.
   Units operating under the most unfavourable electrical conditions.
   Measurements after 250, 500, 1000 and 1500 hours.
8. Terminals tested on strength, tests on mounting, soldering, lacquer and coding.

TIME DEFINITIONS

1 Fall time : t_f

The time in which the input- respectively output voltage changes from 2/3 Vp to 0.5 V.

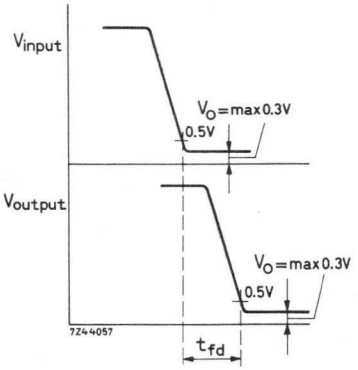


2 Fall delay : t_{fd}

The time, between the 0.5V-points of the negative-going transients of the input- and output voltages.
This fall delay t_{fd} is related to:

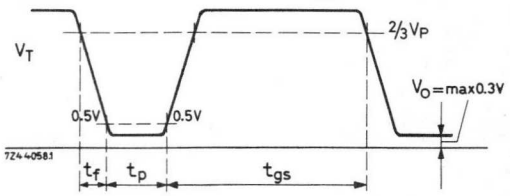
a) Gate invertors (GI's) — the input- and output voltage, the latter measured over 2 stages.

b) Flip-flops (FF's) — the input voltage and the negative-going output voltage.



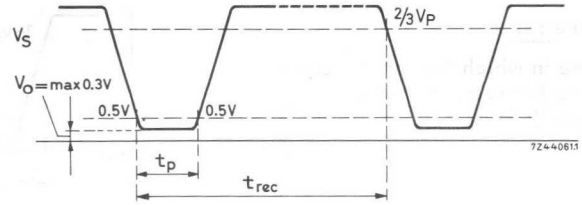
3 Trigger input data FF's and TG's

t_f = fall time
t_p = pulse duration
t_{gs} = trigger gate setting time



4 Set/reset input data FF's

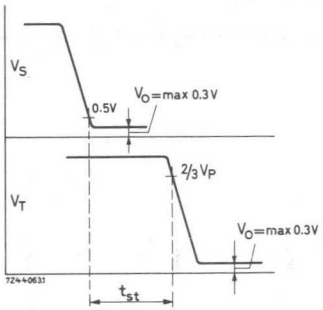
t_p = the duration of the set/reset (S)-pulse
t_{rec} = the recovery time, which is the time between the successive pulses on the different S-terminals of a flip-flop.

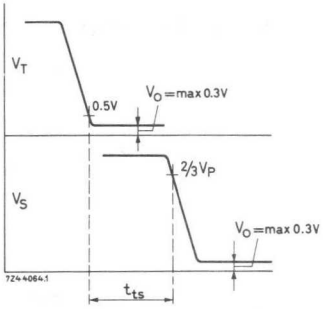


5 Inhibiting time between S- and T-signals of FF's

a) t_{st} = the inhibiting time between a set(S)-signal and a successive trigger(T)-signal of a flip-flop.

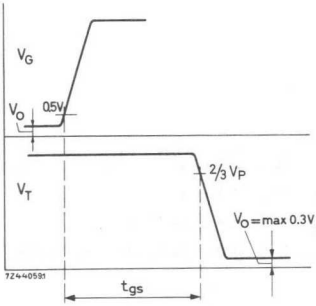
b) t_{ts} = the inhibiting time between a trigger(T)-signal and a successive set(S)-signal of a flip-flop.





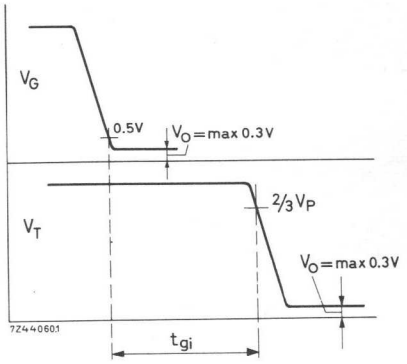
6 Trigger gate setting-time : t_{gs}

The time the gate(G)-signal shall be present in advance to open the gate for the trigger(T)-signal.



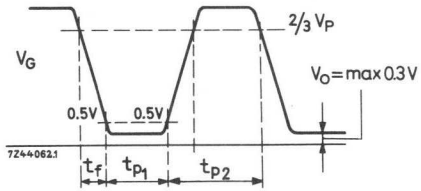
7 Trigger gate inhibiting time : t_{gi}

The time the gate(G)-signal shall be present in advance to close the gate for the trigger(T)-signal.



8 Input data GI's

t_{p1} = the duration of "positive low" input signals
t_{p2} = the duration of "positive high" input signals



INPUT AND OUTPUT DATA

INPUT DATA

unit	terminal	note	direct current	transient charge
FF11, FF12	G		1.1 mA	1.2 nC
2.TG13, 2.TG14, 4.TG15	T	gate open	1.1 mA	3.4 nC
FF10, FF11, FF12	S		1.95 mA	2.8 nC
2.GI 10, 2.GI 11, 2.GI 12	G		1.1 mA	2.1 nC
GA11	G		1.1 mA	1.2 nC
OS11	G		1.1 mA	1.2 nC
	T	gate open	1.1 mA	2.3 nC
TU10, PD11	G		1.1 mA	1.2 nC
	T	gate open	1.1 mA	3.2 nC
RD10, RD11	G		4.7 mA	3.4 nC
PA10	G		5.3 mA	5.2 nC

OUTPUT DATA

unit	terminal	note	direct current	transient charge
FF10, FF11, FF12	Q_1, Q_2		8.2 mA	27 nC
2.GI 10, 2.GI 11, 2.GI 12	Q		8.2 mA	9 nC
GA11	Q		62 mA	75 nC
OS11	Q_1		8.6 mA	24 nC
	Q_2		12.8 mA	29 nC
TU10	Q		32 mA	30 nC
PD11	Q		100 mA	185 nC
PS10	Q		10 mA	39 nC
RD10, RD11	Q		200 mA	
PA 10	Q		2 A	

LOADING RULES

1 Verify that the sum of the required d.c. input currents of the driven units does not exceed the available d.c. output current of the driving unit.

2 When however T-inputs are incorporated in the driven units, the transient charges must also be verified.

3 Only driven units, of which all inputs are high, do load the driving stage during the negative going transient.

4 The wiring capacitance consumes an extra charge of 0.007 nC/pF.

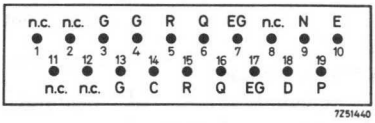
5 T-inputs of closed gates do not require any current or charge.

6 The verifications mentioned above hold for operations at the worst combination of supply voltage tolerance (12V $\pm$ 5%) and ambient temperature between 0 and +55 °C. For temperatures below 0 °C, derating figures are issued in the individual data sheets.

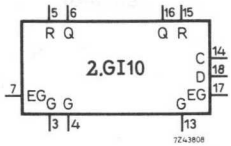
DUAL POSITIVE GATE INVERTER AMPLIFIER

The unit comprises a single input-and a double input positive diode gate-inverter combination, together with one separate diode which can be used to extend the number of gate (G) inputs on any of the two circuits at the extension gate inputs EG.
The collectors Q of the two transistors are not connected with their corresponding collector resistors R. Therefore with the two transistors a logical operation can be performed by interconnecting the two collectors Q with one collector resistor R. The second collector resistor R must be left disconnected.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

Ambient temperature range:		
	operating	-25 to +55 °C below 0 °C: derated output data
	storage	-55 °C to +75 °C
Weight		approx. 30 g
Case		low standard case



terminal location

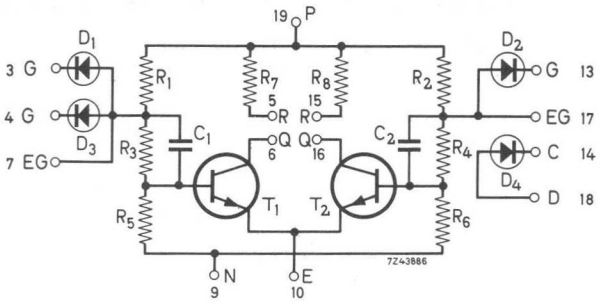


drawing symbol

CIRCUIT DATA

Terminal

1 = not connected
2 = not connected
3 = G = gate input
4 = G = gate input
5 = R = connection collector resistor
6 = Q = output
7 = EG = extension gate input
8 = not connected
9 = N = supply −12 V
10 = E = common supply 0 V
11 = not connected
12 = not connected
13 = G = gate input
14 = C = cathode separate diode
15 = R = connection collector resistor
16 = Q = output
17 = EG = extension gate input
18 = D = anode separate diode
19 = P = supply +12 V



Power supply

Terminal 9 : V_N = −12 V ±5%, $-I_N$ = 0.6 mA
10 : V_E = 0 V common
19 : V_P = +12 V ±5%,
I_P = 2.8 mA (both transistors non-conducting)
= 3.9 mA (one transistor conducting)
= 5.1 mA (both transistors conducting)

The current values are nominal

INPUT REQUIREMENTS (at V_P = 11.4 V and V_N = −12.6 V unless specified differently).

Transistor conducting (output level "positive low")

Voltage at all gate inputs V_G = min. 2/3 V_P
= max. V_P

Type of diodes and maximum number connected in parallel at terminal EG:
12 x AAY21/AAY32

Transistor non-conducting (output level "positive high")

Voltage at one or more gate inputs V_G = min. 0 V, = max. 0.3 V

Total required direct current $-I_{GD}$ = max. 1.1 mA

Total required transient charge when V_G changes from $2/3V_p$ to 0.5 V in 1.5 µs $-Q_{GT}$ = max. 2.1 nC

Time data

Pulse duration t_{p1} = min. 6 µs, t_{p2} = min. 6 µs } See point 8*

OUTPUT DATA (at V_p = 11.4 V and V_N = -12.6 V unless specified differently).

Voltages, direct currents and transient charges

Transistor conducting (output level "positive low")

Voltage V_Q = min. 0 V, = max. 0.3 V

Available direct current I_{QD} = min. 8.2 mA, min. 7.0 mA (T_{amb} = min. -25 °C)**

Available transient charge when V_Q changes from 2/3 Vp to 0.5 V in 1.5 µs Q_{QT} = min. 9 nC, min. 7 nC (T_{amb} = min. -25 °C)**

If 2 or 3 collectors Q are paralleled, all but one collector resistor R must be left disconnected. If 4 to 16 collectors Q are paralleled, all but two collector resistors R must be left disconnected. In the latter case the available direct current respectively available transient charge must be reduced to: I_{QD} = min. 6.7 mA, Q_{QT} = min. 7.4 nC, I_{QD} = min. 5.5 mA, Q_{QT} = min. 5.4 nC } (T_{amb} = min -25 °C)**

Transistor non-conducting (output level "positive high")

Voltage V_Q = min. 2/3 Vp, = max. Vp

*Of section "Time definitions 10-series circuit blocks".
** Between 0 and - 25 °C to be derived by linear interpolation.

Time data

Fall time	t_f	= max. 1.5 µs	See point 1*
Fall delay	t_{fd}	= max. 3 µs	See point 2*

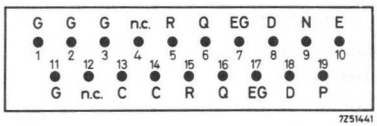
Maximum wiring capacitance 200 pF.

*) Of section "Time definitions 10-series circuit blocks".

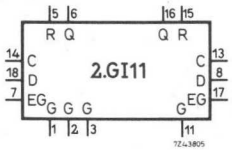
DUAL POSITIVE GATE INVERTER AMPLIFIER

The unit comprises a single input-and a triple input positive diode gate-inverter combination, together with two separate diodes which can be used to extend the number of gate (G) inputs on any of the two circuits at the extension gate inputs EG.
The collectors Q of the two transistors are not connected with their corresponding collector resistor R. Therefore with the two transistors a logical operation can be performed by interconnecting the two collectors Q with one collector resistor R. The second collector resistor R must be left disconnected.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

Ambient temperature range:		
	operating	-25 to +55 °C below 0 °C: derated output data
	storage	-55 °C to +75 °C
Weight		approx. 40 g
Case		high standard case



terminal location

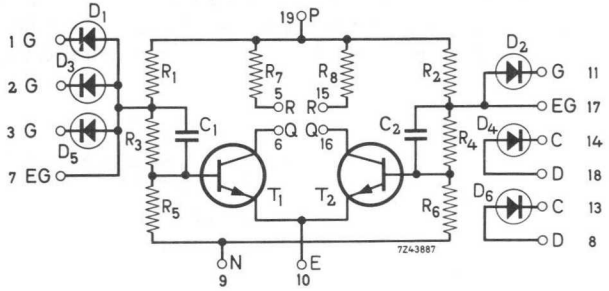


drawing symbol

CIRCUIT DATA

Terminal

1 = G = gate input
2 = G = gate input
3 = G = gate input
4 = not connected
5 = R = connection collector resistor
6 = Q = output
7 = EG = extension gate input
8 = D = anode separate diode
9 = N = supply -12V
10 = E = common supply 0 V
11 = G = gate input
12 = not connected
13 = C = cathode separate diode
14 = C = cathode separate diode
15 = R = connection collector resistor
16 = Q = output
17 = EG = extension gate input
18 = D = anode separate diode
19 = P = supply +12V



Power supply

Terminal 9 : V_N = -12 V ±5%, $-I_N$ = 0.6 mA
10 : V_E = 0 V common
19 : V_P = +12 V ±5%,
I_P = 2.8 mA (both transistors non-conducting)
= 3.9 mA (one transistor conducting)
= 5.1 mA (both transistors conducting)

The current values are nominal

INPUT REQUIREMENTS (at V_P = 11.4 V and V_N = -12.6 V unless specified differently).

Transistor conducting (output level "positive low").

Voltage at all gate inputs V_G = min. $2/3V_P$
max. V_P

Type of diodes and maximum number connected in parallel at terminal EG:
12 x AAY21/AAY32

Transistor non-conducting (output level "positive high").

Voltage at one or more gate inputs V_G = min. 0 V = max. 0.3 V

Total required direct current $-I_{GD}$ = max. 1.1 mA

Total required transient charge when V_G changes from 2/3 Vp to 0.5 V in 1.5 µs

$-Q_{GT}$ = max. 2.1 nC

Time data

Pulse duration t_{p1} = min. 6 µs, t_{p2} = min. 6 µs } See point 8*

OUTPUT DATA (at V_P = 11.4 and V_N = -12.6 V unless specified differently).

Voltages, direct currents and transient charges

Transistor conducting (output level "positive low")

Voltage V_Q = min. 0 V = max. 0.3 V

Available direct current I_{QD} = min. 8.2 mA = min. 7.0 mA (T_{amb} = min. -25 °C)**

Available transient charge when V_Q changes from 2/3 Vp to 0 V in 1.5 µs Q_{QT} = min. 9 nC = min. 7 nC (T_{amb} = min. -25 °C)**

If 2 or 3 collectors Q are paralleled all but one collector resistor R must be left disconnected. If 4 to 16 collectors Q are paralleled, all but two collector resistors R must be left disconnected. In the latter case the available direct current respectively available transient charge must be reduced to: I_{QD} = min. 6.7 mA, Q_{QT} = min. 7.4 nC, I_{QD} = min. 5.5 mA, Q_{QT} = min. 5.4 nC } (T_{amb} = min -25 °C)**

Transistor non-conducting (output level "positive high")

Voltage V_Q = min. 2/3 Vp = max. Vp

* Of section "Time definitions 10-series circuit blocks".

** Between 0 and - 25 °C to be derived by linear interpolation.

Time data

Fall time	t_f	= max. 1.5 µs	See point 1*
Fall delay	t_{fd}	= max. 3 µs	See point 2*

Maximum wiring capacitance 200 pF.

* Of section "Time definitions 10-series circuit blocks".

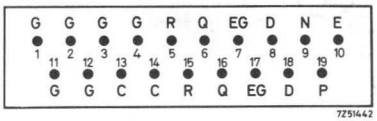
DUAL POSITIVE GATE INVERTER AMPLIFIER

The unit comprises a double input- and a quadruple input positive diode gate-inverter combination, together with two separate diodes which can be used to extend the number of gate (G) inputs on any of the two circuits at the extension gate inputs EG.

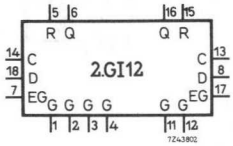
The collectors Q of the two transistors are not connected with their corresponding collector resistors R. Therefore with the two transistors a logical operation can be performed by interconnecting the two collectors Q with one collector resistor R. The second collector resistor R must be left disconnected.

The circuit is mounted inside a sealed metal can with 19 wire terminals.

Ambient temperature range:		
	operating	-25 to +55 °C below 0 °C: derated output data
	storage	-55 °C to +75 °C
Weight		approx. 40 g
Case		high standard case



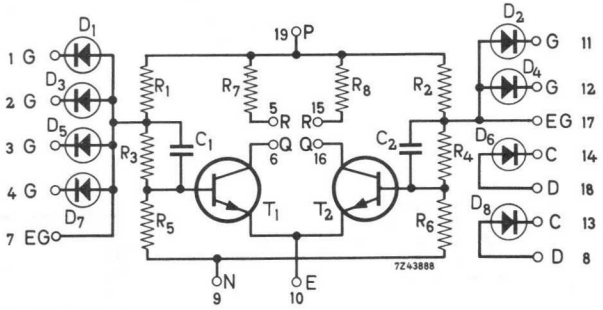
terminal location



drawing symbol

CIRCUIT DATA

Terminal
1 = G = gate input
2 = G = gate input
3 = G = gate input
4 = G = gate input
5 = R = connection collector resistor
6 = Q = output
7 = EG = extension gate input
8 = D = anode separate diode
9 = N = supply −12 V
10 = E = common supply 0 V
11 = G = gate input
12 = G = gate input
13 = C = cathode separate diode
14 = C = cathode separate diode
15 = R = connection collector resistor
16 = Q = output
17 = EG = extension gate input
18 = D = anode separate diode
19 = P = supply +12 V



Power supply

Terminal 9 : V_N = −12 V ± 5%, $-I_N$ = 0.6 mA
10 : V_E = 0 V common
19 : V_P = +12 V ± 5%,
I_P = 2.8 mA (both transistors non-conducting)
= 3.9 mA (one transistor conducting)
= 5.1 mA (with transistors conducting)

Current values are nominal

INPUT REQUIREMENTS (at V_P = 11.4 V and V_N = -12.6 V unless specified differently).

Transistor conducting (output level "positive low").

Voltage at all gate inputs V_G = min. 2/3 V_P, max. V_P

Type of diodes and maximum number connected in parallel at terminal EG: 12 x AAY21/AAY32

Transistor non-conducting (output level "positive high").

Voltage at one or more gate inputs V_G = min. 0 V, = max. 0.3 V

Total required direct current $-I_{GD}$ = max. 1.1 mA

Total required transient charge, when V_G changes from 2/3 V_P to 0.5 V in 1.5 µs $-Q_{GT}$ = max. 2.1 nC

Time data

Pulse duration t_{p1} = min. 6 µs, t_{p2} = min. 6 µs } See point 8*

OUTPUT DATA (at V_P = 11.4 V and V_N = -12.6 V, unless specified differently).

Voltages, direct currents and transient charges

Transistor conducting (output level "positive low")

Voltage V_Q = min. 0 V, = max. 0.3 V

Available direct current I_{QD} = min. 8.2 mA, = min. 7.0 mA (T_{amb} = min. -25 °C)**

Available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 µs Q_{QT} = min. 9 nC, = min. 7 nC (T_{amb} = min -25 °C)**

If 2 or 3 collectors Q are paralleled all but one collector resistor R must be left disconnected. If 4 to 16 collectors Q are paralleled,

* Of section "Time definitions 10-series circuit blocks".

** Between 0 and -25 °C to be derived by linear interpolation.

all but two collector resistors R must be left disconnected. In the latter case the available direct current respectively available transient charge must be reduced to: I_{QD} = min. 6.7 mA
Q_{QT} = min. 7.4 nC
I_{QD} = min. 5.5 mA
Q_{QT} = min. 5.4 nC

(T_{amb} = min. -25 °C)**

Transistor non-conducting (output level "positive high")

Voltage	V_Q = min. 2/3 V_P = max. V_P	
Time data		
Fall time	t_f = max. 1.5 µs	See point 1*
Fall delay	t_{fd} = max. 3 µs	See point 2*

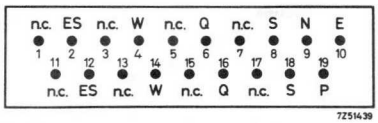
Maximum wiring capacitance 200 pF.

* Of section "Time definitions 10-series circuit blocks".
** Between 0 and - 25 °C to be derived by linear interpolation.

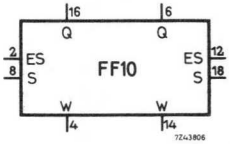
FLIP-FLOP

The unit comprises a set/reset bi-stable multivibrator circuit. The number of set/reset (S) inputs can be extended with the aid of external diodes at the extension inputs ES.
The circuit constitutes a memory function, driven by means of a d.c. level at the S-inputs. In conjunction with the dual trigger gates 2TG 13 or 2TG 14 an a.c. -driven (triggered) flip-flop can be formed, normally used in binary counters and shift registers; in conjunction with the quadruple trigger gate 4TG 15 one stage of a bi-directional counter or bi-directional shift register is formed. Up to 10 trigger gates can be paralleled at W-inputs of the flip-flop. In these applications the Q-output terminals of the trigger gates are connected to the W-input terminals of the flip-flop FF 10.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

Ambient temperature range:		
	operating	-25 to +55 °C below 0 °C: derated output data
	storage	-55 °C to +75 °C
Weight		approx. 30 g
Case		low standard case



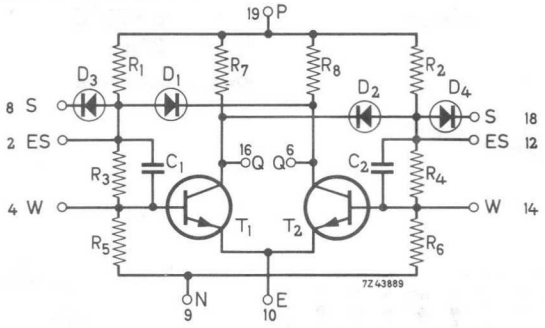
terminal location



drawing symbol

CIRCUIT DIAGRAM

Terminal 1 = not connected
2 = ES = extension set/reset input
3 = not connected
4 = W = extension trigger gate
5 = not connected
6 = Q = output
7 = not connected
8 = S = set/reset input
9 = N = supply - 12 V
10 = E = common supply 0 V
11 = not connected
12 = ES = extension set/reset input
13 = not connected
14 = W = extension trigger gate
15 = not connected
16 = Q = output
17 = not connected
18 = S = set/reset input
19 = P = supply + 12 V



Power supply

Terminal 9 : $V_N = -12V \pm 5\%$, $-I_N = 0.6$ mA
10 : $V_E = 0$ V common
19 : $V_P = +12V \pm 5\%$, $I_P = 4.8$ mA
} nominal value of the current

INPUT REQUIREMENTS (at $V_P = 11.4V$ and $V_N = -12.6V$ unless specified differently).

Set/reset input (S-terminals)

A d.c. voltage level is applied to terminal S. A "positive low" voltage (between 0 V and 0.3 V) drives the corresponding transistor into the non-conducting state.

Transistor conducting (output level "positive low")

Voltage	V_S = min. 2/3 V_P = max. + V_P	
	Type of diodes and maximum number connected in parallel at terminal ES: 12 x OA 85/OA 95	

Transistor non-conducting (output level "positive high")

Voltage	V_S = min. 0 V = max. 0.3 V	
Required direct current	$-I_{SD}$ = max. 1.95 mA	
Required transient charge when V_S changes from 2/3 V_P to 0.5 V in 1.5 µs	$-Q_{ST}$ = max. 2.8 nC	

Time data

Pulse duration	t_p = min. 2 µs	See point 4 *
Recovery time	t_{rec} = min. 15 µs	

Base-input (W-terminal)

Capacitance (wiring + output TG13/ TG14/TG15)	C_W = max. 100 pF	

OUTPUT DATA (at V_P = 11.4 V and V_N = −12.6 V, unless specified differently).

Voltages, direct currents and transient charges

Transistor conducting (output level "positive low")

Voltage	V_Q = min. 0 V = max. 0.3 V	
Available direct current	I_{QD} = min. 8.2 mA = min. 6.6 mA (T_{amb} = min. −25 °C)**	
Available transient charge, when V_Q changes from 2/3 V_P to 0.5 V in 1.5 µs	Q_{QT} = min. 27 nC min. 22 nC (T_{amb} = min. −25 °C)**	

Transistor non-conducting (output level "positive high")

Voltage	V_Q = min. 2/3 V_P = max. V_P	

Time data

Fall time	t_f = max. 1.5 µs	See point 1*
Fall delay	t_{fd} = max. 2 µs	See point 2*

Maximum wiring capacitance 200 pF

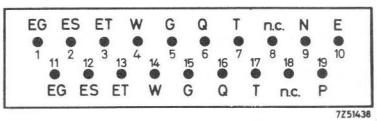
* Of section "Time definitions 10-series circuit blocks".

** Between 0 and −25 °C to be derived by linear interpolation.

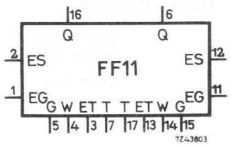
FLIP-FLOP

The unit comprises a set/reset bi-stable multivibrator circuit with built-in trigger gates. The number of set/reset inputs, gate (G) inputs as well as the trigger (T) inputs can be extended by the aid of external diodes at the extension inputs ES, EG or ET respectively.
The circuit constitutes a memory function when driven by means of a d.c. level at the ES-inputs via an external diode or a negative-going trigger signal at the T-inputs.
In the case of trigger drive, the switching of the flip-flop can be controlled by a d.c. level applied to the built-in G-inputs (e.g. in shift registers), whilst the T-inputs are interconnected.
It can also be used as a binary divider, when the G-inputs are connected to the appropriate Q-outputs. With the aid of trigger gates 2TG 13 and 2TG 14 extra triggering facilities can be made by connecting their Q-outputs to the W-inputs of the flip-flop (e.g. in bi-directional shift registers and counters).
With the aid of the quadruple trigger gate 4TG 15, of which the Q-output terminals are connected to the appropriate W-input terminals of two units FF 11, two stages of a bi-directional counter or bi-directional shift register are formed.
Up to 9 extra trigger gates can be paralleled to one flip-flop.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

Ambient temperature range:		
	operating	-25 to +55 °C below 0 °C: derated output data
	storage	-55 °C to +75 °C
Weight		approx. 40g
Case		high standard case



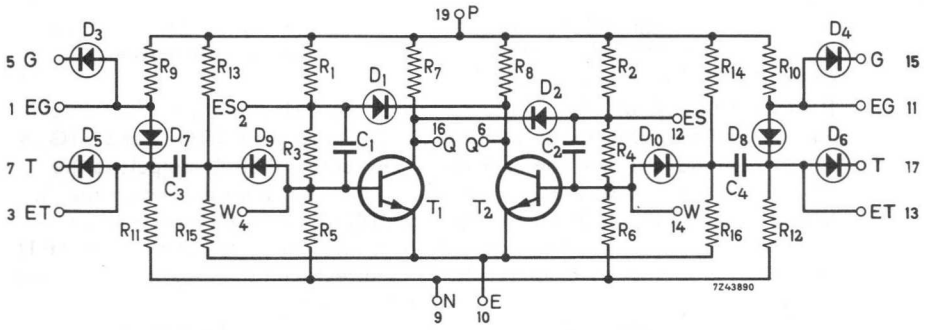
terminal location



drawing symbol

CIRCUIT DATA

Terminal
1 = EG = extension gate input
2 = ES = extension set/reset input
3 = ET = extension trigger input
4 = W = extension trigger gate
5 = G = gate input
6 = Q = output
7 = T = trigger input
8 = not connected
9 = N = supply -12 V
10 = E = common supply 0 V
11 = EG = extension gate input
12 = ES = extension set/reset input
13 = ET = extension trigger input
14 = W = extension trigger gate
15 = G = gate input
16 = Q = output
17 = T = trigger input
18 = not connected
19 = P = supply +12 V



Power supply

Terminal 9 : V_N = -12 V ±5%, $-I_N$ = 1.1 mA
10 : V_E = 0 V common
19 : V_P = +12 V ±5%, I_P = 7.0 mA
} nominal value of the current

INPUT REQUIREMENTS (at V_P = 11.4V and V_N = -12.6V unless specified differently).

Set/reset input (ES-terminals)

A d.c. voltage level V_S is applied to the terminal ES via a diode (e.g. type OA 85/OA 95), the anode connected to terminal ES. A "positive low" voltage between 0V and 0.3V drives the corresponding transistor into the non-conducting state.

Transistor conducting (output level "positive low").

Voltage V_S = min. $2/3V_P$.
= max. $+V_P$
Type of diodes and maximum number connected in parallel at terminal ES:
3 x OA 85/OA 95

Transistor non-conducting (output level "positive high").

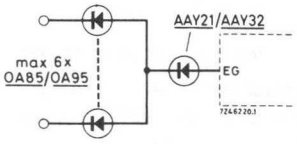
Voltage	V_S = min. 0V = max. 0.3V	
Required direct current	$-I_{SD}$ = max. 1.95 mA	
Required transient charge when V_S changes from 2/3 Vp to 0.5 V in 1.5 µs	$-Q_{ST}$ = max. 2.8 nC	
Time data		
pulse duration	t_p = min. 2 µs	See point 4*
recovery time	t_{rec} = min. 15 µs	
Time delay between S- and T-signals	t_{ts} = min. 15 µs	See point 5*

Gate-input (G-terminals)

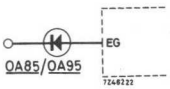
A d.c. voltage level is applied to terminal G. A "positive low" voltage closes the gate, whilst a "positive high" voltage (between 2/3 Vp and Vp) opens the gate.

Gate open

Voltage V_G = min. 2/3 Vp
= max. Vp



Gate extension input EG: max number of parallel input diodes: 6 x OA85/OA95



Gate extension input EG: with only one input diode at EG

Gate closed

Voltage	V_G = min. 0V = max. 0.3V	
Required direct current	$-I_{GD}$ = max. 1.1 mA	

* Of section "Time definitions 10-series circuit blocks".

Required transient charge, when V_G changes from 2/3 V_P to 0.5 V in 1.5 µs	$-Q_{GT}$ = max. 1.2 nC	
Time data		
Trigger gate setting time	t_{gs} = min. 29 µs	See point 6*
Trigger gate inhibiting time	t_{gi} = min. 29 µs	See point 7*

Trigger input (T-terminals).

A negative-going voltage step is applied to the terminals T separately or to both terminals interconnected in the case of binary divider applications. This voltage step on terminal T drives the transistor into the non-conducting state if the corresponding gate has been opened by the appropriate input signal on terminal G.

	Gate open	Gate closed
V_G	= min. 2/3 V_P = max. V_P	= min. 0 V = max. 0.3 V
Required direct current when V_T = max. 0.3 V	$-I_{TD}$ = max. 1.1 mA	0 mA
Required transient charge when V_T changes from 2/3 V_P to 0.5 V in 1.5 µs	$-Q_{TT}$ = max. 3.4 nC	0 nC
Input noise level	V_n = max. 1.2 V peak to peak	
	Recommended type of diode and maximum number connected in parallel at terminal ET: 6 x BAY 38	

Time data		
Fall time	t_f = max. 1.5 µs	
Pulse duration	t_P = min. 2 µs	See point 3*
Trigger gate setting time	t_{gs} = min. 29 µs	
Time delay between T- and S-signals	t_{ts} = min. 15 µs	See point 5*

Base input (W-terminal)

Capacitance (wiring + output TG13/TG14/TG15): C_W = max. 95 pF

* Of section "Time definitions 10-series circuit blocks".

OUTPUT DATA (At V_P = 11.4V and V_N = -12.6V, unless specified differently).

Voltages, direct currents and transient charges

Transistor conducting	(output level "positive low")		
Voltage	V_Q	= min. 0V = max. 0.3V	
Available direct current	I_{QD}	= min. 8.2 mA = min. 6.6 mA (T_{amb} = min. -25 °C) **	
Available transient charge, when V_Q changes from 2/3Vp to 0.5V in 1.5 µs	Q_{QT}	= min. 27 nC = min. 22 nC (T_{amb} = min. -25 °C)**	
Transistor non-conducting	(output level "positive high")		
Voltage	V_Q	= min. 2/3Vp = max. V_P	
Time data			
Fall time	t_f	= max. 1.5 µs	See point 1*
Fall delay	t_{fd}	= max. 2 µs	See point 2*

Maximum wiring capacitance 200 pF

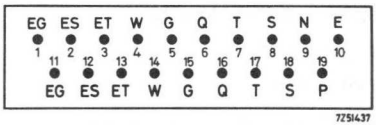
* Of section "Time definitions 10-series circuit blocks".
** Between 0 and -25 °C to be derived by linear interpolation.

FLIP-FLOP

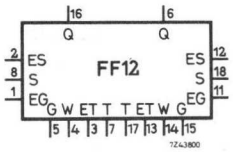
The unit comprises a set/reset bi-stable multivibrator circuit with built-in trigger gates. The number of set/reset (S) inputs, the gate (G) inputs as well as the trigger (T) inputs can be extended with the aid of external diodes at the extension inputs ES, EG or ET respectively.
The circuit constitutes a memory function when driven by means of a d.c. level at the S-inputs or a negative-going trigger signal at the T-inputs. In the case of trigger drive, the switching of the flip-flop can be controlled by a d.c. level applied to the built-in G-inputs (e.g. in shift registers), whilst the T-inputs are interconnected. It can also be used as a binary divider, when the G-inputs are connected to the appropriate Q-outputs.
With the aid of trigger gates 2TG 13 and 2TG 14 extra triggering facilities can be made by connecting their Q-outputs to the corresponding W-inputs of the flip-flop (e.g. in bi-directional shift registers and counters).
With the aid of the quadruple trigger gate 4TG 15, of which the Q-output terminals are connected to the appropriate W-input terminals of two units FF 12, two stages of a bi-directional counter or bi-directional shift register are formed.
Up to 9 extra trigger gates can be paralleled to one flip-flop.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

Ambient temperature range:

	operating	-25 to +55 °C below 0 °C: derated output data
	storage	-55 °C to +75 °C
Weight		approx. 40 g
Case		high standard case



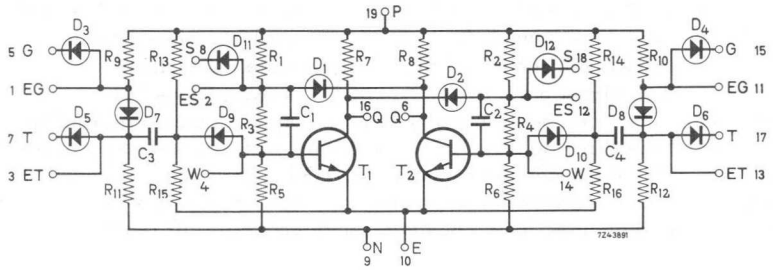
terminal location



drawing symbol

CIRCUIT DATA

Terminal
1 = EG = extension gate input
2 = ES = extension set/reset input
3 = ET = extension trigger input
4 = W = extension trigger gate
5 = G = gate input
6 = Q = output
7 = T = trigger-input
8 = S = set/reset input
9 = N = supply - 12 V
10 = E = common supply 0 V
11 = EG = extension gate input
12 = ES = extension set/reset input
13 = ET = extension trigger input
14 = W = extension trigger gate
15 = G = gate input
16 = Q = output
17 = T = trigger input
18 = S = set/reset input
19 = P = supply + 12 V



Power supply

Terminal 9 : V_N = -12 V ±5 %, $-I_N$ = 1.1 mA
10 : V_E = 0 V common
19 : V_P = +12 V ±5 %, I_P = 7.0 mA
} nominal value of the current

INPUT REQUIREMENTS (at V_P = 11.4 V and V_N = -12.6 V unless specified differently).

Set/reset input (S-terminals)

A d.c. voltage level is applied to terminal S. A "positive low" voltage (between 0 V and 0.3 V) drives the corresponding transistor into the non-conducting state.

Transistor conducting (output level "positive low").

Voltage V_S = min. 2/3 V_P
= max. V_P

Type of diodes and maximum number connected in parallel at terminal ES:
3 x OA 85/OA 95

Transistor non-conducting (output level "positive high")

Voltage	V_S = min. 0 V = max. 0.3 V	
Required direct current	$-I_{SD}$ = max. 1.95 mA	
Required transient charge, when V_S changes from 2/3 Vp to 0.5 V in 1.5 µs	$-Q_{ST}$ = max. 2.8 nC	

Time data

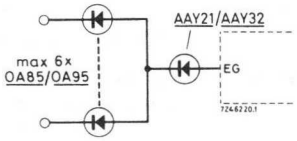
pulse duration recovery time	t_p = min. 2 µs t_{rec} = min. 15 µs	See point 4*
Time delay between S- and T-signal	t_{st} = min. 15 µs	See point 5*

Gate-input (G-terminals)

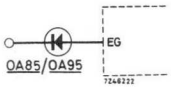
A d.c. voltage level is applied to terminal G. A "positive low" voltage closes the gate, whilst a "positive high" voltage (between 2/3 Vp and Vp) opens the gate.

Gate open

Voltage V_G = min. 2/3 Vp
= max. V_P



Gate extension input EG: max number of parallel input diodes: 6 x OA85/OA95



Gate extension input EG: with only one input diode at EG

Gate closed

Voltage	V_G = min. 0 V = max. 0.3 V	
Required direct current	$-I_{GD}$ = max. 1.1 mA	

*Of section "Time definitions 10-series circuit blocks".

Required transient charge, when V_G changes from 2/3Vp to 0.5 V in 1.5 µs: $-Q_{GT}$ = max. 1.2 nC

Time data

Trigger gate setting time	t_{gs}	= min. 29 µs	See point 6*
Trigger gate inhibiting time	t_{gi}	= min. 29 µs	See point 7*

Trigger input (T-terminals).

A negative-going voltage step is applied to the terminals T separately or to both terminals interconnected in the case of binary divider applications. This voltage step on terminal T drives the transistor into the non-conducting state if the corresponding gate has been opened by the appropriate input signal on terminal G.

	Gate open	Gate closed
V_G	= min. 2/3Vp = max. V_P	= min. 0 V = max. 0.3 V
Required direct current when V_T = max. 0.3 V	$-I_{TD}$ = max. 1.1 mA	0 mA
Required transient charge when V_T changes from 2/3Vp to 0.5V in 1.5 µs	$-Q_{TT}$ = max. 3.4nC	0 nC
Input noise level	V_n = max. 1.2 V peak to peak	

Recommended type of diodes and maximum number connected in parallel at terminal ET: 6 x BAY 38

Time data

Fall time	t_f	= max. 1.5 µs	
Pulse duration	t_p	= min. 2 µs	See point 3*
Trigger gate setting time	t_{gs}	= min. 29 µs	
Time delay between T- and S-signals	t_{ts}	= min. 15 µs	See point 5*

Base input (W-terminal)

Capacitance (wiring + output TG13/TG14/TG15): C_W = max. 95 pF

* Of section "Time definitions 10-series circuit blocks".

OUTPUT DATA (At V_P = 11.4 V and V_N = -12.6 V, unless specified differently).

Voltages, direct currents and transient charges

Transistor conducting	(output level "positive low")		
Voltage	V_Q	= min. 0 V = max. 0.3 V	
Available direct current	I_{QD}	= min. 8.2 mA = min. 6.6 mA (T_{amb} = min. -25 °C)**	
Available transient charge, when V_Q changes from 2/3 V_P to 0.5 V in 1.5 µs	Q_{TT}	= min. 27 nC = min. 22 nC (T_{amb} = min. -25 °C)**	
Time data			
Fall time	t_f	= max. 1.5 µs	See point 1*
Fall delay	t_{fd}	= max. 2 µs	See point 2*
Transistor non-conducting	(output level "positive high")		
Voltage	V_Q	= min. 2/3 V_P = max. V_P	

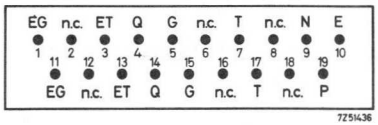
Maximum wiring capacitance 200 pF

* Of section "Time definitions 10-series circuit blocks".
** Between 0 and -25 °C to be derived by linear interpolation.

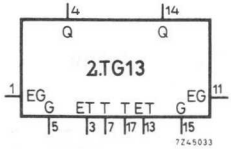
DUAL TRIGGER GATE

The unit comprises two identical trigger gate circuits, which are normally used in conjunction with flip-flop units FF 10, FF 11 and FF 12.
With the dual trigger gate a second-pair of trigger inputs are formed for the flip-flops FF 11 and FF 12, to make one stage of a bi-directional counter or shift register.
In these applications the 2TG13 output Q-terminals are to be connected directly to the flip-flop W-terminals.
The trigger gates are controlled by a d.c. voltage level, applied to the G-terminals.
The number of gate (G) inputs or trigger (T) inputs can be extended with the aid of external diodes at the extension inputs EG or ET.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

Ambient temperature range:		
	operating	-25 to +55 °C
	storage	-55 to +75 °C
Weight		approx. 30 g
Case		low standard case



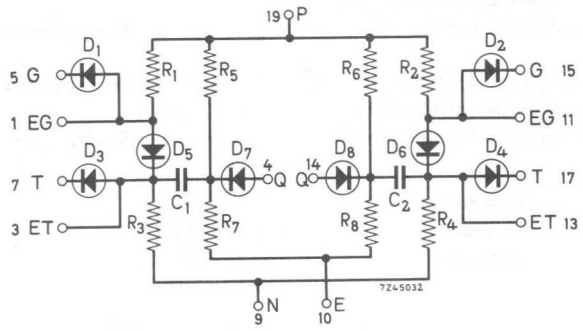
terminal location



drawing symbol

CIRCUIT DATA

Terminal
1 = EG = extension gate input
2 = not connected
3 = ET = extension trigger input
4 = Q = output
5 = G = gate input
6 = not connected
7 = T = trigger input
8 = not connected
9 = N = supply −12 V
10 = E = common supply 0 V
11 = EG = extension gate input
12 = not connected
13 = ET = extension trigger input
14 = Q = output
15 = G = gate input
16 = not connected
17 = T = trigger input
18 = not connected
19 = P = supply +12 V



Power supply

Terminal 9 : $V_N = -12$ V ±5%, $-I_N = 0.5$ mA
10 : $V_E = 0$ V common
19 : $V_P = +12$ V ±5%, $I_P = 2.2$ mA
} nominal value of the current

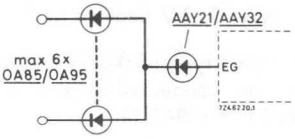
INPUT REQUIREMENTS (at $V_P = 11.4$ V and $V_N = -12.6$ V unless specified differently).

Gate input (G-terminals)

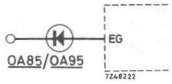
A d.c. voltage level is applied to terminal G. A "positive low" voltage closes the gate, whilst a "positive high" voltage opens the gate.

Gate open

Voltage V_G = min. 2/3 V_P
= max. V_P



Gate extension input EG: max number of parallel input diodes: 6 x OA85/OA95



Gate extension input EG: with only one input diode at EG

Gate closed

Voltage	V_G	= min. 0 V = max. 0.3 V	
Required direct current	$-I_{GD}$	= max. 1.1 mA	
Required transient charge when V_G changes from 2/3 V_P to 0.5 V in 1.5 µs	$-Q_{GT}$	= max. 1.2 nC	

Time data

Trigger gate setting time	t_{gs}	= min. 29 µs	See point 6 *
Trigger gate inhibiting time	t_{gi}	= min. 29 µs	See point 7 *

Trigger input (T-terminals)

A negative-going voltage step is applied to the terminals T separately or to both terminals interconnected.
This voltage step on terminal T passes the trigger gate if it has been opened by an appropriate input signal on terminal G.

		Gate open	Gate closed
	V_G	= min. 2/3 V_P = max. V_P	= min. 0V = max. 0.3V
Required direct current when V_T = max. 0.3V	$-I_{TD}$	= max. 1.1 mA	0 mA
Required transient charge when V_T changes from 2/3 V_P to 0.5 V in 1.5 µs	$-Q_{TT}$	= max. 3.4 nC	0 nC

*) Of section "Time definitions 10-series circuit blocks .

Input noise level	V_n = max. 1.2 V peak to peak	
	Recommended type of diodes and maximum number connected in parallel at terminal ET: 6 x BAY 38	

Time data

Fall time	t_f = max. 1.5 µs	See point 3 *
Pulse duration	t_p = min. 2 µs	
Trigger gate setting time	t_{gs} = min. 29 µs	

OUTPUT DATA

When the 2TG13 is used in conjunction with flip-flops FF 10, FF 11 and FF 12, the Q-output terminals are directly connected to the W-terminals of the flip-flop.

Output capacitance:	C_o max. 5 pF

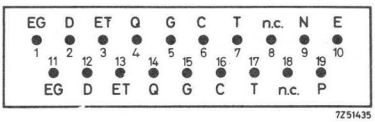
* Of section "Time definitions 10-series circuit blocks".

DUAL TRIGGER GATE

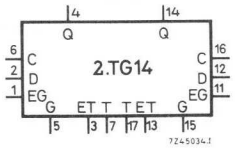
The unit comprises two identical trigger gate circuits, which are normally used in conjunction with flip-flop units FF 10, FF 11 and FF 12.
With the dual trigger gate a second pair of trigger inputs are formed for the flip-flops FF 11 and FF 12, to make one stage of a bi-directional counter or shift register. In these applications the 2TG 14 output Q-terminals are to be connected directly to the flip-flop W-terminals.
The trigger gates are controlled by a d.c. voltage level applied to the G-terminals.
Two separate built-in diodes can be used to extend the number of gate (G) inputs on any of the extension inputs EG.

The circuit is mounted inside a sealed metal can with 19 wire terminals.

Ambient temperature range:		
	operating	- 25 to + 55 °C
	storage	- 55 to + 75 °C
Weight		approx. 30 g
Case		low standard case



terminal location

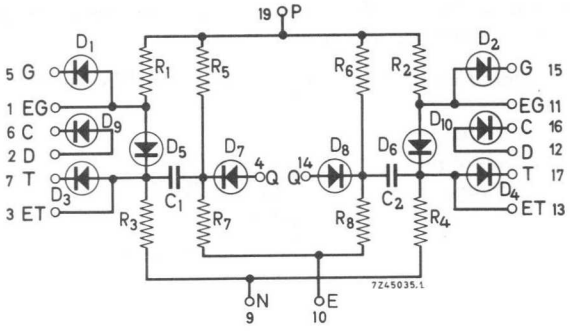


drawing symbol

CIRCUIT DATA

Terminal

1 = EG = extension gate input
2 = D = anode separate diode
3 = ET = extension trigger input
4 = Q = output
5 = G = gate input
6 = C = cathode separate diode
7 = T = trigger input
8 = not connected
9 = N = supply −12 V
10 = E = common supply 0 V
11 = EG = extension gate input
12 = D = anode separate diode
13 = ET = extension trigger input
14 = Q = output
15 = G = gate input
16 = C = cathode separate diode
17 = T = trigger input
18 = not connected
19 = P = supply +12 V



Power supply

Terminal 9 : V_N = −12 V ±5%, $-I_N$ = 0.5 mA
10 : V_E = 0 V common
19 : V_P = +12 V ±5%, I_P = 2.2 mA
} nominal value of the current

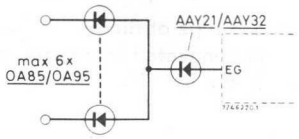
INPUT REQUIREMENTS (at V_P = 11.4 V and V_N = − 12.6 V unless specified differently).

Gate input (G-terminals)

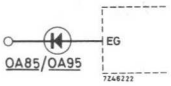
A d.c. voltage level is applied to terminal G. A "positive low" voltage closes the gate, whilst a "positive high" voltage opens the gate.

Gate open

Voltage V_G = min. 2/3 V_P
= max. V_P



Gate extension input EG: max number of parallel input diodes: 6 x OA85/OA95



Gate extension input EG: with only one input diode at EG

Gate closed

Voltage	V_G	= min. 0 V = max. 0.3 V	
Total required direct current	$-I_{GD}$	= max. 1.1 mA	
Total required transient charge, when V_G changes from $2/3V_p$ to 0.5 V in 1.5 µs	$-Q_{GT}$	= max. 1.2 nC	

Time data

Trigger gate setting time	t_{gs}	= min 29 µs	See point 6*
Trigger gate inhibiting time	t_{gi}	= min 29 µs	See point 7*

Trigger-input (T-terminals)

A negative-going voltage step is applied to the terminals T separately or to both terminals interconnected. This voltage step on terminal T passes the trigger gate if it has been opened by an appropriate input signal on terminal G.

		Gate open	Gate closed
	V_G	= min $2/3V_p$ = max V_p	= min. 0 V = max. 0.3V
Required direct current when V_T = max. 0.3V	$-I_{TD}$	= max 1.1mA	0 mA
Required transient charge when V_T changes from $2/3V_p$ to 0.5V in 1.5 µs	$-Q_{TT}$	= max 3.4nC	0 nC

* Of section "Time definitions 10-series circuit blocks".

Input noise level	V_n = max 1.2 V peak to peak	
	Recommended type of diodes and maximum number connected in parallel at terminal ET: 6 x BAY 38	

Time data

Fall time	t_f	= max 1.5 µs	See point * 3
Pulse duration	t_p	= min 2 µs	
Trigger gate setting time	t_{gs}	= min 29 µs	

OUTPUT DATA

When the 2TG14 is used in conjunction with flip-flops FF10, FF11 and FF12, the Q-output terminals are directly connected to the W-terminals of the flip-flop.

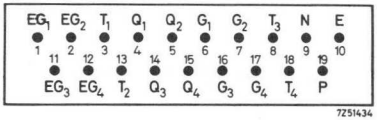
Output capacitance: C_o = max. 5 pF

* Of section "Time definitions 10-series circuit blocks".

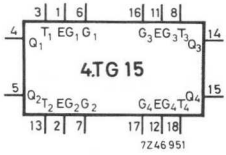
QUADRUPLE TRIGGER GATE

The unit comprises four separate identical trigger gate circuits, which are normally used in conjunction with flip-flop units FF 10, FF 11 and FF 12.
By connecting the output Q-terminals of the 4TG 15 directly to the appropriate W-terminals of a flip-flop FF 10 one stage of a bi-directional counter or bi-directional shift register is formed.
When, however, the Q-terminals of one 4TG 15 are connected to the appropriate W-terminals of two units FF 11 or FF 12, two stages of a bi-directional counter or bi-directional shift register are formed.
The trigger gates are controlled by a d.c. voltage level, applied to the G-terminals.
The number of gate (G) inputs can be extended with the aid of external diodes at the extension inputs EG.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

Ambient temperature range:		
	operating	- 25 to + 55 °C
	storage	- 55 to + 75 °C
Weight		approx. 40 g
Case		high standard case



terminal location

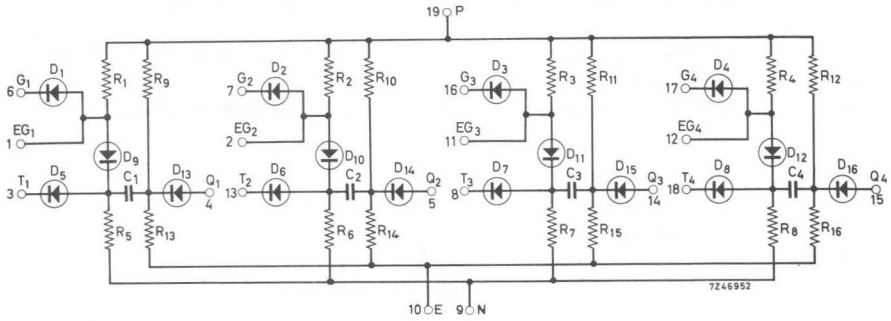


drawing symbol

CIRCUIT DATA

Terminal

1 = EG_1 = extension gate input
2 = EG_2 = extension gate input
3 = T_1 = trigger input
4 = Q_1 = output
5 = Q_2 = output
6 = G_1 = gate input
7 = G_2 = gate input
8 = T_3 = trigger input
9 = N = supply - 12V
10 = E = common supply 0V
11 = EG_3 = extension gate input
12 = EG_4 = extension gate input
13 = T_2 = trigger input
14 = Q_3 = output
15 = Q_4 = output
16 = G_3 = gate input
17 = G_4 = gate input
18 = T_4 = trigger input
19 = P = supply + 12V



Power supply

Terminal 9: $V_N = -12V \pm 5\%$, $-I_N = 1.0mA$ } nominal value
10: $V_E = 0V$ common } of the current
19: $V_P = +12V \pm 5\%$, $I_P = 4.4mA$ } of the current

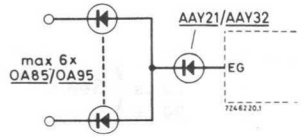
INPUT REQUIREMENTS (at $V_P = 11.4V$ and $V_N = -12.6V$ unless specified differently)

Gate inputs (G-terminals)

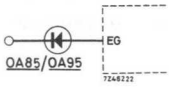
A d.c. voltage level is applied to terminal G. A "positive low" voltage closes the gate, whilst a "positive high" voltage opens the gate.

Gate open

Voltage V_G = min. 2/3 V_P
= max. V_P



Gate extension input EG: max. number of parallel input diodes: 6 x OA85/OA95 ←



Gate extension input EG: with only one input diode at EG.

Gate closed

Voltage V_G = min. 0 V
= max. 0.3 V

Required direct current $-I_{GD}$ = max. 1.1 mA.

Required transient charge when V_G changes from 2/3Vp to 0.5 V in 1.5 µs $-Q_{GT}$ = max. 1.2 nC

Time data

Trigger gate setting time t_{gs} = min. 29 µs See point 6 *
Trigger gate inhibiting time t_{gi} = min. 29 µs See point 7 *

Trigger input (T-terminals)

A negative-going voltage step is applied to the terminals T separately or to both terminals interconnected.
This voltage step on terminal T passes the trigger gate if it has been opened by an appropriate input signal on terminal G.

	Gate open	Gate closed
V_G	= min. 2/3V_P = max. V_P	= min. 0 V = max. 0.3 V
Required direct current when V_T = max. 0.3V	$-I_{TD}$ = max. 1.1 mA	0 mA
Required transient charge when V_T changes from 2/3 V_P to 0.5 V in 1.5 µs	$-Q_{TT}$ = max. 3.4 nC	0 nC
Input noise level	V_n = max. 1.2 V peak to peak	

* Of section "Time definitions 10-series circuit blocks".

Time data

Fall time	t_f = max. 1.5 µs	See point 3 *
Pulse duration	t_p = min. 2.0 µs	
Trigger gate setting time	t_{gs} = min. 29 µs	

OUTPUT DATA

When the 4TG 15 is used in conjunction with flip-flops FF 10, FF 11 and FF 12, the Q-output terminals are directly connected to the W-terminals of the flip-flop.

Output capacitance: C_o = max. 5 pF

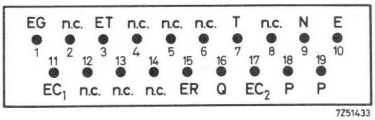
* Of section "Time definitions 10-series circuit blocks".

TIMER UNIT

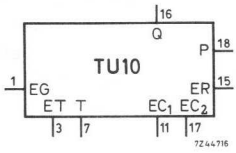
The unit TU10 contains a timing circuit followed by a Schmitt trigger circuit and an inverting amplifier. This unit comprises a built-in trigger gate as well. The trigger gate can be controlled by a d.c. voltage level applied via an external diode to terminal EG.
The number of the trigger (T) inputs can be extended with the aid of external diodes at the extension input ET.
When a negative-going voltage step is applied to terminal T, the circuit generates a positive-going pulse at the output Q - terminal, provided the gate is open. The duration of the output pulse is determined by the values of the external capacitor to be connected between the terminals EC_1 and EC_2 and the external resistor between the terminals ER and P.

The terminals ER and P must be interconnected when no external resistor is used.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

Ambient temperature range:		
	operating	-25 to +55 °C below 0 °C: derated output data.
	storage	-55 °C to +75 °C
Weight		approx. 40g
Case		high standard case

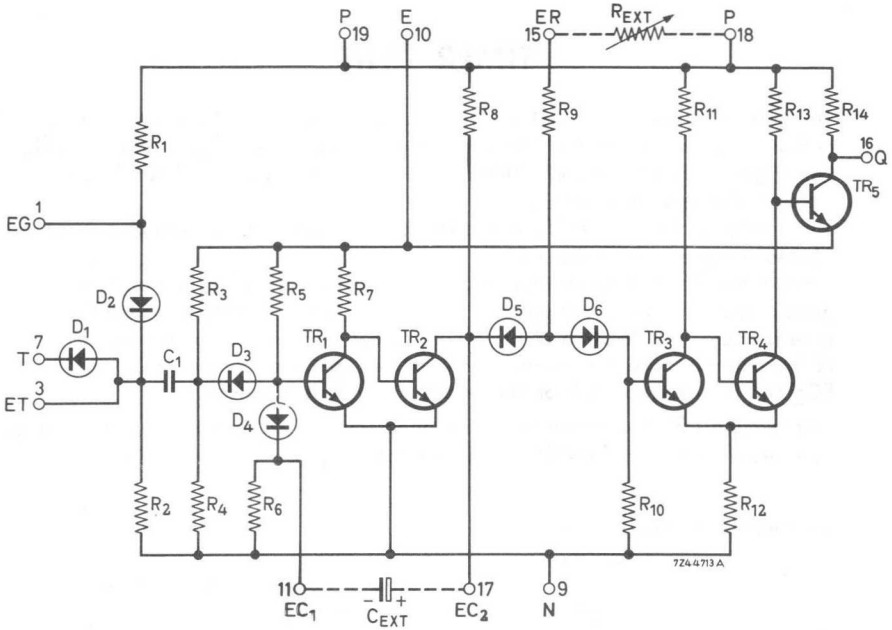


terminal location



drawing symbol

CIRCUIT DATA



Terminal

1 = EG	= extension gate input	11 = EC_1	= for external capacitor(-side)
2 =	not connected	12 =	not connected
3 = ET	= extension trigger input	13 =	not connected
4 =	not connected	14 =	not connected
5 =	not connected	15 = ER	= for external resistor
6 =	not connected	16 = Q	= output
7 = T	= trigger input	17 = EC_2	= for external capacitor (+side)
8 =	not connected	18 = P	= supply + 12V (internally connected to terminal 19)
9 = N	= supply - 12 V		
10 = E	= common supply 0 V	19 = P	= supply + 12V

Power supply

Terminal 9: V_N = - 12V ± 5%, - I_N = 9.5mA
10: V_E = 0V common
19: V_P = + 12V ± 5%, I_P = 5.0 mA
} nominal value of the current

INPUT REQUIREMENTS (at V_P = 11.4V and V_N = - 12.6V unless specified differently).

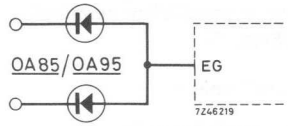
Gate input (EG-terminal)

A d.c. voltage level is applied to terminal EG via an external diode. A "positive low" voltage closes the gate, whilst a "positive high" voltage opens the gate.

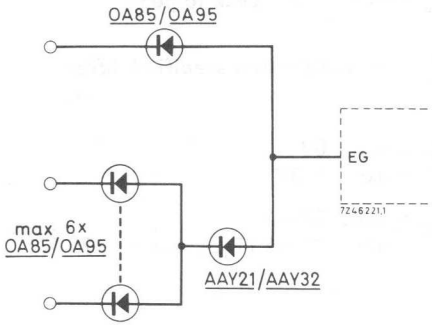
Gate open

Voltage

V_G = min. 2/3 V_P
= max. V_P



Gate extension input EG: with two input diodes



Gate extension input EG: max number of parallel input diodes:
7 x OA85/OA95/AAY21/AAY32

Gate closed

Voltage

V_G = min. 0V
= max. 0.3V

Required direct current

$-I_{GD}$ = max. 1.1 mA

Required transient charge when V_G changes from 2/3 V_P to 0.5V in 1.5 µs

$-Q_{GT}$ = max. 1.2 nC

Time data

Trigger gate setting time t_{gs} = min. 26 µs see point 6*
Trigger gate inhibiting time t_{gi} = min. 26 µs see point 7*

Trigger input (T-terminal)

A negative-going voltage step is applied to terminal T. This voltage step on terminal T passes the gate, when it has been opened by the appropriate voltage level on terminal EG and transistor TR5 is driven in the non-conducting state.

* Of section "Time definitions 10-series circuit blocks".

	Gate open	Gate closed
Voltage	V_G = min. 2/3 V_P = max. V_P	= min. 0 V = max. 0.3V
Required direct current	$-I_{TD}$ = max. 1.1 mA	= 0 mA
Required transient charge when V_T changes from 2/3V_P to 0.5V in 1.5 µs	$-Q_{TT}$ = max. 3.2 nC	0 nC

Recommended type of diodes and maximum number connected in parallel at terminal ET: 6 x BAY 38/BAX 13

Time data : see par. "Delay and swiching times" below

Input noise level V_n = max. 1.2 V peak to peak

OUTPUT DATA (at V_P = 11.4V and V_N = - 12.6V unless specified differently).

Transistor TR5 conducting

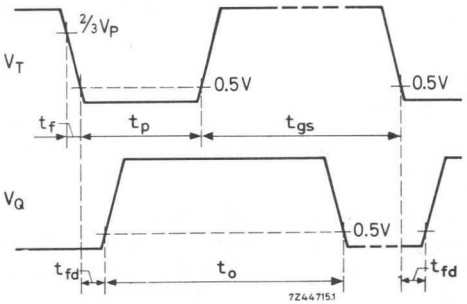
Voltage V_Q = min . 0V
= max. 0.3V

Available direct current I_{QD} = min. 32 mA
= min. 29 mA (T_{amb} = min. - 25 °C)**

Available transient charge when V_Q changes from 2/3V_P to 0.5V in 1.5 µs Q_{QT} = min. 30 nC
= min. 27 nC (T_{amb} = min. - 25 °C)**

Maximum wiring capacitance 200 pF

Delays and switching times



** Between 0 and - 25 °C to be derived by linear interpolation.

fall time t_f = max. 1.5 µs
fall delay t_{fd} = max. 2 µs
input pulse duration t_p = min. 2 µs
output pulse duration t_o = depends on the values of the external capacitor C_{ext} and the external resistor R_{ext}.

- The minimum time between two successive input pulses is only determined by the trigger gate setting time (t_{gs}).
- Besides the above mentioned restriction no recovery time of the unit has to be taken into account.
- When during the delay the input is triggered for a second time, the delay action will start all over again.

Duration of the output pulse : dependent on the values of R_{ext} and C_{ext}

	Increase of the duration with external capacitor C_{ext} *)
R_{ext} = 47 kΩ ± 10%	44 - 79 ms/µF
terminals ER and P interconnected	23 - 35 ms/µF

The absolute max.values: R_{ext} = 52 kΩ and C_{ext} = 1800 µF.
By means of this resistor the output pulse duration can be varied by a factor 2. The terminals ER and P must be interconnected, if no external resistor is used.

Stability of the output pulse duration (for orientation only)

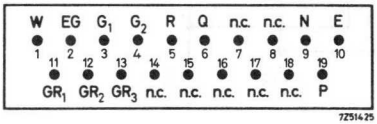
A variation of the supply voltages V_N and V_P of ± 5% varies the pulse duration by less than ± 1.5% with $R_{ext.}$ = 52 kΩ and ± 0.6% with $R_{ext.}$ = 0
A variation in ambient temperature of 1 °C varies the pulse duration by less than 0.1%.
A variation of the leakage current of the external capacitor (C_{ext}) with 1µA varies the pulse duration by less than 0.8%.

* The maximum leakage current of the external capacitor must be less than 20 µA. The working voltage of the external capacitor must be >25 V.

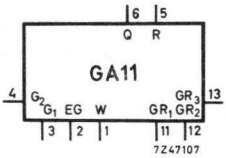
GATE AMPLIFIER

The unit contains a gate circuit and a non-inverting amplifier. The two amplifier stages give an appreciable power amplification between input and output. The amplifier of the unit GA 11 can be preceded by one-level as well as two level logic circuits, performing an AND respectively an AND-AND or AND-OR operation for "positive high" signals.
Three resistors of 10 kΩ have been mounted inside the block, possibly needed for the AND-OR operation.
The collector resistor R of the output stage can be left floating for driving e.g. inductive loads. In this case the available output current is increased, and less I_p is drawn from the stabilised V_p.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

Ambient temperature range:		
	operating	- 25 to + 55 °C
	storage	- 55 to + 75 °C
Weight		approx. 30 g
Case		low standard case



terminal location

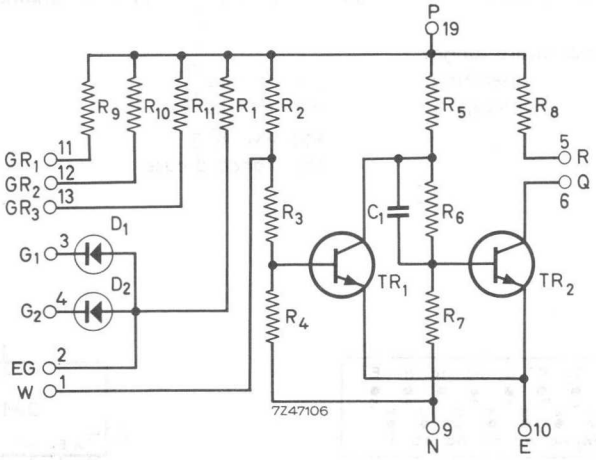


drawing symbol

CIRCUIT DATA

Terminal

1 = W = input amplifier
2 = EG = extension gate input
3 = G_1 = gate input
4 = G_2 = gate input
5 = R = connection collector resistor
6 = Q = output
7 = not connected
8 = not connected
9 = N = supply - 12V
10 = E = common supply 0V
11 = GR_1 = connection gate resistor
12 = GR_2 = connection gate resistor
13 = GR_3 = connection gate resistor
14 = not connected
15 = not connected
16 = not connected
17 = not connected
18 = not connected
19 = P = supply + 12V



Power supply

Terminal 9: V_N = - 12V ± 5% $-I_N$ = 1.5mA
10: V_E = 0V common
19: V_P = + 12V ± 5% I_P = 15mA (Q and R interconnected)
I_P = 6mA (Q and R not interconnected)
nominal value of the current

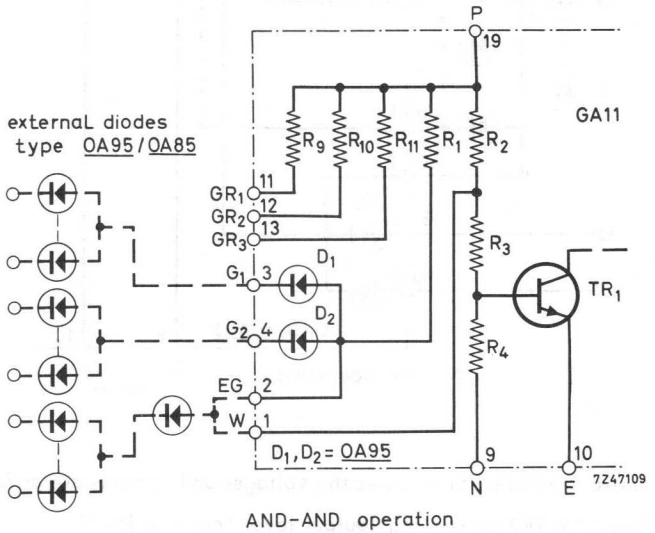
INPUT REQUIREMENTS (at V_P = 11.4V and V_N = - 12.6V unless specified differently)

Input (G, EG and W-terminals)

The three logic circuit configurations, which can be performed and connected to the input terminals are:

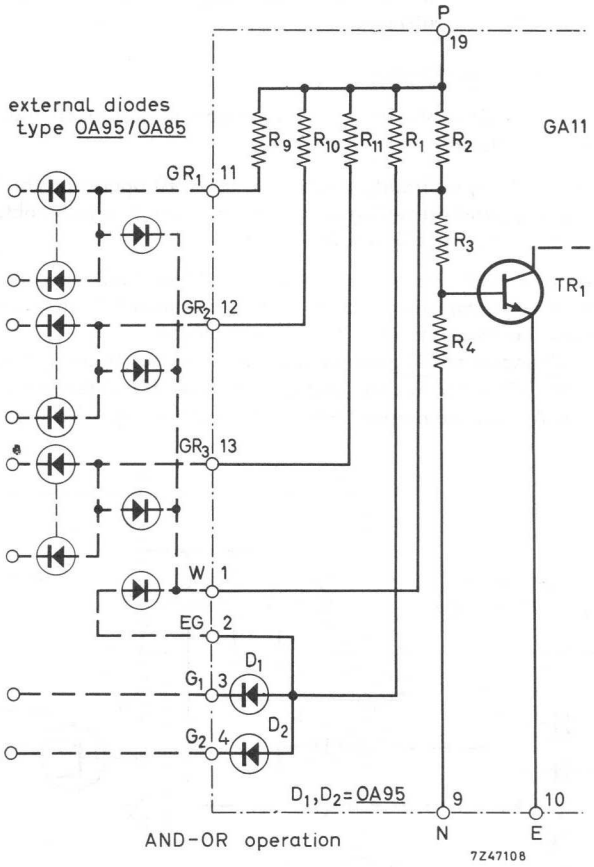
1 A one-level logic circuit, performing an AND operation for "positive high" signals and preceding the amplifier circuit, can be obtained by interconnecting the EG and W terminals.

2 A two-level logic circuit, performing an AND-AND operation and preceding the amplifier circuit, can be obtained by connecting the external diodes as shown in the diagram below.
When all inputs of all gate circuits are at a "positive high" level, transistor TR_1 is conducting and consequently transistor TR_2 is non-conducting. So the output level is at "positive high" voltage as well.



AND-AND operation

3 A two-level logic circuit, performing an AND-OR operation and preceding the amplifier can be obtained by connecting the external diodes as shown in the diagram below.
When all inputs of only one gate circuit are at "positive high" level, transistor TR_1 is conducting and consequently transistor TR_2 is non-conducting. So the output level is at "positive high" voltage as well.



In the above mentioned three cases the voltages and currents are as follows:

Transistor TR2 conducting (output level "positive low")

Voltage	V_W = max. 1.5 V
Required direct current	$-I_{GD}$ = max. 1.1 mA
Required transient charge when V_Q changes from 2/3 Vp to 0.5 V in 1.5 µs	$-Q_{GT}$ = max. 1.2 nC

Transistor TR2 non-conducting (output level "positive high")

Voltage	V_W = min. 3.25 V

OUTPUT DATA (at V_P = 11.4 V and V_N = - 12.6 V unless specified differently)

Transistor TR2 conducting (output level "positive low")

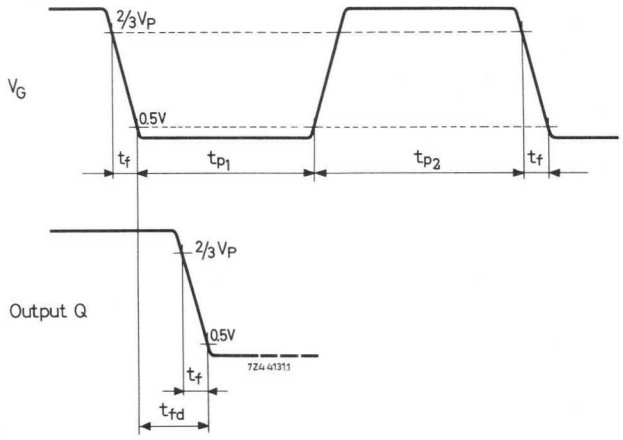
Voltage	V_Q	= min. 0 V = max. 0.3 V
Available direct current	I_{QD}	= min. 62 mA (Q and R interconnected) = min. 71 mA (Q and R not interconnected) *
Available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 µs	Q_{QT}	= min. 75 nC (Q and R interconnected) = min. 80 nC (Q and R not interconnected)

Transistor TR2 non-conducting

Voltage	V_Q	= absolute max. 15 V

Maximum wiring capacitance 1000 pF

Delays and switching times



Pulse duration: t_{p1} = min. 6 µs
t_{p2} = min. 6 µs

Fall delay : t_{fd} = max. 3 µs (at t_f = max. 1.5 µs)

* When inductive loads are switched, the output transistor must be protected against voltage transients by means of a diode, mounted across the load, the anode connected to the Q-output terminal. Recommended type of diode: BY100.

ONE-SHOT MULTIVIBRATOR

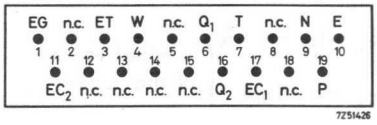
The unit OS 11 contains a monostable multivibrator circuit and a trigger gate. The trigger gate can be controlled by a d.c. voltage level, applied via an external diode, to terminal EG. The number of the trigger (T)-inputs can be extended with the aid of external diodes at the extension input ET.

With the aid of the trigger gates 2. TG 13, 2. TG 14 and 4. TG 15 extra triggering facilities can be made by connecting their Q-outputs to the W-input of the one-shot multivibrator.

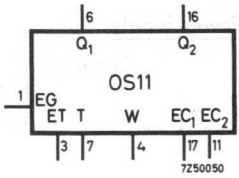
When a negative-going voltage step is applied to terminal T, the circuit generates a pulse at the output(Q)-terminals, provided the gate is open. The duration of the output pulse can be increased by an external capacitor to be connected between the terminals EC_1 and EC_2.

The circuit is mounted inside a sealed metal can with 19 wire terminals.

Ambient temperature range:		
	operating	- 25 to + 55 °C below 0 °C: derated output data
	storage	- 55 °C to + 75 °C
Weight		approx. 40 g
Case		high standard case



terminal location

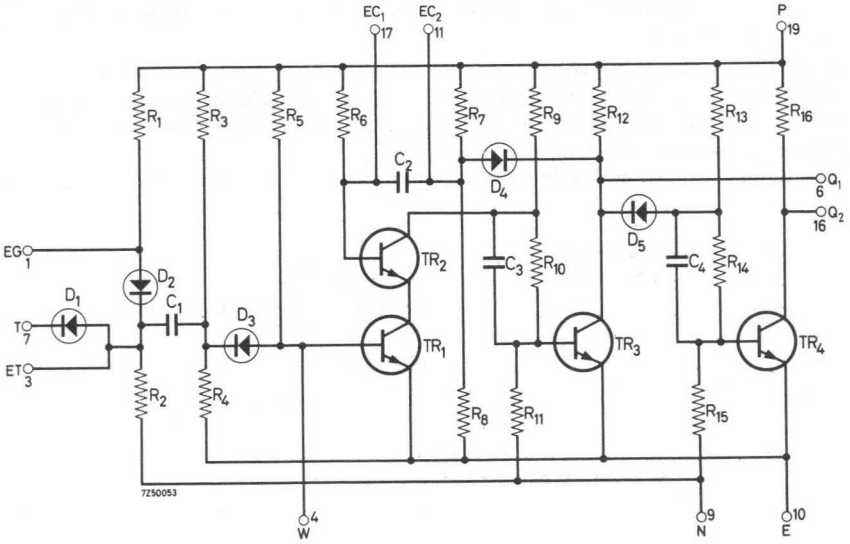


drawing symbol

CIRCUIT DATA

Terminal

1 = EG = extension gate input
2 = not connected
3 = ET = extension trigger input
4 = W = extension trigger gate
5 = not connected
6 = Q_1 = output 1
7 = T = trigger input
8 = not connected
9 = N = supply −12 V
10 = E = common supply 0 V
11 = EC_2 = for external capacitor
12 = not connected
13 = not connected
14 = not connected
15 = not connected
16 = Q_2 = output 2
17 = EC_1 = for external capacitor
18 = not connected
19 = P = supply +12 V



Power supply

Terminal 9 : V_N = −12 V ±5 %, $-I_N$ = 1 mA
10 : V_E = 0 V common
19 : V_P = +12 V ±5 %, I_P = 6 mA

} nominal value of the current

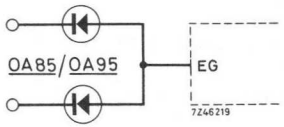
INPUT REQUIREMENTS (at V_P = 11.4 V and V_N = -12.6 V unless specified differently).

Gate input (EG-terminals)

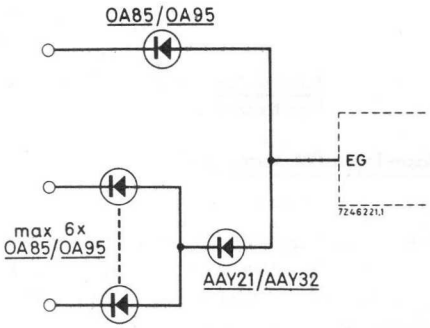
A d.c. voltage level is applied to terminal EG via an external diode.
A "positive low" voltage closes the gate, whilst a "positive high" voltage opens the gate.

Gate open

Voltage V_G = min. 2/3 V_P
= max. V_P



Gate extension input EG: with two input diodes



Gate extension input EG: max. number of parallel input diodes: 7xOA85/OA95

Gate closed

Voltage	V_G	= min. 0 V = max. 0.3 V
Required direct current	$-I_{GD}$	= max. 1.1 mA
Required transient charge when V_G changes from 2/3Vp to 0.5V in 1.5 µs	$-Q_{GT}$	= max. 1.2 nC

Time data

Trigger gate setting time	t_{gs}	= min 20 µs	See point 6*
Trigger gate inhibiting time	t_{gi}	= min 20 µs	See point 7*

Trigger input (T-terminal)

A negative-going voltage step is applied to terminal T. This voltage step on terminal T passes the gate, when it has been opened by the appropriate voltage level on terminal EG, and drives transistor TR_3 in the conducting state and transistor TR_4 in the non-conducting state.

*Section "Time definitions" of "Circuit blocks 10-Series".

	Gate open	Gate closed
Voltage	V_G = min. 2/3 V_p = max. V_p	= min 0 V = max 0.3 V
Required direct current	$-I_{TD}$ = max. 1.1 mA	0 mA
Required transient charge when V_T changes from 2/3 V_p to 0.5 V in 1.5 µs	$-Q_{TT}$ = max. 2.3 nC	0 nC

Recommended type of diodes and maximum number connected in parallel at terminal ET: 6 x BAY 38/BAX13

Time data: see par. "Delays and switching times", below.
Input noise level V_n = max. 1.2 V peak to peak

Base-input (W-terminal)

Input capacitance max. 60 pF

Additional triggering facilities can be obtained by connecting the output of the trigger gates to terminal W of the one-shot multivibrator, e.g. 6 trigger gates may be connected in parallel to terminal W provided the total wiring capacitance C_W = max. 30 pF

OUTPUT DATA (at V_P = 11.4 V and V_N = - 12.6 V unless specified differently)

Transistor TR3 respectively TR4 conducting

Voltage	$V_{Q\,1,2}$ = min. 0 V = max. 0.3 V	
	T_{amb} = min. 0 °C	T_{amb} = min. - 25 °C*
Available direct current		
output Q_1	I_{QD} = min. 8.6 mA	min. 5.5 mA
output Q_2	= min. 12.8 mA	min. 9.5 mA
Available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 µs		
output Q_1	Q_{QT} = min. 24 nC	min. 17.2 nC
output Q_2	Q_{QT} = min. 29 nC	min. 22 nC

* Between 0 and - 25 °C to be derived by linear interpolation

Maximum wiring capacitance: 200 pF

Duration of the output pulse·

Intrinsic value	$t_f + t_o$ = max. 4 µs
Increase with external capacitor	1 µs per 58 pF
Tolerance	± 15%

Stability of output pulse duration

An increase in ambient temperature by 1 °C gives a reduction of the pulse duration of less than 0.1 % and vice versa.

There is practically no difference in duration between different output pulses at any combination of permitted supply voltages.

An increase of the leakage current of the external capacitor (C_{ext}) with 1 µA decreases the pulse duration by less than 0.4 % and vice versa.

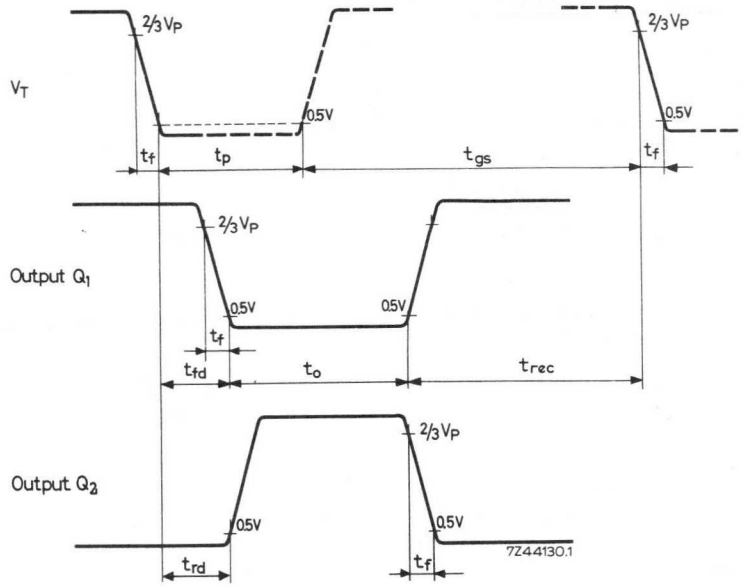
Delays and switching times

fall time	: t_f	= max. 1.5 µs
fall delay	: t_{fd}	= max. 2 µs
rise delay	: t_{rd}	= max. 2 µs
input pulse duration	: t_p	= min. 2 µs
output pulse duration	: t_o	= depends on value of external bipolar capacitor between terminals 11 and 17.
recovery time	: t_{rec}	= min. t_o

The minimum time between two successive input pulses is determined by two factors (see also the figure on the next page):

1) $2 \times t_o \geq t_p + t_{gs}$: the next input pulse may start a time = t_o after the trailing edge of the output pulse.

2) $2 \times t_o < t_p + t_{gs}$: the next input pulse may start a time = t_{gs} (20 µsec) after the trailing edge of the preceding input pulse.


V_T
$\frac{2}{3}V_P$
0.5V
t_f
t_p
t_{gs}
Output Q_1
t_{fd}
t_o
t_{rec}
Output Q_2
t_{rd}
7244130.1

PULSE DRIVER

The unit PD 11 contains a monostable multivibrator circuit and a trigger gate. The trigger gate can be controlled by a d.c. voltage level applied via an external diode to terminal EG. The number of the trigger(T) inputs can be extended with the aid of external diodes at the extension input ET.

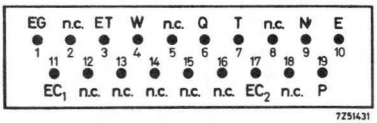
With the aid of the trigger gates 2. TG 13, 2. TG 14 and 4. TG 15 extra triggering facilities can be made by connecting their Q-outputs to the W-input of the pulse driver.

When a negative-going voltage step is applied to terminal T, the circuit generates a pulse at the output Q -terminal, provided the gate is open.

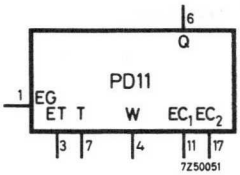
The duration of the output pulse can be increased by an external capacitance to be connected between the terminals EC_1 and EC_2.

The circuit is mounted inside a sealed metal can with 19 wire terminals.

Ambient temperature range:		
	operating	- 25 to + 55 °C
	storage	- 55 to + 75 °C
Weight		approx. 40 g
Case		high standard case



terminal location

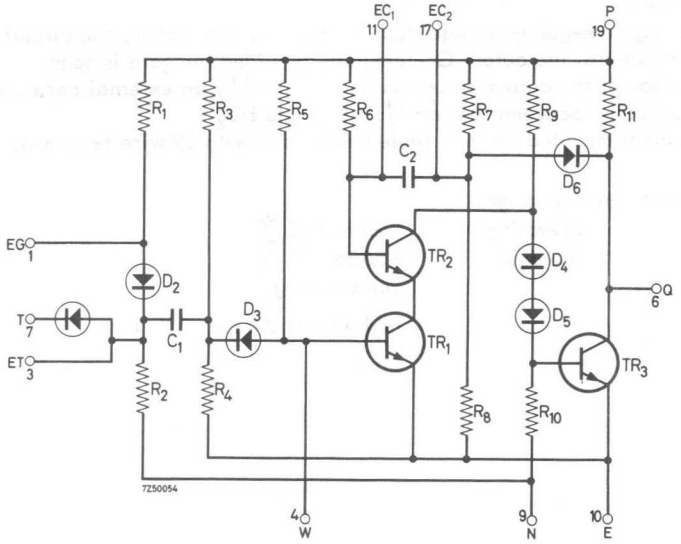


drawing symbol

CIRCUIT DATA

Terminal

1 = EG = extension gate input
2 = not connected
3 = ET = extension trigger input
4 = W = extension trigger gate
5 = not connected
6 = Q = output
7 = T = trigger input
8 = not connected
9 = N = supply -12 V
10 = E = common supply 0 V
11 = EC_1 = for external capacitor
12 = not connected
13 = not connected
14 = not connected
15 = not connected
16 = not connected
17 = EC_2 = for external capacitor
18 = not connected
19 = P = supply +12 V



Power supply

Terminal 9 : V_N = -12 V ±5 %, $-I_N$ = 1.5 mA
(transistor TR_3 non-conducting)
= 1.7 mA
(transistor TR_3 conducting)
10 : V_E = 0 V common
19 : V_P = +12 V ±5 %, I_P = 19 mA
(transistor TR_3 non-conducting)
= 28 mA
(transistor TR_3 conducting)

The current values are nominal

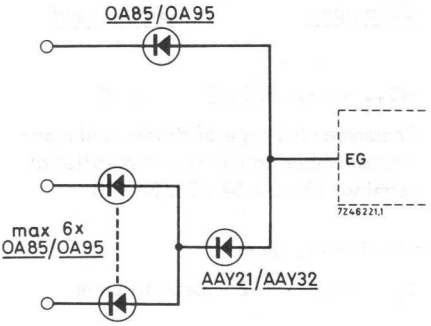
INPUT REQUIREMENTS (at V_P = 11.4 V and V_N = -12.6 V unless specified differently).

Gate input (EG-terminal)

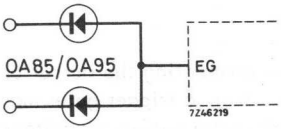
A d.c. voltage level is applied to terminal EG via an external diode. A "positive low" voltage closes the gate, whilst a "positive high" voltage opens the gate.

Gate open

Voltage V_G = min. 2/3Vp
= max. V_P.



Gate extension input EG: max number of parallel input diodes: 7xOA85/OA95



Gate extension input EG: with two input diodes

Gate closed

Voltage V_G = min. 0 V
= max. 0.3 V

Required direct current $-I_{GD}$ = max. 1.1 mA

Required transient charge when VG changes from 2/3 Vp to 0.5 V in 1.5 µs $-Q_{GT}$ = max. 1.2 nC

Time data

Trigger gate setting time	t_{gs}	= min. 26 µs	See point 6*
Trigger gate inhibiting time	t_{gi}	= min. 26 µs	See point 7*

*Section "Time definitions" of "Circuit blocks 10-Series".

Trigger input (T-terminal)

A negative-going voltage step is applied to terminal T. This voltage step on terminal T passes the gate, when it has been opened by the appropriate voltage level on terminal EG, and drives transistor TR_3 in the conducting state.

	Gate open	Gate closed
Voltage	V_G = min. 2/3 V_p = max. V_p	= min. 0 V = max. 0.3 V
Required direct current	$-I_{TD}$ = max. 1.1 mA	0 mA
	Gate open	Gate closed
Required transient charge when V_T changes from 2/3 V_P to 0.5 V in 1.5 µs	$-Q_{TT}$ = max. 3.2 nC	0 nC

Recommended type of diodes and maximum number connected in parallel at terminal ET: 6 x BAY38/BAX13

Time data : see par. "Delays and switching times".

Input noise level V_n = max. 1.2 V peak to peak

Base-input (W-terminal)

Input capacitance max. 60 pF

Additional triggering facilities can be obtained by connecting the output of the trigger gates to terminal W of the pulse driver, e.g. 6 trigger gates may be connected in parallel to terminal W provided the total wiring capacitance C_W = max. 30 pF

OUTPUT DATA (at V_P = 11.4 V and V_N = -12.6 V unless specified differently).

Transistor TR3 conducting

Voltage	V_Q = min. 0 V = max. 0.3 V
Available direct current	I_{QD} = min. 100 mA
Available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 µs	Q_{QT} = min. 185 nC

Maximum wiring capacitance 1500 pF

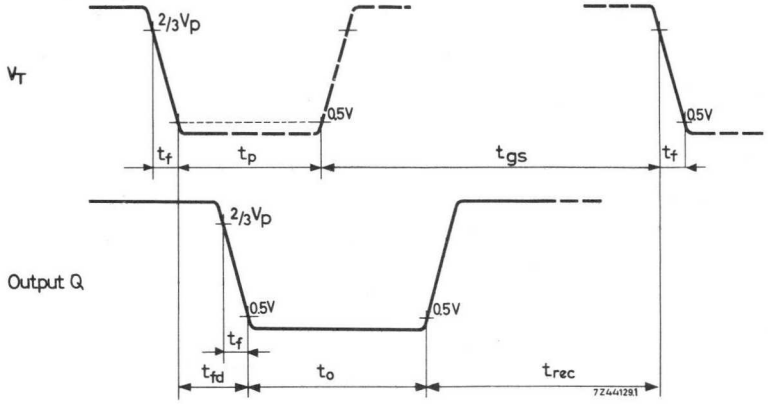
Delays and switching times

fall time	: t_f	= max. 1.5 µs
fall delay	: t_{fd}	= max. 2 µs
input pulse duration	: t_p	= min. 2 µs
output pulse duration	: t_o	= depends on value of external capacitor between terminals 11 and 17.
		= max. 5 ms
recovery time	: t_{rec}	= min. $2\,t_o$

The minimum time between two successive input pulses is determined by two factors:

1) $3 \times t_o \geq t_p + t_{gs}$: the next input pulse may start a time = $2\,t_o$ after the trailing edge of the output pulse.

2) $3 \times t_o < t_p + t_{gs}$: the next input pulse may start a time = t_{gs} (26 µsec) after the trailing edge of the preceding input pulse.



Duration of the output pulse

Intrinsic value	$t_f + t_o$ = max. 4 µs
Increase with external capacitor	1 µs per 280 pF
Tolerance	± 15 %

Stability of output-pulse duration

An increase in ambient temperature by 1 °C gives a reduction of the pulse duration of less than 0.1 % and vise versa.
There is practically no difference in duration between different output pulses at any combination of permitted supply voltages.
An increase of the leakage current of the external capacitor (C_{ext}) with 1 µA decreases the pulse duration by less than 0.15 % and vice versa.

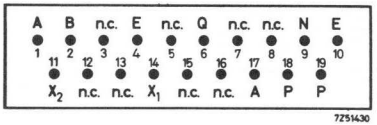
PULSE SHAPER

The unit PS 10 contains a Schmitt trigger (squaring) circuit followed by an inverting amplifier.
An input signal of a magnitude exceeding the tripping level of the unit, is re-shaped and inverted into the standard d.c. level at the output. The output voltage transients are short and suitable for driving the various circuits at their trigger(T) inputs.
The ferminals A and B are provided in order to be able to use the PS 10 for the following purposes:

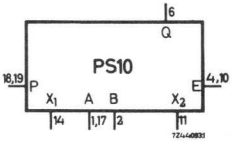
1 as a pulse shaper, driven by an external source
2 as a relaxation oscillator circuit
3 as a pulse shaper, driven by circuit blocks of the 10-series.

The circuit is mounted inside a sealed metal can with 19 wire terminals.

Ambient temperature range:		
	operating	-25 to +55 °C
		below 0 °C: derated data
	storage	-55 °C to +75 °C
Weight		approx. 30 g
Case		low standard case



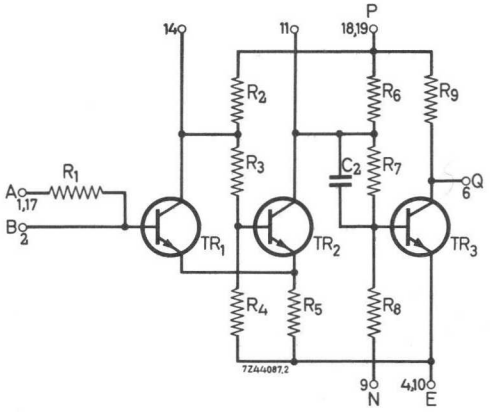
terminal location



drawing symbol

CIRCUIT DATA

Terminal
1 = A = resistor input (interconnected to terminal 17)
2 = B = direct base input
3 = not connected
4 = E = common supply 0 V (interconnected to terminal 10)
5 = not connected
6 = Q = output
7 = not connected
8 = not connected
9 = N = supply - 12 V
10 = E = common supply 0 V (interconnected to terminal 4)
11 = X_2 = internally connected
12 = not connected
13 = not connected
14 = X_1 = internally connected
15 = not connected
16 = not connected
17 = A = resistor input (interconnected to terminal 1)
18 = P = supply + 12 V } terminals 18 and 19 interconnected
19 = P = supply + 12 V }



Power supply

Terminal 9 : V_N = - 12 V ±5%, $-I_N$ = 1 mA } nominal value of the current
10 : V_E = 0 V common
19 : V_P = + 12 V ±5%, I_P = 6 mA }

INPUT REQUIREMENTS (at V_P = 11.4 V and V_N = -12.6 V unless specified differently).

Application 1

Unit driven by an external source with R_i = max. 24 kΩ
= max. 16 kΩ (T_{amb} = min. -25 °C)*

Input voltage to be applied to terminal B

Transistor TR3 conducting (output level "positive low")

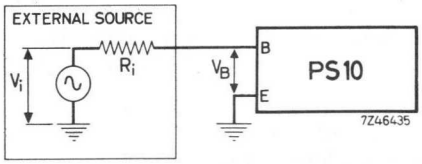
Voltage	V_B	= max. 0.36 V_P
limiting value		= max. 10 V
Current	I_B	= min. 0.1 mA
limiting value		= max. 12 mA

Transistor TR3 non-conducting (output level "positive high")

Voltage	V_B	= min. 0.13 V_P
limiting value	$-V_B$	= max. 1.2 V
Current	$-I_B$	= max. 0.01 mA

Hysteresis (difference between on and off tripping level)

Voltage ΔV_B = min. 0.12 V_P



The hysteresis is affected by the R_i of the external source.
The relation is given by the following formula:

T_{amb} = min. 0 °C	T_{amb} = min. - 25 °C
ΔV_i = min. (0.12 V_P - 0.057 R_i)	= min. (0.12 V_P - 0.085 R_i)
$\Delta V_B = \frac{\Delta V_i}{1 + 0.07\ R_i}$	$= \frac{\Delta V_i}{1 + 0.084\ R_i}$

R_i in kΩ and Vin volt

Application 2 : Unit used in a relaxation oscillator circuit

Application information will be issued separately.

Application 3 : Unit driven by circuit blocks of the 10-series

For this operation terminal A has to be connected to V_P (terminal 18) and the input voltage V_G has to be applied to terminal B via a diode, e.g. type OA 85/OA 95.

* Between 0 and - 25 °C to be derived by linear interpolation.

Transistor TR3 non-conducting (output level "positive high")

Voltage	V_G = min. 0 V = max. 0.3 V
Required direct current	$-I_{GD}$ = max. 0.9 mA
Required transient charge when V_B changes from 2/3 V_P to 0.5 V in 1.5 µs	$-Q_{GT}$ = max. 0.8 nC

Transistor TR3 conducting (output level "positive low")

Voltage	V_G = min. 2/3 V_P Type of diodes and number to be connected in parallel to terminal B: 30 x OA 85/OA 95/AAY 21/AAY32

OUTPUT DATA (at V_P = 11.4 V and V_N = - 12.6 V unless specified differently)

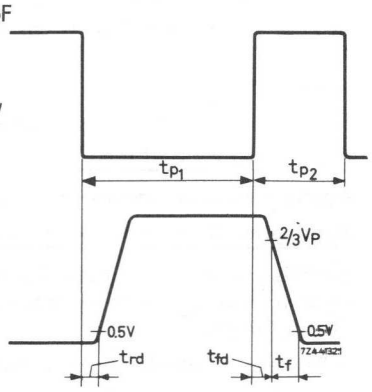
Transistor TR3 conducting (output level "positive low")

Voltage	V_Q = min. 0 V = max. 0.3 V
Available direct current	I_{QD} = min. 10 mA = min. 7.7 mA (T_{amb} = min. - 25 °C)*
Available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 µs	Q_{QT} = min. 39 nC min. 21 nC (T_{amb} = min. - 25 °C)*

Maximum wiring capacitance 200 pF

Delays and switching times

pulse duration : t_{p1} = min. 6 µs
t_{p2} = min. 3 µs
fall delay : t_{fd} = max. 0.1 µs
rise delay : t_{rd} = max. 0.1 µs
fall time : t_f = max. 1.5 µs

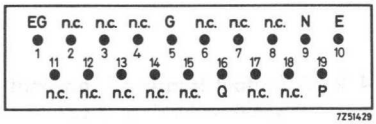


* Between 0 and - 25 °C to be derived by linear interpolation.

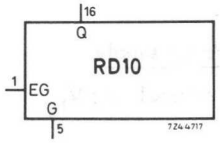
RELAY DRIVER

The unit comprises a single input positive diode gate followed by a non-inverting amplifier, intended for driving relays. The number of gate (G) inputs can be extended by means of external diodes to be connected to the extension gate input EG.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

Maximum pulse repetition frequency	100 Hz
Ambient temperature range:	
operating	-25 to +55 °C below 0 °C: derated output data
storage	-55 °C to +75 °C
Weight	approx. 30 g
Case	low standard case



terminal location

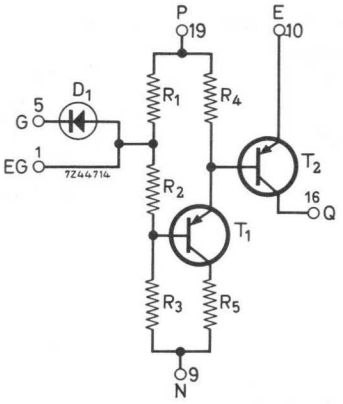


drawing symbol

CIRCUIT DATA

Terminal

1 = EG	= extension gate input	11 =	not connected
2 =	not connected	12 =	not connected
3 =	not connected	13 =	not connected
4 =	not connected	14 =	not connected
5 = G	= gate input	15 =	not connected
6 =	not connected	16 = Q	= output
7 =	not connected	17 =	not connected
8 =	not connected	18 =	not connected
9 = N	= supply - 12V	19 = P	= supply + 12V
10 = E	= common supply 0V		



Power supply

Terminal 9 : V_N = - 12V ± 5%; - I_N = 4.2 mA (output transistor non-conducting) } nominal values of the current

- I_N = 16.8 mA (output transistor conducting) } nominal values of the current

10 : V_E = 0V common

19 : V_P = + 12V ± 5% I_P = 4.6 mA (output transistor non-conducting) } nominal values of the current

I_P = 8 mA (output transistor conducting) } nominal values of the current

INPUT REQUIREMENTS (at V_P = 11.4V and V_N = - 12.6V unless specified differently).

Output transistor conducting

Voltage V_G = max. 0.3V
= min. 0V

Total required direct current $-I_{GD}$ = max. 4.7 mA

Total required transient charge, when V_G changes from 2/3 V_P to 0.5V in 1.5 µs $-Q_{GT}$ = max. 3.4 nC

Output transistor non-conducting

Voltage V_G = min. 2/3 V_P
= max. V_P
Type of diodes and maximum number connected in parallel at terminal EG:
12 x AAY21/AAY32

OUTPUT DATA

Output transistor conducting

Voltage $-V_Q$ = max. 0.5V

Available load current $-I_Q$ = min. 200 mA
= min. 132 mA (T_{amb} = min. - 25 °C)*

Output transistor non-conducting

Voltage $-V_Q$ = absolute max. 55V (resistive load)
= absolute max. 30V (inductive load)

Leakage current $-I_Q$ = max. 2.5 mA

Notes: 1) Protection diode

When inductive loads are switched, the output transistor T_2 must be protected against voltage transients by means of a diode, mounted across the load, the cathode connected to the Q - output terminal. Recommended type of diode: BY100.

2) Mounting rules

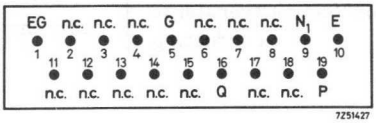
Due to heat dissipation it is not allowed to mount more than 8 units RD10 on e.g. a printed-wiring board of the standard dimensions (121.8 mm x 207.0 mm x 1.6 mm).
This holds for vertical mounting as well as for horizontal mounting. Moreover the units must be spread over the board as much as possible. Mounting of 3 printed-wiring boards equipped with RD 10's adjacent to each other in the mounting chassis 4322 026 38240 is prohibited without forced cooling.

* Between 0 and - 25 °C to be derived by linear interpolation.

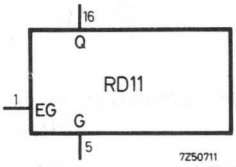
RELAY DRIVER

The unit comprises a single input positive diode gate followed by a non-inverting amplifier, intended for driving inductive and resistive loads. The number of gate (G) inputs can be extended by means of external diodes to be connected to the extension gate input EG.
The output transistor TR_3 is cut off, only when all inputs are at a positive high level (min. 2/3 V_p).
The terminal location is exactly similar to that of the RD 10.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

Maximum pulse repetition frequency		100 Hz
Ambient temperature range:		
	operating	−25 to +55 °C
	storage	−55 to +75 °C
Weight		approx. 30 g
Case		low standard case



terminal location

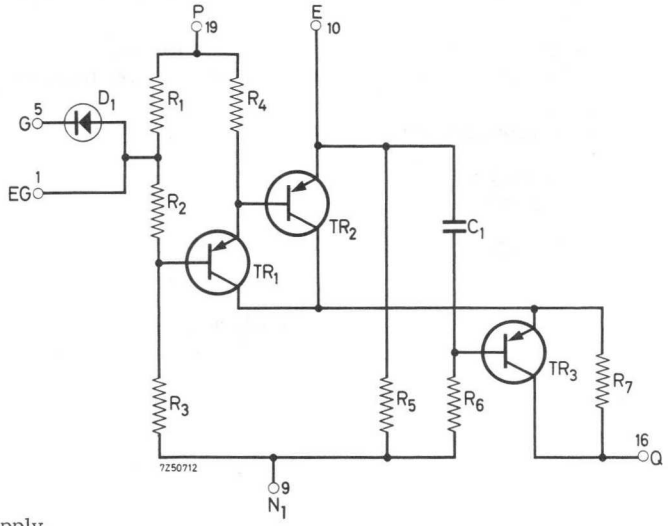


drawing symbol

CIRCUIT DATA

Terminal

1 = EG	= extension gate input	11 =	not connected
2 =	not connected	12 =	not connected
3 =	not connected	13 =	not connected
4 =	not connected	14 =	not connected
5 = G	= gate input	15 =	not connected
6 =	not connected	16 = Q	= output
7 =	not connected	17 =	not connected
8 =	not connected	18 =	not connected
9 = N_1	= supply - 12 V	19 = P	= supply + 12 V
10 = E	= common supply 0 V		



Power supply

Terminal 9 : V_{N_1} = −12 V ± 5% ; $-I_{N_1}$ = 17 mA (output transistor conducting)
10 : V_E = 0 V common
19 : V_p = +12 V ± 5% ; I_p = 8 mA (output transistor conducting)

} nominal values of the current

Output voltage: $-V_{N_2}$ = 12 V up to max. 55 V;
$-I_{N_2}$ = max. 200 mA

INPUT REQUIREMENTS (at V_p = 11.4 V and V_{N_1} = −12.6 V unless specified differently)

Output transistor conducting

Voltage V_G = max. 0.3 V, min. 0 V

Total required direct current	$-I_{GD}$	= max. 4.7 mA
Total required transient charge, when V_G changes from 2/3 V_p to 0.5 V in 1.5 μs	$-Q_{GT}$	= max. 3.4 nC

Output transistor non-conducting

Voltage	V_G	= min. 2/3 V_p max. V_p

Type of diodes and maximum number connected in parallel at terminal EG: 12 x OA95/OA85

OUTPUT DATA

Output transistor conducting

Voltage	$-V_Q$	= max. 0.8 V
Available load current	$-I_Q$	= min. 200 mA

Output transistor non-conducting

Voltage	$-V_Q$	= absolute max. 55 V
Leakage current	$-I_Q$	= max. 5 mA

Notes:

1. Protection diode

When inductive loads are switched, the output transistor TR_3 must be protected against voltage transients by means of a diode, mounted across the load, the cathode connected to the Q - output terminal. Recommended types of diode: BAY39/1N921/1N922/BAX78.

2. Mounting rules

Due to heat dissipation it is not allowed to mount more than 8 units RD 11 on e.g. a printed-wiring board of the standard dimensions (121.8 mm x 207.0 mm x 1.6 mm).
This holds for vertical mounting as well as for horizontal mounting. Moreover the units must be spread over the board as much as possible. Mounting of 3 printed-wiring boards equipped with RD 11's adjacent to each other in the mounting chassis 4322 026 38240 is prohibited without forced cooling.

3. Power supply

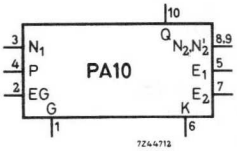
When the power supplies are switched on or switched off, care must be taken that the output voltage V_{N2} may only be applied without the presence of the other supply voltages V_{N1} and V_p for a time of max. 60 s.

POWER AMPLIFIER

The PA10 consists of a npn/pnp/pnp transistor amplifier circuit, designed to be used as a power amplifier in the "10-series" of circuit blocks.
The amplifier can be driven directly by the circuit blocks FF 10, FF 11, FF 12, 2GI10, 2GI11, 2GI12, OS11, PD11, PS10, GA 11 and TU10.
The output loadability is 2A, 55 V (abs. max. values). The built-in diode across the output terminals protects the output transistor against voltage transients which occur when the unit is driving an inductive load.
The circuit is mounted on a glass epoxy printed-wiring board, the output transistor is provided with an aluminium heat sink.

Ambient temperature range:

operating	-25 to +55 °C
storage	-55 to +75 °C
Weight	approx. 90 g

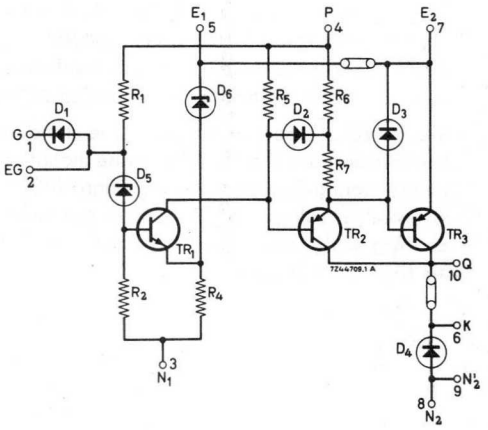


drawing symbol

CIRCUIT DATA

Terminal

1 = G = gate input
2 = EG = extention gate input
3 = N_1 = supply - 12 V
4 = P = supply + 12V
5 = E_1 = common supply 0 V
6 = K = cathode of diode D 4
7 = E_2 = common supply 0 V
8 = N_2 = supply abs. max. 55 V
9 = N_2' = supply abs. max. 55 V
10 = Q = output



Power supply

Terminal 3 : V_{N_1} = - 12 V ± 5%, - I_{N1} = max. 30 mA (TR_3 conducting)
= max. 18 mA (TR_3 non-conducting)

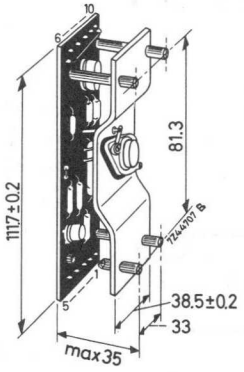
4: V_P = + 12 V ± 5%, I_P = max. 41 mA (TR_3 conducting)
= max. 39.5 mA (TR_3 non-conducting)

5: V_{E1} = 0 V common

7: V_{E2} = 0 V common

8: $-V_{N2}$ = 12 V up to max. 55 V, - I_{N2} = max. 2A

MECHANICAL CONSTRUCTION



The dimensions (max 111.9 mm x 38.7 mm x 35 mm) and terminal location can be seen from the drawing given above.
Since the aluminium heat-sink is insulated from the circuit, no special measures need be taken regarding the mounting of the unit. The mechanical design of the PA 10 is based on its use in the standardized mounting chassis 4322 026 38240. For this purpose the PA 10 is to be mounted directly on a printed-wiring board. On such a standard printed-wiring board (4322 026 38680), up to four PA 10's can be mounted; it takes two positions in the chassis 4322 026 38240. To ensure proper cooling of the unit, the PA 10 has to be mounted in such a way that a free flow of air through it is guaranteed.

INPUT REQUIREMENTS

A d.c. voltage level is applied to terminal G.

Output transistor TR_3 non-conducting

voltage	V_G = max. 0.3 V = min. 0 V
required direct current	$-I_{GD}$ = max. 5.3 mA
required transient charge when V_G changes from 2/3 V_P to 0.5 V in 1.5 µs	$-Q_{GT}$ = max. 5.2 nC

Output transistor TR_3 conducting

voltage	V_G = min. 2/3 V_P = max. V_P

Type of diodes and maximum number connected in parallel at terminal EG:
12 x OA85/OA95

OUTPUT DATA

Output transistor TR_3 non-conducting

voltage	$-V_Q$ = absolute max. 55 V
leakage current	$-I_Q$ = max. 30 mA

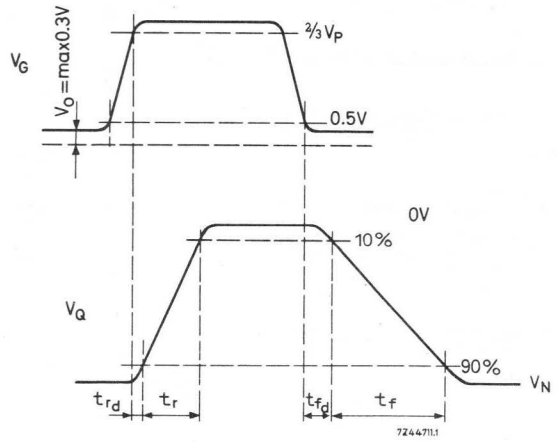
Output transistor TR_3 conducting

voltage	$-V_Q$ = max. 1.2 V
available load current	$-I_Q$ = min. 2A (switching rate = max. 40 Hz) For load currents less than 2A the maximum switching rate has to be determined with the formula below: $f_{max} = 360 - 160\,\lvert I_Q \rvert$

Delays and switching times (for orientation only)

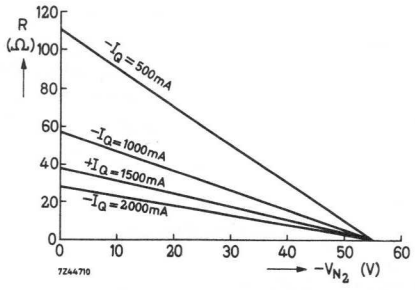
Unit loaded with a resistor of 30 Ω

Rise delay : t_{rd} = max. 10 µs
Rise time : t_r = max. 50 µs
Fall delay : t_{fd} = max. 25 µs
Fall time : t_f = max. 100 µs



Unit loaded with an inductive load

The unit is provided with a built-in diode to protect the output transistor against voltage transients which occur when an inductive load is switched. This protection is realized at the expense of a very long fall delay time of the current in this load.
At supply voltages below 55 V , however, a wire jumper in series with this diode can be interchanged with a resistor to decrease this delay time.
The max. permissible value of this resistor is given in the figure below with the current, flowing through the load at the moment of switching-off, as parameter.



NUMERICAL INDICATOR TUBE DRIVER

The unit ID 10 can drive the numerical indicator tube ZM1000, ZM1020 or ZM1080. It has to be driven by a decade counter operating in the 1-2-4-8 or 1-2-4-2 (jump at 8) code.

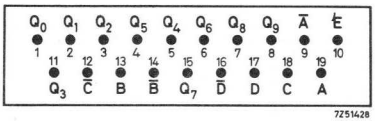
The unit comprises the decoding circuits for both codes as well as the driver stages for the ZM1000, ZM1020 or ZM1080.

When the decade counter is set on digit number 0, the inputs A, B, C and D of the ID 10 are to be connected to the outputs of the flip-flops in the decade, which are at low level. Consequently the inputs $\overline{A}$, $\overline{B}$, $\overline{C}$ and $\overline{D}$ are to be connected to the flip-flop outputs which are at high level.

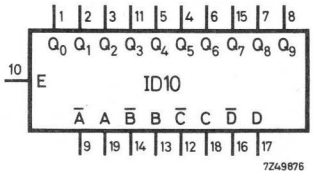
Primarily the ID 10 forms a load for outputs of flip-flops, which are at high level. For flip-flop outputs at low level the ID 10 forms a relative low load.
So any additional load in excess of the ID 10 is restricted by the specified minimum value of the high level for the flip-flop outputs.
The last flip-flop of the decade counter is still capable to drive the next decade.

The circuit is mounted inside a sealed metal can with 19 wire terminals.

Ambient-temperature range:		
	operating	−55 to +55 °C
	storage	−55 to +85 °C
Weight		approx. 40 g
Case		high standard case

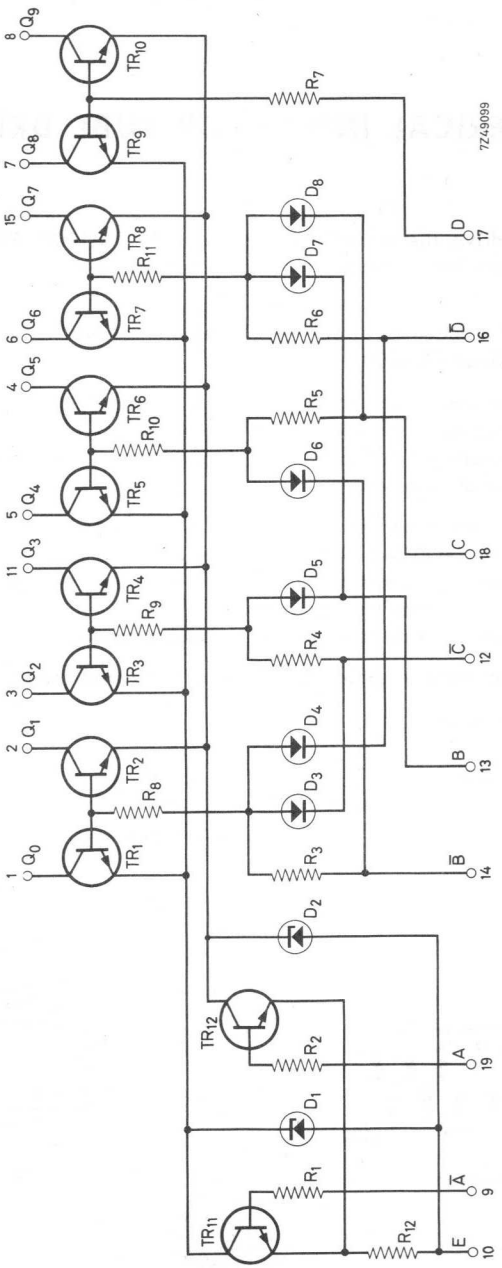


terminal location



drawing symbol

CIRCUIT DATA



Terminals

1 = Q_0 = output to be connected to pin k_0 of indicator tube
2 = Q_1 = output to be connected to pin k_1 of indicator tube
3 = Q_2 = output to be connected to pin k_2 of indicator tube
4 = Q_5 = output to be connected to pin k_5 of indicator tube
5 = Q_4 = output to be connected to pin k_4 of indicator tube
6 = Q_6 = output to be connected to pin k_6 of indicator tube
7 = Q_8 = output to be connected to pin k_8 of indicator tube
8 = Q_9 = output to be connected to pin k_9 of indicator tube
9 = $\overline{A}$ = input to be connected to $\overline{Q}$ of driving flip-flop A
10 = E = common supply 0V
11 = Q_3 = output to be connected to pin k_3 of indicator tube
12 = $\overline{C}$ = input to be connected to $\overline{Q}$ of driving flip-flop C
13 = B = input to be connected to Q of driving flip-flop B
14 = $\overline{B}$ = input to be connected to $\overline{Q}$ of driving flip-flop B
15 = Q_7 = output to be connected to pin k_7 of indicator tube
16 = $\overline{D}$ = input to be connected to $\overline{Q}$ of driving flip-flop D
17 = D = input to be connected to Q of driving flip-flop D
18 = C = input to be connected to Q of driving flip-flop C
19 = A = input to be connected to Q of driving flip-flop A

Power supply

Terminal 10 : 0V common, connected to the metal case

V_b = 250V ± 10%, R_a = 68kΩ ± 2% } power supply for the ZM1000,
V_b = 250V ± 15%, R_a = 62kΩ ± 2% } ZM1020 or ZM1080

INPUT REQUIREMENTS

Input at low level

Voltage V_I = min. 0V
= max. 0.3V

	A, $\overline{A}$, D	$\overline{B}$, C, $\overline{C}$, $\overline{D}$	B
Required direct current	0mA	0.3mA	0.6mA

Input at high level

Voltage V_I = min. 7.6V
= max. 15V

	A, $\overline{A}$, D	$\overline{B}$, C, $\overline{C}$, $\overline{D}$	B
Required direct current	0.2mA	0.28mA	0mA

When the ID 10 is driven by flip-flops with only the Q-outputs connected to the inputs of the ID 10, the Q-outputs of these flip-flops may furthermore be loaded with a number of 10-series diode-inputs, provided each driven input represents a load of $-I_D$ = max. 1.1mA and $-Q_T$ = max. 3.4nC, as stated on the next page.

input ID 10	number of diode-inputs	
	min. 0 °C	min. -25 °C
A, $\overline{A}$, D	6	6
B	7	5
$\overline{B}$, C, $\overline{C}$, $\overline{D}$	4	4

The loadability of the flip-flop outputs can be increased by connecting an external resistor of 51 kΩ ± 5% in parallel for each additional diode-input with the built-in collector resistor of the corresponding output. This resistor has to be connected between the output terminal and the positive voltage supply V_p.
This resistor however represents a load at low level for the driving unit.

Required direct current : I_R = max. 0.2 mA
Required transient charge: Q_R = max. 0.2 nC

Note - When a current is flowing towards the unit the positive sign is used.

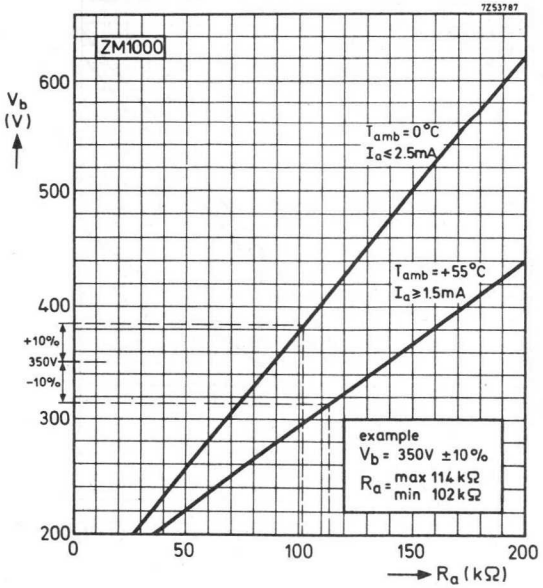
OUTPUT DATA

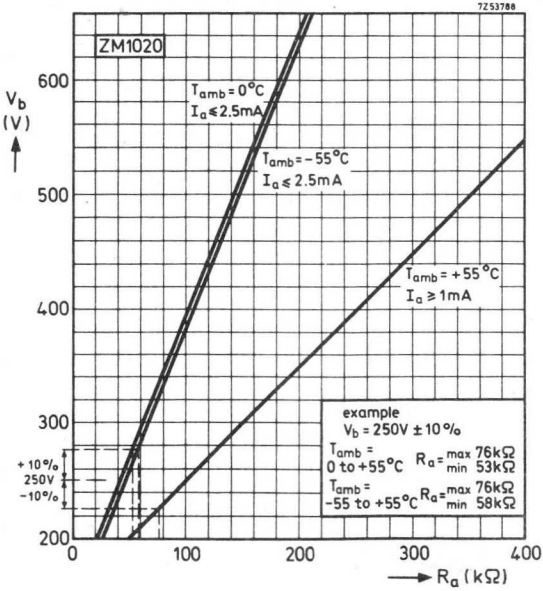
The outputs Q_0 up to and including Q_9 of the ID 10 have to be connected to the pins k_0 up to and including k_9 of the numerical indicator tube ZM1000, ZM1020 or ZM1080.
The anode of these tubes has to be connected via a resistor R_a to the high voltage power supply V_b.

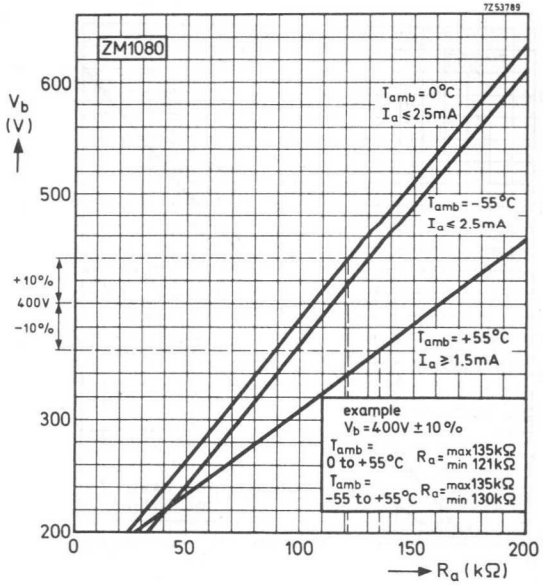
The current available at these 10 numerical outputs of the ID 10 can cope with the required cathode current I_k of the indicator tube ZM1000, ZM1020 or ZM1080, when the following conditions are observed:

a. operation temperature range
b. power supply V_b for ZM1000, ZM1020 or ZM1080
c. anode series resistor R_a

In the following graphs these data are specified.

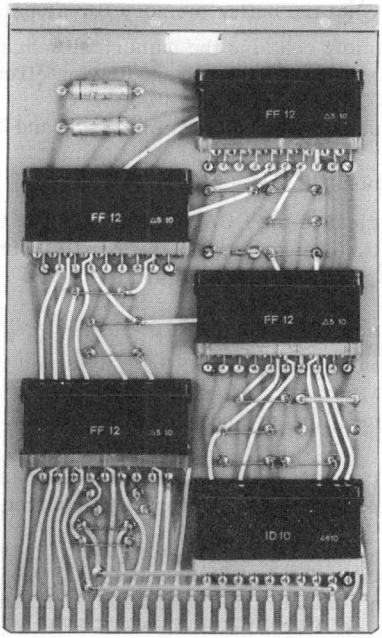

7Z53787
ZM1000
V_b (V)
600
500
400
300
200
+10%
350V
-10%
T_{amb} = 0°C
$I_a \leq$ 2.5mA
T_{amb} = +55°C
$I_a \geq$ 1.5mA
example
V_b = 350V ±10%
R_a = max 114kΩ
min 102kΩ
0
50
100
150
200
R_a (kΩ)


7Z53788
ZM1020
V_b (V)
600
500
400
300
200
+10%
250V
-10%
T_{amb} = 0°C
$I_a \leq$ 2.5mA
T_{amb} = −55°C
$I_a \leq$ 2.5mA
T_{amb} = +55°C
$I_a \geq$ 1mA
example
V_b = 250V ±10%
T_{amb} = 0 to +55°C R_a = max 76kΩ min 53kΩ
T_{amb} = −55 to +55°C R_a = max 76kΩ min 58kΩ
0
100
200
300
400
R_a (kΩ)



Wiring capacitance at each output Q-terminal of the ID10: max. 500 pF

DECADE COUNTER AND NUMERICAL INDICATOR TUBE DRIVER ASSEMBLY



RZ 22603-11

The assembly consists of four circuit blocks FF 12, with or without a circuit block ID 10, mounted on a printed-wiring board. It is available in five versions.

- DCA 10 A catalog number 2722 009 02001.

  This assembly contains four flip-flops FF 12, intended to be used as a single decade counter, operating in the 1-2-4-8 code, and a numerical indicator tube driver ID 10, providing the BCD - to decimal decoding- and driving circuits for the numerical indicator tube ZM1000, ZM1020 or ZM1080.
  The required interconnections are shown in Figs. 1 and 2.

- DCA 10 B catalog number 2722 009 02011.

  This assembly is identical to the DCA 10 A but without the circuit block ID 10 mounted on the board. The lay-out of the printed-wiring board allows the mounting of the ID 10 separately (see Figs. 7 and 8).

- DCA 10 C catalog number 2722 009 02021.

  This assembly contains four flip-flops FF 12, intended to be used as a buffer memory. When the trigger inputs of the four flip-flops are interconnected externally, with one trigger pulse applied to this common trigger line, the contents of a decade counter can be shifted in parallel into the buffer memory. To this end the Q-outputs of the decade counter have to be connected to the corresponding gate inputs (G) of the buffer memory flip-flops.

  Furthermore the assembly contains the numerical indicator tube driver ID 10, providing the BCD - to decimal decoding and driving circuits for the numerical indicator tube ZM1000, ZM1020 or ZM1080.
  The required interconnections are shown in Figs. 9 and 10.

- DCA 10 D catalog number 2722 009 02031.

  This assembly is identical to the DCA 10 C but without the circuit block ID 10 mounted on the board. The lay-out of the printed-wiring board allows the mounting of the ID 10 separately (see Figs. 11 and 12).

- DCA 10 E catalog number 2722 009 02041.

  This assembly contains four flip-flops FF 12, intended to be used as a binary counter, scaler of 16.
  The required interconnections are shown in Figs. 13 and 14.

All these versions are provided with the capacitors C_1 and C_2, which filter the supply voltages from noise. These capacitors are mounted on the printed-wiring board.

The bare printed-wiring board (catalog number 4322 026 38700), provided with plated-through holes and double-sided goldplated contacts, is made of glass-epoxy material. Moreover, the printed-wiring board is delivered with an extractor and a locking device. With the mating connector (catalog number 2422 020 52591), not supplied with the assembly, the printed-wiring board of standard dimensions (121.8 mm x 207.0 mm x 1.6 mm) can be used directly in the standard mounting chassis (catalog number 4322 026 38240). The circuit blocks are secured to the printed-wiring board by means of locking caps (catalog number 4322 026 32150).

Counting rate		max. 30 kHz
Ambient temperature range		
	operating	−25 to +55 °C
		below 0 °C: derated output data
	storage	−55 to +75 °C
Weight		approx. 300 g

The date specified below apply to the DCA 10 A in particular.
For the sake of simplicity for the other versions only data are specified separately, which differ from those of the DCA 10 A.

DECADE COUNTER AND NUMERICAL INDICATOR TUBE DRIVER DCA 10 A

CIRCUIT DATA

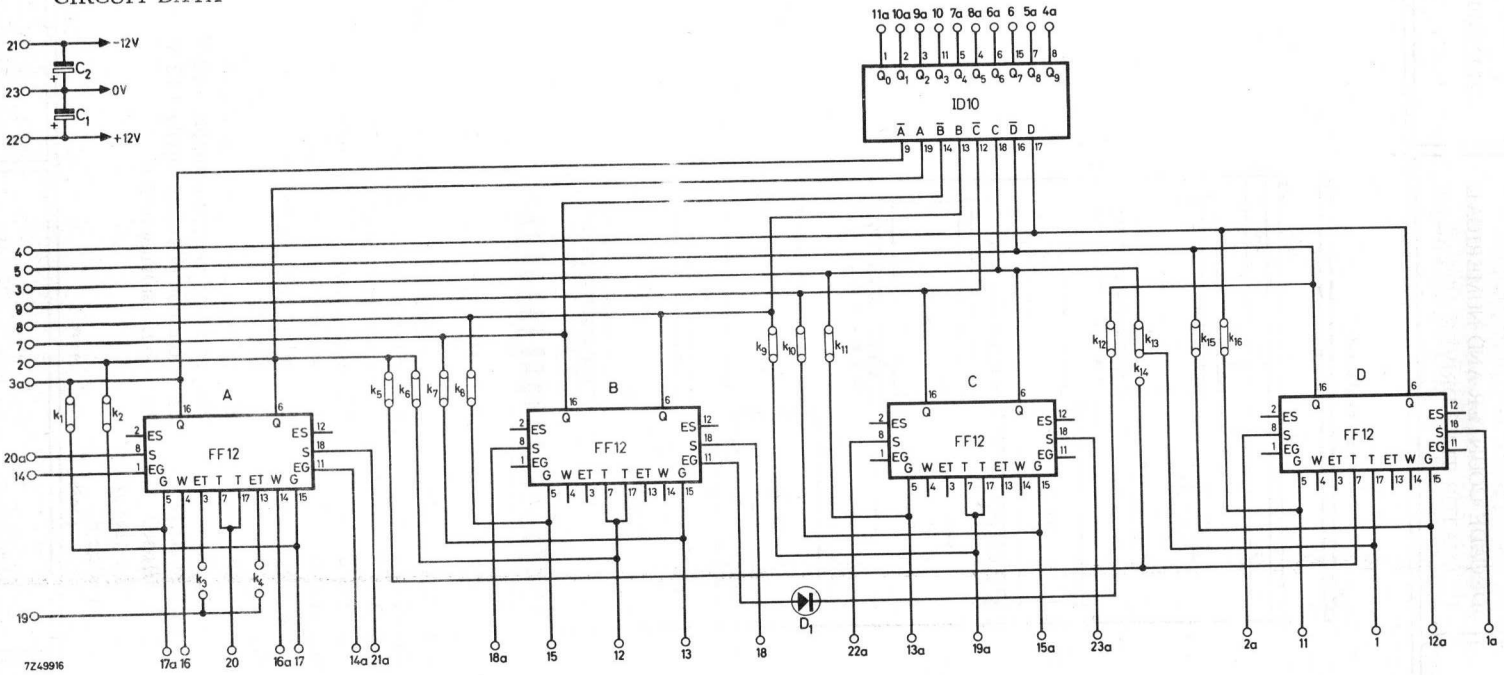


Fig. 1

D105

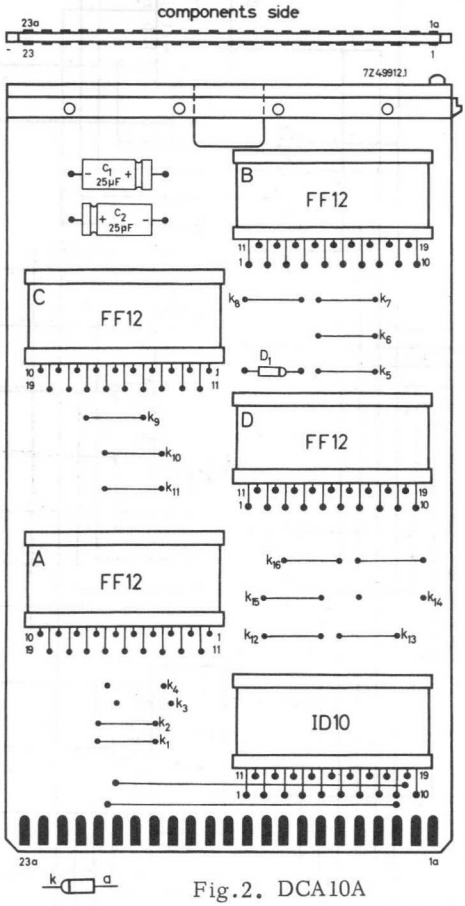


Fig.2. DCA10A

Terminals

1 = trigger input T of flip-flop D
2 = output Q of flip-flop A
3 = output Q of flip-flop C
4 = output Q of flip-flop D
5 = output $\overline{Q}$ of flip-flop D
6 = numerical output 7 of ID 10
7 = output $\overline{Q}$ of flip-flop B
8 = output Q of flip-flop B
9 = output $\overline{Q}$ of flip-flop C
10 = numerical output 3 of ID 10
11 = gate input G of flip-flop D
12 = trigger input T of flip-flop B
13 = gate input G of flip-flop B
14 = extension gate input EG of flip-flop A
15 = gate input G of flip-flop B
16 = base input W of flip-flop A
17 = gate input G of flip-flop A
18 = set input S of flip-flop B
19 = additional trigger input T of flip-flop A
20 = trigger input T of flip-flop A
21 = common negative supply −12 V
22 = common positive supply +12 V
23 = common supply 0 V

1a = set input S of flip-flop D
2a = set input S of flip-flop D
3a = output $\overline{Q}$ of flip-flop A
4a = numerical output 9 of ID 10
5a = numerical output 8 of ID 10
6a = numerical output 6 of ID 10
7a = numerical output 4 of ID 10
8a = numerical output 5 of ID 10
9a = numerical output 2 of ID 10
10a = numerical output 1 of ID 10
11a = numerical output 0 of ID 10
12a = gate input G of flip-flop D
13a = gate input G of flip-flop C
14a = extension gate input EG of flip-flop A
15a = gate input G of flip-flop C
16a = base input W of flip-flop A
17a = gate input G of flip-flop A
18a = set input S of flip-flop B
19a = trigger input T of flip-flop C
20a = set input S of flip-flop A
21a = set input S of flip-flop A
22a = set input S of flip-flop C
23a = set input S of flip-flop C

Power supply

Terminal 21 : $V_N = -12\ V \pm 5\%$, $-I_N = 4.1$ mA
22 : $V_P = +12\ V \pm 5\%$, $I_P = 30$ mA
23 : $V_E = 0$ V common

} The current values are nominal

INPUT REQUIREMENTS (at $V_P = 11.4$ V and $V_N = -12.6$ V unless specified differently)

Set/reset input (S-terminals)

Each S-input of the four flip-flops is brought out separately. A "positive low" voltage (between 0 V and 0.3 V) drives the corresponding transistor into the non-conducting state.

Transistor-conducting		
Voltage	V_S	= min. 2/3 V_P = max. V_P
Transistor non-conducting		
Voltage	V_S	= min. 0 V = max. 0.3 V
Required direct current	$-I_{SD}$	= max. 1.95 mA
Required transient charge when V_S changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{ST}$	= max. 2.8 nC

When the four flip-flops are reset simultaneously

Required direct current	$-I_{SD}$	=	min. 7.8	mA	
Required transient charge when V_S changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{ST}$	=	max. 11.2	nC	

Time data

Pulse duration	t_p	=	min. 8	μs	See point 4 x)
Recovery time	t_{rec}	=	min. 15	μs	
Time delay between S- and T-signal	t_{st}	=	min. 15	μs	See point 5 x)

Gate input (G-terminals)

A d.c. voltage level is applied to terminal G.
A "positive low" voltage closes the gate, whilst a "positive high" voltage (between 2/3 V_P and V_P) opens the gate.

Gate open

Voltage	V_G	=	min. 2/3	V_P	
		=	max.	V_P	

Gate closed

Voltage	V_G	=	min. 0	V	
		=	max. 0.3	V	
Required direct current	$-I_{GD}$	=	max. 1.1	mA	
Required transient charge when V_G changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{GT}$	=	max. 1.2	nC	

Time data

Trigger gate setting time	t_{gs}	=	min. 29	μs	See point 6 x)
Trigger gate inhibiting time	t_{gi}	=	min. 29	μs	See point 7 x)

Trigger input (T-terminals)

A negative-going voltage step or trigger pulse is applied to the trigger inputs T of flip-flop A (terminal 20).
Each trigger pulse applied to this terminal switches the flip-flop, provided that the corresponding G- and EG inputs are left floating or min. 2/3 V_P (gate open).

x) Section "Time definitions" of "Circuit blocks 10-Series".

		Gate open	Gate closed
	V_G	= min. 2/3 V_P = max. V_P	= min. 0 V = max. 0.3 V
Required direct current when V_T = max. 0.3 V	$-I_{TD}$	= max. 1.1 mA	= 0 mA
Required transient charge when V_T changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{TT}$	= max. 3.4 nC	= 0 nC
Time data			
Fall time	t_f	= max. 1.5 μs	See point 3 *)
Pulse duration	t_p	= min. 2 μs	
Trigger gate setting time	t_{gs}	= min. 29 μs	

Base input (W-terminals)

Capacitance (wiring plus output of TG 13, TG 14 or TG 15) max. 95 pF

Note - The output capacitance of the trigger gates TG 13, TG 14 and TG 15 is max. 5 pF

OUTPUT DATA (at V_P = 11.4 V and V_N = −12.6 V, unless specified differently)

Decade counter section

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board, including the numerical indicator tube driver ID 10, the Q-outputs of each flip-flop in the decade counter may furthermore be loaded as specified in the following table.

The loadability of the flip-flop outputs can be increased by connecting an external resistor in parallel with the built-in collector resistor of the corresponding output. This resistor has to be connected between the output terminal and V_P.
For each additional driven input, a parallel resistor of 51 k$\Omega \pm 5\%$ is required.
The total number of driven inputs is also specified in the following table.

*) Section "Time definitions" of "Circuit blocks 10-Series".

flip-flop		FF 12-A		FF 12-B		FF 12-C		FF 12-D	
output terminal		$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
		3a	2	7	8	9	3	5	4
max. number of 10-series circuit blocks, that may be driven, provided each driven input represents a load: $-I_D$ = max. 1.1 mA and $-Q_T$ = max. 3.4 nC	T_{amb} = min. 0 °C	5	2	3	5	3	3	2	5
	T_{amb} = min. −25 °C	5	2	3	3	3	3	2	5
max. number of driven 10-series circuit blocks with external parallel collector resistor(s)	T_{amb} = min. 0 °C	6	5	5	5	5	4	4	6
	T_{amb} = min. −25 °C	5	3	4	3	4	3	3	5

Wiring capacitance at each Q-output max. 175 pF

Output levels during counting

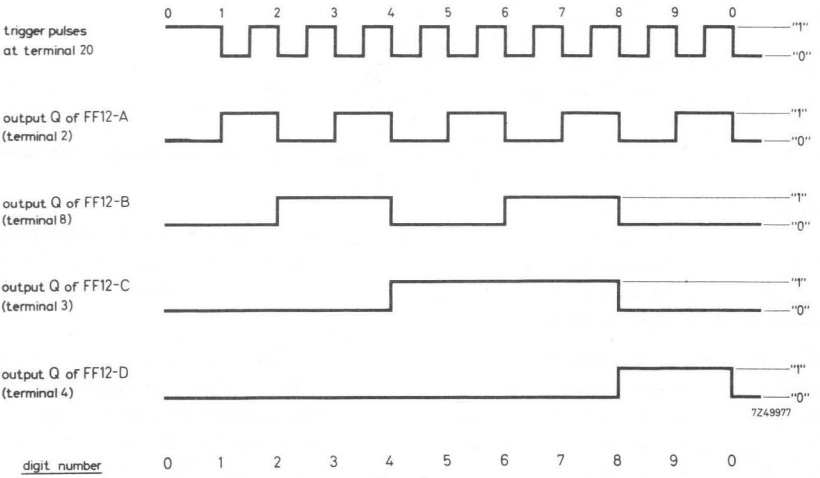


Fig.3

The output levels at the Q-outputs of each flip-flop are shown in Fig.3.
Note that when a Q-output is at "positive low" ("0") level the corresponding $\overline{Q}$-output is at "positive high" ("1") level and vice versa.
After 10 negative-going pulses at the trigger input terminal 20, the output Q of flip-flop D delivers the negative-going carry pulse for the next decade, while the decade counter has resumed its initial position, namely all Q-output terminals being at "positive low" level.
The relation between a digit number (output ID 10) and the corresponding state of each flip-flop is shown in the figure as well.

Numerical indicator tube driver section

The outputs Q_0 (terminal 11a) up to and including Q_9 (terminal 4a) of the ID 10 have to be connected to the pins k_0 up to and including k_9 of the numerical indicator tube ZM1000, ZM1020 or ZM1080. The anode of these tubes has to be connected via a resistor (R_a) to the high voltage power supply (V_b).

The current available at these 10 numerical outputs of the ID 10 can cope with the required cathode current I_k of the indicator tubes ZM1000, ZM1020 and ZM1080, when the following conditions are observed:
- operating-temperature range
- power supply V_b for ZM1000, ZM1020 and ZM1080
- anode series resistor R_a.

In the following graphs these data are specified.

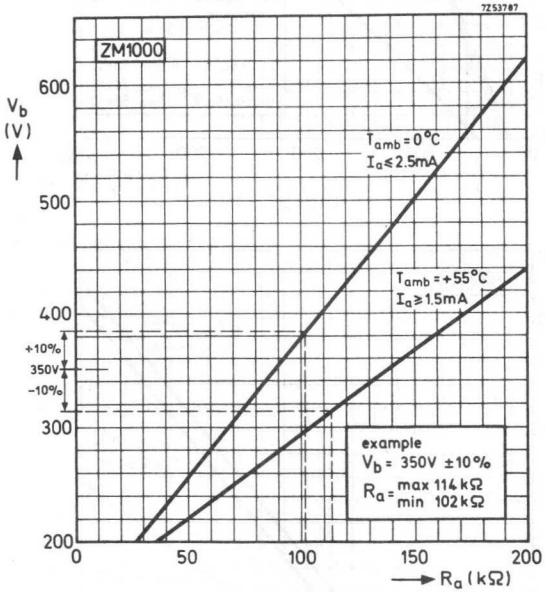


Fig.4

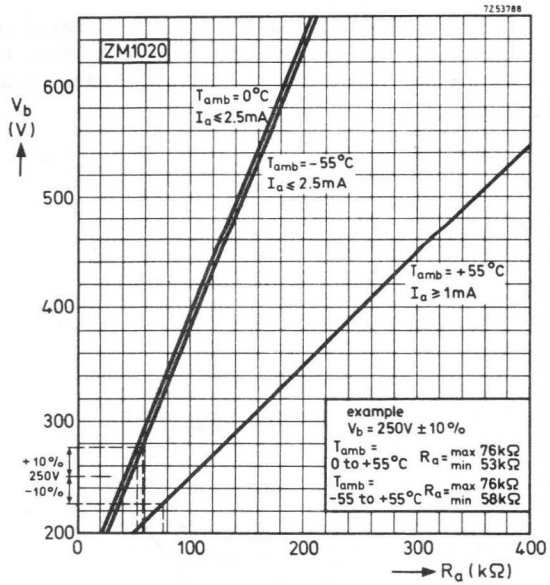


Fig. 5

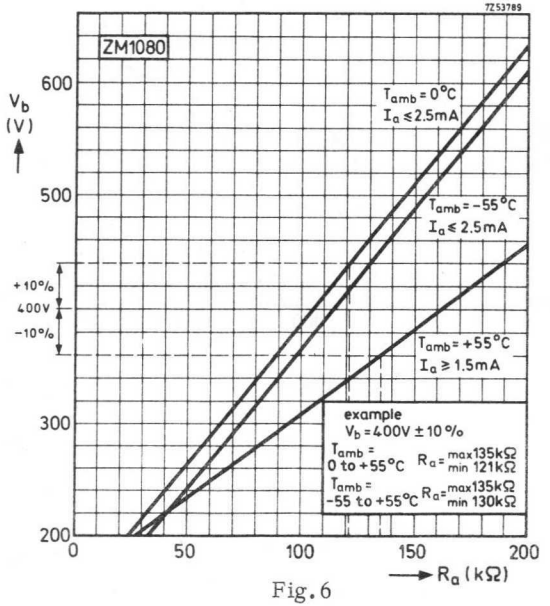


Fig. 6

Wiring capacitance at each Q-output of the ID10 max. 500 pF

DECADE COUNTER DCA 10 B

CIRCUIT DATA

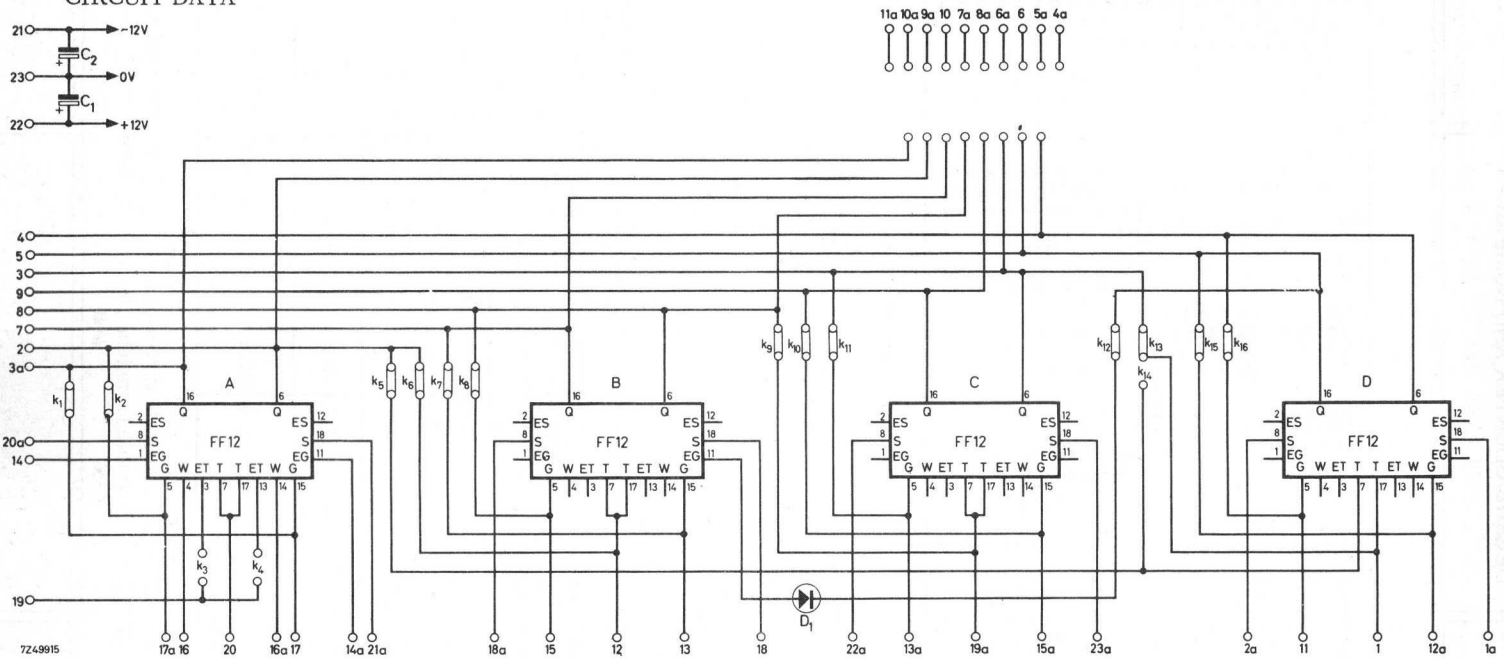


Fig. 7

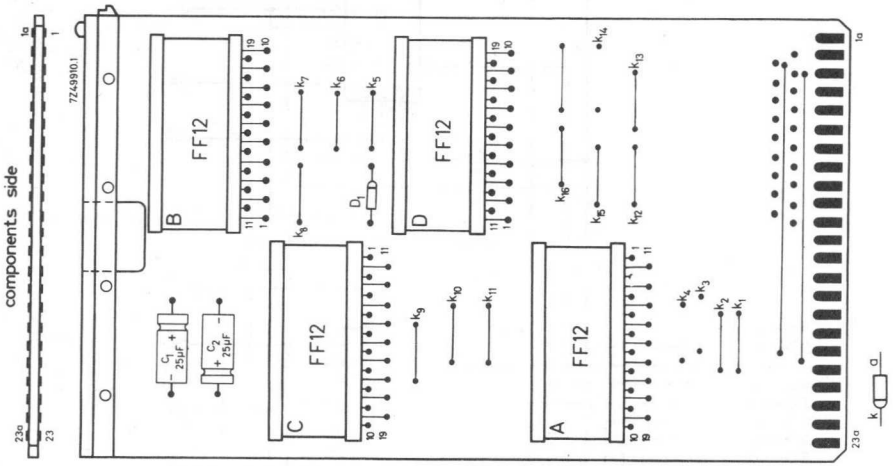


Fig.8. DCA10B

Terminals (Fig.8)

Similar to DCA 10 A, with exception of terminals 4a, 5a, 6, 6a, 7a, 8a, 9a, 10, 10a, 11a, which are inoperative.

INPUT REQUIREMENTS

Similar to DCA 10 A.

OUTPUT DATA (at V_P = 11.4 V and V_N = −12.6 V, unless specified differently)

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board, the Q-outputs of each flip-flop in the decade counter may furthermore be loaded as specified in the table below.

flip-flop	FF 12-A		FF 12-B		FF 12-C		FF 12-D	
output terminal	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
	3a	2	7	8	9	3	5	4
available direct current: I_{QD} in mA	7.1	6	7.1	6	7.1	6	6	7.1
available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 μs: Q_{QT} in nC	25.8	22.4	25.8	22.4	25.8	22.4	25.8	25.8

For T_{amb} = min. −25 °C the available direct current I_{QD} has to be reduced with 1.6 mA and similarly the available transient charge Q_{QT} with 5 nC.

CIRCUIT DATA

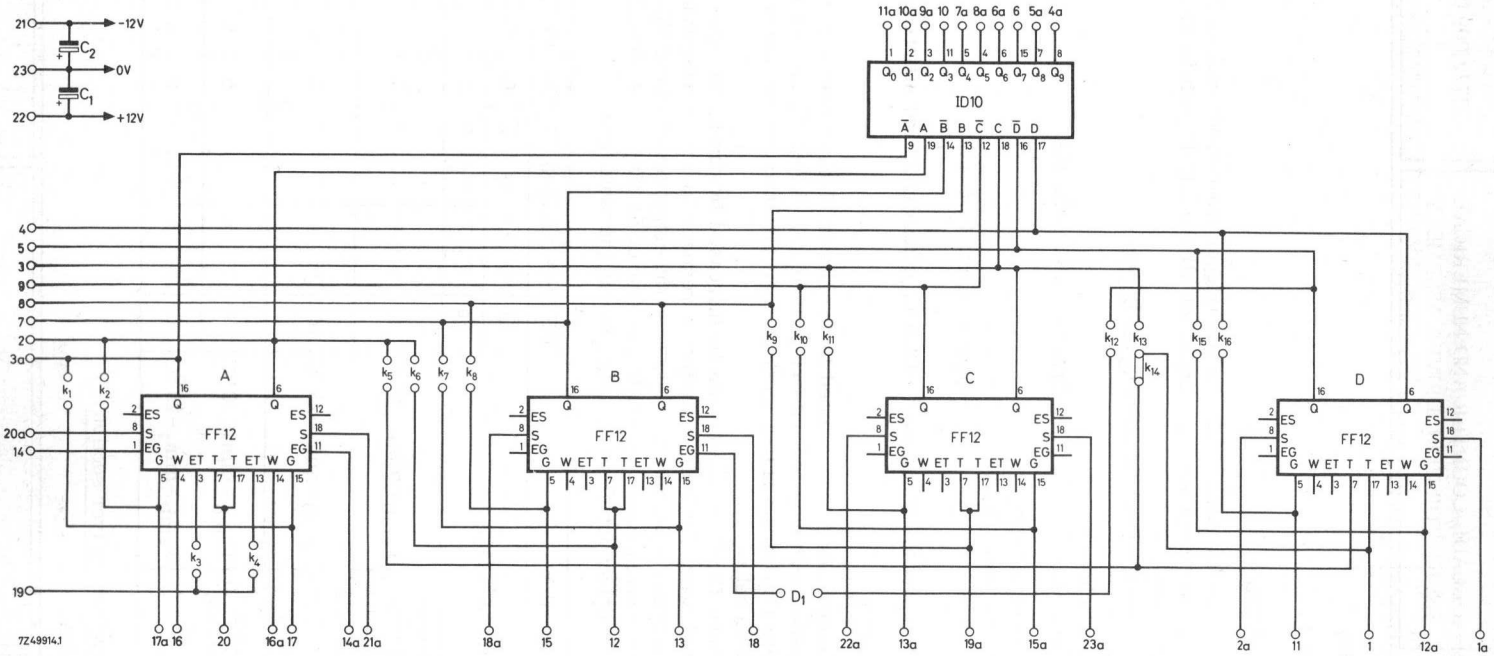


Fig. 9

Terminals (Fig.10)

Similar to DCA 10 A.

INPUT REQUIREMENTS

Similar to DCA 10 A, with the exception of the trigger input requirements due to the fact that in this version the trigger inputs of all the flip-flops have to be interconnected externally.
The input requirements for this common trigger line are:

Required direct current
when V_T = max. 0.3 V $\quad -I_{TD}$ = max. 4.4 mA

Required transient charge
when V_T changes from 2/3 V_P
to 0.5 V in 1.5 μs $\quad -Q_{TT}$ = max. 13.6 nC

OUTPUT DATA (at V_P = 11.4 V and V_N = −12.6 V, unless specified differently)

Buffer memory section

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board, including the numerical indicator driver ID 10, the Q-outputs of each flip-flop in the buffer memory may furthermore be loaded as specified in the table below.
The loadability of the flip-flop outputs can be increased by putting an external resistor in parallel with the built-in collector resistor of the corresponding output. This resistor has to be connected between the output terminal and V_P.
For each additional driven input a parallel resistor of 51 kΩ ±5% is required.
The total number of driven inputs is also specified in the table below.

flip-flop		FF 12-A		FF 12-B		FF 12-C		FF 12-D	
output terminal		$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
		3a	2	7	8	9	3	5	4
max. number of 10-series circuit blocks, that may be driven provided each driven input represents a load of $-I_D$ = max.1.1 mA and $-Q_T$ = max. 3.4 nC	T_{amb} = min. 0 °C	6	6	4	7	4	4	4	6
	T_{amb} = min. −25 °C	6	6	4	5	4	4	4	6
max. number of driven 10-series circuit blocks, with external parallel collector resistor(s)	T_{amb} = min. 0 °C	7	7	6	7	6	6	6	7
	T_{amb} = min. −25 °C	6	6	5	5	5	5	5	6

Numerical indicator tube driver section

Similar to DCA 10 A.

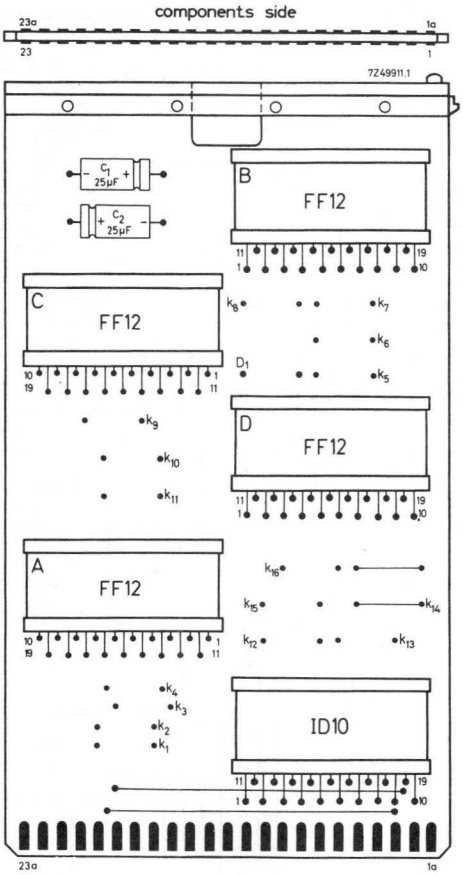


Fig.10. DCA 10 C

BUFFER MEMORY DCA 10 D

CIRCUIT DATA

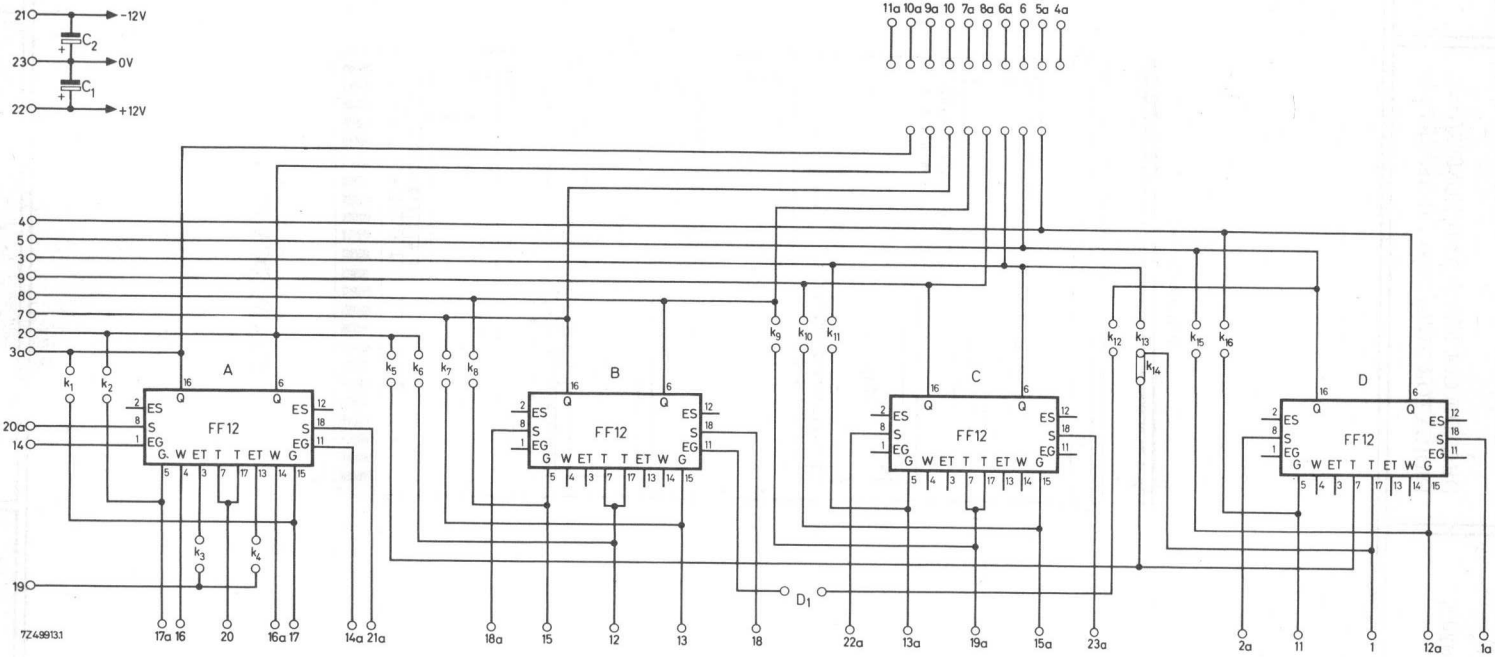


Fig.11

Terminals (Fig.12)

Similar to DCA 10 A, with the exception of terminals 4a, 5a, 6, 6a, 7a, 8a, 9a, 10, 10a and 11a, which are inoperative.

INPUT REQUIREMENTS

Similar to DCA 10 C.

OUTPUT DATA (at V_P = 11.4 V and V_N = −12.6 V, unless specified differently)

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board, the Q-outputs of each flip-flop in the buffer memory may furthermore be loaded as specified in the table below.

flip-flop	FF 12-A		FF 12-B		FF 12-C		FF 12-D	
output terminal	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
	3a	2	7	8	9	3	5	4
available direct current: I_{QD} in mA	8.2	8.2	8.2	8.2	8.2	8.2	8.2	8.2
available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 μs: Q_{QT} in nC	27	27	27	27	27	27	27	27

For T_{amb} = min. −25 °C the available direct current I_{QD} has to be reduced with 1.6 mA and similarly the available transient charge Q_{QT} with 5 nC.

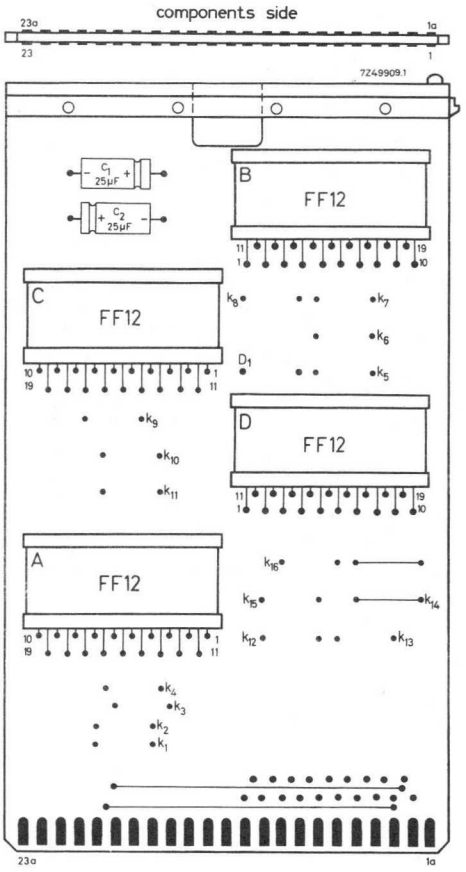


Fig.12. DCA 10 D

BINARY COUNTER DCA 10 E

CIRCUIT DATA

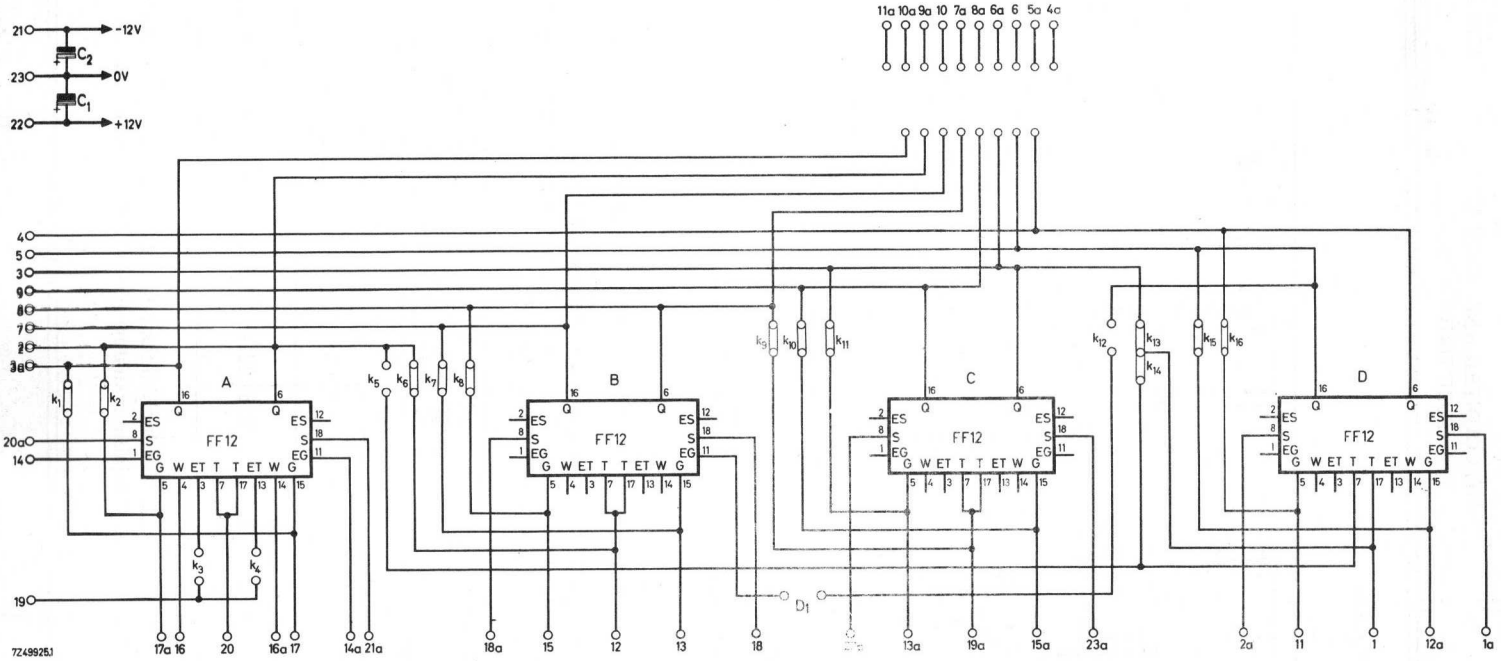


Fig.13

Terminals (Fig.14)

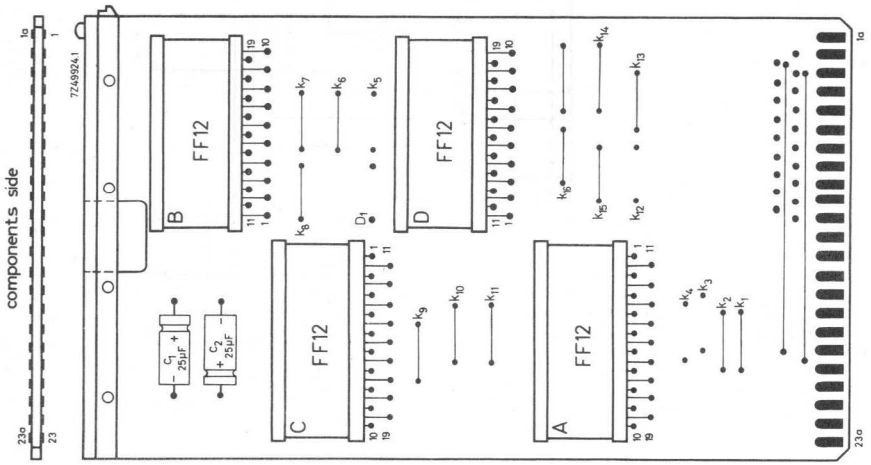


Fig.14. DCA 10 E

Similar to DCA 10 B.

INPUT REQUIREMENTS

Similar to DCA 10 A.

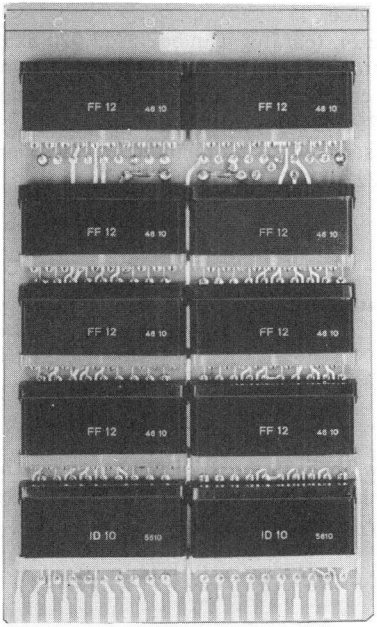
OUTPUT DATA (at V_P = 11.4 V and V_N = −12.6 V, unless specified differently)

In excess of the internal load, represented by the circuit blocks on the printed-wiring board, the Q-outputs of each flip-flop in the binary counter may furthermore be loaded as specified in the table below.

flip-flop	FF 12-A		FF 12-B		FF 12-C		FF 12-D	
output terminal	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
	3a	2	7	8	9	3	5	4
available direct current: I_{QD} in mA	7.1	6	7.1	6	7.1	6	7.1	7.1
available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 µs: Q_{QT} in nC	25.8	22.4	25.8	22.4	25.8	22.4	25.8	25.8

For T_{amb} = min. −25 °C the available direct current I_{QD} has to be reduced with 1.6 mA and similarly the available transient charge Q_{QT} with 5 nC.

DUAL DECADE COUNTER AND NUMERICAL INDICATOR TUBE DRIVER ASSEMBLY



RZ 22603-9

This assembly consists of eight circuit blocks FF 12, with or without a circuit block ID 10, mounted on a printed-wiring board. It is available in two versions.

- 2.DCA 11 A, catalog number 2722 009 02051.

  This assembly contains eight flip-flops FF 12, intended to be used as a dual decade counter, operating in the 1-2-4-8 code, each decade provided with a common reset line. It contains also two numerical indicator tube drivers ID 10, providing the BCD - to decimal decoding - and driving circuits for the numerical indicator tube ZM 1000, ZM 1020 or ZM 1080.
  The circuit diagram and the required interconnections are shown in Figs. 1 and 2.

- 2.DCA 11 B, catalog number 2722 009 02061.

  This assembly is identical to the 2.DCA 11 A, but without the circuit blocks ID 10 mounted on the board. The lay-out of the printed-wiring board allows the mounting of the ID 10's separately (see Figs. 7 and 8).

The bare printed-wiring board (catalog number 4322 026 38710), provided with plated-through holes and double-sided goldplated contacts, is made of glass-epoxy material. Moreover the printed-wiring board is delivered with an extractor and a locking device.
With the mating connector (catalog number 2422 020 52591), not supplied with the assembly, the printed-wiring board of standard dimensions (121.8 mm x 207.0 mm x 1.6 mm) can be used directly in the standard mounting chassis (catalog number 4322 026 38240).
The circuit blocks are secured to the printed-wiring board by means of locking caps (catalog number 4322 026 32150).

Counting rate		max. 30 kHz
Ambient-temperature range		
	operating	−25 to +55 °C below 0 °C: derated output data
	storage	−55 to +75 °C
Weight		approx. 500 g

The data specified below apply to the 2.DCA 11 A in particular.
For the sake of simplicity for the version 2.DCA 11 B only data are specified separately, which differ from those of the 2.DCA 11 A.

DUAL DECADE COUNTER AND NUMERICAL INDICATOR TUBE DRIVER 2.DCA 11 A

CIRCUIT DATA

For circuit diagram see next pages.

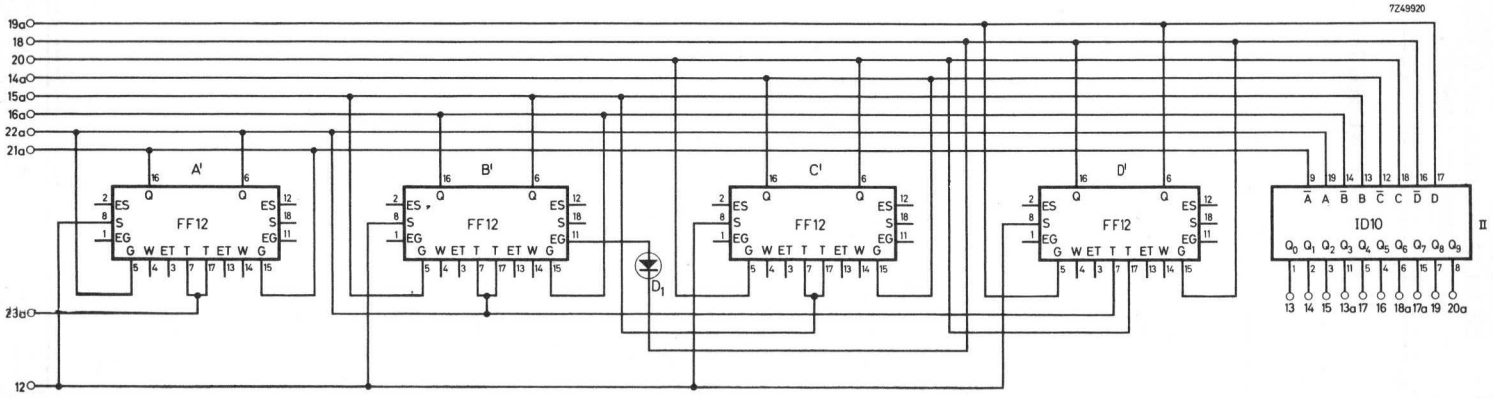


Fig.1a. 2.DCA 11 A

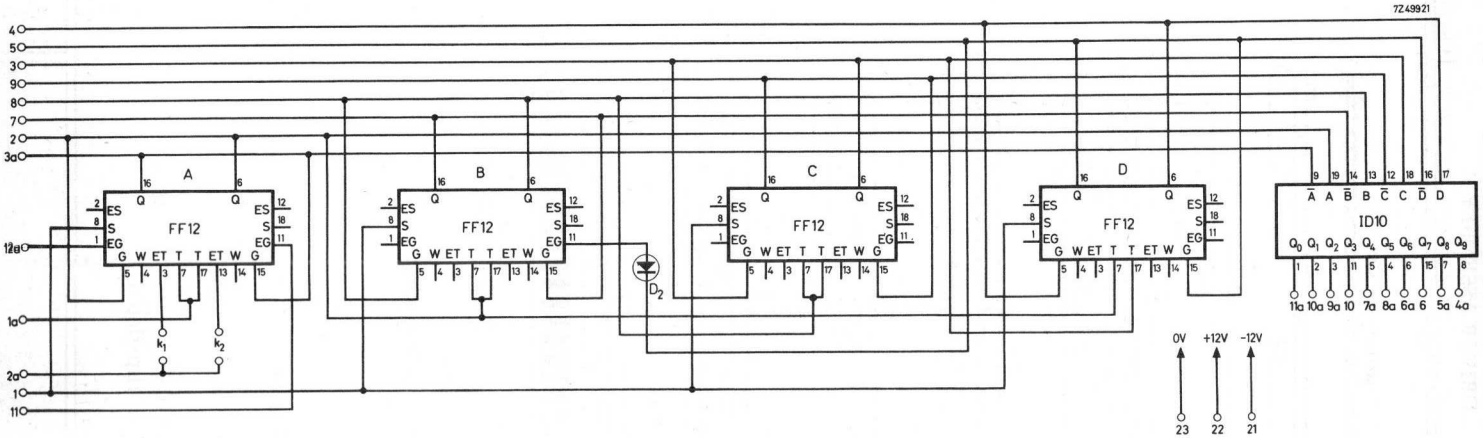


Fig.1b. 2.DCA 11 A

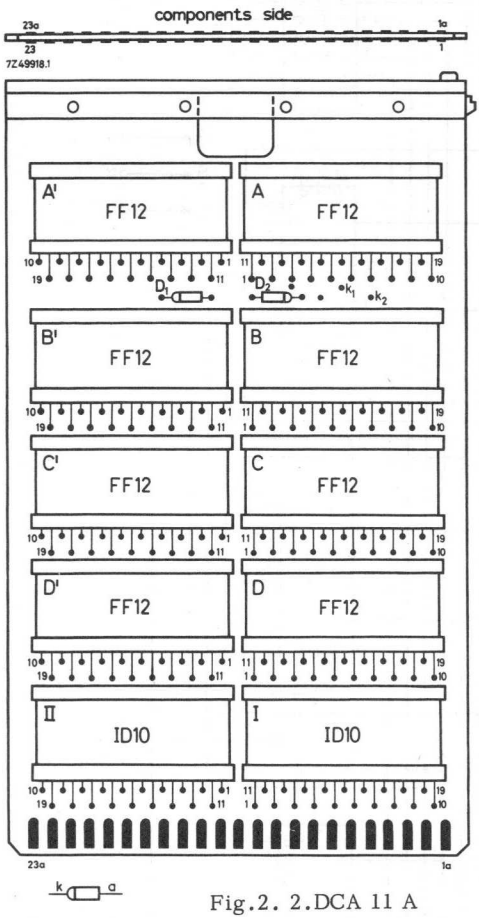


Fig.2. 2.DCA 11 A

Terminals

1 = common reset input S of decade counter I
2 = output Q of flip-flop A
3 = output Q of flip-flop C
4 = output Q of flip-flop D
5 = output $\overline{Q}$ of flip-flop D
6 = numerical output 7 of ID 10-I
7 = output $\overline{Q}$ of flip-flop B
8 = output Q of flip-flop B
9 = output $\overline{Q}$ of flip-flop C
10 = numerical output 3 of ID 10-I
11 = extension gate input EG of flip-flop A

12 = common reset input S of decade II
13 = numerical output 0 of ID 10-II
14 = numerical output 1 of ID 10-II
15 = numerical output 2 of ID 10-II
16 = numerical output 5 of ID 10-II
17 = numerical output 4 of ID 10-II
18 = output $\overline{Q}$ of flip-flop D'
19 = numerical output 8 of ID 10-II
20 = output Q of flip-flop C'
21 = common negative supply − 12 V
22 = common positive supply +12 V
23 = common supply 0 V

1a = trigger input T of flip-flop A
2a = additional trigger input T of flip-flop A
3a = output $\overline{Q}$ of flip-flop A
4a = numerical output 9 of ID 10-I
5a = numerical output 8 of ID 10-I
6a = numerical output 6 of ID 10-I
7a = numerical output 4 of ID 10-I
8a = numerical output 5 of ID 10-I
9a = numerical output 2 of ID 10-I
10a = numerical output 1 of ID 10-I
11a = numerical output 0 of ID 10-I
12a = extension gate input EG of flip-flop A
13a = numerical output 3 of ID 10-II
14a = output $\overline{Q}$ of flip-flop C'
15a = output Q of flip-flop B'
16a = output $\overline{Q}$ of flip-flop B'
17a = numerical output 7 of ID 10-II
18a = numerical output 6 of ID 10-II
19a = output Q of flip-flop D'
20a = numerical output 9 of ID 10-II
21a = output $\overline{Q}$ of flip-flop A'
22a = output Q of flip-flop A'
23a = trigger input T of flip-flop A'

Power supply

Terminal 21: $V_N = -12\ V \pm 5\%$, $-I_N = 8\ mA$
22: $V_P = +12\ V \pm 5\%$, $I_P = 60\ mA$
23: $V_E = 0\ V$ common

} The current values are nominal

INPUT REQUIREMENTS (at V_P = 11.4 V and V_N = −12.6 V unless specified differently)

Set/reset input (S-terminals)

The flip-flops of the decades I and II are reset simultaneously at the terminals 1 and 12 respectively, when a "positive low" voltage (between 0 V and 0.3 V) is applied to the corresponding S-terminal.

Required direct current	$-I_{SD}$	= min.	7.8	mA	
Required transient charge when V_S changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{ST}$	= max.	11.2	nC	

When the decade is not reset, the voltage V_S must be kept between max. V_P and min. 2/3 V_P.

Time data

Pulse duration	t_p	= min.	8	μs	See point 4*
Recovery time	t_{rec}	= min.	15	μs	See point 4*
Time delay between S- and T-signal	t_{st}	= min.	15	μs	See point 5*

Extension gate input (EG-terminals)

A d.c. voltage level can be applied to the EG-terminals 12a and 11 via diodes type OA 95. A "positive low" voltage closes the gate, whilst a "positive high" voltage (between 2/3 V_P and V_P) opens the gate.

Gate open

Voltage	V_G	= min.	2/3	V_P	
		= max.		V_P	

Gate closed

Voltage	V_G	= min.	0	V	
		= max.	0.3	V	
Required direct current	$-I_{GD}$	= max.	1.1	mA	
Required transient charge when V_G changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{GT}$	= max.	1.2	nC	

Time data

Trigger gate setting time	t_{gs}	= min.	29	μs	See point 6*
Trigger gate inhibiting time	t_{gi}	= min.	29	μs	See point 7*

* Section "Time definitions" of "Circuit blocks 10-Series".

Trigger input (T-terminals)

A negative-going voltage step or trigger pulse is applied to the interconnected trigger inputs T of flip-flops A and A' (terminals 23a and 1a respectively). Decade counter I can be provided with a second trigger input (terminal 2a). Two diodes BAY 38 have to be mounted on the printed-wiring board.
Each trigger pulse applied to the terminal T switches the decade counter, provided that the G-inputs (EG-inputs via diode) are left floating or at min. 2/3 V_P (gate open).

		Gate open	Gate closed
	V_G	= min. 2/3 V_P	= min. 0 V
		= max. V_P	= max. 0.3 V
Required direct current when V_T = max. 0.3 V	$-I_{TD}$	= max. 1.1 mA	= 0 mA
Required transient charge when V_T changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{TT}$	= max. 3.4 nC	= 0 nC
Time data			
Fall time	t_f	= max. 1.5 μs	See point 3 *
Pulse duration	t_p	= min. 2 μs	
Trigger gate setting time	t_{gs}	= min. 29 μs	

OUTPUT DATA (at V_P = 11.4 V and V_N = −12.6 V, unless specified differently)

Decade counter section

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board, including the numerical indicator tube driver ID 10, the Q-outputs of each flip-flop in the decade counter may furthermore be loaded as specified in the following table.

The loadability of the flip-flop outputs can be increased by connecting an external resistor in parallel with the built-in collector resistor of the corresponding output. This resistor has to be connected between the output terminal and V_P. For each additional driven input, a parallel resistor of 51 k$\Omega \pm 5\%$ is required. The total number of driven inputs is also specified in the following table.

Wiring capacitance at each Q-output max. 175 pF

* Section "Time definitions" of "Circuit blocks 10-series".

flip-flop		FF 12-A(A')		FF 12-B(B')		FF 12-C(C')		FF 12-D(D')	
output terminal		$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
		3a(21a)	2(22a)	7(16a)	8(15a)	9(14a)	3(20)	5(18)	4(19a)
max. number of 10-series circuit blocks, that may be driven, provided each driven input represents a load of $-I_D$ = max. 1.1 mA and $-Q_T$ = max. 3.4 nC	T_{amb} = min. 0 °C	5	2	3	5	3	3	2	5
	T_{amb} = min. −25 °C	5	2	3	3	3	3	2	5
max. number of driven 10-series circuit blocks, with external parallel collector resistor(s)	T_{amb} = min. 0 °C	6	5	5	5	5	4	4	6
	T_{amb} = min. −25 °C	5	3	4	3	4	3	3	5

Output levels during counting

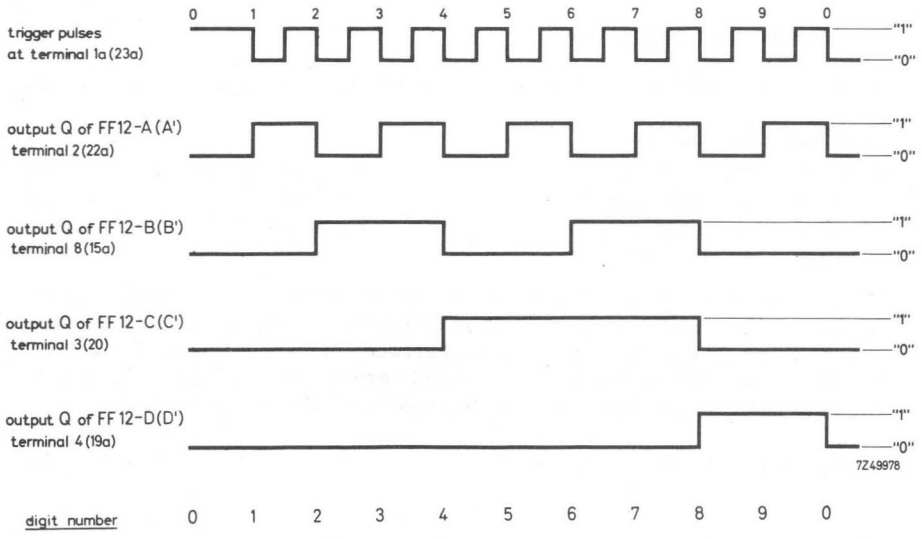


Fig. 3

The output levels at the Q-outputs of each flip-flop are shown in figure 3.
Note that, when a Q-output is at "positive low" ("0") level the corresponding $\overline{Q}$-output is at "positive high" ("1") level and vice versa.
After 10 negative-going pulses at the trigger input terminal 1a (23a) the output Q of flip-flop D (D') delivers the negative-going carry pulse for the next decade, while the decade counter has resumed its initial position, namely all Q-output terminals being at "positive low" level.
The relation between a digit number (output ID 10) and the corresponding state of each flip-flop is shown in figure 3 as well.

Numerical indicator tube driver section

The outputs Q_0 (terminals 11a and 13) up to and including Q_9 (terminals 4a and 20a) of the ID 10-I and ID 10-II respectively have to be connected to the pins k_0 up to and including k_9 of the corresponding numerical indicator tube ZM 1000, ZM 1020 or ZM 1080. The anode of these tubes has to be connected via a resistor (R_a) to the high voltage power supply (V_b).
The current available at these ten numerical outputs of the ID 10 can cope with the required cathode current I_k of the indicator tubes ZM 1000, ZM 1020 and ZM 1080, when the following conditions are observed:
- operating-temperature range
- power supply V_b for ZM 1000, ZM 1020 and ZM 1080
- anode series resistor R_a.

In the following graphs these data are specified.

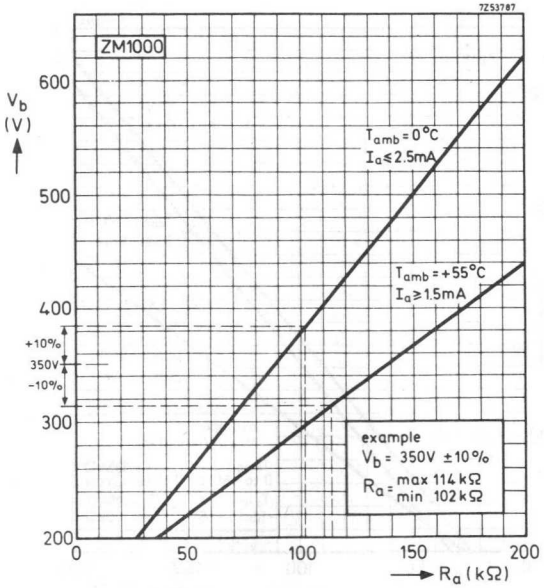


Fig.4

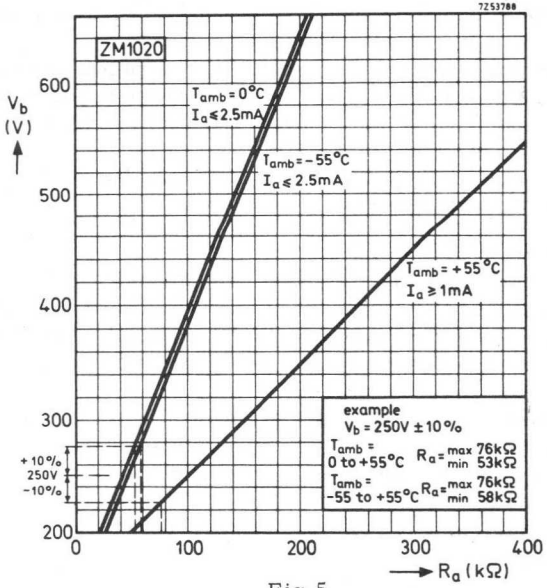


Fig.5

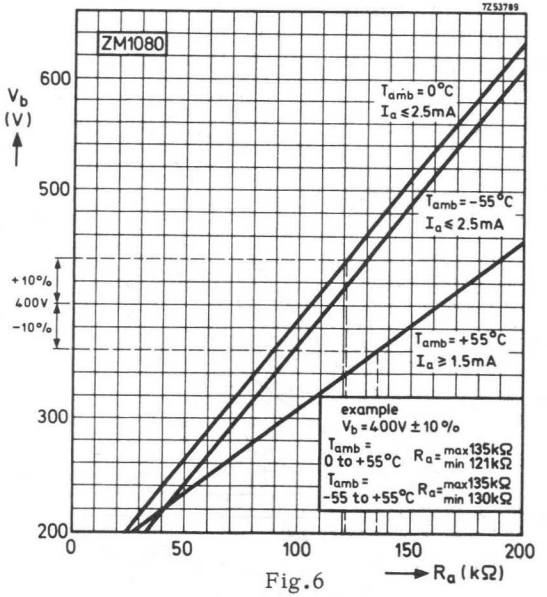


Fig.6

Wiring capacitance at each Q-output of the ID 10 max. 500 pF

DUAL DECADE COUNTER 2.DCA 11 B

CIRCUIT DATA

For circuit diagram see next pages.

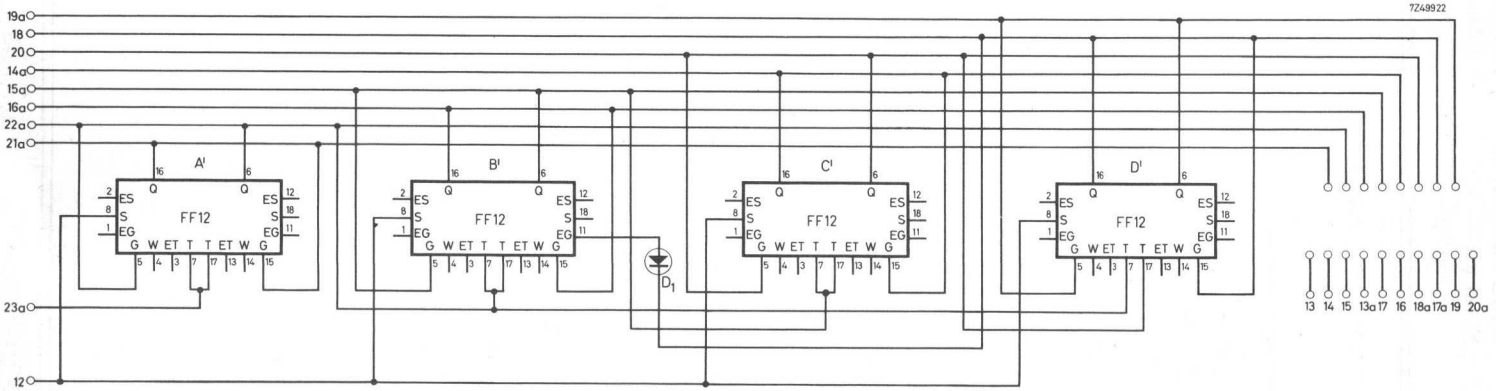


Fig.7a. 2.DCA 11 B

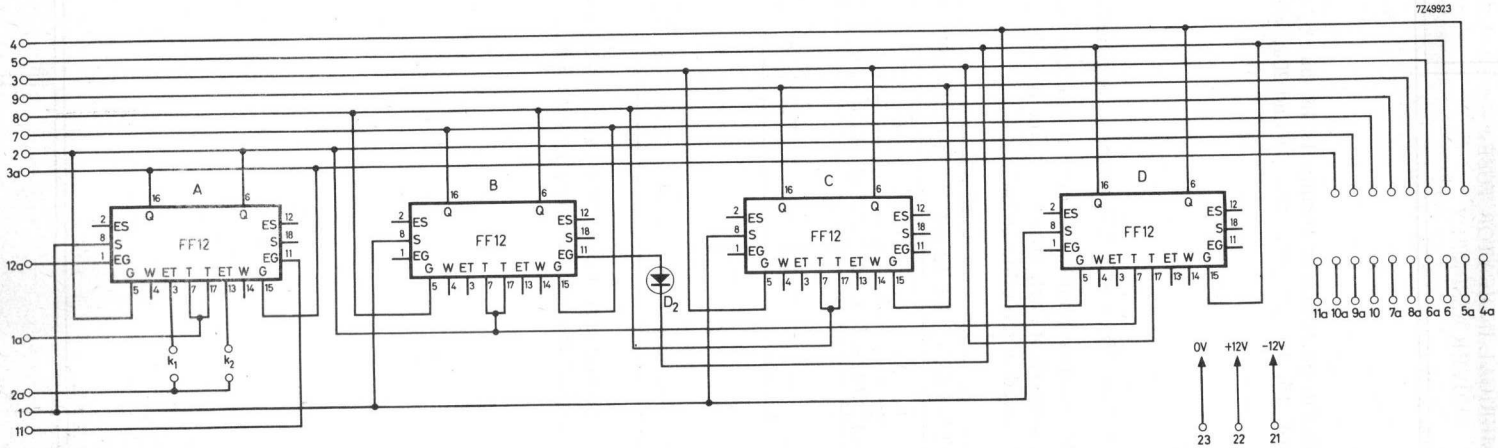


Fig.7b. 2.DCA 11 B

Terminals (Fig.8)

Similar to 2.DCA 11 A, with the exception of terminals 4a, 5a, 6, 6a, 7a, 8a, 9a, 10, 10a, 11a, 13, 13a, 14, 15, 16, 17, 17a, 18a, 19 and 20a, which are inoperative.

INPUT REQUIREMENTS

Similar to 2.DCA 11 A.

OUTPUT DATA (at V_P = 11.4 V and V_N = −12.6 V, unless specified differently)

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board, the Q-outputs of each flip-flop in the decade counter may furthermore be loaded as specified in the table below.

flip-flop	FF 12-A (A')		FF 12-B (B')		FF 12-C (C')		FF 12-D (D')	
output terminal	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
	3a(21a)	2(22a)	7(16a)	8(15a)	9(14a)	3(20)	5(18)	4(19a)
available direct current: min. I_{QD} in mA	7.1	6	7.1	6	7.1	6	6	7.1
available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 μs: min. Q_{QT} in nC	25.8	22.4	25.8	22.4	25.8	22.4	25.8	25.8

For T_{amb} = min. −25 °C the available direct current I_{QD} has to be reduced with 1.6 mA and similarly the available transient charge Q_{QT} with 5 nC.

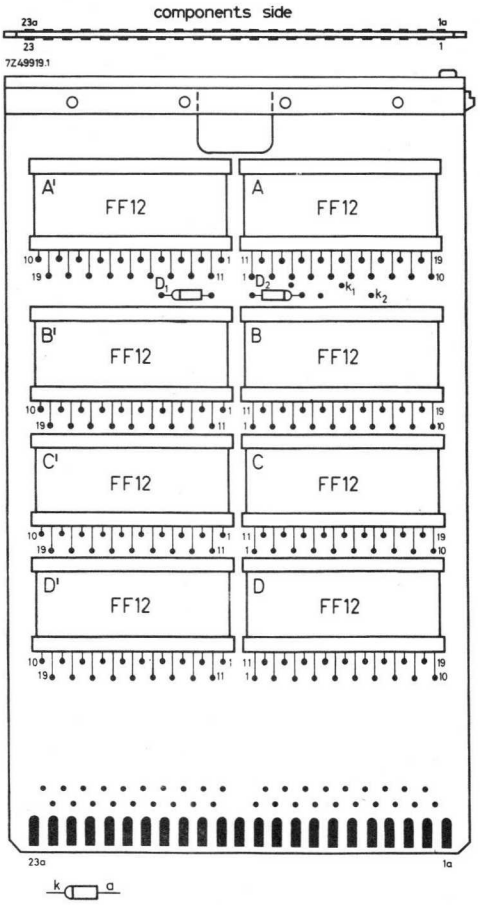
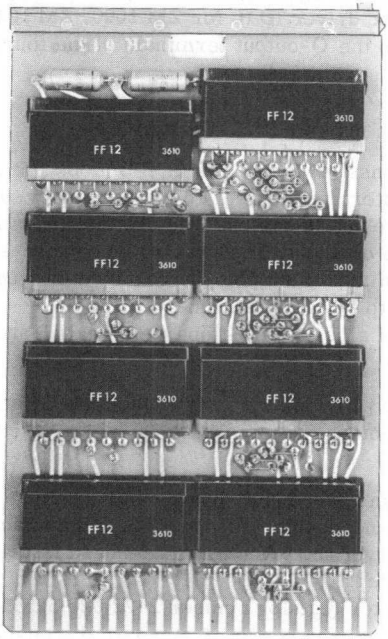


Fig.8. 2.DCA 11 B

DUAL DECADE COUNTER ASSEMBLY



RZ 22603-10

This assembly consists of eight circuit blocks FF 12 mounted on a printed-wiring board. It is available in three versions.

- 2. DCA 12 A, catalog number 2722 009 02071

  This assembly contains eight flip-flops FF 12, intended to be used as a dual decade counter, operating in the 1 - 2 - 4 - 8 code.
  The circuit diagram and the required interconnections made on the printed-wiring board are shown in Figs. 1 and 2.

- 2. DCA 12 B, catalog number 2722 009 02081.

  This assembly contains four flip-flops FF12, intended for use as a decade counter operating in the 1 - 2 - 4 - 8 code, and four flip-flops FF 12 intended for use as a buffer memory.
  The circuit diagram and the required interconnections made on the printed-wiring board are shown in Figs. 4 and 5.

The contents of the decade counter can be stored in the buffer memory by means of one trigger pulse on the common trigger line of the buffer memory section (terminal 4).
When the contents of the buffer memory has to be numerically indicated the numerical indicator tube driver ID 10 for ZM 1000, ZM 1020 and ZM 1080 can be connected directly to the Q-output terminals of the four flip-flops forming the buffer memory.

- 2. DCA 12 C, catalog number 2722 009 02091.

This assembly contains two chains of four flip-flops FF 12, intended to be used either as binary counters, scalers of 16 or as a binary scaler of 256, the latter when both chains are put in series. The circuit diagram and the required interconnections made on the printed-wiring board are shown in Figs.6 and 7.
To obtain a scaler of maximum 256 the required interconnection between terminal 9a and 19 has to be made externally.
For reset purposes of all eight flip-flops, terminals 3 and 20 have to be interconnected externally.

All these versions are provided with the capacitors C_1 and C_2, which filter the supply voltages from noise. These capacitors are mounted on the printed-wiring board.

The bare printed-wiring board (catalog number 4322 026 38720), provided with plated-through holes and double-sided gold plated contacts, is made of glass-epoxy material. Moreover the printed-wiring board is delivered with an extractor and a locking device.
With the mating connector (catalog number 2422 020 52591), not supplied with the assembly, the printed-wiring board of standard dimensions (121.8 mm x 207.0 mm x 1.6 mm) can be used directly in the standard mounting chassis (catalog number 4322 026 38240).

The circuit blocks are secured to the printed-wiring board by means of locking caps (catalog number 4322 026 32150).

Counting rate	max. 30 kHz
Ambient-temperature range	
operating	−25 to +55 °C below 0 °C: derated output data
storage	−55 to +75 °C
Weight	approx. 450 g

The data specified below apply to the 2.DCA 12 A in particular.
For the sake of simplicity for the versions 2.DCA 12 B and 2.DCA 12 C only data are specified separately, which differ from those of the 2.DCA 12 A.

DUAL DECADE COUNTER 2.DCA 12 A

CIRCUIT DATA

For circuit diagram see next pages.

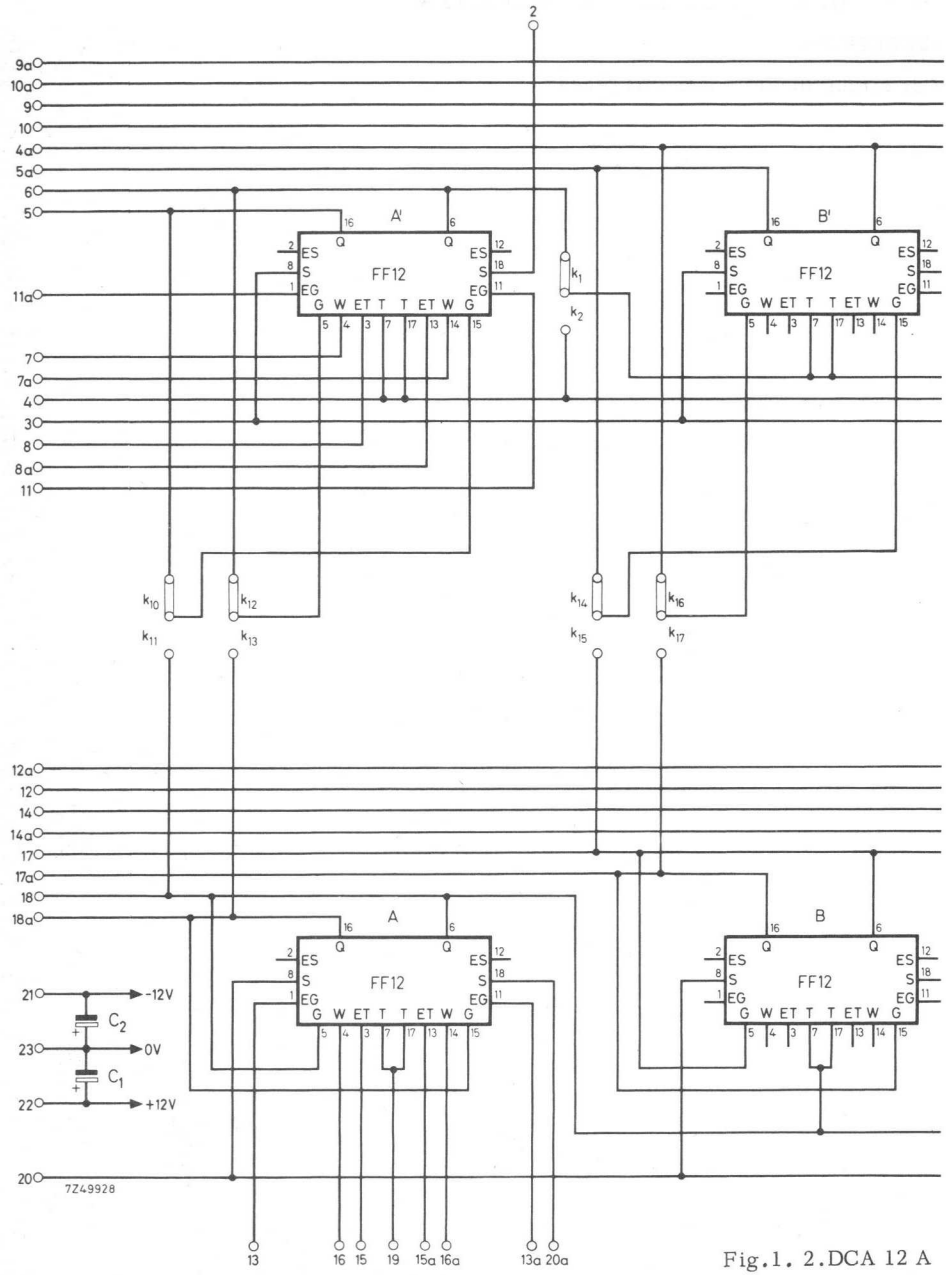


Fig.1. 2.DCA 12 A

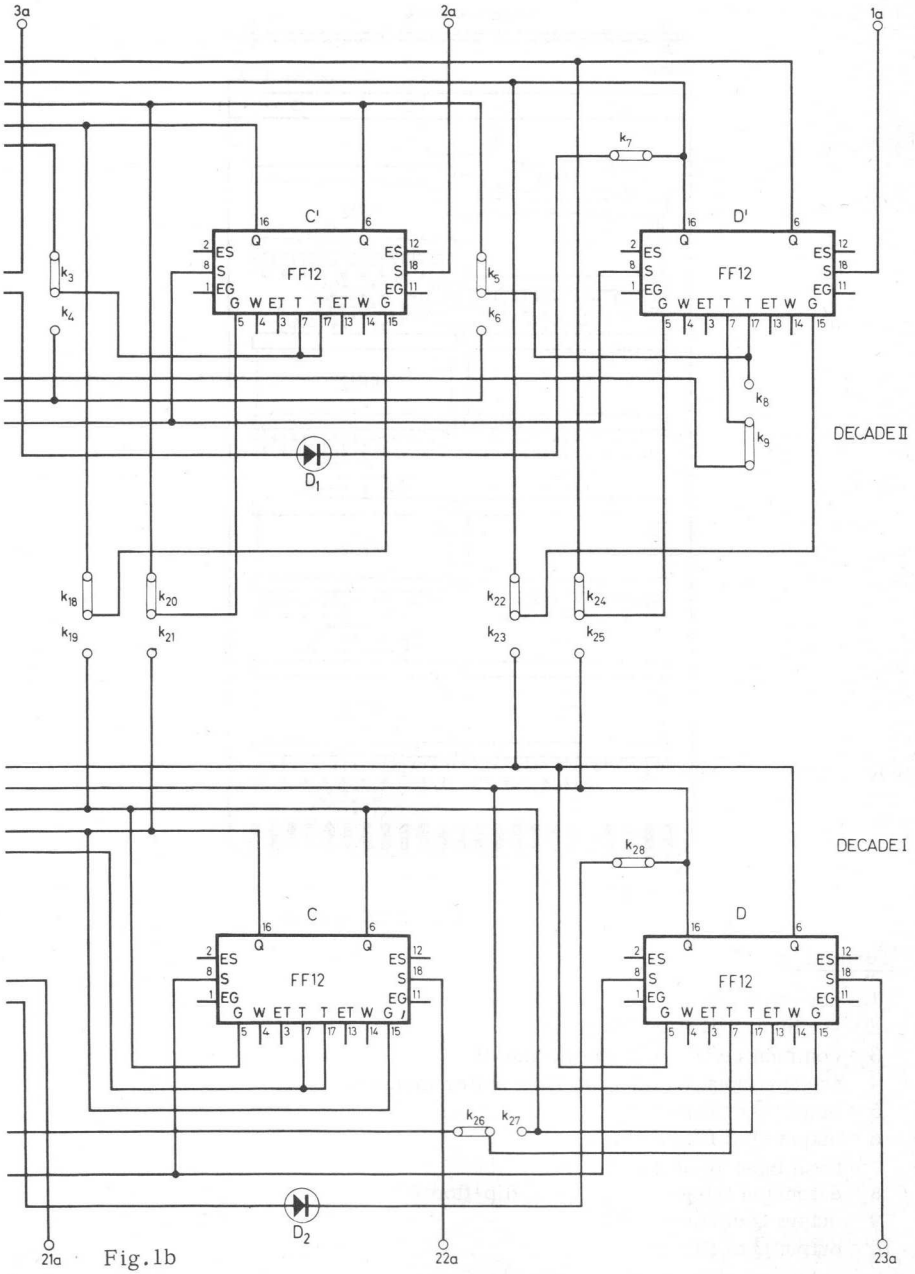

3a
2a
1a
C'
D'
C
D
FF12
ES
S
EG
Q
G W ET T T ET W G
k3
k4
k5
k6
k7
k8
k9
k18
k19
k20
k21
k22
k23
k24
k25
k26
k27
k28
D1
D2
DECADE II
DECADE I
21a
22a
23a

Fig.1b

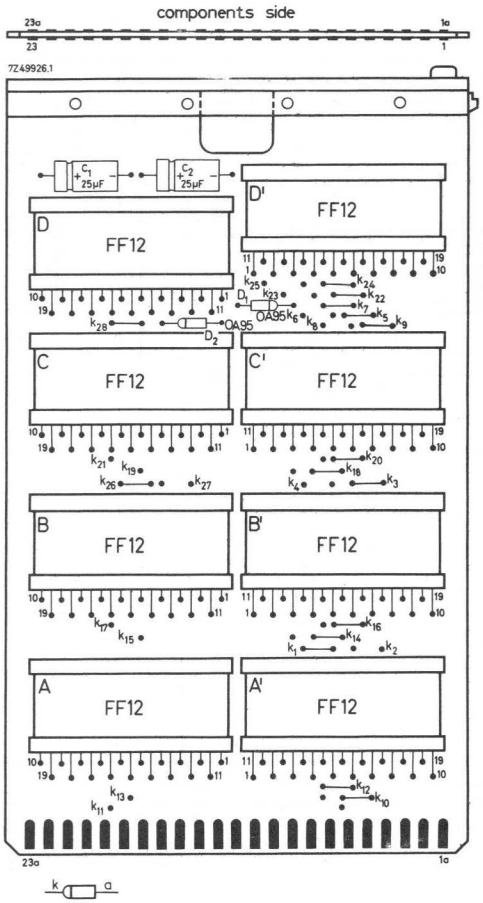


Fig.2. 2.DCA 12 A

Terminals

1 = not connected
2 = set input S of flip-flop A'
3 = common reset input S of decade II
4 = trigger input T of decade II or buffer memory
5 = output $\overline{Q}$ of flip-flop A'
6 = output Q of flip-flop A'
7 = base input W of flip-flop A'
8 = extension trigger input ET of flip-flop A'
9 = output Q of flip-flop C'
10 = output $\overline{Q}$ of flip-flop C'

11 = extension gate input EG of flip-flop A'
12 = output $\overline{Q}$ of flip-flop D
13 = extension gate input EG of flip-flop A
14 = output Q of flip-flop C
15 = extension trigger input ET of flip-flop A
16 = base input W of flip-flop A
17 = output Q of flip-flop B
18 = output Q of flip-flop A
19 = trigger input T of decade counter I
20 = common reset input S of decade counter I
21 = common negative supply −12 V
22 = common positive supply +12 V
23 = common supply 0 V

1a = set input S of flip-flop D'
2a = set input S of flip-flop C'
3a = set input S of flip-flop B'
4a = output Q of flip-flop B'
5a = output $\overline{Q}$ of flip-flop B'
6a = not connected
7a = base input W of flip-flop A'
8a = extension trigger input ET of flip-flop A'
9a = output Q of flip-flop D'
10a = output $\overline{Q}$ of flip-flop D'
11a = extension gate input EG of flip-flop A'
12a = output Q of flip-flop D
13a = extension gate input EG of flip-flop A
14a = output $\overline{Q}$ of flip-flop C
15a = extension trigger input ET of flip-flop A
16a = base input W of flip-flop A
17a = output $\overline{Q}$ of flip-flop B
18a = output $\overline{Q}$ of flip-flop A
19a = not connected
20a = set input S of flip-flop A
21a = set input S of flip-flop B
22a = set input S of flip-flop C
23a = set input S of flip-flop D

Power supply

Terminal 21 : V_N = −12 V ± 5 %, $-I_N$ = 8.5 mA
22 : V_P = +12 V ± 5 %, I_P = 60 mA
23 : V_E = 0 V common

} The current values are nominal

INPUT REQUIREMENTS (at V_P = 11.4 V and V_N = −12.6 V unless specified differently)

Set/reset inputs (S-terminals)

For reset- or preset purposes a "positive low" voltage V_S is required between 0 V and 0.3 V, otherwise this voltage must be kept between V_P and 2/3 V_P.

Common reset (terminals 3 and 20)

With one pulse at terminals 3 or 20 all flip-flops in the decade will be reset simultaneously.

Required direct current	$-I_{SD}$	= min. 7.8	mA	
Required transient charge when V_S changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{ST}$	= min. 11.2	nC	
Time data				
Pulse duration	t_p	= min. 8	μs	See point 4*
Recovery time	t_{rec}	= min. 15	μs	
Time delay between S- and T-signal	t_{st}	= min. 15	μs	See point 5*

Individual flip-flop preset (terminals 2, 3a, 2a, 1a and 20a, 21a, 22a, 23a)

For this purpose one S-input of each flip-flop in the decade has been brought out.

Required direct current	$-I_{SD}$	= max. 1.95	mA	
Required transient charge when V_S changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{ST}$	= max. 2.8	nC	

Extension gate input (EG-terminals)

A d.c. voltage level can be applied to the EG-terminals 13a and 13 of flip-flop FF 12-A and 11 and 11a of flip-flop FF 12-A', via a diode type OA 95.
A "positive low" voltage closes the gate, whilst a "positive high" voltage (between 2/3 V_P and V_P) opens the gate.

Gate open			
Voltage	V_G	= min. 2/3	V_P
		= max.	V_P

* Section "Time definitions" of "Circuit blocks 10-Series".

Gate closed

Voltage	V_G	= min. 0 V max. 0.3 V		
Required direct current	$-I_{GD}$	= max. 1.1	mA	
Required transient charge when V_G changes from 2/3 V_p to 0.5 V in 1.5 μs	$-Q_{GT}$	= max. 1.2	nC	

Time data

Trigger gate setting time	t_{gs}	= min. 29	μs.	See point 6 *
Trigger gate inhibiting time	t_{gi}	= min. 29	μs.	See point 7 *

Trigger input (T-terminals 19 and 4)

A negative-going voltage step or trigger pulse is applied to the interconnected trigger inputs T of flip-flops A and A' (terminals 19 and 4 respectively). Each trigger pulse applied to the terminals T switches the decade counters, provided that the G-inputs (EG-inputs via diode) are left floating or at min. 2/3 V_P (gate open).

Required direct current when V_T = max. 0.3 V	$-I_{TD}$	= max. 1.1	mA	
Required transient charge when V_T changes from 2/3 V_p to 0.5 V in 1.5 μs	$-Q_{TT}$	= max. 3.4	nC	

Time data

Fall time	t_f	= max. 1.5	μs	See point 3 *
Pulse duration	t_p	= min. 2	μs	
Trigger gate setting time	t_{gs}	= min. 29	μs	

Base inputs (W-terminals)

Capacitance (wiring plus output of TG 13, TG 14 or TG 15) max. 95 pF

Note

The output capacitance of the trigger gates TG 13, TG 14 and TG 15 is max. 5 pF.

* Section "Time definitions" of "Circuit blocks 10-Series".

OUTPUT DATA (at V_P = 11.4 V and V_N = −12.6 V, unless specified differently)

In excess of the internal load, represented by the circuit blocks on the printed-wiring board, the Q-outputs of each flip-flop in the decade counters may furthermore be loaded as specified in the table below.

flip-flop	FF 12-A (A')		FF 12-B (B')		FF 12-C (C')		FF 12-D (D')	
output terminal	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
	18a (5)	18 (6)	17a (5a)	17 (4a)	14a (10)	14 (9)	12 (10a)	12a (9a)
available direct current: min. I_{QD} in mA	7.1	6	7.1	6	7.1	6	6	7.1
available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 μs: min. Q_{QT} in nC	25.8	22.4	25.8	22.4	25.8	22.4	25.8	25.8

For T_{amb} = min. −25 °C the available direct current I_{QD} has to be reduced with 1.6 mA and similarly the available transient charge Q_{QT} with 5 nC.

Wiring capacitance at each Q-output max. 175 pF

Output levels during counting

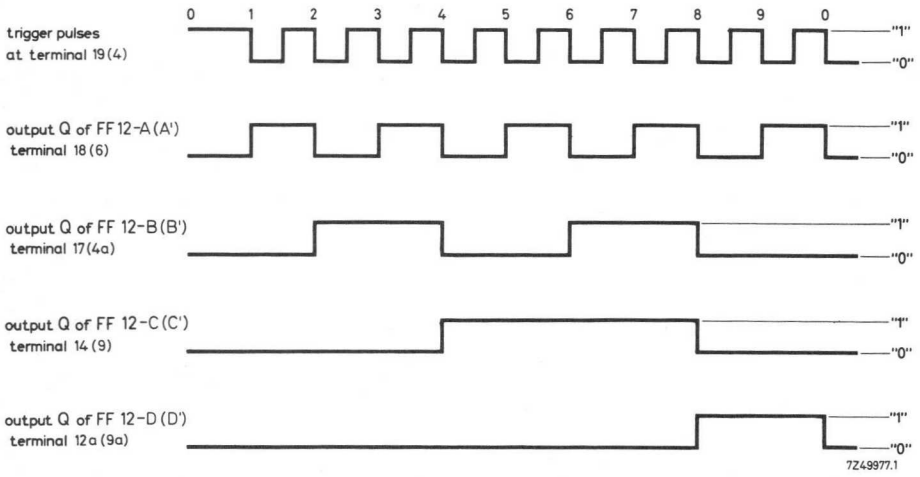


Fig.3

DECADE COUNTER AND BUFFER MEMORY 2.DCA 12B

For circuit diagram
see next page

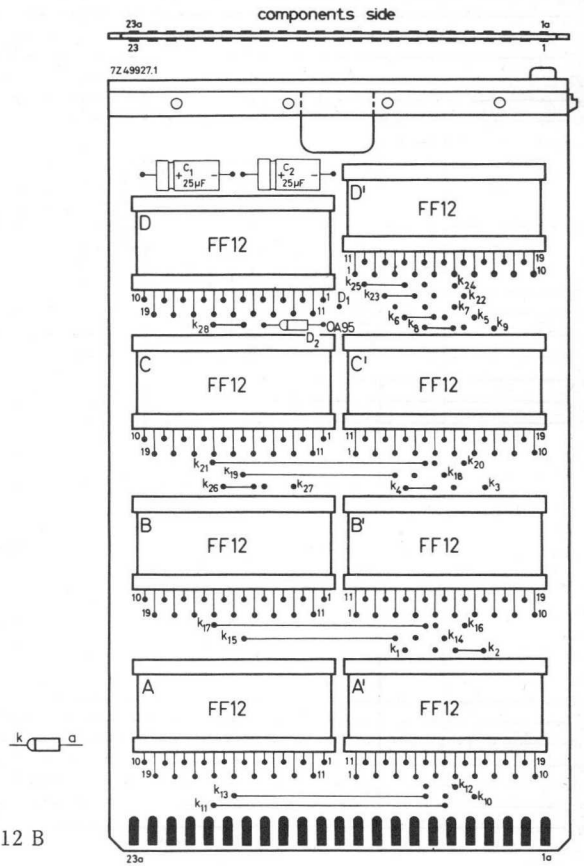


Fig.5. 2.DCA 12 B

INPUT REQUIREMENTS (at V_P = 11.4 V and V_N = -12.6 V unless specified differently)

Set/reset input (S-terminals)

Common reset decade counter (terminal 20)

With one pulse at terminal 20 all flip-flops in the decade will be reset simultaneously. For further data, see 2.DCA 12 A.

Common reset buffer memory (terminal 3)

With one pulse at terminal 3 all flip-flops in the buffer memory will be reset simultaneously.
Pulse duration t_p = min. 2 μs
For further set/reset data, see 2.DCA 12 A.

CIRCUIT DATA

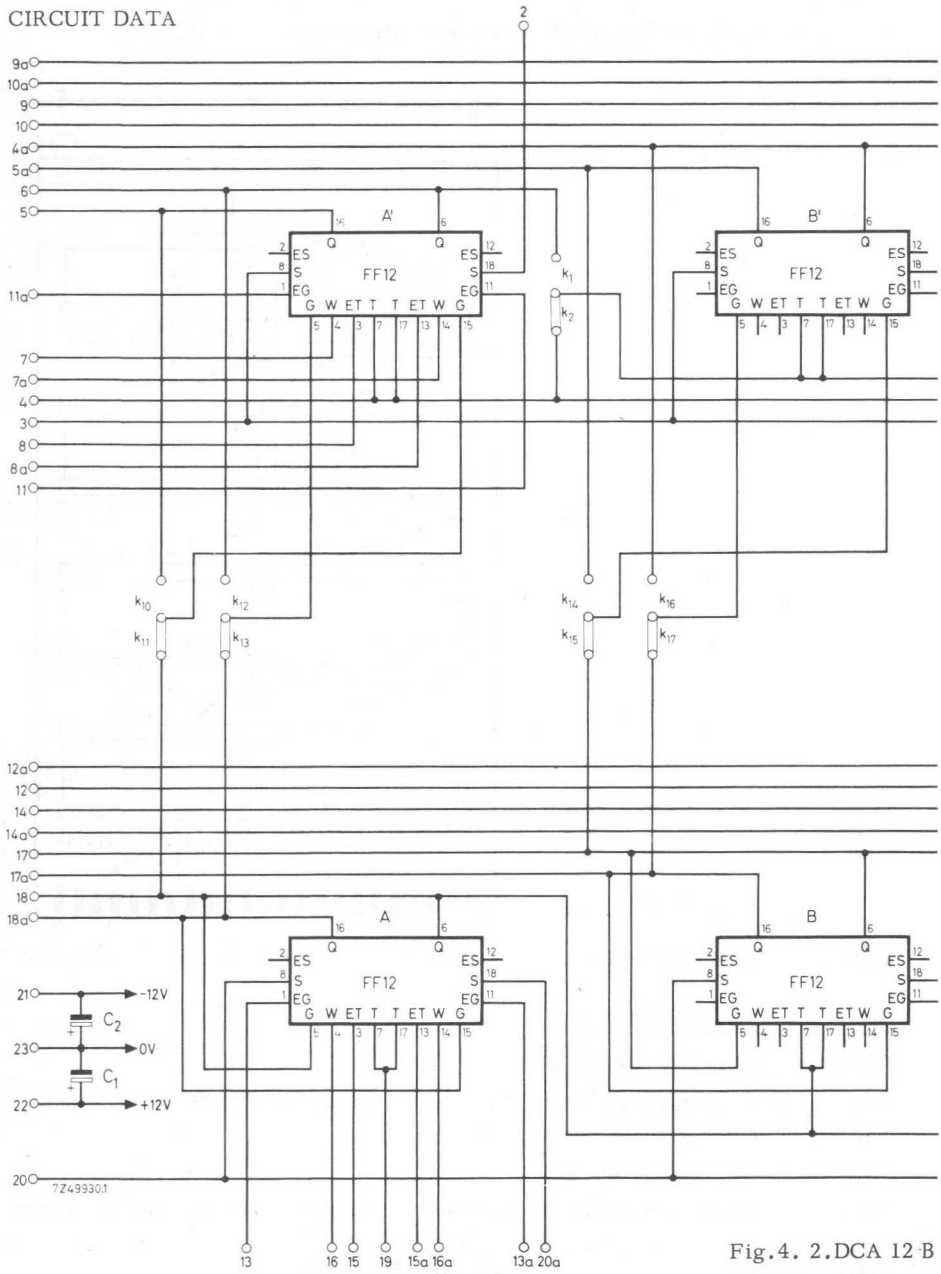
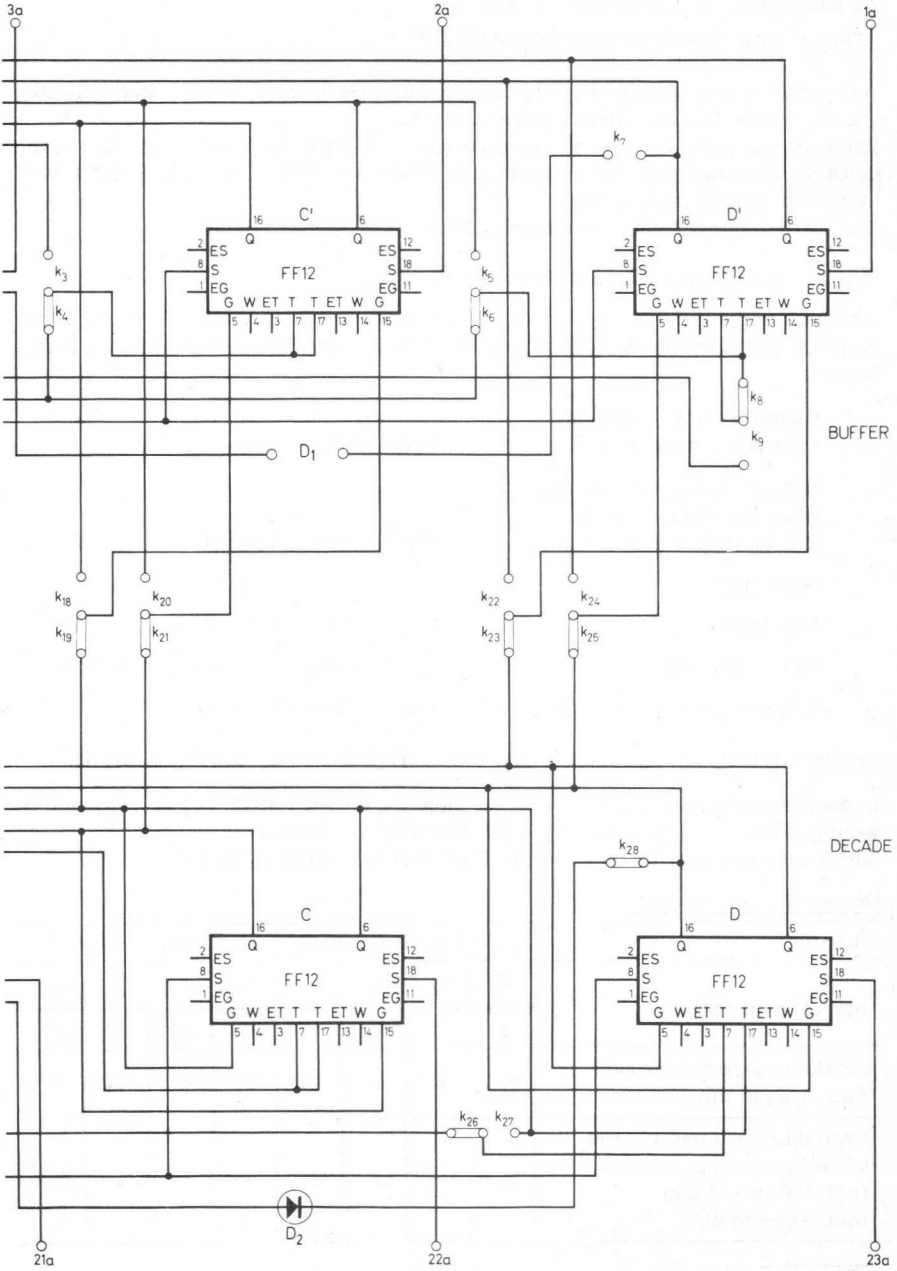


Fig.4. 2.DCA 12 B


3a
2a
1a
C'
D'
FF12
FF12
k3
k4
k5
k6
k7
k8
k9
BUFFER
D1
k18
k19
k20
k21
k22
k23
k24
k25
DECADE
k28
C
D
FF12
FF12
k26
k27
D2
21a
22a
23a

Trigger input (T-terminals 19 and 4)

Trigger input decade counter (terminal 19)

A negative-going voltage step or trigger pulse is applied to the interconnected trigger inputs T of flip-flop A (terminal 19).
Each trigger pulse applied to the terminal T of flip-flop A switches the decade counter, provided that the G-inputs (EG-inputs via diode) are left floating or at minimum 2/3 V_P (gate open).
For further trigger data, see 2.DCA 12 A.

Trigger input buffer memory (terminal 4)

With one trigger pulse applied to the interconnected terminals T of the buffer memory (terminal 4) the contents of the decade counter is shifted into the buffer memory.

Required direct current when V_T = max. 0.3 V	$-I_{TD}$ = max. 4.4 mA	
Required transient charge when V_T changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{TT}$ = max. 13.6 nC	
Time data		
Fall time	t_f = max. 1.5 μs	See point 3*
Pulse duration	t_p = min. 2 μs	
Trigger gate setting time	t_{gs} = min. 29 μs	

OUTPUT DATA (at V_P = 11.4 V and V_N = −12.6 V unless specified differently)

In excess of the internal load, represented by the circuit blocks on the printed-wiring board, the Q-outputs of each flip-flop in the decade counter and in the buffer memory may furthermore be loaded as specified in the tables below.

Decade counter section

flip-flop	FF 12-A		FF 12-B		FF 12-C		FF 12-D	
output terminal	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
	18a	18	17a	17	14a	14	12	12a
available direct current: min. I_{QD} in mA	6	4.9	6	4.9	6	4.9	4.9	6
available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 μs: min. Q_{QT} in nC	24.6	21.2	24.6	21.2	24.6	21.2	24.6	24.6

* Section "Time definitions" of "Circuit blocks 10 series".

Buffer memory section

flip-flop	FF 12-A'		FF 12-B'		FF 12-C'		FF 12-D'	
output terminal	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
	5	6	5a	4a	10	9	10a	9a
available direct current: min. I_{QD} in mA	8.2	8.2	8.2	8.2	8.2	8.2	8.2	8.2
available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 μs: min. Q_{QT} in nC	27	27	27	27	27	27	27	27

For T_{amb} = min. −25 °C the available direct current I_{QD} has to be reduced with 1.6 mA and similarly the available transient charge Q_{QT} with 5 nC.

Buffer memory loaded with the numerical indicator tube driver ID 10

When the buffer memory is loaded with the circuit block ID 10, the available output data of each flip-flop is specified separately in the table below.
The loadability of the flip-flop outputs can be increased by connecting an external resistor in parallel with the built-in collector resistor of the corresponding output. This resistor has to be connected between the output terminal and V_P. For each additional driven input, a parallel resistor of 51 kΩ ± 5 % is required. The total number of driven inputs is also specified in the table below.

flip-flop		FF 12-A'		FF 12-B'		FF 12-C'		FF 12-D'	
output terminal		$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
		5	6	5a	4a	10	9	10a	9a
max. number of 10-series circuit blocks, that may be driven, provided each driven input represents a load of $-I_D$ = max. 1.1 mA and $-Q_T$ = max. 3.4 nC	T_{amb} = min. 0 °C	6	6	4	6	4	4	4	6
	T_{amb} = min. −25 °C	6	6	4	5	4	4	4	6
max. number of driven 10-series circuit blocks, with external parallel collector resistor (s)	T_{amb} = min. 0 °C	7	7	6	6	6	6	6	7
	T_{amb} = min. −25 °C	6	6	5	5	5	5	5	6

BINARY COUNTER 2.DCA 12 C

CIRCUIT DATA

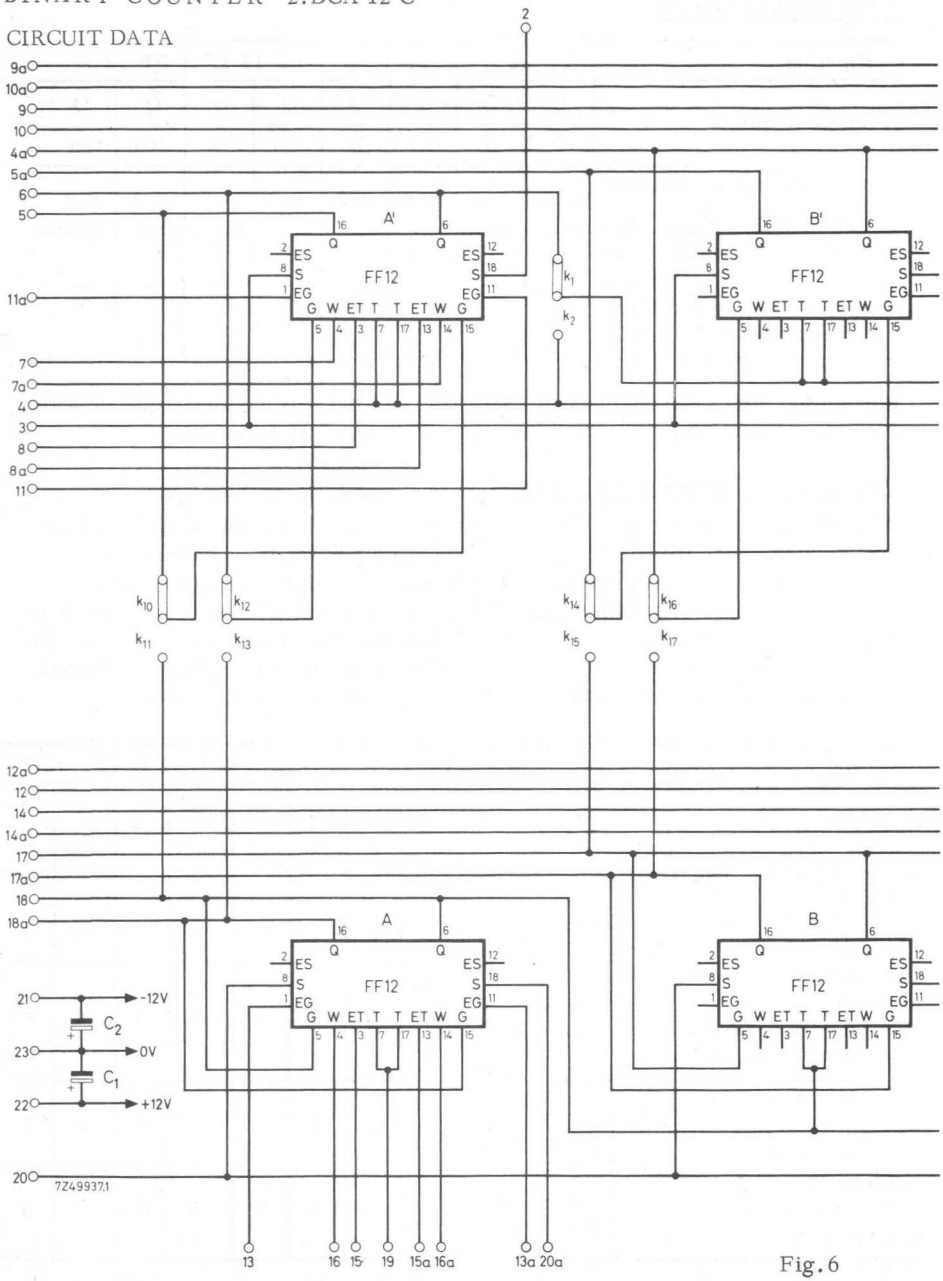
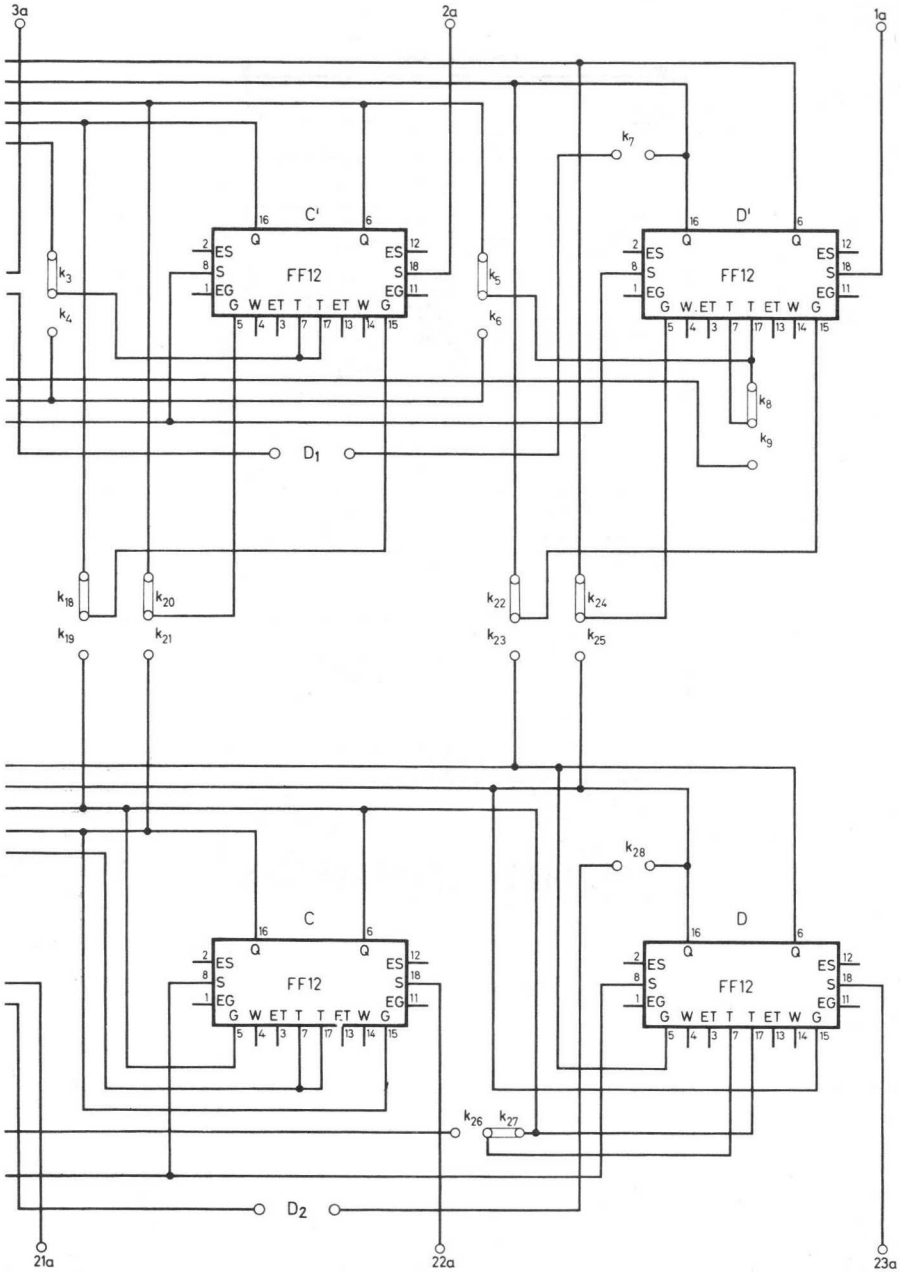


Fig. 6


3a
2a
1a
C'
D'
C
D
FF12
ES
S
EG
Q
G W ET T T ET W G
k3
k4
k5
k6
k7
k8
k9
D1
k18
k19
k20
k21
k22
k23
k24
k25
k26
k27
k28
D2
21a
22a
23a

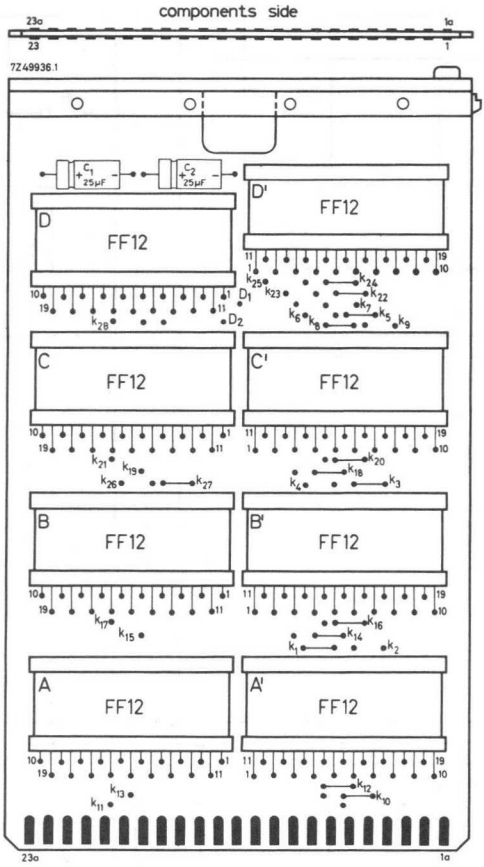


Fig.7. 2.DCA 12C

INPUT REQUIREMENTS

Similar to 2.DCA 12 A, with the exception of:

Common reset (terminals 3 and/or 20)

Pulse duration t_p = min. 2 μs per flip-flop

OUTPUT DATA (at V_P = 11.4 V and V_N = −12.6 V unless specified differently)

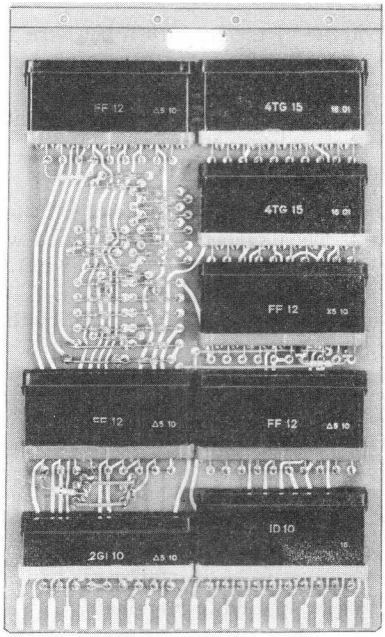
In excess of the internal load, represented by the circuit blocks on the printed-wiring board, the Q-outputs of each flip-flop in the binary counter (scaler of 16) may furthermore be loaded as specified in the table below.

flip-flop	FF 12-A (A')		FF 12-B (B')		FF 12-C (C')		FF 12-D (D')	
output terminal	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
	18a (5)	18 (6)	17a (5a)	17 (4a)	14a (10)	14 (9)	12 (10a)	12a (9a)
available direct current: min. I_{QD} in mA	7.1	6	7.1	6	7.1	6	7.1	7.1
available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 μs: min. Q_{QT} in nC	25.8	22.4	25.8	22.4	25.8	22.4	25.8	25.8

For T_{amb} = min. −25 °C the available direct current I_{QD} has to be reduced with 1.6 mA and similarly the available transient charge Q_{QT} with 5 nC.

When the flip-flops are connected to form a binary counter, scaler of 256, the available I_{QD} and Q_{QT} of output Q of FF 12-D (D') have to be decreased till 6 mA and 22.4 nC respectively.

REVERSIBLE DECADE COUNTER AND NUMERICAL INDICATOR TUBE DRIVER ASSEMBLY



RZ 22603-13

The assembly consists of four circuit blocks FF 12, two circuit blocks 4.TG 15, a circuit block 2.GI 10 and a circuit block ID 10, mounted on a printed-wiring board.
Versions without the 2.GI 10 and/or the ID 10 are also available.

- BCA 10 A, catalog number 2722 009 02101.

  This assembly contains four flip-flops FF 12, two quadruple trigger gates 4.TG 15 and a dual positive gate inverter amplifier 2.GI 10, interconnected as a reversible decade counter, operating in the 1-2-4-8 code for both forward and reverse counting. It contains also the numerical indicator tube driver ID 10 providing the BCD - to decimal decoding - and driving circuits for the numerical indicator tube ZM1000, ZM1020 or ZM1080. One half of the 2.GI 10 is inoperative in the BCA 10 A and can therefore be used for other purposes in the logic.
  The required interconnections are shown in Figs. 1 and 2.

- BCA 10 B, catalog number 2722 009 02111.

  This assembly is identical to the BCA 10 A but without the circuit block ID 10 mounted on the board. The lay-out of the printed-wiring board allows the mounting of the ID 10 separately (see Figs. 7 and 8).

- BCA 10 C, catalog number 2722 009 02121

  This assembly is identical to the BCA 10 A but here reverse counting is performed in the 1-2-4-2 (jump at 8) code. Therefore the circuit block 2.GI 10 is not mounted.
  The required interconnections are shown in Figs. 9 and 10.

- BCA 10 D, catalog number 2722 009 02131.

  This assembly is identical to the BCA 10 C but without the circuit block ID 10 mounted on the board. The lay-out of the printed-wiring board allows the mounting of the ID 10 separately (see Figs. 11 and 12).

In all versions the counting direction is determined by the voltage levels applied to terminals 18 and 19.
For forward counting holds:

- the positive level has to be applied to terminal 19,
- the "0" level has to be applied to terminal 18,
- the trigger pulse has to be applied to terminal 13.

For reverse counting holds:

- the positive level has to be applied to terminal 18,
- the "0" level has to be applied to terminal 19,
- the trigger pulse has to be applied to terminal 2a.

When two of these assemblies are operating in series the following interconnections have to be made.

For forward counting: terminal 5a of the first decade has to be connected to terminal 13 of the second decade.
For reverse counting: terminal 6a of the first decade has to be connected to terminal 2a of the second decade.

The bare printed-wiring board (catalog number 4322 026 38730), provided with plated-through holes and double-sided goldplated contacts, is made of glass-epoxy material. Moreover the printed-wiring board is delivered with an extractor and a locking device.
With the mating connector (catalog number 2422 020 52591), not supplied with the assembly, the printed-wiring board of standard dimensions (121.8 mm x 207.0 mm x 1.6 mm) can be used directly in the standard mounting chassis (catalog number 4322 026 38240).

The circuit blocks are secured to the printed-wiring board by means of locking caps (catalog number 4322 026 32150).

Counting rate	max. 30 kHz
Ambient-temperature range	
operating	−25 to +55 °C below 0 °C: derated output data
storage	−55 to +75 °C
Weight	approx. 400 g

The data specified below apply to the BCA 10 A in particular.
For the sake of simplicity for the other versions only data are specified separately, which differ from those of the BCA 10 A.

REVERSIBLE DECADE COUNTER AND NUMERICAL INDICATOR TUBE DRIVER BCA 10 A

CIRCUIT DATA

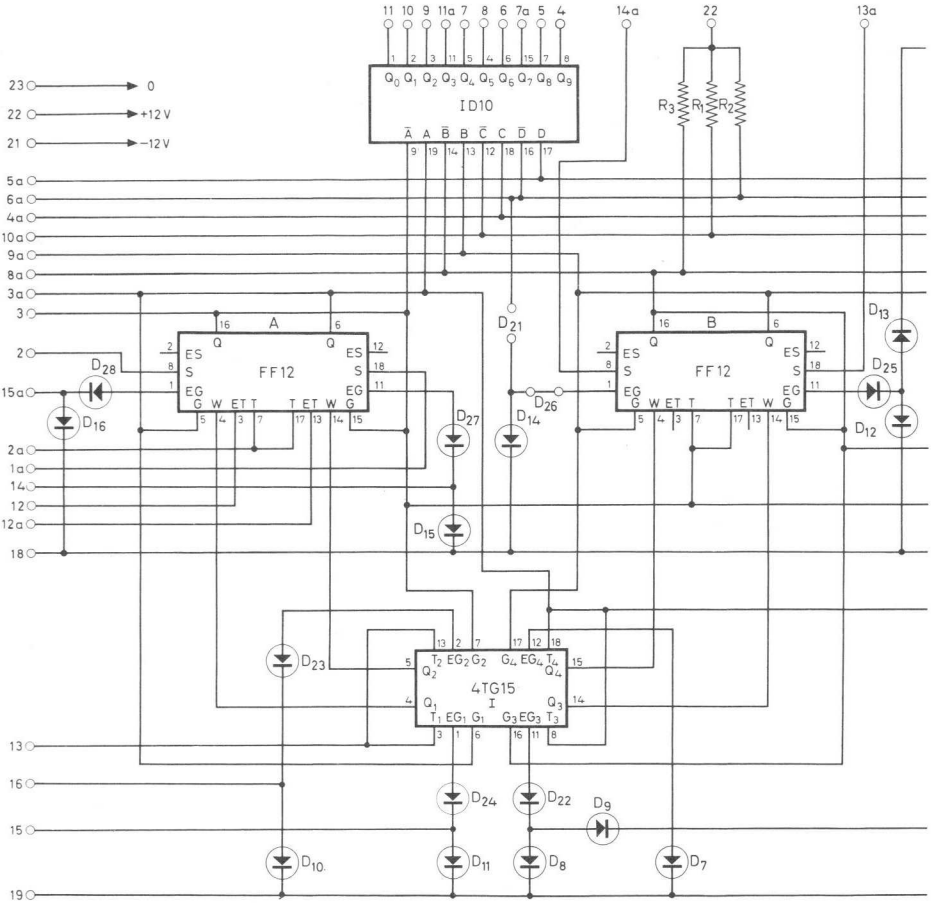
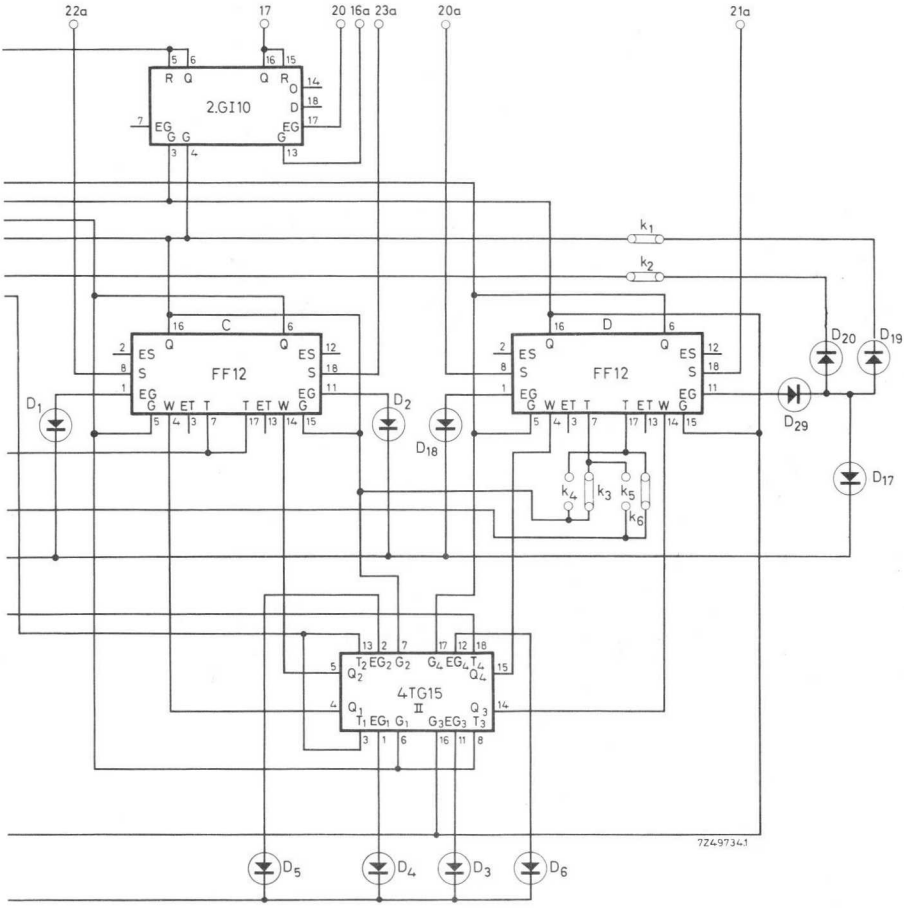


Fig.1


22a
17
20 16a 23a
20a
21a
2.GI10
FF12
FF12
4TG15
II
k1
k2
k3
k4
k5
k6
D1
D2
D5
D4
D3
D6
D18
D29
D17
D20
D19
7Z49734.1

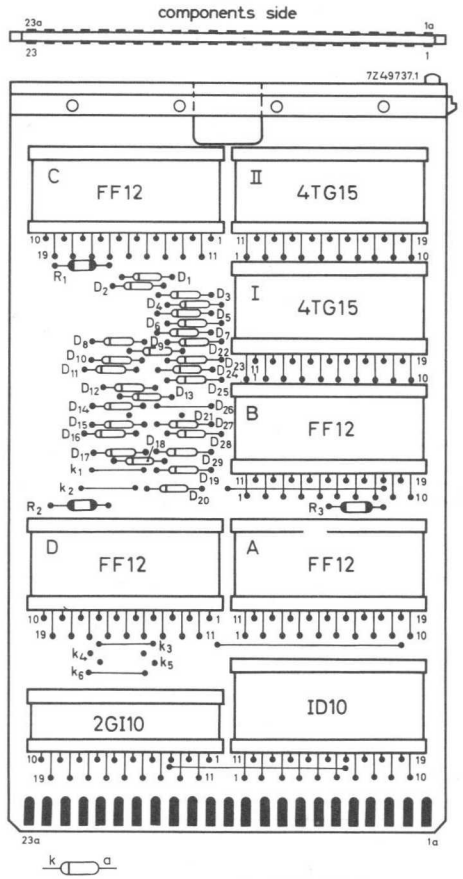


Fig.2. BCA 10 A

Terminals

1 = not connected
2 = set input S of flip-flop A
3 = output $\overline{Q}$ of flip-flop A
4 = numerical output 9 of ID 10
5 = numercial output 8 of ID 10
6 = numercial output 6 of ID 10
7 = numerical output 4 of ID 10
8 = numerical output 5 of ID 10
9 = numerical output 2 of ID 10
10 = numerical output 1 of ID 10

11 = numerical output 0 of ID 10
12 = extension trigger input ET of flip-flop A
13 = trigger input forward counting
14 = extension gate input EG of flip-flop A
15 = extension gate input EG of trigger gate 4.TG 15-I
16 = extension gate input EG of trigger gate 4.TG 15-I
17 = output Q of GI 10
18 = condition input for counting direction
19 = condition input for counting direction
20 = extension gate input EG of GI 10
21 = common negative supply −12 V
22 = common positive supply +12 V
23 = common supply 0 V

1a = set input S of flip-flop A
2a = trigger input reverse counting
3a = output Q of flip-flop A
4a = output Q of flip-flop C
5a = output Q of flip-flop D
6a = output $\overline{Q}$ of flip-flop D
7a = numerical output 7 of ID 10
8a = output $\overline{Q}$ of flip-flop B
9a = output Q of flip-flop B
10a = output $\overline{Q}$ of flip-flop C
11a = numerical output 3 of ID 10
12a = extension trigger input ET of flip-flop A
13a = set input S of flip-flop B
14a = set input S of flip-flop B
15a = extension gate input EG of flip-flop A
16a = gate input G of GI 10
17a = not connected
18a = not connected
19a = not connected
20a = set input S of flip-flop D
21a = set input S of flip-flop D
22a = set input S of flip-flop C
23a = set input S of flip-flop C

Power supply

Terminal 21 : V_N = −12 V ± 5 %, $-I_N$ = 6.5 mA
22 : V_P = +12 V ± 5 %, I_P = 36 mA
} The current values are nominal
23 : V_E = 0 V common

INPUT REQUIREMENTS (at V_P = 11.4 V and V_N = -12.6 V unless specified differently)

Set/reset input (S-terminals)

Each S-input of the four flip-flops is brought out separately. A "positive low" voltage (between 0 V and 0.3 V) drives the corresponding transistor into the non-conducting state.

Transistor conducting					
Voltage	V_S	= min.	2/3 V_P		
		= max.	V_P		
Transistor non-conducting					
Voltage	V_S	= min.	0	V	
		= max.	0.3	V	
Required direct current	$-I_{SD}$	= max.	1.95	mA	
Required transient charge when V_S changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{ST}$	= max.	2.8	nC	
When the four flip-flops are reset simultaneously					
Required direct current	$-I_{SD}$	= min.	7.8	mA	
Required transient charge when V_S changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{ST}$	= max.	11.2	nC	
Time data					
Pulse duration	t_p	= min.	8	μs	See point 4 *
Recovery time	t_{rec}	= min.	15	μs	See point 4 *
Time delay between S- and T-signal	t_{st}	= min.	15	μs	See point 5 *

Condition inputs for controlling counting direction (terminals 18 and 19)

For forward counting the "positive high" level is applied to terminal 19 and the "positive low" level to terminal 18.
For reverse counting the "positive low" level is applied to terminal 19 and the "positive high" level to terminal 18.
When both terminals 18 and 19 carry the "positive low" level, the unit is blocked for both directions of counting.

---

* Section "Time definitions" of "Circuit blocks 10-Series".

"Positive high" level

Voltage	V_C	= min. 2/3 V_P = max. V_P	

"Positive low" level

Voltage	V_C	= min. 0 V = max. 0.3 V	
Total required direct current	$-I_{CD}$	= max. 4.4	mA
Total required transient charge when V_C changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{CT}$	= max. 4.8	nC

Trigger input (terminals 13 and 2a)

For forward counting the trigger pulse has to be applied to terminal 13.
For reverse counting the trigger pulse has to be applied to terminal 2a.

		V_C "positive high"	V_C "positive low"
Required direct current when V_T = max. 0.3 V	$-I_{TD}$	= max. 1.1 mA	= 0 mA
Required transient charge when V_T changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{TT}$	= max. 3.4 nC	= 0 nC
Input noise level	V_n	= max. 1.2 V_{p-p}	

Time data

Fall time	t_f	= max. 1.5 μs	See point 3 *
Pulse duration	t_p	= min. 2 μs	
Trigger gate setting time	t_{gs}	= min. 29 μs	

OUTPUT DATA (at V_P = 11.4 V and V_N = −12.6 V, unless specified differently)

Decade counter section

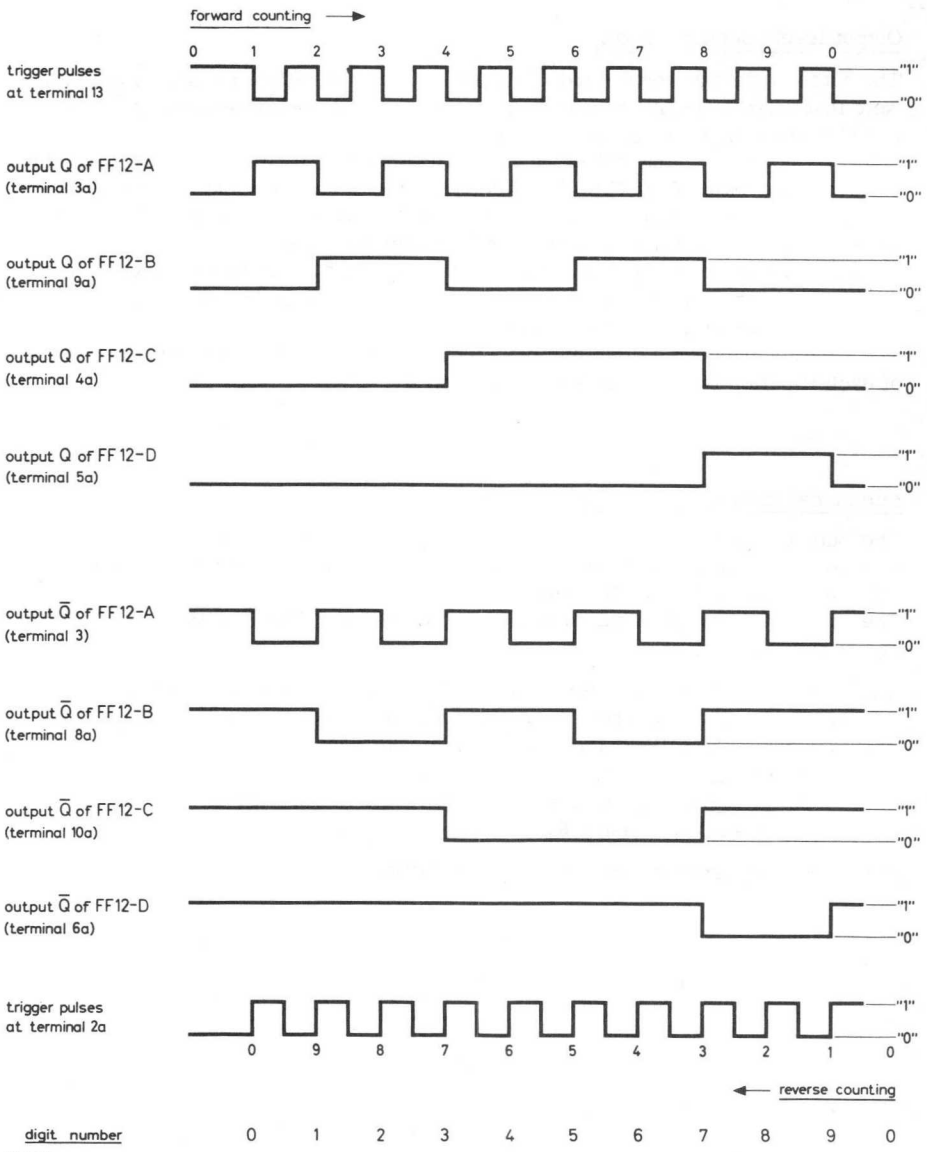
In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board including the numerical indicator tube driver ID 10, the Q-outputs of each flip-flop in the decade counter may furthermore be loaded as specified in the following table.

* Section "Time definitions" of "Circuit blocks 10-Series".

The loadability of the flip-flops FF 12-A, FF 12-C and FF 12-D can be increased by connecting an external resistor of 51 kΩ ±5% in parallel with the built-in collector resistor of the corresponding output, as specified in the table below. This resistor has to be connected between the output terminal and V_P.

flip-flop		FF 12-A		FF 12-B		FF 12-C		FF 12-D	
output terminal		$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
		3	3a	8a	9a	10a	4a	6a	5a
max. number of 10-series circuit blocks, that may be driven, provided each driven input represents a load of $-I_D$ = max. 1.1 mA and $-Q_T$ = max. 3.4 nC	T_{amb} = min. 0 °C	1	1	2	3	2	1	2	4
	T_{amb} = min. −25 °C	1	1	1	2	1	1	1	4
max. number of driven 10-series circuit blocks with external parallel collector resistor(s)	T_{amb} = min. 0 °C	3	3	2	3	2	3	2	5
	T_{amb} = min. −25 °C	2	2	1	2	1	2	1	4

Wiring capacitance at each Q-output max. 150 pF


forward counting
0 1 2 3 4 5 6 7 8 9 0
trigger pulses at terminal 13
output Q of FF12-A (terminal 3a)
output Q of FF12-B (terminal 9a)
output Q of FF12-C (terminal 4a)
output Q of FF12-D (terminal 5a)
output $\overline{Q}$ of FF12-A (terminal 3)
output $\overline{Q}$ of FF12-B (terminal 8a)
output $\overline{Q}$ of FF12-C (terminal 10a)
output $\overline{Q}$ of FF12-D (terminal 6a)
trigger pulses at terminal 2a
"1"
"0"
0 9 8 7 6 5 4 3 2 1 0
reverse counting
digit number
0 1 2 3 4 5 6 7 8 9 0
7249976

Output levels during counting

The output levels at the Q- and $\overline{Q}$-outputs of each flip-flop are shown in Fig.3. Note that when a Q-output is at "positive low" level the corresponding $\overline{Q}$-output is at "positive high" level and vice versa.
After 10 negative-going pulses at the trigger input terminal 13 for forward counting, the output Q of flip-flop D delivers the negative going carry pulse for the next decade, whilst the decade counter has resumed its initial position, namely all Q-output terminals being at "positive low" ("0") level.
When in this state of the counter a trigger pulse is applied to the trigger input terminal 2a, the output $\overline{Q}$ of flip-flop D delivers the negative going carry pulse to the next decade for reverse counting.
The relation between a digit number (output ID 10) and the corresponding state of each flip-flop is shown in the figure as well.

Numerical indicator tube driver section

The outputs Q_0 (terminal 11) up to and including Q_9 (terminal 4) of the ID 10 have to be connected to the pins k_0 up to and including k_9 of the numerical indicator tube ZM 1000, ZM 1020 and ZM 1080.
The anode of these tubes has to be connected via a resistor (R_a) to the high voltage power supply (V_b).

The current available at these 10 numerical outputs of the ID 10 can cope with the required cathode current I_k of the indicator tubes ZM 1000, ZM 1020 and ZM 1080, when the following conditions are observed:

- operating-temperature range
- power supply V_b for ZM 1000, ZM 1020 and ZM 1080
- anode series resistor R_a.

In the following graphs these data are specified.

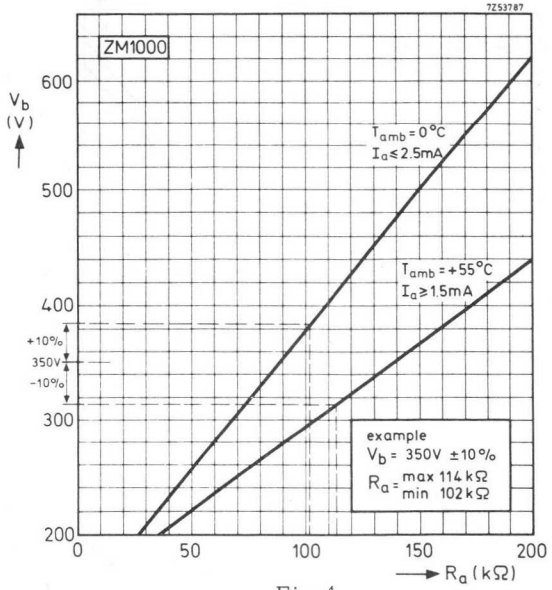

7Z53787
ZM1000
V_b (V)
600
500
400
300
200
+10%
350V
-10%
T_{amb} = 0°C
$I_a \leq$ 2.5mA
T_{amb} = +55°C
$I_a \geq$ 1.5mA
example
V_b = 350V ±10%
R_a = max 114kΩ
min 102kΩ
0
50
100
150
200
R_a (kΩ)

Fig.4

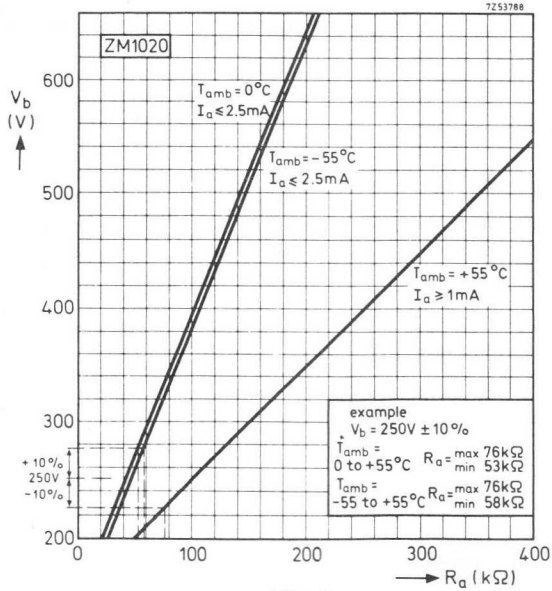

7Z53788
ZM1020
V_b (V)
600
500
400
300
200
+10%
250V
-10%
T_{amb} = 0°C
$I_a \leq$ 2.5mA
T_{amb} = -55°C
$I_a \leq$ 2.5mA
T_{amb} = +55°C
$I_a \geq$ 1mA
example
V_b = 250V ±10%
T_{amb} = 0 to +55°C R_a = max 76kΩ min 53kΩ
T_{amb} = -55 to +55°C R_a = max 76kΩ min 58kΩ
0
100
200
300
400
R_a (kΩ)

Fig.5

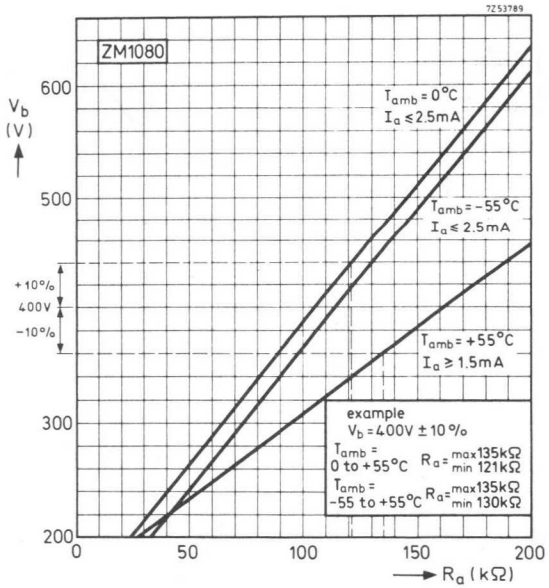


Fig.6

Wiring capacitance at each Q-output of the ID 10: max. 500 pF

REVERSIBLE DECADE COUNTER BCA 10 B

CIRCUIT DATA

For circuit diagram see next pages.

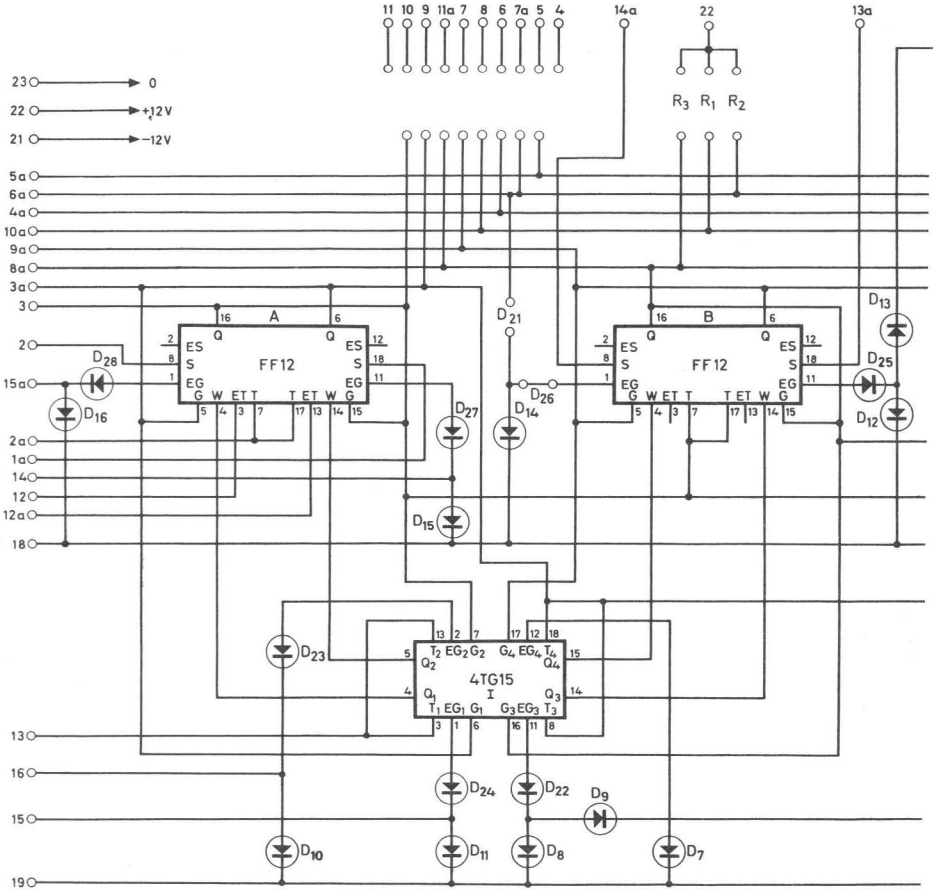
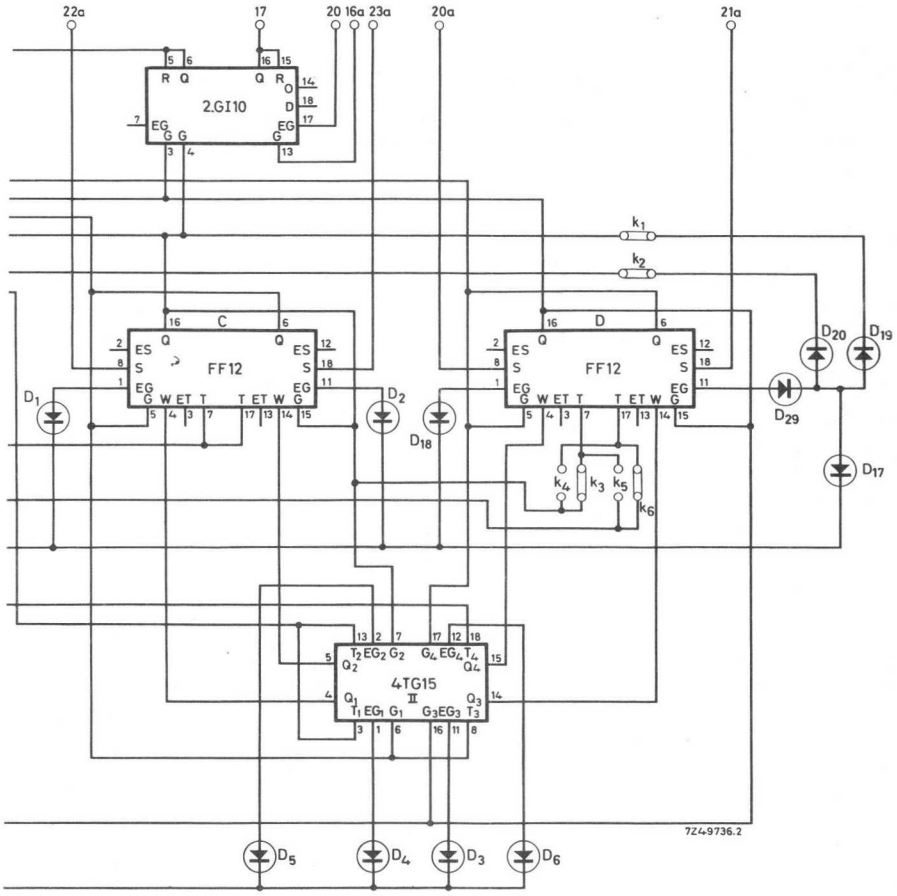

11 10 9 11a 7 8 6 7a 5 4
14a
22
13a
23 → 0
22 → +12V
21 → −12V
R3 R1 R2
5a 6a 4a 10a 9a 8a 3a 3
2 15a 2a 1a 14 12 12a 18
13 16 15 19
A
B
FF12
4TG15
D28 D16 D21 D27 D14 D26 D15 D13 D25 D12 D23 D24 D22 D9 D10 D11 D8 D7

Fig.7. BCA 10B


22a
17
20
16a
23a
20a
21a
2.GI10
FF12
FF12
4TG15
k1
k2
k3
k4
k5
k6
D1
D2
D18
D20
D19
D29
D17
D5
D4
D3
D6
7Z49736.2

Terminals (Fig.8)

Similar to BCA 10 A, with the exception of terminals 4, 5, 6, 7, 7a, 8, 9, 10, 11 and 11a, which are inoperative.

INPUT REQUIREMENTS

Similar to BCA 10 A.

OUTPUT DATA (at V_P = 11.4 V and V_N = −12.6 V, unless specified differently)

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board, the Q-outputs of each flip-flop in the decade counter may furthermore be loaded as specified in the table below.

flip-flop	FF 12-A		FF 12-B		FF 12-C		FF 12-D	
output terminal	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
	3	3a	8a	9a	10a	4a	6a	5a
available direct current min. I_{QD} in mA	3.8	3.8	3.8	4.9	3.8	4.9	3.8	6
available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 μs: min. Q_{QT} in nC	22.4	22.4	22.4	22.4	22.4	22.4	23.7	25.8

For T_{amb} = min. −25 °C the available direct current I_{QD} has to be reduced with 1.6 mA and similarly the available transient charge Q_{QT} with 5 nC.

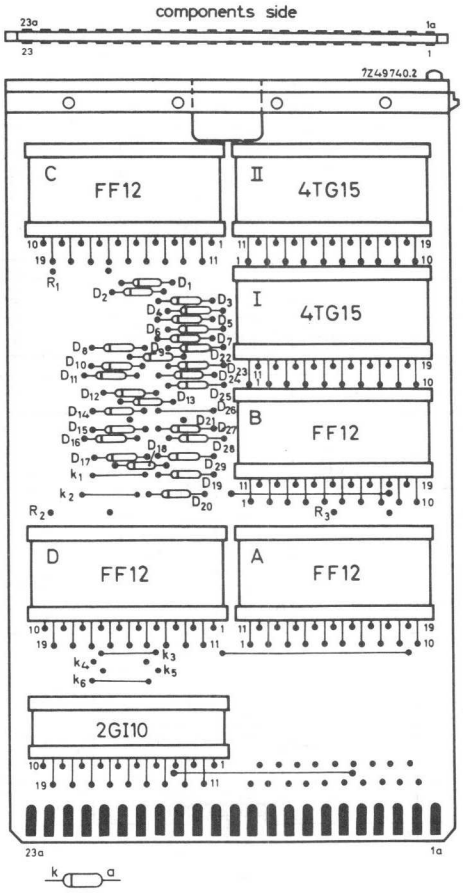

components side
23a
1a
23
1
7Z49740.2
C
FF12
II
4TG15
I
4TG15
B
FF12
D
FF12
A
FF12
2GI10
R1
R2
R3
k1
k2
k3
k4
k5
k6
k
a

Fig.8. BCA 10 B

REVERSIBLE DECADE COUNTER AND NUMERICAL INDICATOR TUBE DRIVER BCA 10 C

CIRCUIT DATA

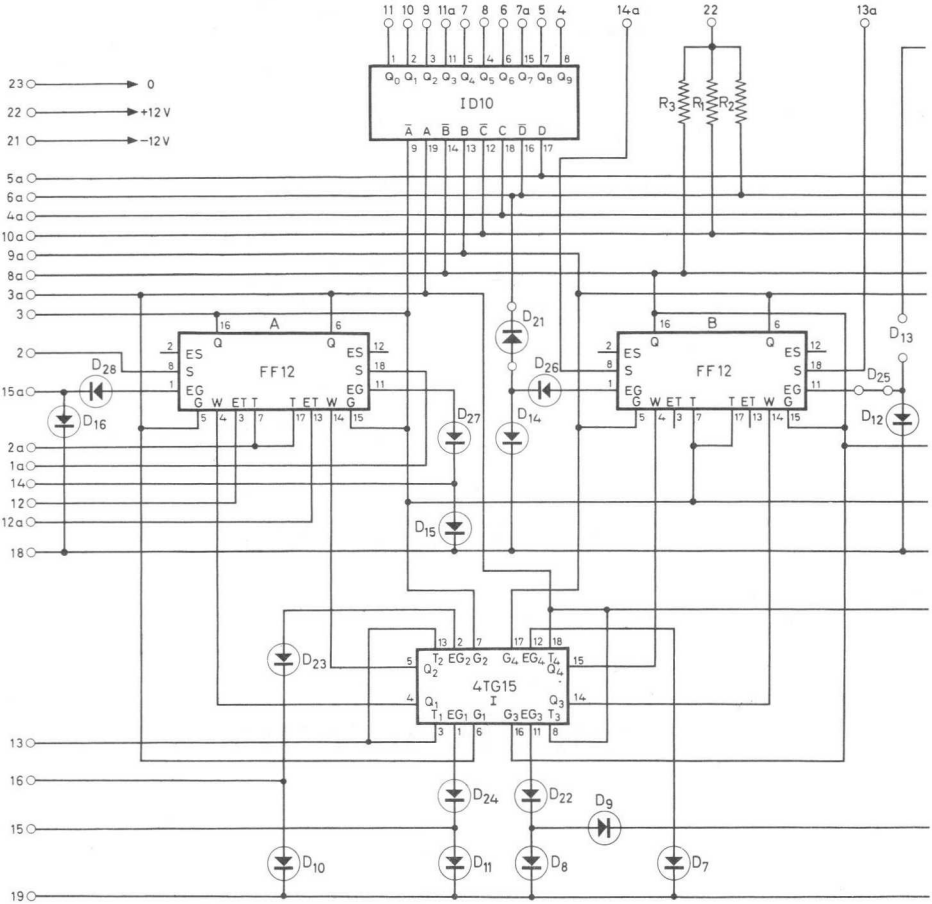
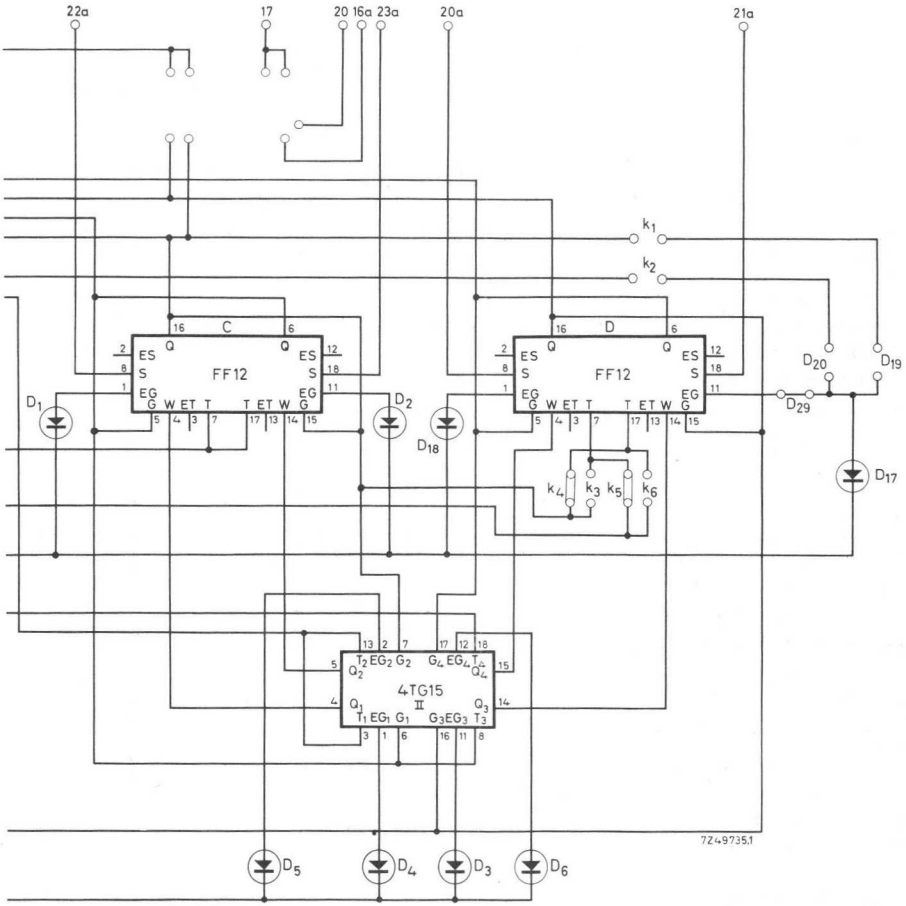


Fig. 9


22a
17
20 16a 23a
20a
21a
k1
k2
FF12
C
D
D1
D2
D18
D20
D29
D19
D17
k4
k3
k5
k6
4TG15
II
D5
D4
D3
D6
7Z49735.1

Terminals (Fig.10)

Similar to BCA 10 A, with the exception of terminals 16a, 17 and 20, which are inoperative.

INPUT REQUIREMENTS

Similar to BCA 10 A.

OUTPUT DATA (at V_P = 11.4 V and V_N = −12.6 V, unless specified differently)

Decade counter section

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board including the numerical indicator tube driver ID 10, the Q-outputs of each flip-flop in the decade counter may furthermore be loaded as specified in the table below.

The loadability of the flip-flops FF 12-A, FF 12-C and FF 12-D can be increased by connecting an external resistor of 51 kΩ±5% in parallel with the built-in collector resistor of the corresponding output. This resistor has to be connected between the output terminal and V_P.

flip-flop		FF 12-A		FF 12-B		FF 12-C		FF 12-D	
output terminal		$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
		3	3a	8a	9a	10a	4a	6a	5a
max. number of 10-series circuit blocks, that may be driven, provided each driven input represents a load of $-I_D$ = max. 1.1 mA and $-Q_T$ = max. 3.4 nC	T_{amb} = min. 0 °C	1	1	3	3	3	1	2	4
	T_{amb} = min. −25 °C	1	1	2	2	2	1	1	4
max. number of driven 10-series circuit blocks, with external parallel collector resistor(s)	T_{amb} = min. 0 °C	3	3	3	3	3	3	2	5
	T_{amb} = min. −25 °C	2	2	2	2	2	2	1	4

Numerical indicator tube driver section

Similar to BCA 10 A.

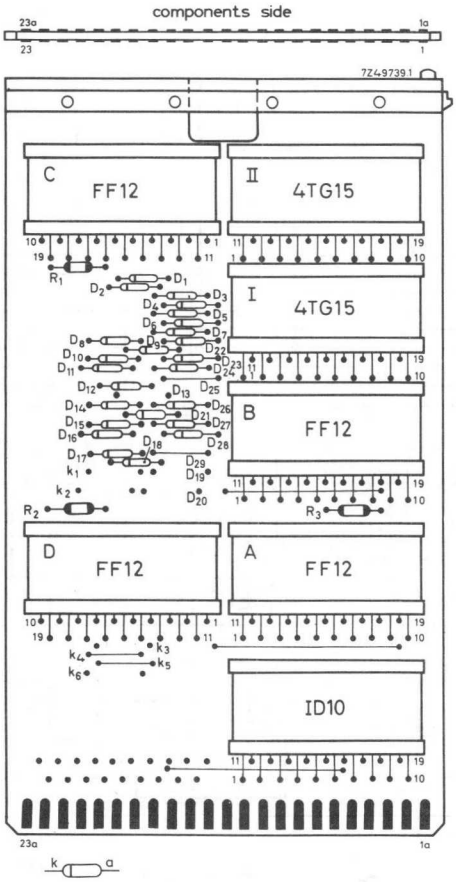


Fig.10. BCA 10 C

REVERSIBLE DECADE COUNTER BCA 10 D

CIRCUIT DATA

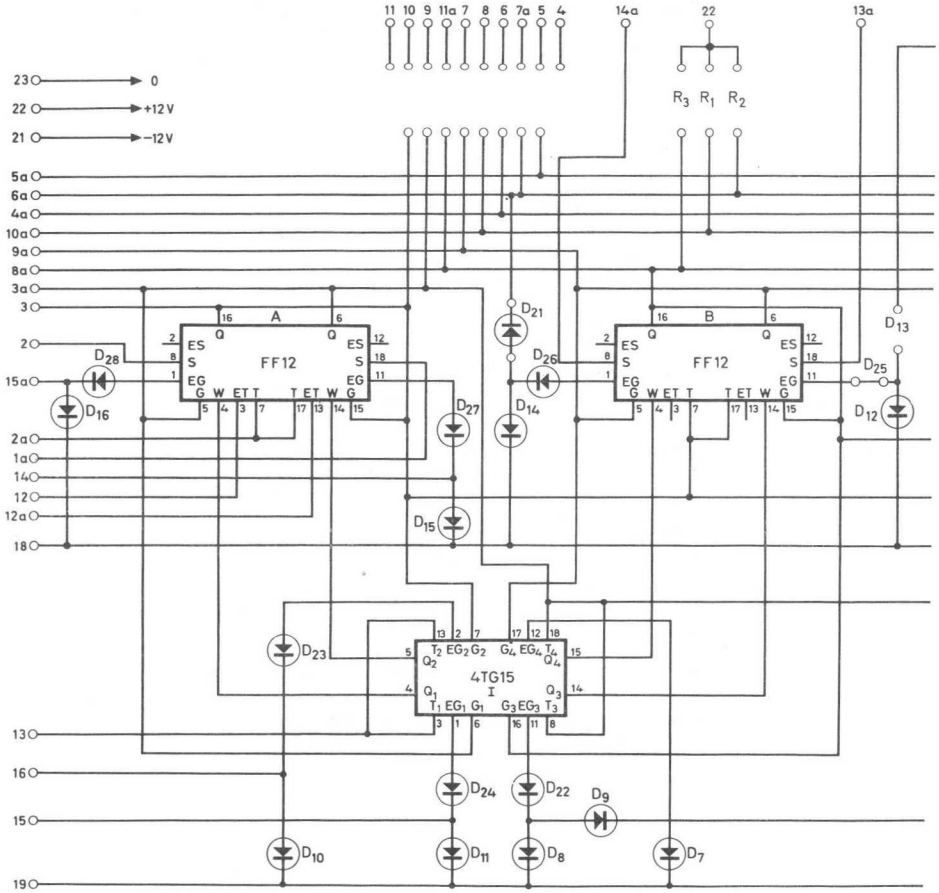
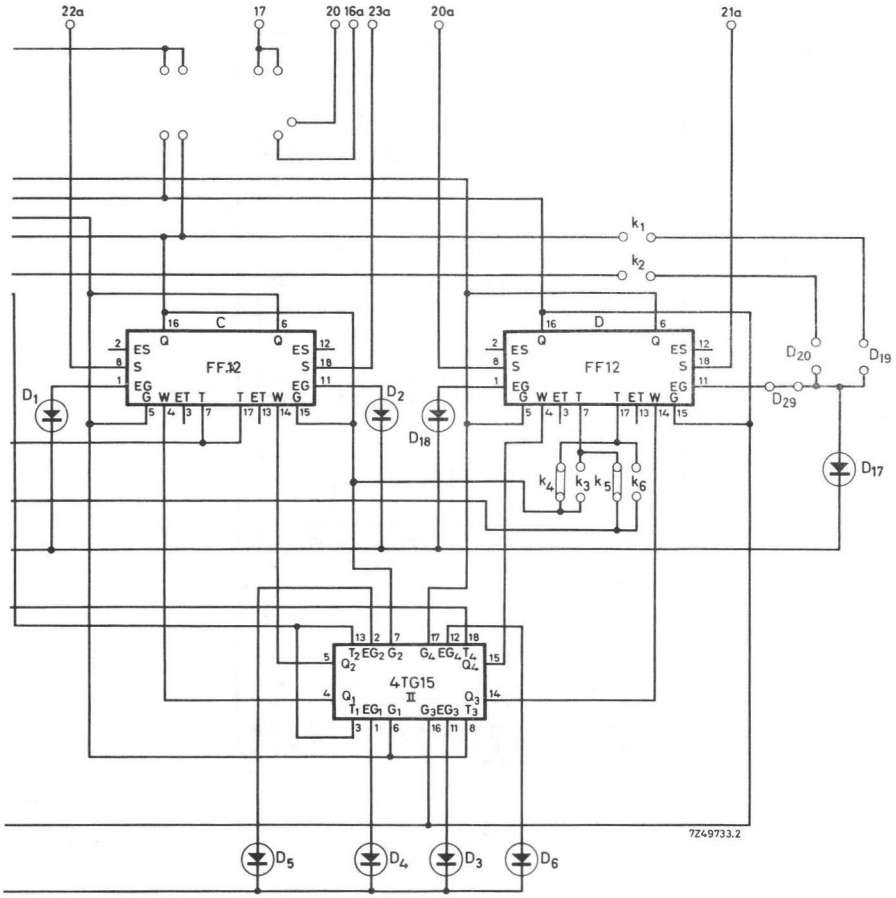


Fig.11


22a
17
20 16a 23a
20a
21a
k1
k2
FF12
C
D
D1
D2
D18
D17
D20
D19
D29
k4
k3
k5
k6
4TG15
II
D5
D4
D3
D6
7Z49733.2

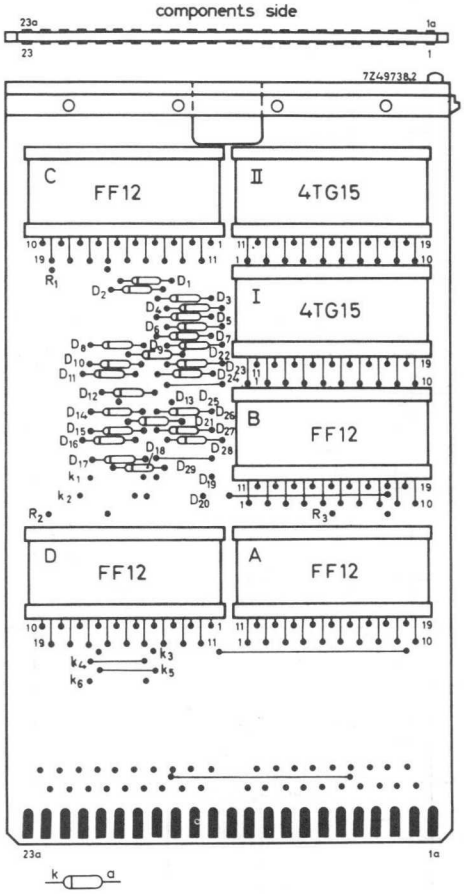


Fig.12. BCA 10 D

Terminals (Fig.12)

Similar to BCA 10 A, with the exception of terminals 4, 5, 6, 7, 7a, 8, 9, 10, 11, 11a, 16a, 17 and 20, which are inoperative.

INPUT REQUIREMENTS

Similar to BCA 10 A.

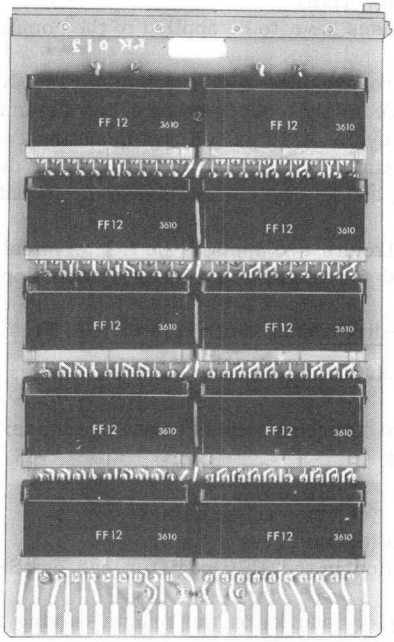
OUTPUT DATA (at V_P = 11.4 V and V_N = −12.6 V, unless specified differently)

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board, the Q-outputs of each flip-flop in the decade counter may furthermore be loaded as specified in the table below.

flip-flop	FF 12-A		FF 12-B		FF 12-C		FF 12-D	
output terminal	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
	3	3a	8a	9a	10a	4a	6a	5a
available direct current: min. I_{QD} in mA	3.8	3.8	4.9	4.9	4.9	4.9	3.8	6
available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 μs: min. Q_{QT} in nC	22.4	22.4	22.4	22.4	22.4	22.4	25.8	25.8

For T_{amb} = min. −25 °C the available direct current I_{QD} has to be reduced with 1.6 mA and similarly the available transient charge Q_{QT} with 5 nC.

DUAL SHIFT REGISTER ASSEMBLY



RZ 22603-7

This assembly can be applied to fulfil three major functions as described below.

- Dual 5-stages one-directional shift register (see Figs.1 and 2)
  The information that has to be serially shifted into the register, has to be applied to the gate inputs G of flip-flop FF 12-A (terminals 7 and 7a) or gate inputs G of flip-flop FF 12-A' (terminals 17a and 17).
  The trigger (shift) pulses have to be applied to the common trigger terminals 4 or 19.
  Both shift registers are provided with a common reset line (terminals 3a and 19a) while of each individual flip-flop in both shift registers, one S-input is brought out for pre-set purposes.
  The positions k_1, k_2, k_3 and k_4 on the printed-wiring board have to be left open.

- Dual one-directional decade ring counter (see Figs.1 and 2)

For this function the Q-outputs of flip-flop FF 12-E (FF 12-E') have to be cross-connected externally with the gate inputs G of flip-flop FF 12-A (FF 12-A'). The necessary interconnections are:
terminal 10a (13) with 7a (17) and
terminal 10 (12) with 7 (17a).
The trigger (shift) pulses have to be applied to the common trigger terminal 4 (19).
Both ring counters are provided with a common reset line (terminals 3a and 19a). Any disturbance in the code sequence can automatically be corrected after maximum one cycle of 10 pulses, by mounting two diodes AAY 21 per ring counter on the printed-wiring board. In Fig.2 the diode positions are indicated as k_1, k_2, k_3 and k_4; the diodes have to be mounted with the anode located at "a".
If these correction circuits are applied the EG-terminals 11 and 11a (12a and 13a) may not be used for blocking purposes of flip-flop FF 12-A (FF 12-A').

- Single 10-stages one-directional shift register (see Figs.1 and 2)

This function can be obtained by putting the two 5-stages shift registers in series.
The following external interconnections have to be made:
terminal 10a with 17a
terminal 10 with 17
terminal 4 with 19 (common trigger line)
terminal 3a with 19a (common reset line).
Each individual flip-flop in the shift register has one S-input brought out for preset purposes.
The positions k_1, k_2, k_3 and k_4 on the printed-wiring board have to be left open.

In the three above mentioned functions the trigger pulses can be inhibited by means of a "positive low" voltage applied to the EG-terminals 11 and 11a (12a and 13a) of the first flip-flop FF 12-A (FF 12-A').

The bare printed-wiring board (catalog number 4322 026 38740), provided with plated-through holes and double-sided goldplated contacts, is made of glass-epoxy material. Moreover, the printed-wiring board is delivered with an extractor and a locking device.
With the mating connector (catalog number 2422 020 52591), not supplied with the assembly, the printed-wiring board of standard dimensions (121.8 mm x 207.0 mm x 1.6 mm) can be used directly in the standard mounting chassis (catalog number 4322 026 38240).

The circuit blocks are secured to the printed-wiring board by means of locking caps (catalog number 4322 026 32150).

Counting rate	max. 30 kHz
Ambient temperature range	
operating	−25 to +55 °C below 0 °C: derated output data
storage	−55 to +75 °C
Weight	approx. 500 g

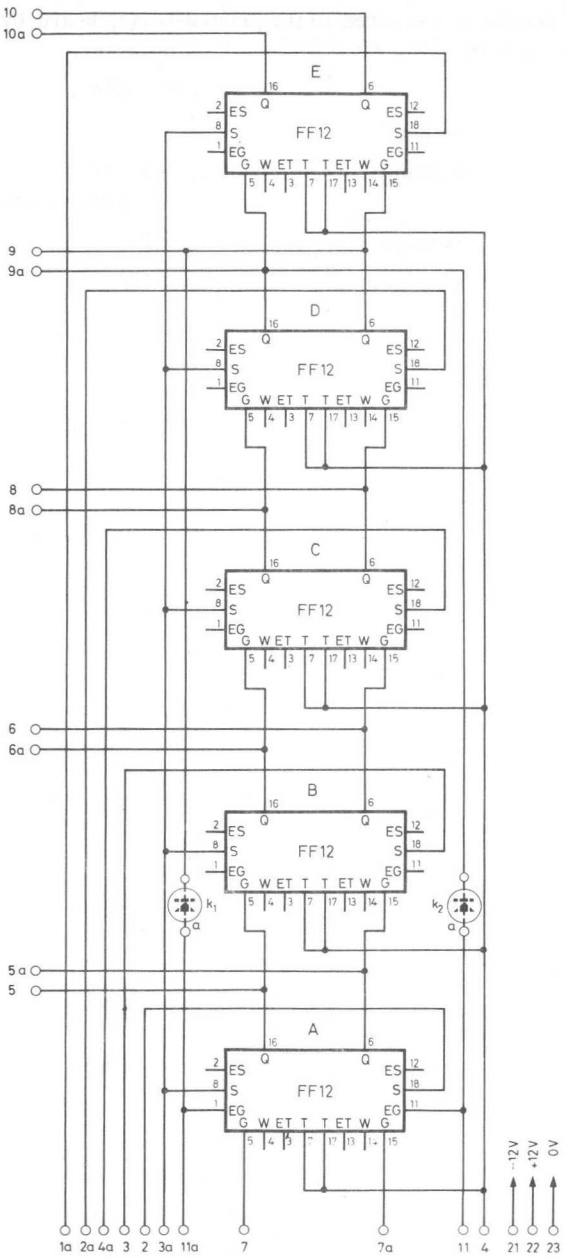

10
10a
E
D
C
B
A
FF12
ES
S
EG
Q
G W ET T T ET W G
9
9a
8
8a
6
6a
5a
5
k_1
k_2
a
1a 2a 4a 3 2 3a 11a 7 7a 11 4 21 22 23
-12V
+12V
0V

Fig.1a

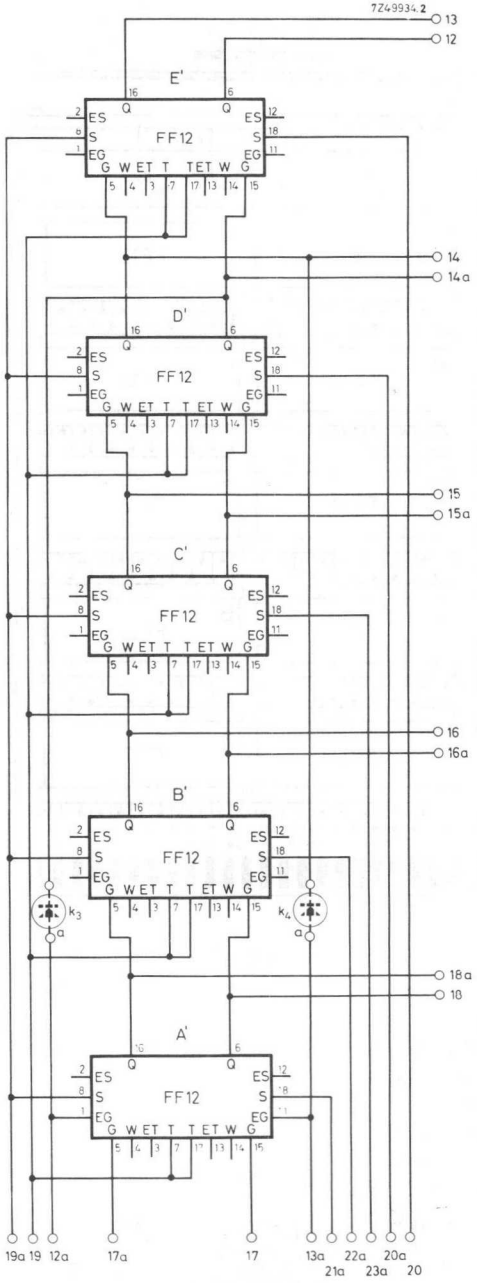

7Z49934.2
13
12
E'
FF12
14
14a
D'
FF12
15
15a
C'
FF12
16
16a
B'
FF12
k_3
k_4
18a
10
A'
FF12
19a 19 12a 17a 17 13a 21a 22a 23a 20a 20

Fig.1b

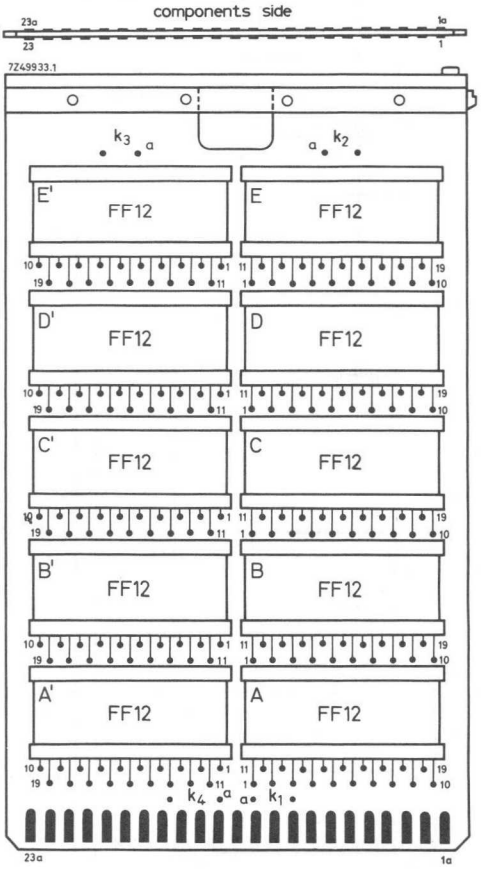


Fig.2

Terminals

1 = not connected
2 = set input S of flip-flop A
3 = set input S of flip-flop B
4 = trigger input T
5 = output $\overline{Q}$ of flip-flop A
6 = output Q of flip-flop B
7 = gate input G of flip-flop A
8 = output Q of flip-flop C
9 = output Q of flip-flop D
10 = output Q of flip-flop E

11 = extension gate input EG of flip-flop A
12 = output Q of flip-flop E'
13 = output $\overline{Q}$ of flip-flop E'
14 = output $\overline{Q}$ of flip-flop D'
15 = output $\overline{Q}$ of flip-flop C'
16 = output $\overline{Q}$ of flip-flop B'
17 = gate input G of flip-flop A'
18 = output Q of flip-flop A'
19 = trigger input T
20 = set input S of flip-flop E'
21 = common negative supply −12 V
22 = common positive supply + 12 V
23 = common supply 0 V

1a = set input S of flip-flop E
2a = set input S of flip-flop D
3a = common reset input S
4a = set input S of flip-flop C
5a = output Q of flip-flop A
6a = output $\overline{Q}$ of flip-flop B
7a = gate input G of flop-flop A
8a = output $\overline{Q}$ of flip-flop C
9a = output $\overline{Q}$ of flip-flop D
10a = output $\overline{Q}$ of flip-flop E
11a = extension gate input EG of flip-flop A
12a = extension gate input EG of flip-flop A'
13a = extension gate input EG of flip-flop A'
14a = output Q of flip-flop D'
15a = output Q of flip-flop C'
16a = output Q of flip-flop B'
17a = gate input G of flip-flop A'
18a = output $\overline{Q}$ of flip-flop A'
19a = common reset input S
20a = set input S of flip-flop D'
21a = set input S of flip-flop A'
22a = set input S of flip-flop B'
23a = set input S of flip-flop C'

Power supply

Terminal 21 : $V_N = -12\ V \pm 5\ \%$, $-I_N = 11\ mA$
22 : $V_P = +12\ V \pm 5\ \%$, $I_P = 70\ mA$
23 : $V_E = 0\ V$ common

} The current values are nominal

INPUT REQUIREMENTS (at V_P = 11.4 V and V_N = −12.6 V, unless specified differently)

Set/reset inputs (S-terminals)

For reset- and preset purposes a "positive low" voltage V_S is required between 0 V and 0.3 V, otherwise this voltage must be kept between V_P and 2/3 V_P.

Common reset (terminals 3a and 19a)

With one pulse at these terminals all flip-flops will be reset simultaneously.

	Ring counter or 5-stages shift register	10-stages shift register
Required direct current	$-I_{SD}$ = max. 9.75 mA	= max. 19.50 mA
Required transient charge when V_S changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{ST}$ = max. 14 nC	= max. 28 nC
Time data		
Pulse duration	t_p = min. 2 μs	= min. 2 μs } See point 4 *
Recovery time	t_{rec} = min. 15 μs	= min. 15 μs }
Time delay between S- and T-signal	t_{st} = min. 15 μs	= min. 15 μs } See point 5 *

Individual flip-flop preset (terminals 1a, 2, 2a, 3, 4a and 20, 20a, 21a, 22a, 23a)

For this purpose one S-input of each individual flip-flop in the register(s) has been brought out.

Required direct current	$-I_{SD}$ = max. 1.95 mA
Required transient charge when V_S changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{ST}$ = max. 2.8 nC

* Section "Time definitions" of "Circuit blocks 10-Series".

Gate input (G-terminals 7, 7a and 17a, 17)

A d.c. voltage level is applied to terminal G.
A "positive low" voltage closes the gate, whilst a "positive high" voltage (between 2/3 V_P and V_P) opens the gate.

Gate open				
Voltage	V_G	= min. 2/3 V_P		
		max. V_P		
Gate closed				
Voltage	V_G	= min. 0	V	
		max. 0.3	V	
Required direct current	$-I_{GD}$	= max. 1.1	mA	
Required transient charge when V_G changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{GT}$	= max. 1.2	nC	
Time data				
Trigger gate setting time	t_{gs}	= min. 29	μs	See point 6*
Trigger gate inhibiting time	t_{gi}	= min. 29	μs	See point 7*

Trigger input (T-terminals 4 and 19)

Negative-going trigger pulses have to be applied to the common trigger (shift) terminals 4 and 19.

		Ring counter or 5-stages shift register	10-stages shift register
Required direct current when V_T = max. 0.3 V	$-I_{TD}$	= max. 5.5 mA	= max.11 mA
Required transient charge when V_T changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{TT}$	= max. 17 nC	= max.34 nC
Time data			
Fall time	t_f	= max. 1.5 μs	
Pulse duration	t_p	= min. 2 μs	See point 3*
Trigger gate setting time	t_{gs}	= min. 29 μs	
Time delay between T- and S-signals	t_{ts}	= min. 15 μs	See point 5*

* Section "Time definitions" of "Circuit blocks 10-Series".

OUTPUT DATA (at V_P = 11.4 V and V_N = −12.6 V, unless specified differently)

The available output data of each flip-flop depend on the circuit configuration.

Dual 5-stages one-directional shift register

In excess of the internal load, represented by the circuit blocks, mounted on the printed-wiring board, the Q-outputs of each flip-flop in the shift register may furthermore be loaded as specified in the table below.

flip-flop	FF 12-A(A')		FF 12-B(B')		FF 12-C(C')		FF 12-D(D')		FF 12-E(E')	
output terminal	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
	5(18a)	5a(18)	6a(16)	6(16a)	8a(15)	8(15a)	9a(14)	9(14a)	10a(13)	10(12)
available direct current: min. I_{QD} in mA	7.1	7.1	7.1	7.1	7.1	7.1	7.1	7.1	8.2	8.2
available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 μs: min. Q_{QT} in nC	25.8	25.8	25.8	25.8	25.8	25.8	25.8	25.8	27	27

For T_{amb} = min. −25 °C the available direct current I_{QD} has to be reduced with 1.6 mA and similarly the available transient charge Q_{QT} with 5 nC.

Dual one-directional decade ring counter

In excess of the internal load (with feedback diodes on k_1, k_2, k_3 and k_4), represented by the circuit blocks, mounted on the printed-wiring board, the Q-outputs of each flip-flop in the ring counter may furthermore be loaded as specified in the table below.

flip-flop	FF 12-A(A')		FF 12-B(B')		FF 12-C(C')		FF 12-D(D')		FF 12-E(E')	
output terminal	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
	5(18a)	5a(18)	6a(16)	6(16a)	8a(15)	8(15a)	9a(14)	9(14a)	10a(13)	10(12)
available direct current: min. I_{QD} in mA	7.1	7.1	7.1	7.1	7.1	7.1	6	6	7.1	7.1
available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 μs: min. Q_{QT} in nC	25.8	25.8	25.8	25.8	25.8	25.8	24.6	24.6	25.8	25.8

For T_{amb} = min. −25 °C the available direct current I_{QD} has to be reduced with 1.6 mA and similarly the available transient charge Q_{QT} with 5 nC.

Output levels of the flip-flops in a decade ring counter configuration

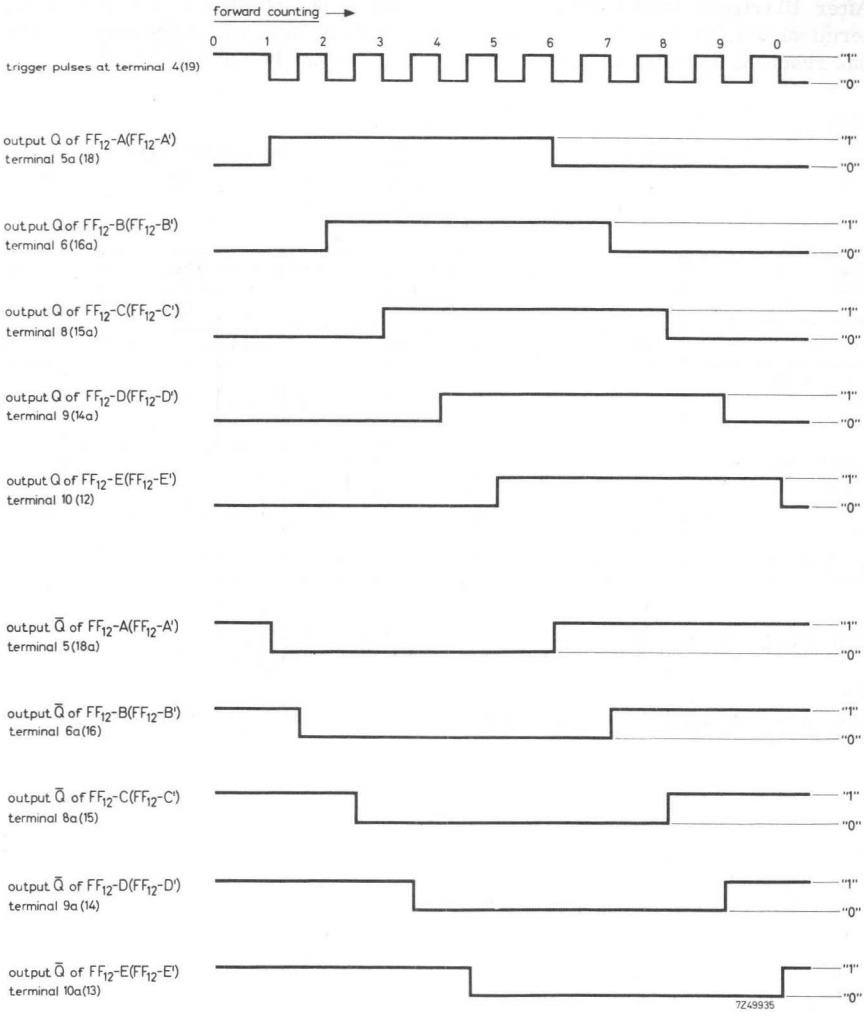


Fig. 3

Note that when a Q-output is at "0" level the corresponding $\overline{Q}$-output is at the "1" level and vice versa.
After 10 trigger (shift) pulses at the trigger input terminal 4 (19), the output terminal 10 (12) delivers one negative-going voltage step, whilst the ring counter has resumed its initial position, namely all Q-outputs being at "0" level.

Single 10-stages one-directional shift register

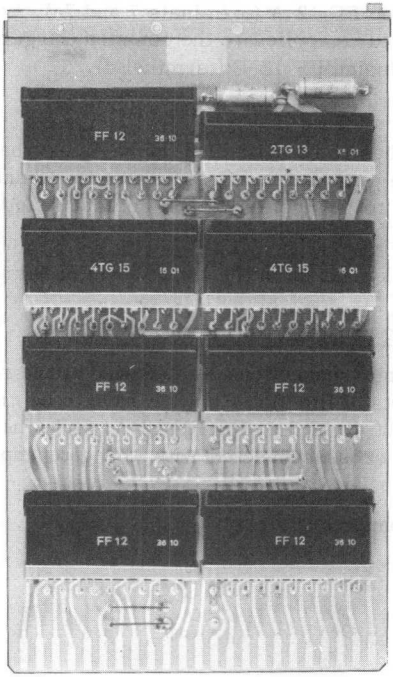
In excess of the internal load, represented by the circuit blocks, mounted on the printed-wiring board, the Q-outputs of each flip-flop in the shift register may furthermore be loaded as specified in the table below.

flip-flop	FF 12-A(A')		FF 12-B(B')		FF 12-C(C')		FF 12-D(D')		FF 12-E(E')	
output terminal	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
	5(18a)	5a(18)	6a(16)	6(16a)	8a(15)	8(15a)	9a(14)	9(14a)	10a(13)	10(12)
available direct current: min. I_{QD} in mA	7.1	7.1	7.1	7.1	7.1	7.1	7.1	7.1	7.1(8.2)	7.1(8.2)
available transient charge when V_Q changes from 2/3 Vp to 0.5 V in 1.5 μs: min. Q_{QT} in nC	25.8	25.8	25.8	25.8	25.8	25.8	25.8	25.8	25.8(27)	25.8(27)

For T_{amb} = min. −25 °C the available direct current I_{QD} has to be reduced with 1.6 mA and similarly the available transient charge Q_{QT} with 5 nC.

Wiring capacitance at each Q-output max. 175 pF

REVERSIBLE SHIFT REGISTER ASSEMBLY



RZ 22752-2

This assembly can be applied to fulfil three major functions as described below.

5-stages reversible shift register (see Figs.1 and 2)

For this function the gate inputs G of the trigger gates 4.TG 15 have to be interconnected externally with the corresponding Q-outputs of the flip-flops FF 12-B up to and including FF 12-E.
The necessary interconnections are:

terminal 10a with 3a
terminal 9a with 4a
terminal 9 with 17
terminal 2a with 17a
terminal 14a with 18
terminal 14 with 18a
terminal 19 with 21a
terminal 19a with 22a

The following signals have to be applied for forward and reverse shifting:

Forward shifting

The information that has to be shifted in the register, has to be applied to the gate inputs G of flip-flop FF 12-A (terminals 7 and 7a).
The trigger pulse has to be applied to the common trigger line of the flip-flops FF 12-A up to and including FF 12-E (terminal 4).

Reverse shifting

The information that has to be shifted in the register, has to be applied to the gate inputs G of the trigger gate 2. TG 13 (terminals 12 and 12a).
The trigger pulse has to be applied to the common trigger line of the trigger gates 4. TG 15 and 2. TG 13 (terminal 13).

The positions k_1, k_2, k_3 and k_4 on the printed-wiring board have to be left open.

Reversible decade ring counter (see Figs. 1 and 2)

For this function the interconnections as specified above remain unchanged. Moreover the Q-outputs of flip-flop FF 12-E have to be cross-connected externally with the gate inputs G of flip-flop FF 12-A, while the Q-outputs of flip-flop FF 12-A have to be cross-connected with the gate inputs G of trigger gate 2. TG 13.

The necessary interconnections are:

terminal 21a with 7a
terminal 22a with 7
terminal 6 with 12a
terminal 5 with 12

Trigger pulses for forward counting have to be applied to the common trigger line of the flip-flops FF 12-A up to and including FF 12-E (terminal 4); for reverse counting the trigger pulses have to be applied to the common trigger line of the trigger gates 4. TG 15 and 2. TG 13 (terminal 13).

Any disturbance in the code sequence can automatically be corrected after maximum one cycle of 10 pulses, by mounting on the printed-wiring board two diodes AAY21 for each counting direction. In Fig. 2 the diode positions are indicated as k_1, k_2, k_3 and k_4; the diodes have to be mounted with the anode located at "a". If these correction circuits are applied, the EG-terminals 11 and 11a may not be used for blocking purposes of flip-flop FF 12-A.

One-directional shift register with additional inputs for parallel information shift (see Figs. 1 and 2)

When information has to be inserted in the shift register in a parallel way, the binary signals have to be applied to the following terminals:

10a and 9a for flip flop FF 12-A
9 and 2a for flip flop FF 12-B
14a and 14 for flip-flop FF 12-C
19 and 19a for flip-flop FF 12-D
12 and 12a for flip-flop FF 12-E.

With one shift pulse at the common trigger line (terminal 13) the externally applied information is shifted into the shift register.
Therefore the shift register is suitable for serial-parallel work.
The positions k_1, k_2, k_3 and k_4 on the printed-wiring board have to be left open.

The capacitors C_1 and C_2 are mounted on the printed-wiring board for noise filtering purposes of the supply lines.

The bare printed-wiring board (catalog number 4322 026 38750), provided with plated-through holes and double-sided goldplated contacts, is made of glass-epoxy material. Moreover, the printed-wiring board is delivered with an extractor and a locking device. With the mating connector (catalog number 2422 020 52591), not supplied with the assembly, the printed-wiring board of standard dimensions (121.8 mm x 207.0 mm x 1.6 mm) can be used directly in the standard mounting chassis (catalog number 4322 026 38240).

The circuit blocks are secured to the printed-wiring board by means of locking caps (catalog number 4322 026 32150).

Counting rate	max. 30 kHz
Ambient-temperature range	
operating	−25 to +55 °C below 0 °C: derated output data
storage	−55 to +75 °C
Weight	approx. 400 g

CIRCUIT DATA

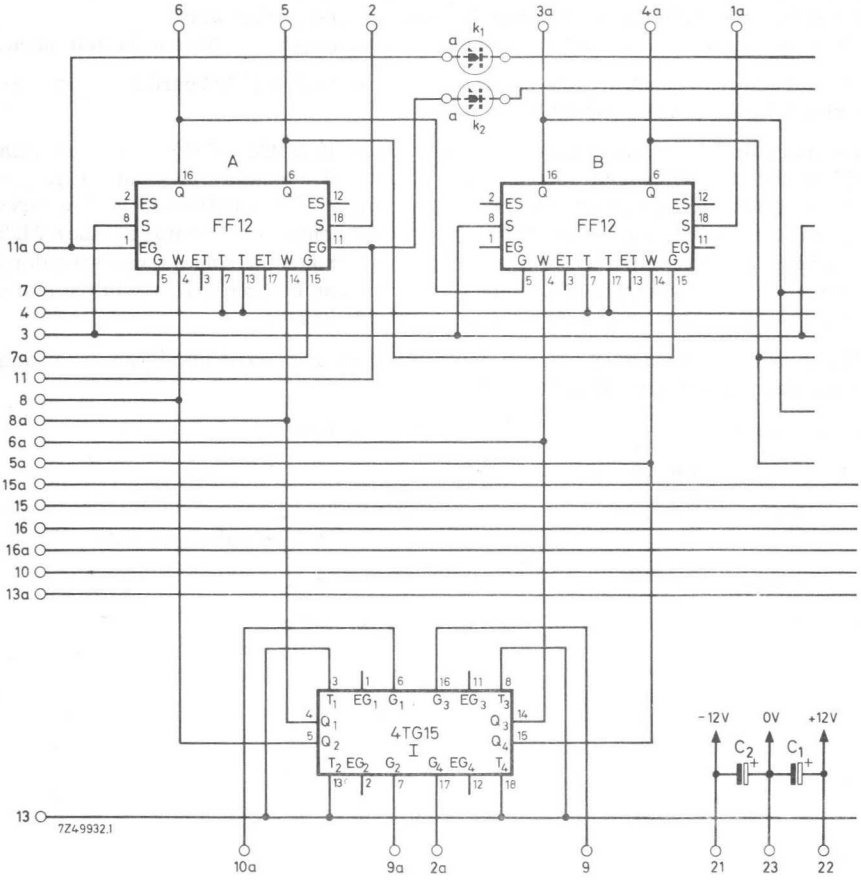


Fig. 1a

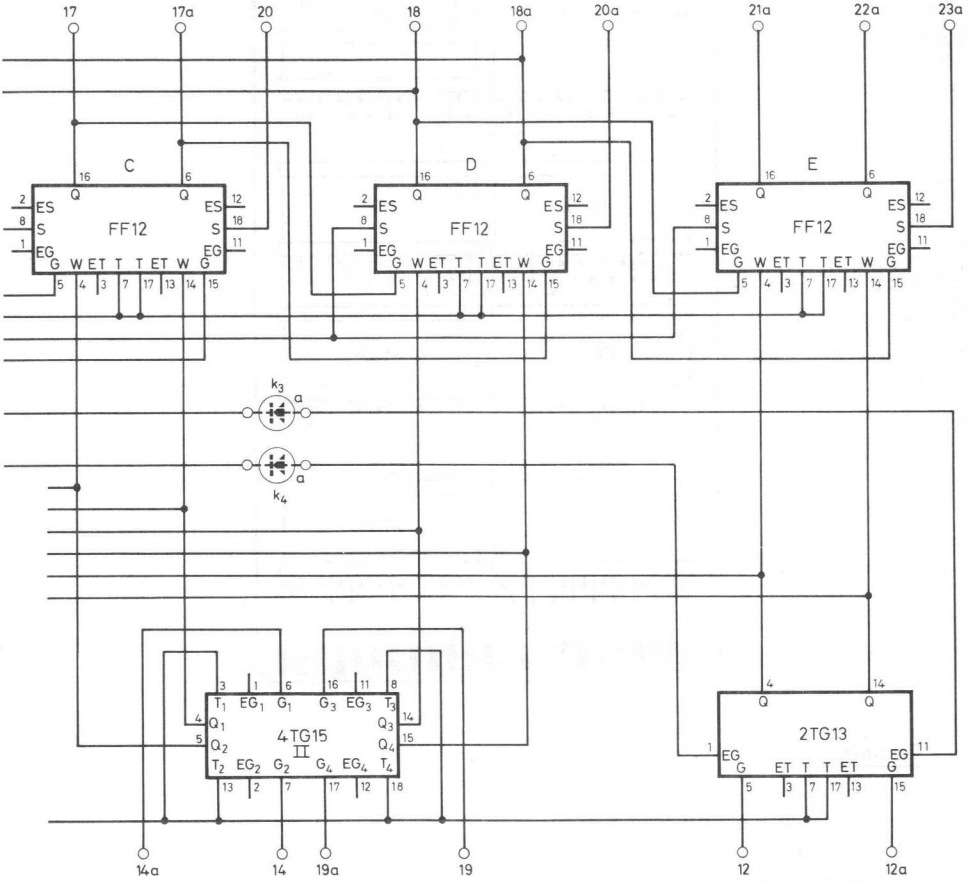

17
17a
20
18
18a
20a
21a
22a
23a
C
D
E
FF12
FF12
FF12
k_3
k_4
a
a
4TG15
II
2TG13
14a
14
19a
19
12
12a

Fig. 1b

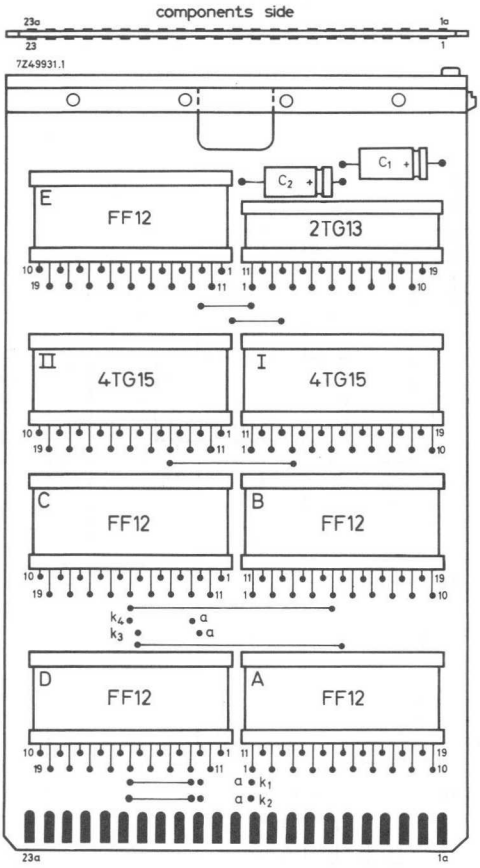


Fig.2

Terminals

1 = not connected
2 = set input S of flip-flop A
3 = common set input S
4 = trigger input for forward counting
5 = output Q of flip-flop A
6 = output $\overline{Q}$ of flip-flop A
7 = gate input G of flip-flop A
8 = base input W of flip-flop A
9 = gate input G of 4.TG 15-I
10 = base input W of flip-flop E

11 = extension gate input EG of flip-flop A
12 = gate input G of 2.TG 13
13 = trigger input for reverse counting
14 = gate input G of 4.TG 15-II
15 = base input W of flip-flop C
16 = base input W of flip-flop D
17 = output $\overline{Q}$ of flip-flop C
18 = output $\overline{Q}$ of flip-flop D
19 = gate input G of 4.TG 15-II
20 = set input S of flip-flop C
21 = common negative supply −12 V
22 = common positive supply +12 V
23 = common supply 0 V

1a = set input S of flip-flop B
2a = gate input G of 4.TG 15-I
3a = output $\overline{Q}$ of flip-flop B
4a = output Q of flip-flop B
5a = base input W of flip-flop B
6a = base input W of flip-flop B
7a = gate input G of flip-flop A
8a = base input W of flip-flop A
9a = gate input G of 4.TG 15-I
10a = gate input G of 4.TG 15-I
11a = extension gate input EG of flip-flop A
12a = gate input G of 2.TG 13
13a = base input W of flip-flop E
14a = gate input G of 4.TG 15-II
15a = base input W of flip-flop C
16a = base input W of flip-flop D
17a = output Q of flip-flop C
18a = output Q of flip-flop D
19a = gate input G of 4.TG 15-II
20a = set input S of flip-flop D
21a = output $\overline{Q}$ of flip-flop E
22a = output Q of flip-flop E
23a = set input S of flip-flop E

Power supply

Terminal 21 : $V_N = -12\ V \pm 5\%$, $-I_N = 9.0$ mA
22 : $V_P = +12\ V \pm 5\%$, $I_P = 45$ mA
} The current values are nominal
23 : $V_E = 0$ V common

INPUT REQUIREMENTS (at V_P = 11.4 V and V_N = −12.6 V unless specified differently)

Set/reset inputs (S-terminals)

For reset- or preset purposes a "positive low" voltage V_S is required between 0 V and 0.3 V, otherwise this voltage must be kept between V_P and 2/3 V_P.

Common reset (terminal 3)

With one pulse at terminal 3 all flip-flops will be reset simultaneously.

Required direct current	$-I_{SD}$ = max. 9.75 mA		
Required transient charge when V_S changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{ST}$ = max. 14 nC		
Time data			
Pulse duration	t_p = min. 2 μs	}	See point 4*
Recovery time	t_{rec} = min. 15 μs	}	
Time delay between S- and T-signal	t_{st} = min. 15 μs		See point 5*

Individual flip-flop preset (terminals 2, 1a, 20, 20a and 23a)

For this purpose one S-input of each flip-flop in the register has been brought out.

Required direct current	$-I_{SD}$ = max. 1.95 mA	
Required transient charge when V_S changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{ST}$ = max. 2.8 nC	

Gate input (G-terminals)

A d.c. voltage level is applied to terminal G.
A "positive low" voltage closes the gate, whilst a "positive high" voltage (between 2/3 V_P and V_P) opens the gate.

Gate open		
Voltage	V_G = min. 2/3 V_P, max. V_P	
Gate closed		
Voltage	V_G = min. 0 V, max. 0.3 V	
Required direct current	$-I_{GD}$ = max. 1.1 mA	
Required transient charge when V_G changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{GT}$ = max. 1.2 nC	

* Section "Time definitions" of "Circuit blocks 10-Series".

Time data

Trigger gate setting time	t_{gs} = min. 29 μs	See point 6 *
Trigger gate inhibiting time	t_{gi} = min. 29 μs	See point 7 *

Trigger input (T-terminals 4 and 13)

For forward counting or shifting the trigger pulses have to be applied to common trigger terminal 4. For reverse counting or shifting the trigger pulses have to be applied to common trigger terminal 13.

Required direct current when V_T = max. 0.3 V	$-I_{TD}$ = max. 5.5 mA	
Required transient charge when V_T changes from 2/3 V_P to 0.5 V in 1.5 μs	$-Q_{TT}$ = max. 17 nC	
Input noise level	V_n = max. 1.2 V_{p-p}	

Time data

Fall time	t_f = max. 1.5 μs	See point 3 *
Pulse duration	t_p = min. 2 μs	
Trigger gate setting time	t_{gs} = min. 29 μs	
Time delay between T- and S-signals	t_{ts} = min. 15 μs	See point 5 *

Base input (W-terminal)

Capacitance (wiring plus output of TG 13, TG 14 or TG 15) max. 80 pF

Note

The output capacitance of the trigger gates TG 13, TG 14 and TG 15 is max. 5 pF.

OUTPUT DATA (at V_P = 11.4 V and V_N = -12.6 V, unless specified differently)

The available output data of each flip-flop depend on the circuit configuration.

Reversible shift register

In excess of the internal load, represented by the circuit blocks, mounted on the printed-wiring board, the Q-outputs of each flip-flop in the shift register may furthermore be loaded as specified in the table on next page.

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* Section "Time definitions" of "Circuit blocks 10-Series".

flip-flop	FF 12-A		FF 12-B		FF 12-C		FF 12-D		FF 12-E	
output terminal	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
	6	5	3a	4a	17	17a	18	18a	21a	22a
available direct current: min. I_{QD} in mA	7.1	7.1	6	6	6	6	6	6	7.1	7.1
available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 μs: min. Q_{QT} in nC	25.8	25.8	24.6	24.6	24.6	24.6	24.6	24.6	25.8	25.8

For T_{amb} = min. −25 °C the available direct current I_{QD} has to be reduced with 1.6 mA and similarly the available transient charge Q_{QT} with 5 nC.

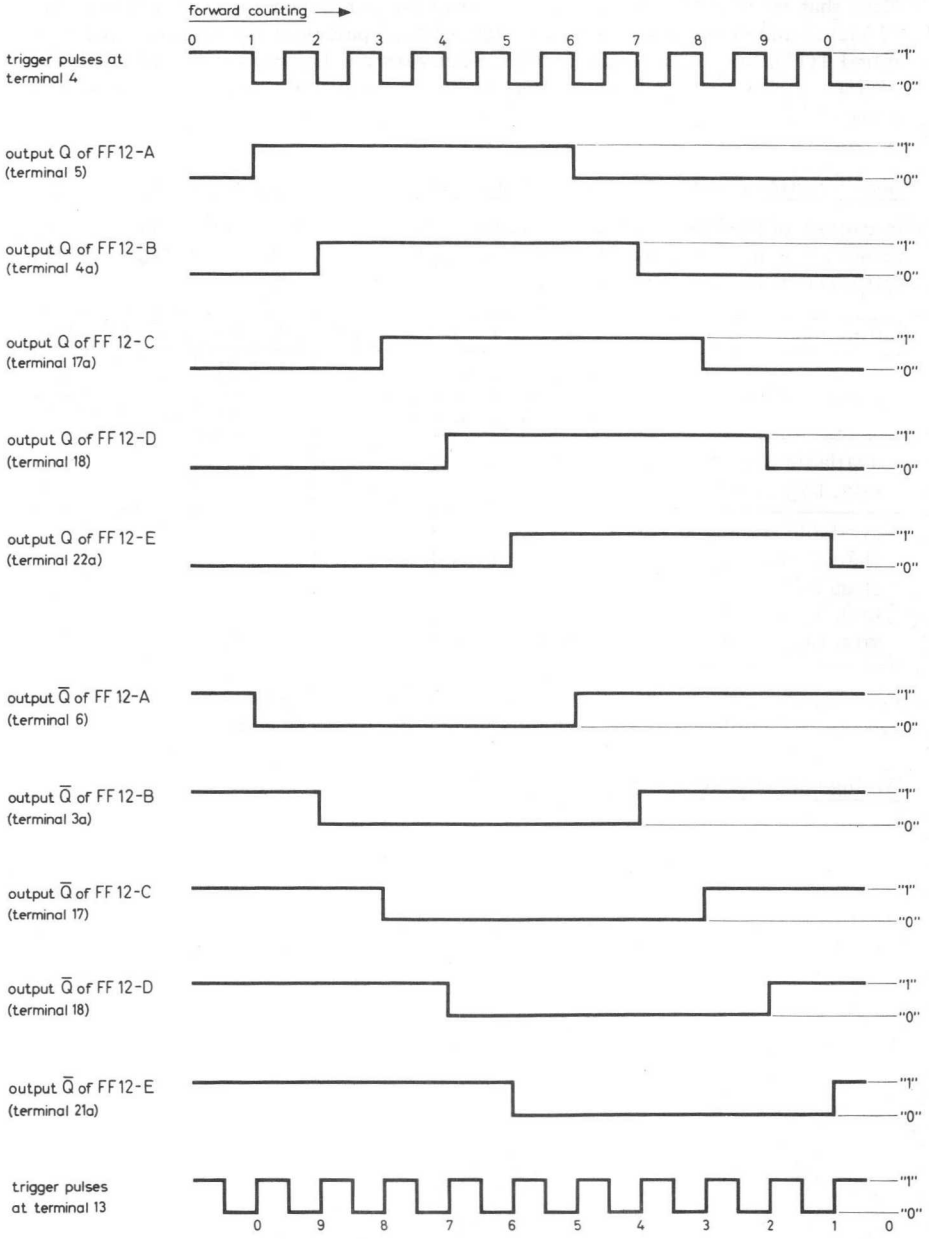
Reversible decade ring counter

In excess of the internal load (with feedback diodes on k_1, k_2, k_3 and k_4), represented by the circuit blocks mounted on the printed-wiring board, the Q-outputs of each flip-flop in the ring counter may furthermore be loaded as specified in the table below.

flip-flop	FF 12-A		FF 12-B		FF 12-C		FF 12-D		FF 12-E	
output terminal	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
	6	5	3a	4a	17	17a	18	18a	21a	22a
available direct current: min. I_{QD} in mA	6	6	4.9	4.9	6	6	4.9	4.9	6	6
available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 μs: min. Q_{QT} in nC	24.6	24.6	23.4	23.4	24.6	24.6	23.4	23.4	24.6	24.6

For T_{amb} = min. −25 °C the available direct current I_{QD} has to be reduced with 1.6 mA and similarly the available transient charge Q_{QT} with 5 nC.

Output levels of the flip-flops in a reversible decade ring counter configuration



7Z49975.1

Fig.3

Note that when a Q-output is at "0" level the corresponding $\overline{Q}$-output is at the "1" level and vice-versa. After 10 trigger (shift) pulses at the trigger input terminal 4 (13), the output terminal 22a (5) delivers one negative-going voltage step, whilst the ring counter has resumed its initial position, namely all Q-outputs being at "0" level.

One-directional shift register with additional inputs for parallel information shift

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board, the Q-outputs of each flip-flop in the shift register may furthermore be loaded as specified in the table below.

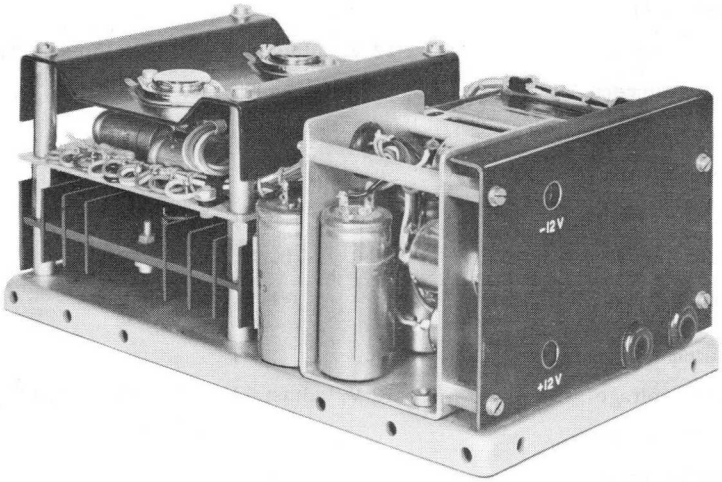
flip-flop	FF 12-A		FF 12-B		FF 12-C		FF 12-D		FF 12-E	
output terminal	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Q
	6	5	3a	4a	17	17a	18	18a	21a	22a
available direct current: min. I_{QD} in mA	7.1	7.1	7.1	7.1	7.1	7.1	7.1	7.1	8.2	8.2
available transient charge when V_Q changes from 2/3 V_P to 0.5 V in 1.5 μs: min. Q_{QT} in nC	25.8	25.8	25.8	25.8	25.8	25.8	25.8	25.8	27	27

For T_{amb} = min. −25 °C the available direct current I_{QD} has to be reduced with 1.6 mA and similarly the available transient charge Q_{QT} with 5 nC.

Wiring capacitance at each Q-output max. 150 pF

ACCESSORIES FOR CIRCUIT BLOCKS
10—SERIES

POWER SUPPLY UNIT



W 10143/B

Input voltage	105 V_{ac} to 120 V_{ac} and 200 V_{ac} to 240 V_{ac} in steps of 5 V
Output voltage	+12 V_{dc} and −12 V_{dc}

APPLICATION

This power supply unit has been designed for use with the circuit blocks of the 10-series. However it is also suitable as a supply for other transistorised circuits.

CONSTRUCTION

The unit is dimensioned for mounting in the 19" chassis 4322 026 38240.

The base plate of the unit functions as a side plate of this chassis, so that replacement of the side plate is made when the unit is mounted in the chassis. The power supply unit occupies the same space as five printed-wiring boards.

Dimensions	214 x 123 x 91	mm
Weight	2.1	kg

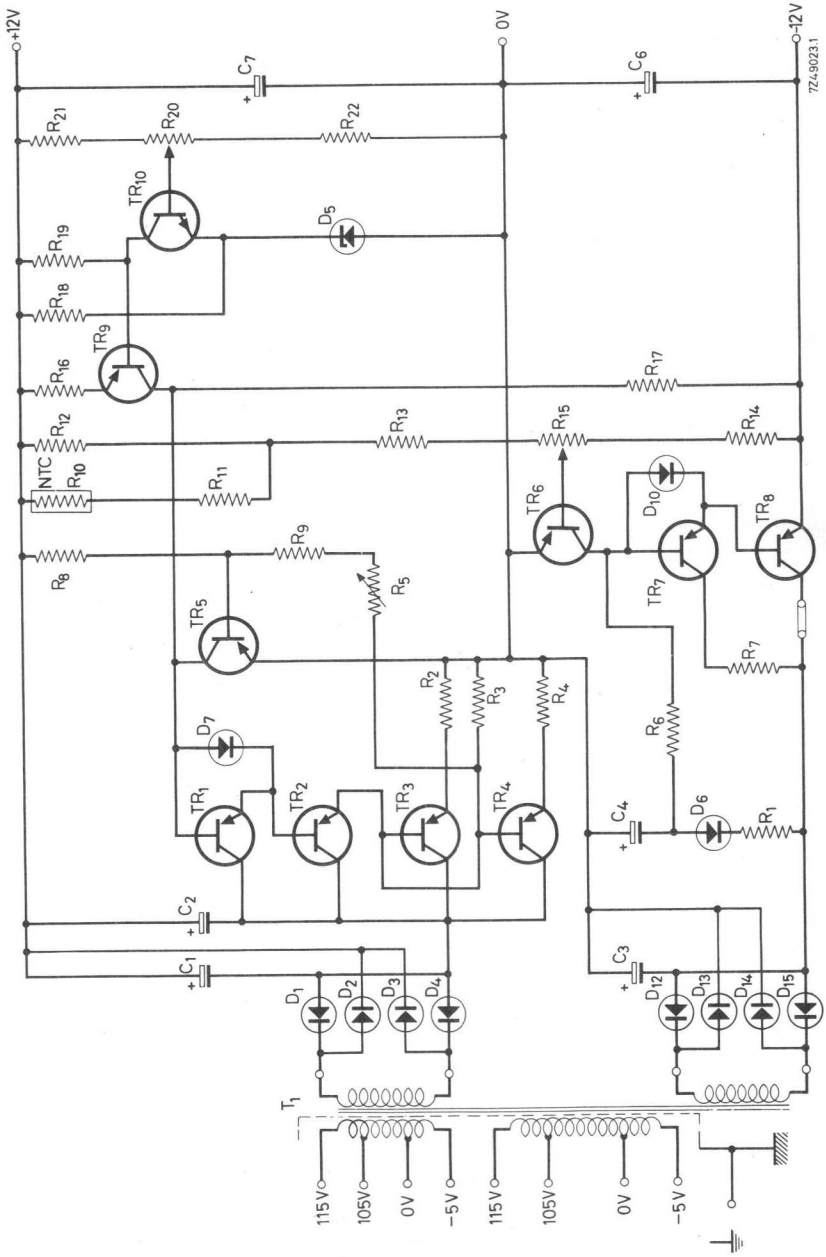
TECHNICAL PERFORMANCE

Input voltage	105 to 120 V_{ac}, 200 to 240 V_{ac} in steps of 5 V	
Frequency	45 to 65 Hz	
-12 V output [1])		
Output voltage	-12 V, adjustable ±10 % (R15, see diagram)	
Output current	400	mA
Stability ratio at 220 V	350:1	
Ripple voltage	5	mV_{rms}
Output resistance	0.4	Ω
Output impedance at 10 kHz	0.15	Ω
Temperature coefficient	-1.2	mV/deg C
+12 V output [1])		
Output voltage	12 V, adjustable ±10 % (R20, see diagram)	
Output current	1000	mA
Stability ratio at 220 V	1000:1	
Ripple voltage	2	mV_{rms}
Output resistance	0.08	Ω
Output impedance at 10 kHz	0.1	Ω
Temperature coefficient	+1.2	mV/deg C
Fusing	automatic	
Operating-temperature range	-20 to +55	°C
Storage-temperature range	-20 to +75	°C

In systems requiring more than one power supply unit, the earth tags (marked "0 V") may be interconnected, the positive tags (marked "+12 V") and the negative tags (marked "--12 V") must remain strictly separated.

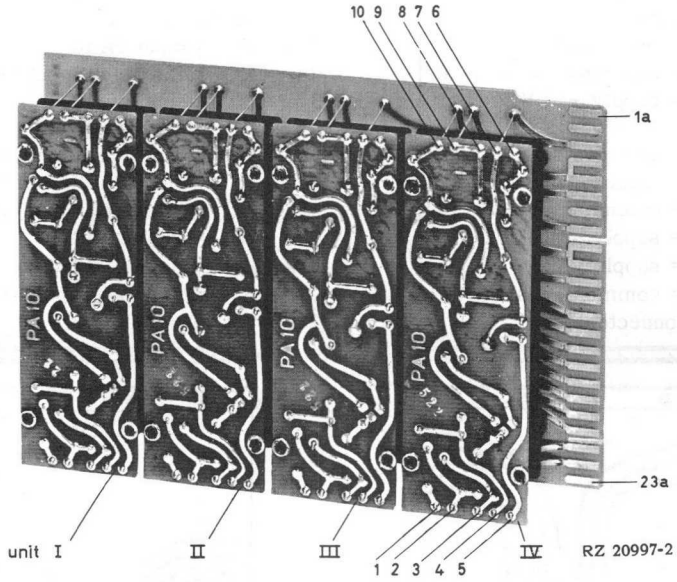
When a system is put into operation for the first time, the output voltages of the power supply units have to be adjusted to 12 V under nominal system load.

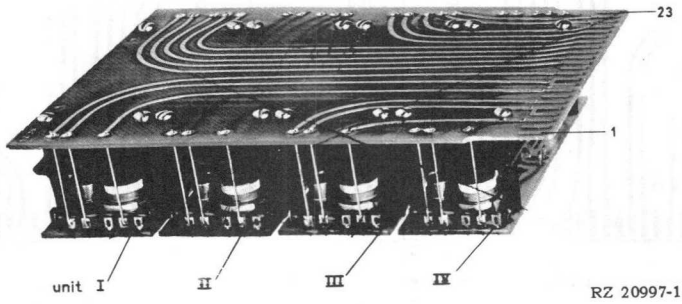
1) All values are given for full load.


+12V
0V
-12V
7Z49023.1
C7
C6
R21
R20
R22
TR10
D5
R19
R18
TR9
R16
R17
R12
R13
R15
R14
NTC
R10
R11
TR6
D10
TR8
R8
R9
R5
TR7
TR5
R7
R2
R3
R4
D7
R6
TR1
TR2
TR3
TR4
C4
D6
R1
C2
C1
C3
D1
D2
D3
D4
D12
D13
D14
D15
T1
115V
105V
0V
-5V
115V
105V
0V
-5V

PRINTED—WIRING BOARD FOR FOUR UNITS PA 10

This printed-wiring board fits the mounting chassis 4322 026 38240. It can be used directly with the aid of the mating connector with double sided contacts 2422 020 52591. On this board up to four PA 10's can be mounted, the next position in the chassis being left empty.

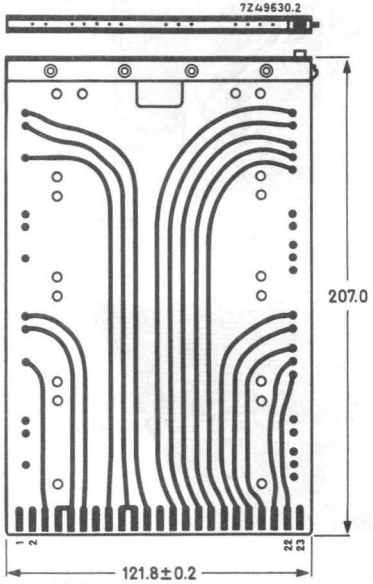


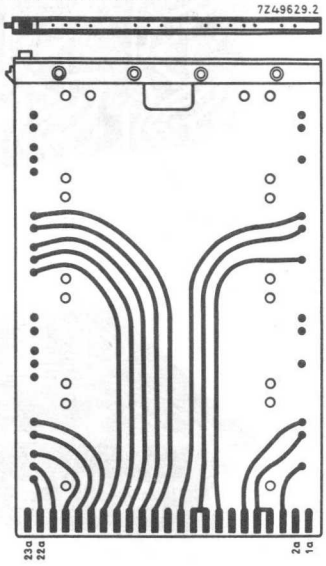


Terminal location:

1 = not connected		
2 = not connected		
3 = E_2 = common supply 0 V		
4 = N_2	= supply max. 55 V	unit nr. III
5 = $N_2 1$		
6 = Q = output PA 10		
7 = not connected		
8 = E_2 = common supply 0 V		
9 = N_2	= supply max. 55 V	unit nr. I
10 = $N_2 1$		
11 = Q = output PA 10		
12 = not connected		
13 = G = input PA 10		
14 = EG = extension input PA 10		unit nr. I
15 = N_1 = supply −12 V		
16 = P = supply +12 V		
17 = E_1 = common supply 0 V		
18 = G = input PA 10		
19 = EG = extension input PA 10		unit nr. III
20 = N_1 = supply −12 V		
21 = P = supply +12 V		
22 = E_1 = common supply 0 V		
23 = not connected		

1a = not connected		
2a = not connected		
3a = E_2 = common supply 0 V		
4a = N_2	= supply max. 55 V	unit nr. IV
5a = $N_2 1$		
6a = Q = output PA 10		
7a = not connected		
8a = E_2 = common supply 0 V		
9a = N_2	= supply max. 55 V	unit nr. II
10a = $N_2 1$		
11a = Q = output PA 10		
12a = not connected		
13a = G = input PA 10		
14a = EG = extension input PA 10		unit nr. II
15a = N_1 = supply −12 V		
16a = P = supply +12 V		
17a = E_1 = common supply 0 V		
18a = G = input PA 10		
19a = EG = extension input PA 10		unit nr. IV
20a = N_1 = supply −12 V		
21a = P = supply +12 V		
22a = E_1 = common supply 0 V		
23a = not connected		



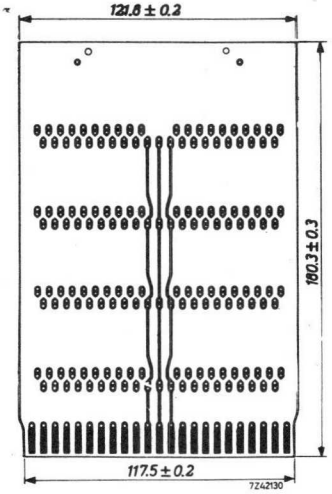


Material glass expoxy

Contacts 2x23, gold plated, pitch 0.2 inch

PRINTED—WIRING BOARD

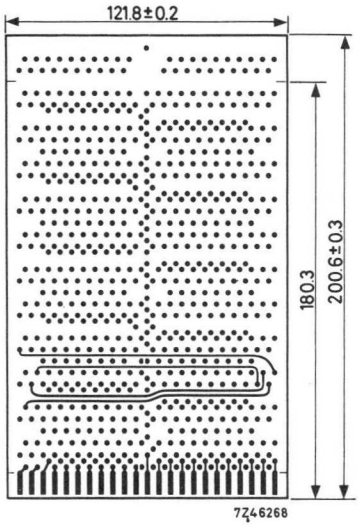
This printed-wiring board for 10-Series circuit blocks fits the mounting chassis 4322 026 38240.

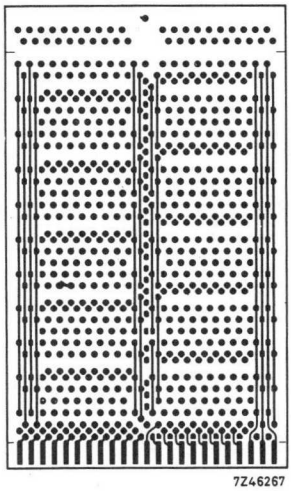


Material	copper-clad phenolic resin bonded paper with plated-through holes
Hole diameter	1.2 mm
Contacts	1 x 23, gold plated, pitch 0.2 inch

EXPERIMENTERS' PRINTED—WIRING BOARD

This experimenters' printed-wiring board for 10-Series circuit blocks can accommodate a maximum of 10 blocks (low cases) or 8 blocks (high cases) mounted horizontally.
The board fits the mounting chassis 4322 026 38240.

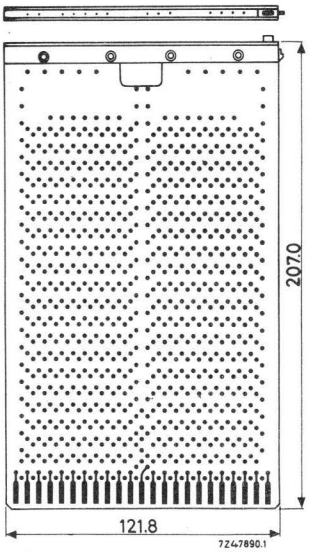


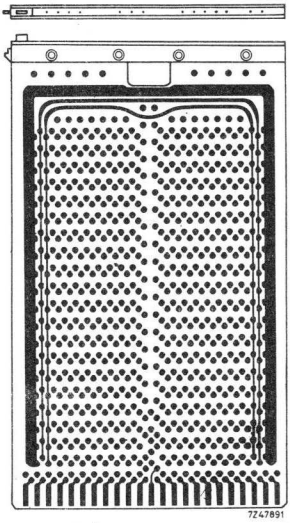


Material	phenolic resin bonded paper with plated-through holes
Hole diameter	1.2 mm
Contacts	2x23, gold plated, pitch 0.2 inch

EXPERIMENTERS' PRINTED—WIRING BOARDS

These experimenters' printed-wiring boards (with extractor) for 10-Series circuit blocks can accommodate a maximum of 20 blocks mounted vertically or 6 to 12 blocks mounted horizontally at most (depending on how many of these are high and how many are low). The boards fit the mounting chassis 4322 026 38240.

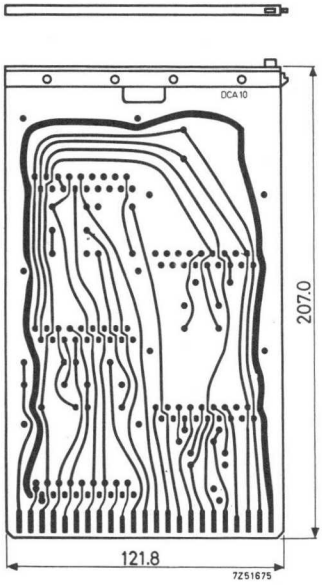


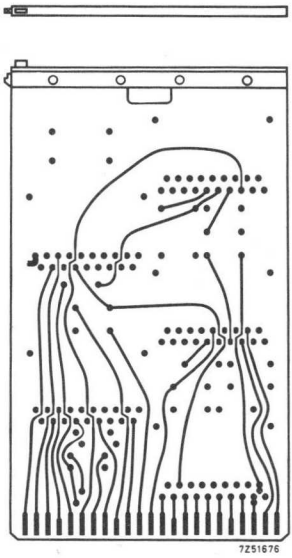


Catalogue number	4322 026 38600	4322 026 38610
Material	glass epoxy	phenolic resin bonded paper
Holes	plated-through; 1.2 mm diameter	
Contacts	2 x 23, gold plated, pitch 0.2 inch	

PRINTED-WIRING BOARD OF DCA 10

This printed-wiring board (with extractor) of the assembly DCA 10 fits the mounting chassis 4322 026 38240.

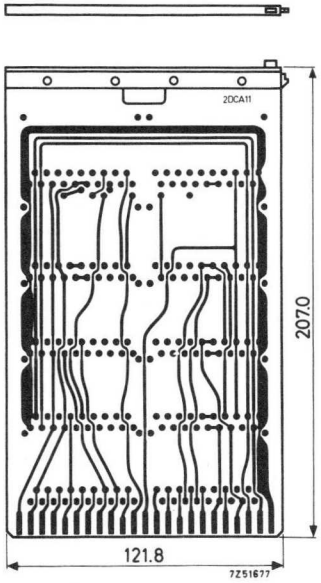


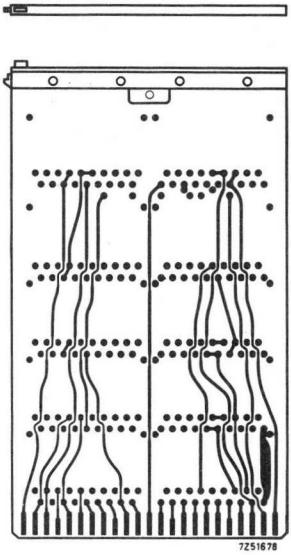


Material	glass epoxy with plated-through holes
Contacts	2 x 23, gold plated, pitch 0.2 inch

PRINTED-WIRING BOARD OF 2.DCA 11

This printed-wiring board (with extractor) of the assembly 2.DCA 11 fits the mounting chassis 4322 026 38240.

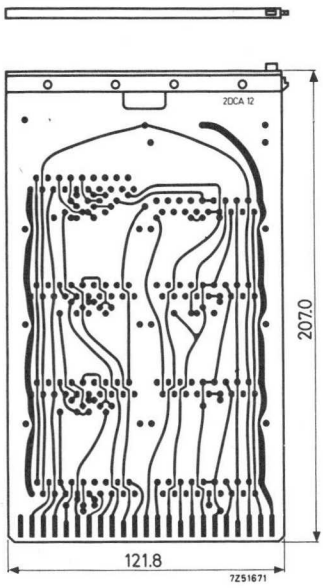


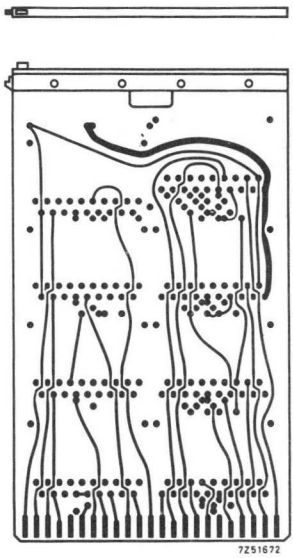


Material	glass epoxy with plated-through holes
Contacts	2 x 23, gold plated, pitch 0.2 inch

PRINTED-WIRING BOARD OF 2.DCA 12

This printed-wiring board (with extractor) of the assembly 2.DCA 12 fits the mounting chassis 4322 026 38240.

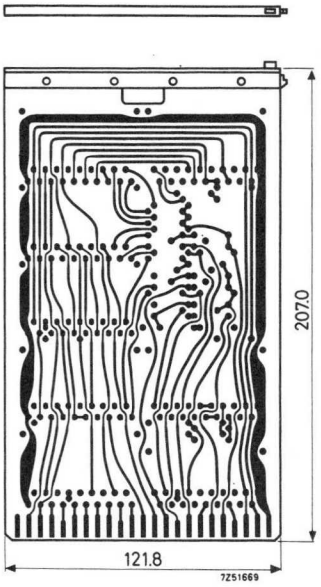


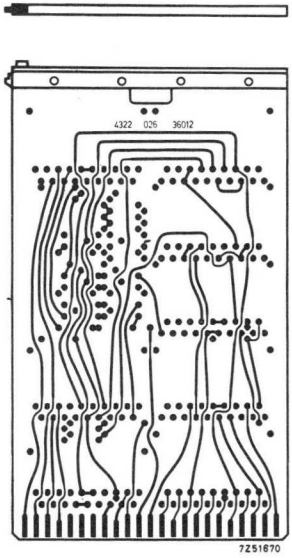


Material	glass epoxy with plated-through holes
Contacts	2 x 23, gold plated, pitch 0.2 inch

PRINTED-WIRING BOARD OF BCA 10

This printed-wiring board (with extractor) of the assembly BCA 10 fits the mounting chassis 4322 026 38240.

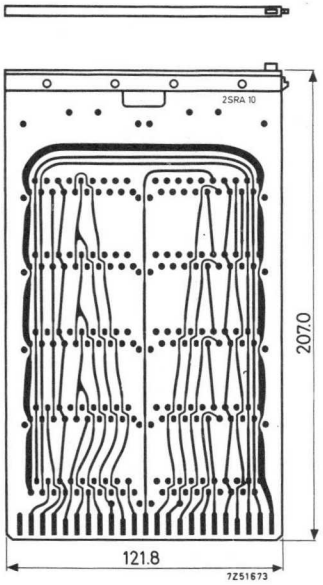


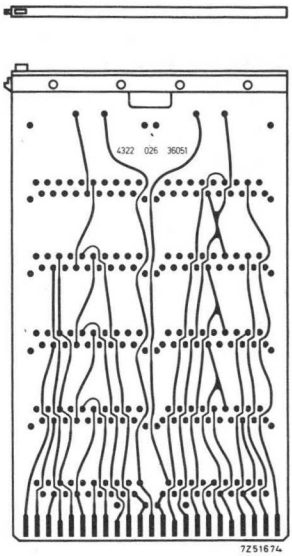


Material	glass epoxy with plated-through holes
Contacts	2 x 23, gold plated, pitch 0.2 inch

PRINTED-WIRING BOARD OF 2.SRA 10

This printed-wiring board (with extractor) of the assembly 2.SRA 10 fits the mounting chassis 4322 026 38240.

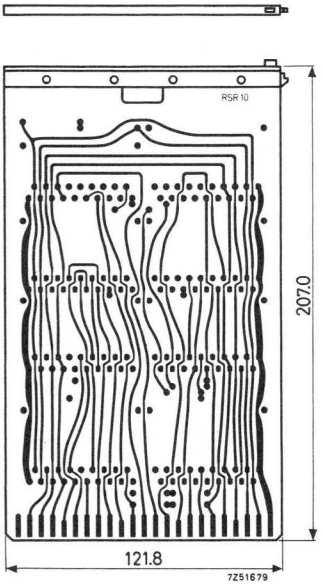


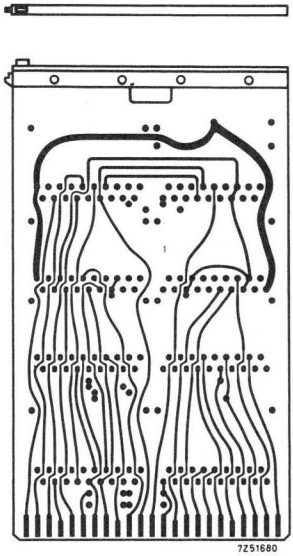


Material	glass epoxy with plated-through holes
Contacts	2 x 23, gold plated, pitch 0.2 inch

PRINTED-WIRING BOARD OF RSR 10

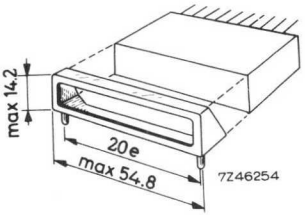
This printed-wiring board (with extractor) of the assembly RSR 10 fits the mounting chassis 4322 026 38240.





Material	glass epoxy with plated-through holes
Contacts	2 x 23, gold plated, pitch 0.2 inch

LOCKING CAP



For better securing 10-Series and 20-Series circuit blocks mounted parallel to a printed-wiring board (horizontal mounting), window-shaped locking caps are available. They fit the top of a circuit block.
The locking caps are provided with two holes and recesses to lodge two soldering tags, with which the caps can be secured to the board.

description	catalog number
locking cap	4322 026 32150
soldering tag	4322 026 32140

STICKERS

These are drawing symbols of circuit blocks printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings. The drawing symbols are as shown on the data sheets of the relevant circuit blocks.
The stickers are available in rolls, each containing 1000 drawing symbols of the same type of circuit block. Each sticker can be separately detached from the roll, without cutting.

for circuit block of type	catalog number of a roll with 1000 stickers
FF 10	4322 026 07610
FF 11	4322 026 07620
FF 12	4322 026 07630
2.GI 10	4322 026 07640
2.GI 11	4322 026 07650
2.GI 12	4322 026 07660
2.TG 13	4322 026 30560
2.TG 14	4322 026 30570
4.TG 15	4322 026 34630
PS 10	4322 026 07700
OS 10	4322 026 07710
OS 11	4322 026 36900
PD 10	4322 026 07720
PD 11	4322 026 36910
GA 11	4322 026 34640
TU 10	4322 026 07741
PA 10	4322 026 07751
RD 10	4322 026 07771
RD 11	4322 026 36990
ID 10	4322 026 36850

Circuit blocks

20-Series

INTRODUCTION

The "20-series" presents a range of circuit blocks, developed to meet the requirements of the Industry for data logging and processing, medium and high speed computers, measuring test apparatus, process and machine control, general industrial instrumentation.
With this "20-series" systems are designed and built quickly, economically and with the utmost reliability.

The "20-series" offers a complete range, consisting of various logic elements together with all necessary auxiliary units including one-shot multivibrator, pulse shaper, line driver, line receiver, etc.

Moreover, all accessories for a quick and easy construction of equipment will be made available e.g. mounting chassis, power supply, printed-wiring boards, connectors, etc.

Types of circuit blocks

In this series the following types of circuit blocks are available:

description	abbreviation	catalog number	page
Dual NAND/NOR Gate	2.GI20	2722 005 08001	E13
Dual NAND/NOR Gate	2.GI21	2722 005 08011	E17
Dual NAND/NOR Gate with high loadability	2.GI22	2722 005 08021	E21
Set-reset Flip-Flop	FF20	2722 005 00001	E25
Triggered Flip-Flop	FF22	2722 005 00011	E27
Triggered Flip-Flop	FF23	2722 005 00021	E31
Dual Trigger Gate	2.TG23	2722 005 15001	E35
One-shot Multivibrator	OS20	2722 005 10001	E37
Pulse Shaper	PS20	2722 005 11001	E41
Dual Line Driver	2.LD21	2722 005 21001	E45
Dual Line Receiver	2.LR22	2722 005 19011	E51
Pulse Driver	PD21	2722 005 13001	E55

A number of static input and output devices can be used in conjunction with 20-series circuit blocks, see chapter "INPUT/OUTPUT DEVICES".

Economic equipment design and construction are inherent to the following features:

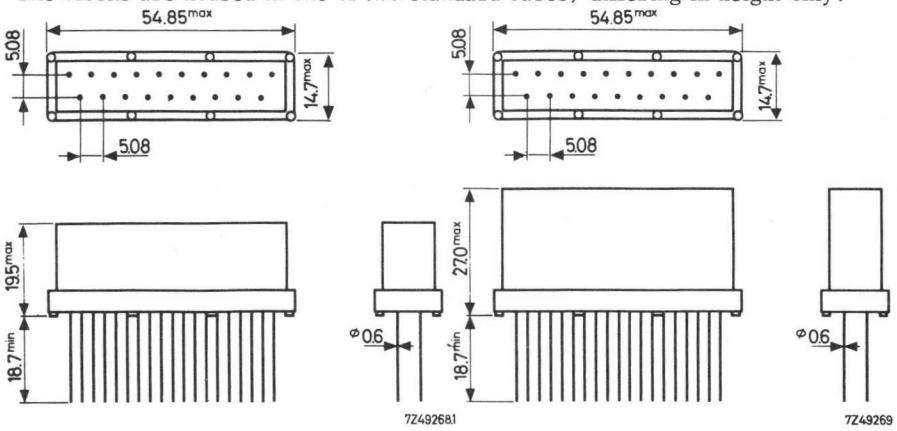
- all circuits are compatable with little circuit diversity permitting simple and direct interconnections of the blocks within the range
- high "fan-out" figures and built-in logic facilities reduce the total number of blocks in a system considerably. They also facilitate later additions and modifications
- easy to use loading table enables the system design to be completed quickly
- the possibility of extending gate-, trigger-, and set-inputs makes the circuit blocks particularly valuable, where flexibility in equipment design is required
- input and output currents of the blocks are designed in a way that external components are unnecessary. Only for extension of the number of inputs diodes have to be mounted externally
- the uniformity of terminal configuration reduces the time for interwiring the blocks and facilitates the design of printed-wiring boards.

Outstanding reliability has been secured by:

- "worst-case" design of all circuits, where calculations have been performed with end-of-life data of all components
- use of professional silicium semi-conductors only
- careful testing and inspection of individual components and assemblies before, during and after manufacture
- quality control on running factory production, which ensures a product of equal and high quality
- built-in thresholds against interference
- printed-wiring circuits with plated through holes, the encapsulation and sealing techniques give the circuit block virtual immunity from the effects of humudity, vibration and shock.

CONSTRUCTION

The blocks are housed in one of two standard cases, differing in height only.



Low standard case
Weight: approximately 30 g

High standard case
Weight: approximately 40 g

Both cases have 19 terminals, protruding the bottom side in two rows.
The distance between the two rows of terminals is 5.08 mm ± 0.1 (0.2") and the distance between the terminals in one row is 5.08 mm ± 0.1 (0.2"), in accordance with the I.E.C. standard hole grid for printed-wiring boards. The blocks can be mounted in any position.
The terminal side of the metal cans is covered by a plastic sleeve for electrical insulation from printed-wiring conductors both when the blocks are mounted horizontally and vertically.
A horizontally mounted block can be mechanically secured to the printed-wiring board at the topside with a locking cap catalogue number 4322 026 32150. The locking cap is provided with two holes and recesses to lodge two soldering tags, catalogue number 4322 026 32140 with which the cap can be secured to the board. (See for more information section "ACCESSORIES FOR CIRCUIT BLOCKS 20-SERIES".)

CHARACTERISTICS

Ambient temperature limits

Storage	T_{amb} = −55 °C to +85 °C
Operating	T_{amb} = −25 °C to +85 °C

Below 0 °C operation is possible with reduced output data; derating figures may be derived from the data given for each type by linear interpolation.
The maximum operating temperature is checked most unambiguously by using the maximum case temperature given for each type.

Supply voltages

terminal		operating	under external fault conditions (max. 24 hours)
19	V_{P_1}	+12 V ± 5 %	max. +18 V
18	V_{P_2}	+ 6 V ±10 %	max. + 9 V
10	V_0	0 V	0 V
9	V_N	−12 V ± 5 %	max. −18 V

Signal levels

	operating	limiting values	
		diode inputs	outputs
Positive level	V_{P_2}	20 V	15 V
0 V level	0 V to +0.5 V	−4 V	0 V

Triggering edge

The negative-going transient (from positive level to 0 V level) is the triggering edge. A maximum duration is given for part of this edge.
This requirement is (unless specified otherwise):

from 0.35 V_{P_1} to 0.5 V in maximum 50 ns.

Currents and transient charges

All currents apply to the 0 V level, all transient charges to the negative-going transient (unless specified otherwise).
Transient charges apply to the maximum allowable triggering edge (see above).
It should be verified that the sum of the required d.c. input currents of driven units does not exceed the available d.c. output current of the driving unit.

Only when one or more trigger inputs T are driven, the transient charges must also be checked.
T-inputs of closed gates do not require any current or charge.
The currents and transient charges are end-of-life values. They permit a verification which guarantees reliable operation within the specified limits of temperature and supply voltages.
The positive level and the positive-going transient need not to be verified.

Wiring capacitance at the outputs

When the maximum wiring capacitance at an output is exceeded, an external collector resistor must be added, giving a time constant of 85 ns with the excess wiring capacitance.
The wiring capacitance C_W consumes a charge of 3.5 pC/pF.

Delays

Delays are measured between 0.5 V points on negative-going transients, if necessary over two stages.

TEST SPECIFICATIONS

Before and during manufacture samples of circuit blocks are regularly subjected to the following tests:

1. Vibration test according to method 201A of MIL-STD-202.
   Frequency 10-55 Hz, amplitude 0.76 mm.
2. Shock test according to method 202A of MIL-STD-202.
   Acceleration 50 g in 3 perpendicular directions.
3. Temperature-cycling test according to method 102A of MIL-STD-202.
   Condition D, 5 cycles from −55 °C to +100 °C.
4. Accelerated humidity test according to method 106A of MIL-STD-202.
   10 cycles as indicated in Fig.1, page 2 of method 106A.
5. Long-term humidity test according to I.E.C.68, C IV. Units not operating. Duration 56 days at 40 °C and relative humidity 95 %. Measurements after 7, 14, 28 and 56 days.
6. As item 5, but units operating under the most unfavourable electrical conditions regarding supply voltages, output load and input characteristics.
7. Long-term test at maximum temperature according to method 108 of MIL-STD-202.
   Test condition E, 85 °C during 1500 hours.
   Units operating under the most unfavourable electrical conditions.
   Measurements after 250, 500, 1000 and 1500 hours.
8. Terminals tested on strength, tests on mounting, soldering, lacquer and coding.

INPUT AND OUTPUT DATA

INPUT DATA

unit	terminal	note	d.c. current (mA)	transient charge (pC)
FF20	S		2	160
FF22	G		2	200
	T		4	300
	S_1		0.8	60
FF23, TG23	G		2	100
	T	gate open	2	290
FF23	S		5	360
GI 20, GI 21	G		2	150
GI 22	G		2	150
OS20	G		2	100
	T	gate open	2	240
PD21	G		3.5	180
	T	gate open	3.5	360
LD21	G		2	150

OUTPUT DATA

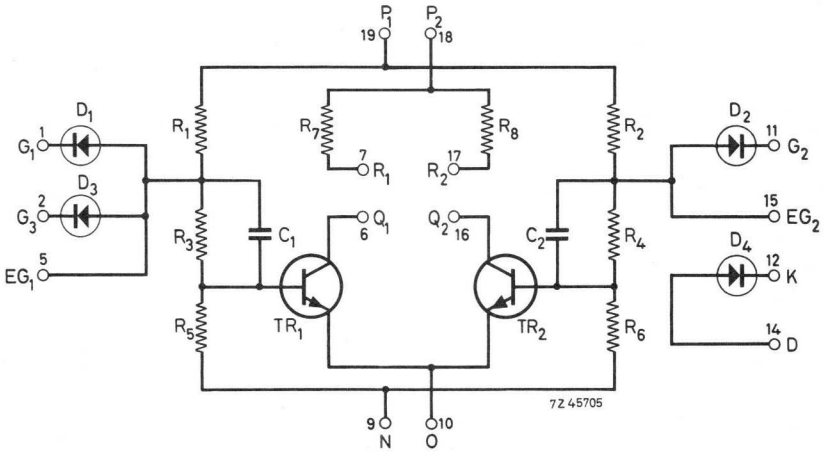
unit	terminal	note	d.c. current (mA)	transient charge (pC)
FF20	Q		17	645
FF22	Q		55	2300
FF23	Q		14	1400
GI 20, GI 21	Q		15	540
GI 22	Q		32	3600
OS20	Q_1		14	1500
	Q_2		15	1500
LR22	Q		15	540
PS20	Q		20	600
PD21	Q		90	7500

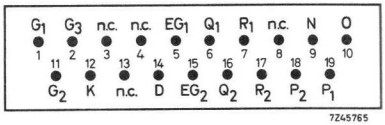
Loading Rules

1. Verify that the sum of the required d.c. input currents of the driven units does not exceed the available d.c. output current of the driving unit.
2. When however T-inputs are incorporated in the driven units, the transient charges must also be verified.
3. The wiring capacitance consumes an extra charge of 3.5 pC/pF.
4. T-inputs of closed gates do not require any current or charge (except of FF22).
5. The verifications mentioned above warrants reliable operation at the worst combination of supply voltage tolerances and ambient temperatures between 0 °C and +85 °C. For operation at temperatures until -25 °C the data for each type are given in the individual data sheets under "OUTPUT DATA".

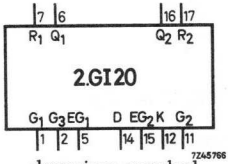
DUAL GATE INVERTER

Function	dual NAND (positive logic), or dual NOR (negative logic)
Case	low standard case





terminal location



drawing symbol

The separate diodes can be used to increase the number of gate inputs of any of the two circuits at the gate extender input EG.

Together with the inputs G they form an AND function on the positive level. When all inputs are at the positive level the corresponding output Q resumes the 0 V level. Application of the 0 V level to one of the inputs G causes the corresponding output Q to attain the positive level.

Any output Q is to be connected to a collector resistor R. A logic function can be obtained by interconnecting two or more outputs Q; in this case only one col-

lector resistor is usually needed and the others are left disconnected. For n interconnected outputs (n - 1) times the output capacitance should be added to the wiring capacitance.
This technique is not recommended when the proper operation of the following circuits will be disturbed by the erratic positive-going output pulses that may be produced.

Logic table

G_1	G_3	Q_1
high	high	low
low	high	high
high	low	high
low	low	high

Case temperature	T_C	max.	100	°C

Power supply currents, nominal (one transistor ON, one transistor OFF)

I_{P_1}		5.0	mA
I_{P_2}		6.0	mA
I_N		1.6	mA

INPUT DATA

Gate inputs G	$-I_G$	max.	2	mA
	$-Q_G$	max.	150	pC

Gate extender inputs EG

Diodes BAY38 may be used to increase the number of gate inputs.
Capacitance (wiring plus diodes) C = max. 10 pF. When this figure is exceeded, connect a resistor between terminal EG and the supply voltage V_{P_2} giving a time constant of 85 ns with the total capacitance.

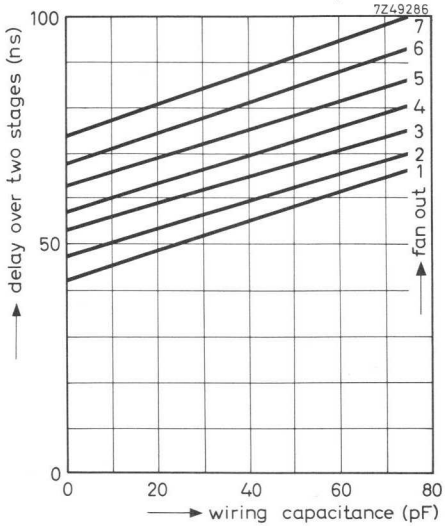
OUTPUT DATA

Output Q

T_{amb} = min. 0 °C	I_Q	min.	15	mA
	Q_Q	min.	540	pC
T_{amb} = min. -25 °C	I_Q	min.	11.5	mA
	Q_Q	min.	380	pC
Output capacitance	C_Q	max.	13	pF
Wiring capacitance at output Q	C_w	max.	75	pF

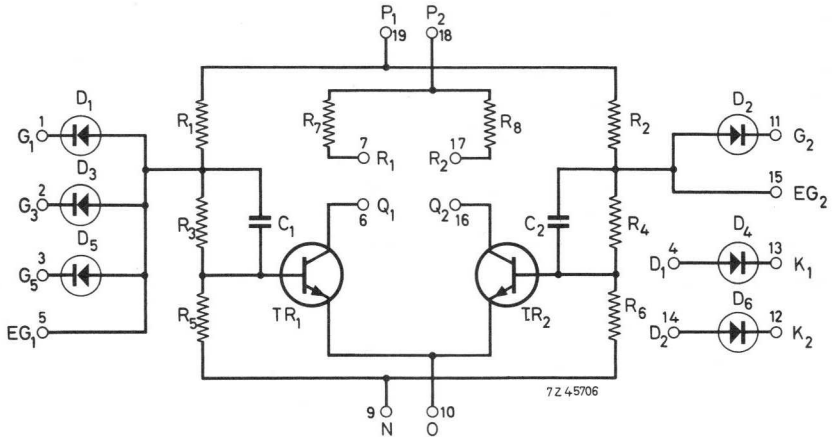
Time Data

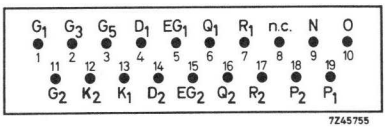
Time between successive output signal changes	t_{recov}	min. 110	ns
Delay over two stages, loaded with 7 GI 20/GI 21 + 75 pF	t_d	typ. 100	ns
		max. 145	ns



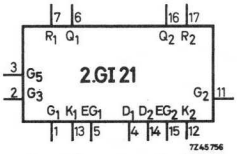
DUAL GATE INVERTER

Function	dual NAND (positive logic), or dual NOR (negative logic)
Case	low standard case





terminal location



drawing symbol

The separate diodes can be used to increase the number of gate inputs of any of the two circuits at the gate extender input EG.

Together with the inputs G they form an AND function on the positive level. When all inputs are at the positive level the corresponding output Q resumes the 0 V level. Application of the 0 V level to one of the inputs G causes the corresponding output Q to attain the positive level.

Any output Q is to be connected to a collector resistor R. A logic function can be obtained by interconnecting two or more outputs Q; in this case only one col-

lector resistor is usually needed and the others are left disconnected. For n interconnected outputs (n - 1) times the output capacitance should be added to the wiring capacitance.
This technique is not recommended when the proper operation of the following circuits will be disturbed by the erratic positive-going output pulses that may be produced.

Logic table

G_1	G_3	G_5	Q_1
high	high	high	low
low	high	high	high
high	low	high	high
low	low	high	high
high	high	low	high
low	high	low	high
high	low	low	high
low	low	low	high

Case temperature T_C max. 100 °C

Power supply currents, nominal (one transistor ON, one transistor OFF)

I_{P_1} 5.0 mA
I_{P_2} 6.0 mA
I_N 1.6 mA

INPUT DATA

Gate inputs G

$-I_G$ max. 2 mA
$-Q_G$ max. 150 pC

Gate extender inputs EG

Diodes BAY38 may be used to increase the number of gate inputs.
Capacitance (wiring plus diodes) C = max. 10 pF. When this figure is exceeded, connect a resistor between terminal EG and the supply voltage V_{P_2} giving a time constant of 85 ns with the total capacitance.

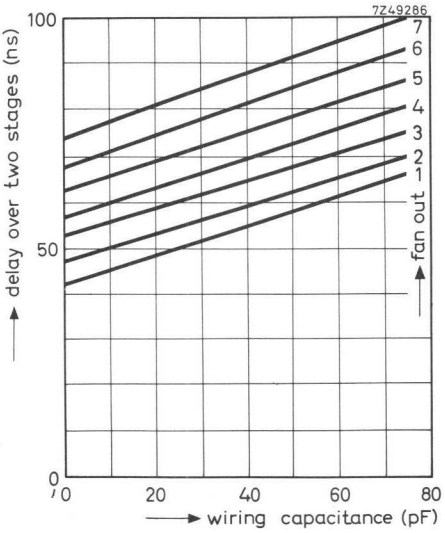
OUTPUT DATA

Output Q

T_{amb} = min. 0 °C	I_Q	min.	15	mA
	Q_Q	min.	540	pC
T_{amb} = min. −25 °C	I_Q	min.	11.5	mA
	Q_Q	min.	380	pC
Output capacitance	C_Q	max.	13	pF
Wiring capacitance at output Q	C_W	max.	75	pF

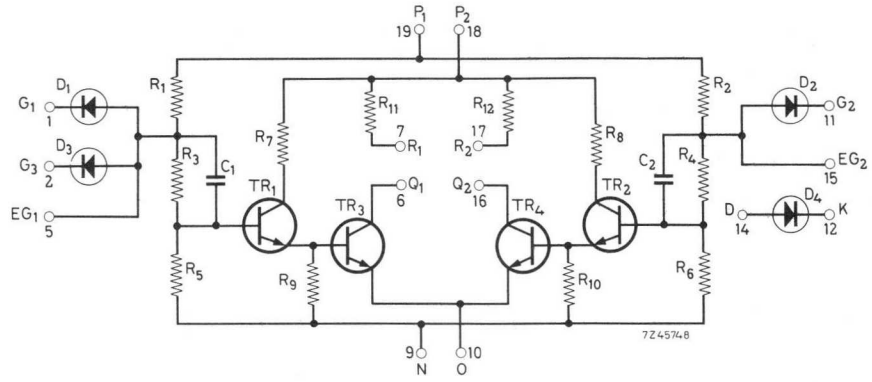
Time Data

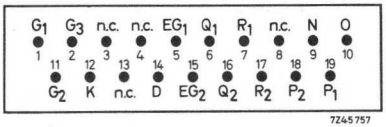
Time between successive output signal changes	t_{recov}	min.	110	ns
Delay over two stages, loaded with 7 GI 20/GI 21 + 75 pF	t_d	typ.	100	ns
		max.	145	ns



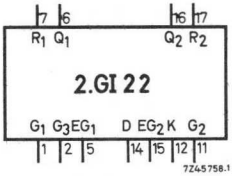
DUAL GATE INVERTER

Function	dual NAND (positive logic), or dual NOR (negative logic) with high loadibility
Case	low standard case





terminal location



drawing symbol

The unit contains two gate inverters with a high loadibility.
The separate diode can be used to increase the number of gate inputs of any of the two circuits at the gate extender input EG.
Together with the inputs G they form an AND function on the positive level. When all inputs are at the positive level the corresponding output Q resumes the 0 V level. Application of the 0 V level to one of the inputs G causes the corresponding output Q to attain the positive level.
Any output Q is to be connected to a collector resistor R. A logic function can be obtained by interconnecting two or more outputs Q; in this case only one collector resistor is usually needed and the others are left disconnected. For n interconnected outputs (n - 1) times the output capacitance should be added to

the wiring capacitance.
This technique is not recommended when the proper operation of the following circuits will be disturbed by the erratic positive-going output pulses that may be produced.

Logic table

G_1	G_3	Q_1
high	high	low
low	high	high
high	low	high
low	low	high

Case temperature T_C max. 100 °C

Power supply currents, nominal (one output low, one output high)

I_{P_1} 4.2 mA
I_{P_2} 35 mA
I_N 5.5 mA

INPUT DATA

Gate inputs G

$-I_G$ max. 2 mA
$-Q_G$ max. 150 pC

Gate extender inputs EG

Diodes BAY38 may be used to increase the number of gate inputs.
Capacitance (wiring plus diodes) C = max. 10 pF. When this figure is exceeded, connect a resistor between terminal EG and the supply voltage V_{P_2} giving a time constant of 85 ns with the total capacitance.

OUTPUT DATA

Output Q

T_{amb} = min. 0 °C

I_Q min. 32 mA
Q_Q min. 3600 pC

T_{amb} = min. −25 °C

I_Q min. 32 mA
Q_Q min. 2900 pC

When terminals R and Q are not connected:

T_{amb} = min. 0 °C

I_Q min. 80 mA
at V_Q 0.6 V

T_{amb} = min. −25 °C

I_Q min. 32 mA
at V_Q 0.5 V

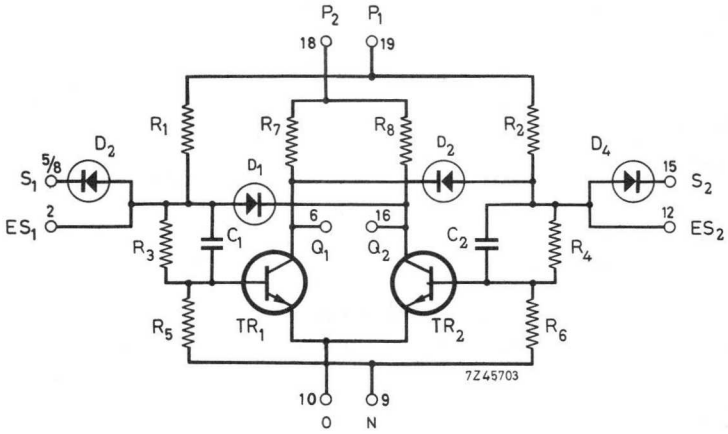
Output capacitance	C_Q	max. 13	pF
Wiring capacitance at output Q	C_w	max. 175	pF

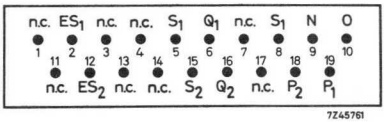
Time Data

Time between successive output signal changes	t_{recov}	min. 110	ns
Delay over two stages, loaded with			
8 x GI 20/GI 21 + 175 pF	t_d	typ. 80 max. 100	ns ns
16 x GI 20/GI 21 + 175 pF	t_d	typ. 100 max. 120	ns ns
Delay over one stage, loaded with 75 Ω line	t_d	max. 100	ns

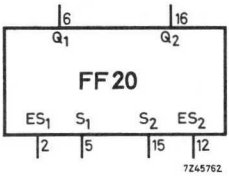
FLIP-FLOP

Function	flip-flop latch, for d.c. logic
Case	low standard case





terminal location



drawing symbol

Upon application of the 0 V level to one of the set inputs S, the corresponding output Q resumes the positive level and the other output the 0 V level.
The positive level applied to a set input is inoperative.
A logic function is obtained by connecting external diodes to a set extender input ES; the diodes form an OR function on the 0 V level.

Logic table

S_1	S_2	Q_1	Q_2
low	high	high	low
high	low	low	high
low	low	high	high
high	high	no change	

Case temperature	T_C	max. 100	°C
Power supply currents (nominal)	I_{P_1}	5	mA
	I_{P_2}	6	mA
	I_N	1.6	mA

INPUT DATA

Set inputs S	$-I_S$	max. 2	mA
	$-Q_S$	max. 160	pC

Set extender inputs ES

Diodes BAY38 may be used to increase the number of inputs. Capacitance (wiring plus diodes) max. 10 pF.

When this figure is exceeded, connect a resistor between terminal ES and the supply voltage V_{P_2} giving a time constant of 85 ns with the total capacitance.

OUTPUT DATA

Output Q

T_{amb} = min. 0 °C	I_Q	min. 17	mA
	Q_Q	min. 645	pC
T_{amb} = min. −25 °C	I_Q	min. 13	mA
	Q_Q	min. 460	pC
Wiring capacitance at each output Q	C_w	max. 75	pF

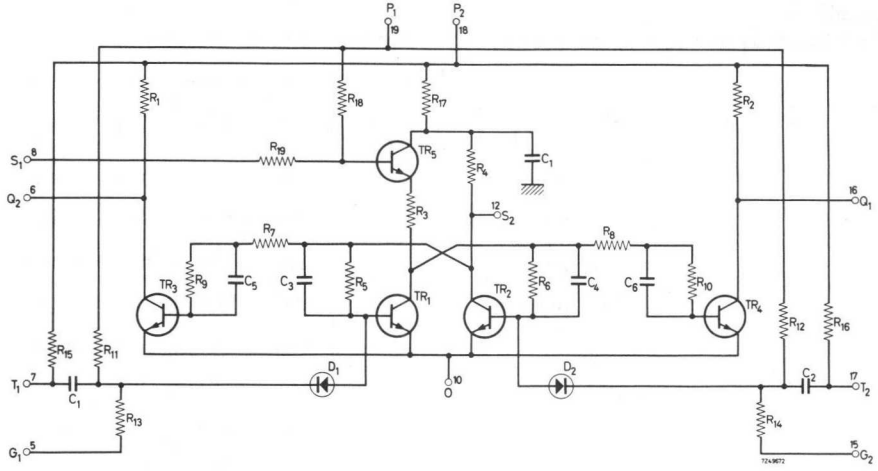
Time Data

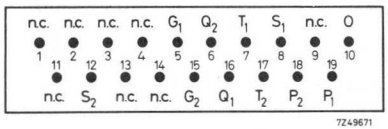
Time between successive output signal changes	t_{recov}	min. 125	ns
Set pulse duration (0 V level)	t_p	equal to delay	
Delay, loaded with 7 GI 20/GI 21 + 75 pF	t_d	typ. 110	ns
		max. 155	ns

FLIP-FLOP

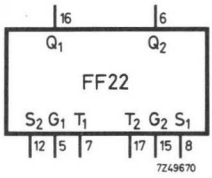
Function
Case

triggered flip-flop for high p.r.f.
high standard case





terminal location



drawing symbol

Trigger pulses are applied to trigger inputs T.
A negative-going pulse changes the state of the flip-flop.
A binary counter is made by connecting G_1 to Q_2 and G_2 to Q_1.
A shift register is made by connecting G_1 to Q_1 and G_2 to Q_2 of the preceding flip-flop.

Applied as binary counter or as shift register the trigger inputs T_1 and T_2 have to be connected.
Terminals G have to be connected directly to the outputs Q of other circuit blocks without using diodes.
A positive level at input G inhibits the trigger gate.
To obtain additional trigger inputs of inhibiting facilities external diodes can be connected to the trigger input T.

It must be noted that any negative-going signal at the input T acts as a trigger pulse if all other inputs T are at the positive level.
The FF22 can be set directly at the set input S_1.
In case multiple setting is required, the various set signals have to be applied via separating diodes to input S_1.
Terminal S_2 may be driven by a gate inverter of the 20-series without collector resistor. A diode between the output Q of the gate inverter and the set input S_2 is not permitted.
Both inputs S_1 and S_2 may be left floating, when setting is not required.

Logic table

Trigger pulse at T_1	Trigger pulse at T_2	S_1	S_2	G_1	G_2	Q_1	Q_2
present	present	-	-	high	low	high	low
present	present	-	-	low	high	low	high
present	present	-	-	low	low	indeterminate	
present	present	-	-	high	high	no change	
present	-	-	-	high	--	no change	
present	-	-	-	low	--	low	high
-	present	-	-	-	high	no change	
-	present	-	-	-	low	high	low
-	-	low	-	-	--	high	low
-	-	high	-	-	--	no change	
-	-	-	low	-	--	low	high
-	-	-	high	-	--	no change	

Case temperature	T_C	max. 100 °C
Power supply currents (nominal)	I_{P1}	1 mA
	I_{P2}	28 mA

INPUT DATA

Gate inputs G	$-I_G$	max. 2 mA
	$-Q_G$	max. 200 pC
Trigger inputs T		
corresponding input G at positive level	$-I_T$	max. 4 mA
	$-Q_T$	max. 300 pC
corresponding input G at 0V level	$-I_T$	max. 4 mA
	$-Q_T$	max. 250 pC

Wiring capacitance at each input T, when driven via a diode	C_w	max. 10 pF
Threshold at input T, when V_G is at 0V level	V_T	max. 0.5 V
Set input S_1	$-I_{S_1}$	max. 0.8 mA
	$-Q_{S_1}$	max. 60 pC

The maximum number of set diodes is 4.
Type of diodes: BAY 38, IN 4009, IN 3604 or equivalent type.

Set input S_2	V_{S_2}	max. 0.5 V
	$-I_{S_2}$	max. 9 mA
	$-Q_{S_2}$	max. 600 pC

OUTPUT DATA

Output Q		
T_{amb} = min. 0 °C	I_Q	min. 55 mA
	Q_Q	min. 2300 pC
T_{amb} = min. - 25 °C	I_Q	min. 40 mA
	Q_Q	min. 1500 pC
Wiring capacitance at each output Q	C_w	max. 75 pF

Time Data

Time that the trigger input T should be at the positive level and the signal level should be present at open input G	t_{prep}	min. $100 + 120 \frac{C_{WT}}{C_{WTmax}}$ ns *
Preparation time, when the input T is driven via a diode	t_{prep}	min. $350 + 120 \frac{C_{WT}}{C_{WTmax}}$ ns *
Preparation time, when the input T is driven via a diode and a resistor of 750 Ω is connected between terminal T and positive supply V_{P2}	t_{prep}	min. $175 + 120 \frac{C_{WT}}{C_{WTmax}}$ ns *
Triggering edge duration (from 0.35 V_{P1} to 0.5 V)	t_e	max. 60 ns
Triggering edge duration + trigger pulse duration (0 V level)	$t_e + t_p$	min. 140 ns
Set pulse duration (0 V level)	t_s	min. 70 ns
Delay, full load	t_d	max. 70 ns

Proper inhibiting is ensured, when $\frac{C_{WT}}{C_{WTmax}} > \frac{C_{WG}}{C_{WG\,max}}$ *

* See note on next page

Note:

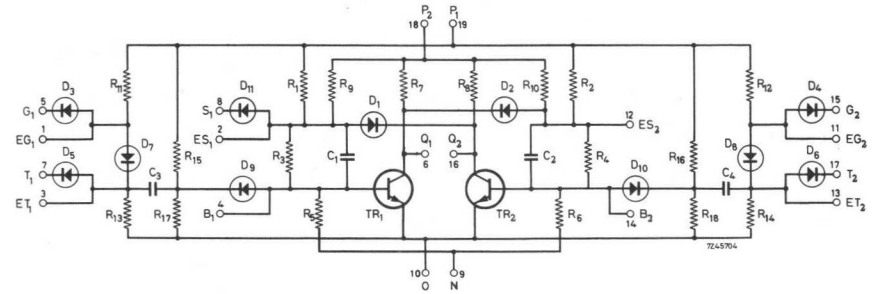
C_{WTmax} = maximum permissible wiring capacitance of the output of the driving unit at the input T.

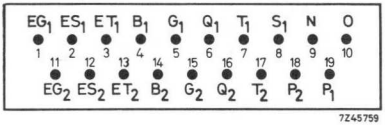
C_{WGmax} = maximum permissible wiring capacitance of the output of the driving unit at the input G.

If a non-standard circuit is used C_{WTmax} as well as C_{WGmax} is the maximum wiring capacitance giving a time constant of 85 ns.

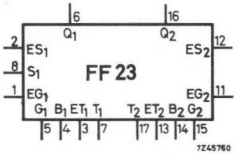
FLIP-FLOP

Function	general-purpose triggered flip-flop
Case	high standard case





terminal location



drawing symbol

Trigger pulses are applied to trigger inputs T.
The built-in trigger gates are opened by applying the positive level to the gate inputs G and are closed by applying the 0 V level.
A binary counter is made by connecting G_1 to Q_2, and G_2 to Q_1.

A shift register is made by connecting G_1 to Q_1, and G_2 to Q_2 of the preceding flip-flop.
Applied as binary counter or as shift register the trigger inputs T_1 and T_2 have to be connected.

A logic function is obtained by connecting external diodes to a gate extender input EG; together with the G input they form an AND function on the positive level, useful in binary-decimal counters, bidirectional shift registers with only one clock source, bidirectional counters, etc.

A dual trigger gate 2.TG23 may be connected to the base inputs B to obtain more triggering facilities (e.g. for bidirectional shift registers and counters).
To set or reset the flip-flop the set input S is taken to the 0 V level.
A logic function is obtained by connecting external diodes to a set extender input ES; the diodes form an OR function on the 0 V level.
Multiple clock lines may be applied via diodes connected to the trigger extender input ET.

Logic table

Trigger pulse at T_1	Trigger pulse at T_2	S_1	G_1	G_2	Q_1	Q_2
-	-	low	-	-	high	low
-	-	high	-	-	no change	
present	present	-	high	low	high	low
present	present	-	low	high	low	high
present	present	-	low	low	no change	
present	present	-	high	high	indeterminate	
present	-	-	high	-	high	low
present	-	-	low	-	no change	
-	present	-	-	high	low	high
-	present	-	-	low	no change	

Case temperature	T_C	max.	100	°C
Power supply currents (nominal)	I_{P_1}		11	mA
	I_{P_2}		11	mA
	I_N		1.6	mA
INPUT DATA				
Gate inputs G	$-I_G$	max.	2	mA
	$-Q_G$	max.	100	pC
Trigger inputs T				
corresponding input G at positive level	$-I_T$	max.	2	mA
	$-Q_T$	max.	290	pC
corresponding input G at 0 V level	$-I_T$		0	mA
	$-Q_T$		0	pC
Set input S	$-I_S$	max.	5	mA
	$-Q_S$	max.	360	pC

Base inputs B

Capacitance (of wiring plus output of 2.TG23) max. 9 pF (absolute maximum)

Gate extender inputs EG and trigger extender inputs ET

Diodes BAY38 may be used to increase the number of inputs. Capacitance to corresponding EG and ET terminals together (wiring plus diode capacitance) max. 10 pF.

When this figure is exceeded, connect a resistor between terminal EG and the positive supply V_{P_2} giving a time constant of 360 ns with the total capacitance.

Set extender inputs ES

Diodes BAY38 may be used to increase the number of inputs.

Capacitance (wiring plus diode capacitance) max. 10 pF (absolute maximum)

OUTPUT DATA

Output Q

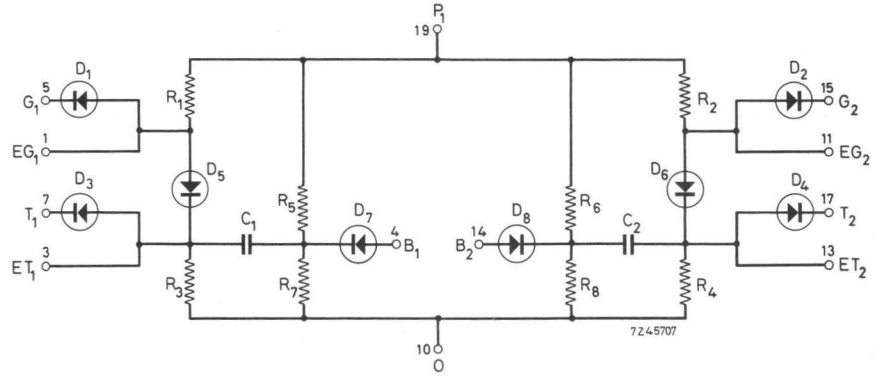
T_{amb} = min. 0 °C	I_Q	min.	14	mA
	Q_Q	min.	1400	pC
T_{amb} = min. −25 °C	I_Q	min.	8.7	mA
	Q_Q	min.	1100	pC
Wiring capacitance at each output Q	C_w	max.	75	pF

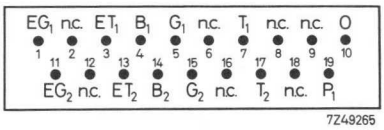
Time Data

Time that the trigger inputs T should be at the positive level and the signal levels should be present at gate inputs G	t_{prep}	min.	800	ns
Time between successive output signal changes	t_{recov}	min.	850	ns
Triggering edge duration (from 0.35 V_{P_1} to 0.5 V)	t_e	max.	50	ns
t_e + trigger pulse duration (0 V level)	$t_e + t_p$	min.	110	ns
Set pulse duration (0 V level)	t_s	min.	100	ns
Delay, full load	t_d	max.	110	ns

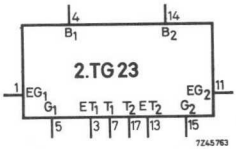
DUAL TRIGGER GATE

Function — additional triggering facility on FF23
Case — low standard case





terminal location



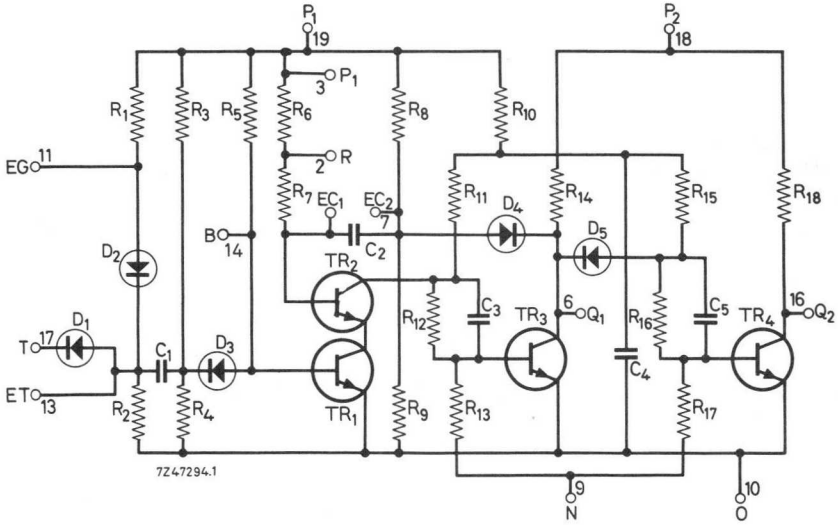
drawing symbol

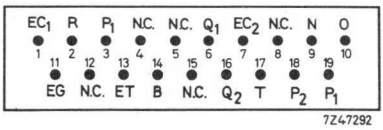
The circuit is identical with the trigger gate in the general-purpose triggered flip-flop FF23.
When the outputs B_1 and B_2 of the trigger gate 2.TG23 are connected to the inputs B_1 and B_2 of the flip-flop FF23 respectively, the inputs G and T of the 2.TG23 operate in the same way as the corresponding inputs of the FF23. Thus with this dual trigger gate a second pair of trigger inputs is formed for the flip-flop FF23 to make one stage of a bidirectional counter or shift register.

Case temperature	T_C	max.	100	°C
Power supply current (nominal)	I_{P_1}		7.6	mA
Input data and time data	similar to FF23			
Output capacitance	C_o	max.	5	pF

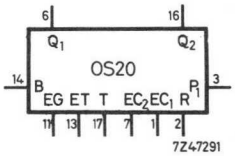
ONE-SHOT MULTIVIBRATOR

Function — generating pulses of defined length
Case — high standard case





terminal location



drawing symbol

The unit OS20 contains a monostable multivibrator circuit with a built-in trigger gate.
Trigger pulses are applied to trigger input T.
The built-in trigger gate is opened by applying the positive level via a diode BAY38 to the extender gate input EG and is closed by applying the 0 V level. Multiple clock lines may be applied via diodes BAY38 connected to the trigger extender input ET. When a trigger pulse is applied to input T the circuit generates a negative going pulse at the output Q_1 and a positive going pulse at the output Q_2.

The duration of the output pulse can be increased by an external capacitor to be connected between the terminals EC_1 and EC_2. The pulse duration can also be decreased by means of a resistor between the terminals R and P_1 or between the terminals R and EC_1.
Max. two trigger gates TG23 may be connected to the base input B to obtain additional triggering facilities.

Case temperature	T_C	max. 100	°C
Power supply currents (nominal)	I_{P_1}	17.5	mA
	I_{P_2}	6	mA
	I_N	1.5	mA

INPUT DATA

Gate inputs G

Diode BAY38 must be connected to EG to obtain gate input G.

	$-I_G$	max. 2	mA
	$-Q_G$	max. 100	pC

Trigger input T

Input G at positive level	$-I_T$	max. 2	mA
	$-Q_T$	max. 240	pC
Input G at 0 V level	$-I_T$	0	mA
	$-Q_T$	0	pC

Base input B

Capacitance (wiring plus output of TG23) max. 10 pF (absolute maximum)

Gate extender inputs EG and trigger extender inputs ET

Diodes BAY38 may be used to increase the number of inputs. Capacitance to corresponding EG and ET terminals together (wiring plus diode capacitance) max. 10 pF.
When this figure is exceeded, connect a resistor between EG and the positive supply V_{P_2}, giving a time constant of 360 ns with the total capacitance.

OUTPUT DATA

Output Q_1

T_{amb} = min. 0 °C at $t_{o1} + t_e$ = 130 ns	I_{Q_1}	min. 14	mA
	Q_{Q_1}	min. 1500	pC
T_{amb} = min. −25 °C at $t_{o_1} + t_e$ = 130 ns	I_{Q_1}	min. 8	mA
	Q_{Q_1}	min. 800	pC

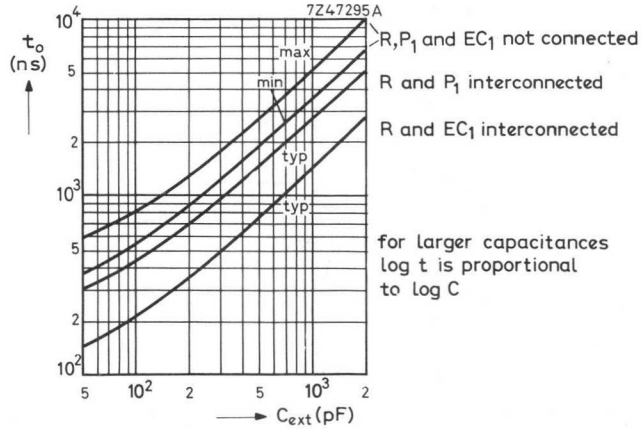
Output Q_2

T_{amb} = min.	0 °C at $t_{o2} + t_e$ = 850 ns	I_{Q2}	min.	15	mA
		QQ_2	min.	1500	pC
	at $t_{o2} + t_e$ = 130 ns	I_{Q2}	min.	15	mA
		QQ_2	min.	400	pC
T_{amb} = min.	−25 °C at $t_{o2} + t_e$ = 850 ns	I_{Q2}	min.	9	mA
		QQ_2	min.	800	pC
	at $t_{o2} + t_e$ = 130 ns	I_{Q2}	min.	9	mA
		QQ_2	min.	230	pC
Wiring capacitance at each output Q		C_W	max.	75	pF

Duration of the output pulse

Intrinsic value (R, P_1 and EC_1 not connected)	$t_e + t_{o(1,2)}$	min.	200	ns
		max.	390	ns
Intrinsic value (R and P_1 interconnected)	$t_e + t_{o(1,2)}$	min.	130	ns
		max.	250	ns

The pulse duration can be increased by an external capacitor between EC_1 and EC_2. The relation between the output pulse duration and the external capacitor (C_{EXT}) is given in the figure below.

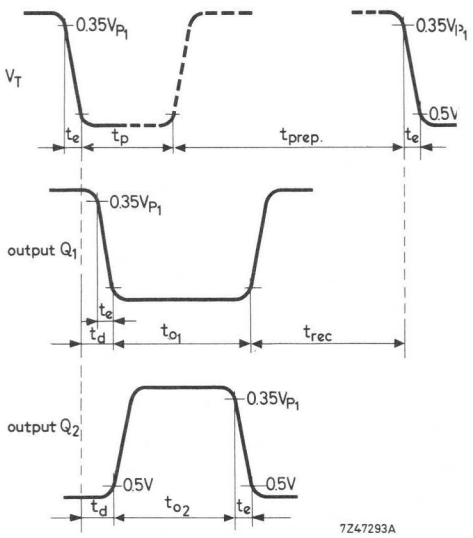


- When R and P_1 are interconnected the min. value of an external resistor between R and EC_1 is 10 kΩ.
- When R and P_1 are left disconnected there is no limitation in the value of the external resistor between R and EC_1.
- To avoid large tolerances of the pulse duration it is not recommended to connect a resistor between EC_1 and R, when output pulses with a duration smaller than 500 ns are required.

Stability of the output pulse duration

An increase in ambient temperature of 1 °C decreases the output pulse duration with less than 0.1 % and vice versa.
An increase in leakage current of the external capacitor (C_{EXT}) with 1 μA decreases the output pulse duration with less than 0.15 % and vice versa.
There is practically no difference in duration between different output pulses at any combination of permitted supply voltages.

Time Data

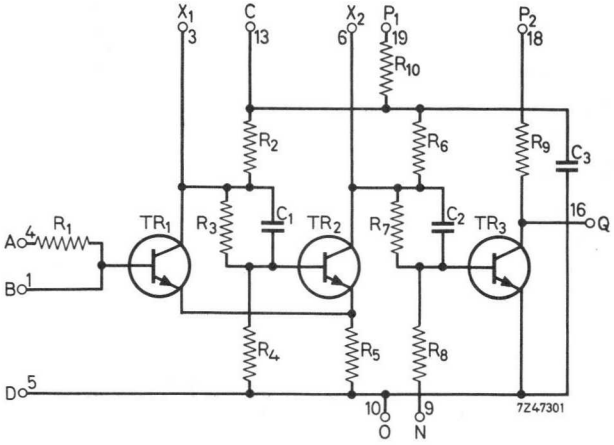


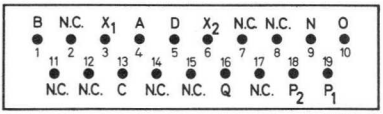
Time that the trigger input T should be at the positive level and the signal level should be present at gate input G	t_{prep}	min. 800	ns
Triggering edge duration (from 0.35 V_{P_1} to 0.5 V)	t_e	max. 50	ns
Triggering edge duration plus trigger pulse duration	$t_e + t_p$	min. 110	ns
Delay, full load	t_d	max. 125	ns
Triggering edge duration plus output pulse duration at Q_1 and Q_2	$t_{o(1,2)} + t_e$ = see data in preceding paragraph		
Recovery time			
R and P_1 interconnected	$t_{rec} = t_{o(1,2)}$	with a min. of 850 ns	
R and EC_1 interconnected	$t_{rec} = 1.5\ t_{o(1,2)}$	with a min. of 850 ns	
	$t_{rec} = 2\ t_{o(1,2)}$	with a min. of 850 ns	

PULSE SHAPER

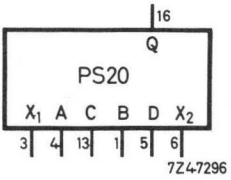
Function — converting non-standard signals into standard signals

Case — low standard case





terminal location



drawing symbol

The unit PS20 contains a Schmitt trigger (squaring) circuit followed by an inverting amplifier.

An input voltage in excess of the ON threshold level at terminal B gives a 0 V level at output terminal Q, a voltage below the OFF threshold level at terminal B gives a positive level at output terminal Q.

The pulse shaper can be driven from either a non-standard circuit or from a circuit block of the 20-series.

The latter via a diode BAY38 at terminal B, whilst terminal A has to be interconnected with terminal C.

Case temperature	T_C	max. 100	°C
Power supply currents (nominal)			
	I_{P_1}	6.5	mA
	I_{P_2}	6.0	mA
	I_N	1.3	mA

INPUT DATA

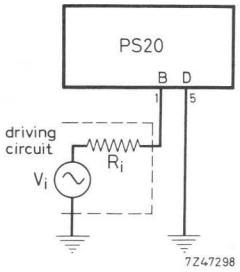
1. Unit driven by a non-standard circuit

		Operating		Limiting value	
ON threshold at input B	V_B	max. 0.23	V_{P_1}	7	V
(output Q at 0 V level)	I_B	max. 0.1	mA	18	mA
OFF threshold at input B	V_B	min. 0.10	V_{P_1}		
(output Q at positive level)	$-V_B$			3	V
	$-I_B$	max. 0.01	mA		

Internal resistance of the driving circuit

T_{amb} = min. 0 °C	R_i	max.	9	kΩ
T_{amb} = min. −25 °C	R_i	max.	6	kΩ

Hysteresis



The hysteresis ΔV_B is affected by the R_i of the driving circuit. The relation is given by the following equation.

T_{amb} = min. 0 °C	ΔV_i	min. $(0.06\ V_{P_1} - 0.076\ R_i)$
	ΔV_B	$\frac{\Delta V_i}{1 + 0.117\ R_i}$
T_{amb} = min. −25 °C	ΔV_i	min. $(0.06\ V_{P_1} - 0.114\ R_i)$
	ΔV_B	$\frac{\Delta V_i}{1 + 0.144\ R_i}$

(R_i in kΩ and V in volts)

Note:

If, for a particular application, a capacitor is required between terminal B (1) and earth, use should be made of terminal D (5).
The main earth terminal 0 (10) can better not be used for this purpose to avoid noise on the common earth point.
The latter could interfere the proper function of the unit.

2. Unit driven by circuit block of the 20-series

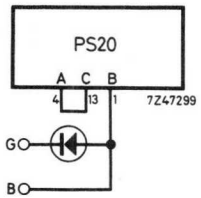
Terminal A has to be interconnected with terminal C and the input voltage V_G has to be applied to terminal B via a diode BAY38, BAX13 or equivalent type.

Gate input G	$-I_G$	max. 2	mA
	$-Q_G$	max. 150	pC

Gate extender input B

Diodes of type BAY38 in parallel may be used to increase the number of inputs.

Capacitance (wiring plus diodes) max. 10 pF.



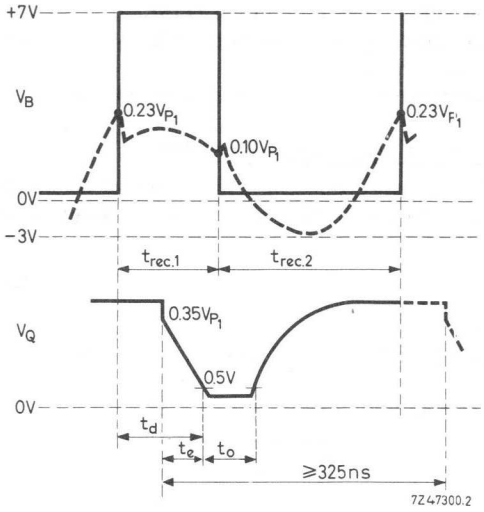
OUTPUT DATA

Output Q

T_{amb} = min. 0 °C	I_Q	min. 20	mA
	Q_Q	min. 700	pC
T_{amb} = min. −25 °C	I_Q	min. 10	mA
	Q_Q	min. 400	pC
Wiring capacitance at output Q	C_w	max. 30	pF

At C_w = max. 30 pF the available Q_Q = 600 pC

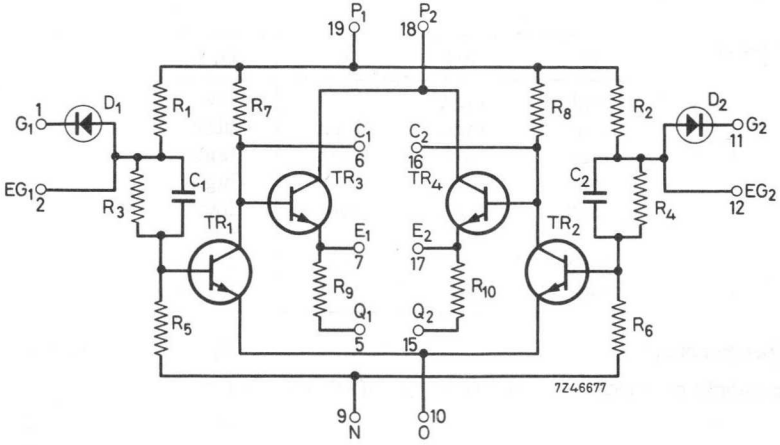
Time Data (when unit is used in combination with 20-series circuit blocks)

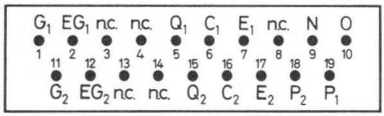


Recovery time	t_{rec_1} t_{rec2}	min. 125 min. 200	ns ns
Delay, full load	t_d	max. 120	ns
Triggering edge duration at output Q	t_e	max. 50	ns
Triggering edge duration + output pulse duration	$t_e + t_o$	min. 90	ns

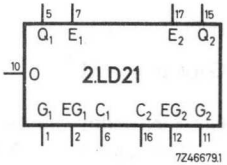
DUAL LINE DRIVER

Function	driving 75 Ω cables with logic gating capability
Case	low standard case





terminal location



drawing symbol

The unit is intended to drive terminated lines which are to be connected to terminal Q. A built-in resistor is provided to drive terminated 75 Ω lines to a 3 V signal level.

The unit is normally used in conjunction with the line receiver unit 2.LR22. Excessive conductor resistance of the line can be compensated by a resistor between E and Q, to preserve the signal level at the end of the cable. Terminated cables of a different characteristic impedance (range 75 to 135 Ω) can be driven to 3 V signal level, using an external series resistor equal to Z_o - R_{dc} of cable, between terminal E and the cable. The corresponding Q-terminal is left floating.

Terminal C is provided to connect two or more outputs Q of the GI 20, GI 21 and GI 22, of which the collector resistors are left floating. In this way a logic function can be obtained. This technique is not recommended when the proper operation of the following circuits will be disturbed by the erratic positive-going output pulses that may be produced.
The number of gate inputs can be increased by external diodes, BAY38, BAX13 or equivalent types, connected to the extender input EG. When all inputs are at the positive level the corresponding output transistor is in its non-conducting state. Application of the 0 V level to one of the inputs G causes the output transistor to become conductive.

Logic table

G	EG	C	Q, E
high	high	high	low
low	high	high	high
high	low	high	high
low	low	high	high
high	high	low	low
low	high	low	low
high	low	low	low
low	low	low	low

Case temperature T_C max. 100 °C

Power supply currents, nominal (average of ON and OFF state)

I_{P_1}	I_Q	22	mA
I_{P_2}		−5	mA
I_N		2	mA

INPUT DATA

Gate inputs G

$-I_G$ max. 2 mA
$-Q_G$ max. 150 pC

Gate extender inputs EG

Diodes BAY38, BAX13 or equivalent types may be used to increase the number of gate inputs.
Capacitance (of wiring plus diodes) max. 10 pF
When this figure is exceeded, connect a resistor between terminal EG and the supply voltage V_{P_2} giving a time constant of 85 ns with the total capacitance.

Terminal C:

I_C max. 12 mA
Q_C max. 700 pC

Collectors of GI 20/21/22 may be connected to this point to obtain the sum of the product functions, formed at the LD- and GI-inputs.
Capacitance: see Time Data.

OUTPUT DATA

Output Q (T_{amb} = min. −25 °C) I_E = max. 80 mA at V_E = min. (VP_2 −0.6 V)

I_Q = min. 40 mA at V_Q = min. (VP_2 −3.2 V)

Time Data

Time between successive output signal changes t_{recov} min. 110 ns

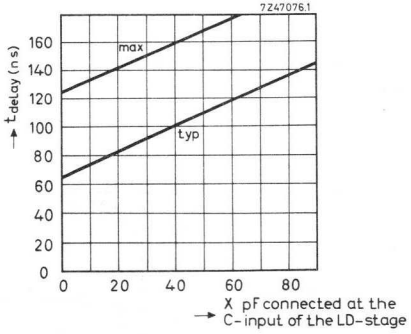
Delay time t_{delay} (cable delay not included)

at 0 to +85 °C of

LD21 { loaded with X pF / at the C input } + LR22 { loaded with 7 G-inputs / of GI 20/21/22 + 75 pF } = see figure below

at −25 °C of

LD21 { loaded with X pF / at the C input } + LR22 { loaded with one G-input / of GI 20/21/22 + 75 pF } = see figure below



Note 1

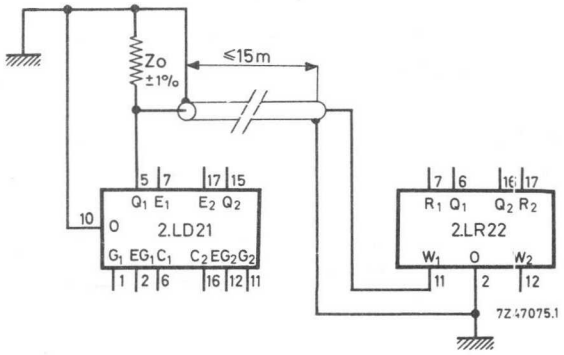
The graph is valid for a cable between the units LD21 and LR22, which has the following characteristics:

attenuation		0.079 dB/m at 10	MHz
		0.138 dB/m at 30	MHz
		0.254 dB/m at 100	MHz
		0.446 dB/m at 300	MHz
		0.840 dB/m at 1000	MHz
capacitance		67	pF/m
characteristic impedance	Z_o	75 Ω ±6	%
	R_{dc}	≤ 0.80	Ω/m

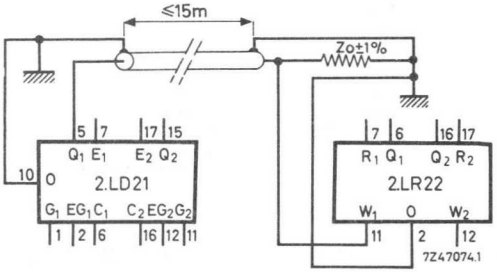
CONNECTION DIAGRAMS FOR SINGLE AND MULTIPLE LINE DRIVING

1. Single line driving

a) Terminated at the input of the line [1])



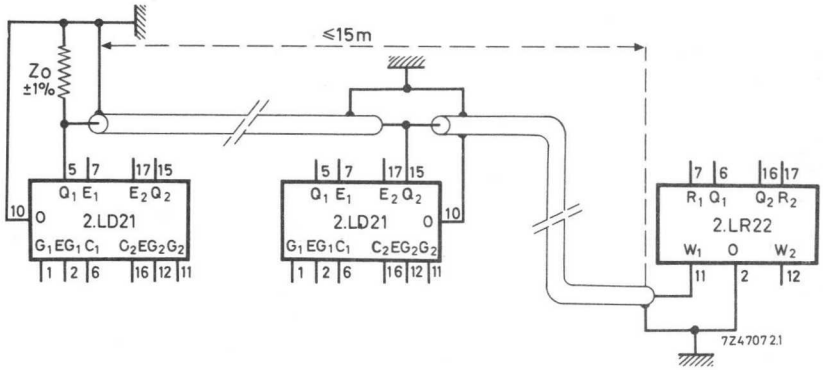
b) Terminated at the end of the line [1])



1) The max. length of the cable is 15 meter for a cable with characteristics as specified in Note 1.

2. Multiple line driving

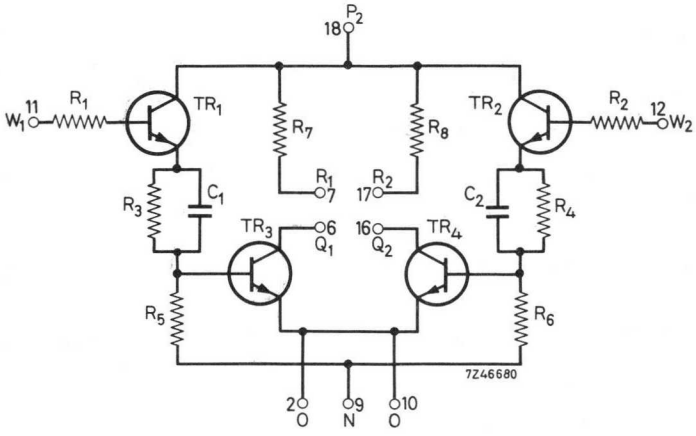
The line must be terminated at the driving side as shown in the figure below [1].

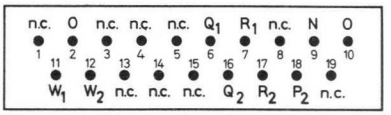


[1]) The max. length of the cable is 15 meter for a cable with characteristics as specified in Note 1.

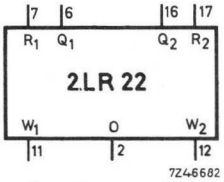
DUAL LINE RECEIVER

Function	converting 3 V signal levels to standard system levels
Case	low standard case





terminal location



drawing symbol

The unit is intended to convert 3 V signal levels on lines to standard signal levels, used in the "20 series" of circuit blocks.

The input impedance is high, so for multiple receiving more units can be connected to different taps on the line. The signal polarity, from input to output, is inverted.

The unit is normally used in conjunction with the line driver unit 2.LD21. In the latter configuration the signal polarity, from the input of the LD21 to the output of the LR22, is not inverted.

Any output Q is to be connected to a collector resistor R. A logic function can be obtained by interconnecting two or more outputs Q; in this case only one collector resistor is usually needed and the others are left disconnected. For n interconnected outputs (n - 1) times the output capacitance should be added to the wiring capacitance.
This technique is not recommended when the proper operation of the following circuits will be disturbed by the erratic positive-going output pulses that may be produced.

Case temperature	T_C	max. 100	°C
Power supply currents, nominal (average of ON and OFF state)			
	I_{P_2}	10	mA
	I_N	2	mA

INPUT DATA

Input high			
T_{amb} = min. −25 °C	V_W	min. 2.5	V
Input low			
T_{amb} = min. −25 °C	V_W	max. 1.0	V
Input impedance	Z_W	min. 8	kΩ//
		min. 15	pF

OUTPUT DATA

Output Q			
T_{amb} = min. 0 °C	I_Q	min. 15	mA
	Q_Q	min. 540	pC [1]
T_{amb} = min. −25 °C	I_Q	min. 2	mA
	Q_Q	min. 180	pC
Output capacitance	C_Q	max. 13	pF
Wiring capacitance at output Q	C_w	max. 75	pF

[1]) Transient data applicable when driven from a LD21 via a cable with a length of max. 15 meter.

Time Data

Time between successive output signal changes t_{recov} min. 110 ns

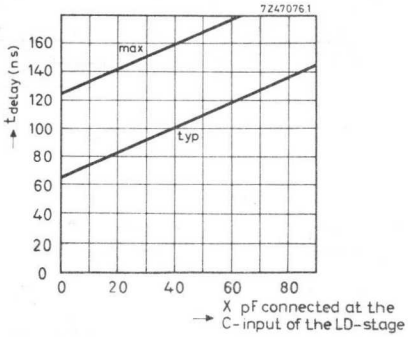
Delay time t_{delay} (cable delay not included)

at 0 to +85 °C of

LD21 { loaded with X pF at the C input } + LR22 { loaded with 7 G-inputs of GI 20/21/22 + 75 pF } = see figure below

at −25 °C of

LD21 { loaded with X pF at the C input } + LR22 { loaded with one G-input of GI 20/21/22 + 75 pF } = see figure below



Note 1

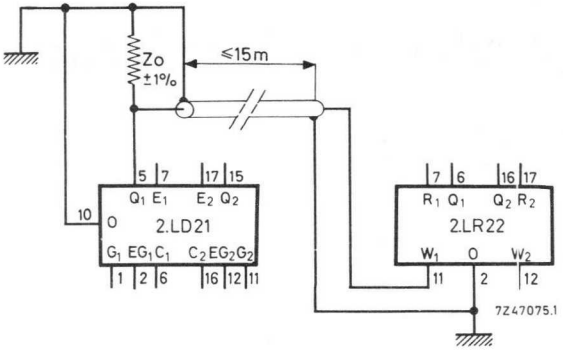
The graph is valid for a cable between the units LD21 and LR22, which has the following characteristics:

attenuation		0.079	dB/m at 10	MHz
		0.138	dB/m at 30	MHz
		0.254	dB/m at 100	MHz
		0.446	dB/m at 300	MHz
		0.840	dB/m at 1000	MHz
capacitance			67	pF/m
characteristic impedance	Z_o		75 Ω ±6	%
	R_{dc}		≤ 0.80	Ω/m

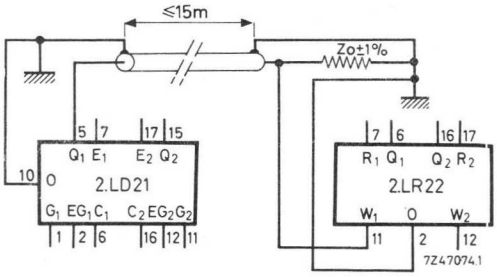
CONNECTION DIAGRAMS FOR SINGLE AND MULTIPLE LINE RECEIVING

1. Single line receiving

a) Terminated at the input of the line [1])

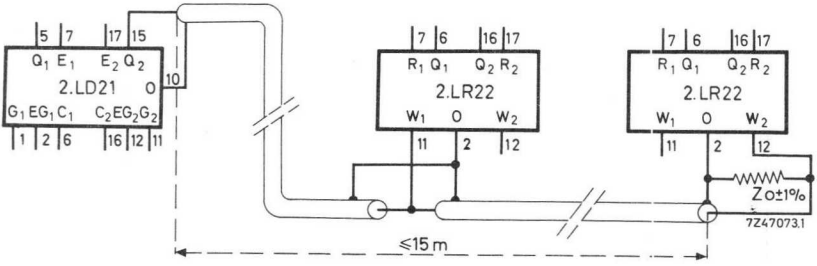


b) Terminated at the end of the line [1])



2. Multiple line receiving

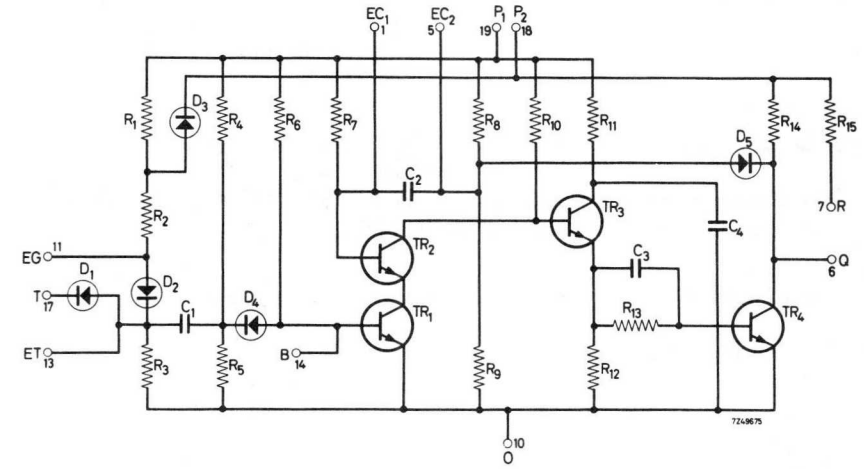
The line must be terminated at the receiving side as shown in the figure below [1]).

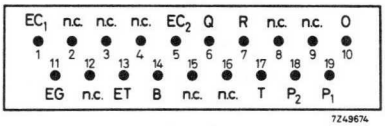


[1]) The max. length of the cable is 15 meter for a cable with characteristics as specified in Note 1.

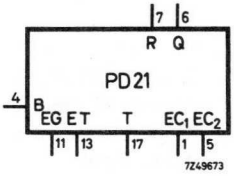
PULSE DRIVER

Function triggering and resetting flip-flops
Case high standard case





terminal location



drawing symbol

The unit contains a monostable multivibrator circuit with a built-in trigger gate.
Trigger pulses are applied to trigger input T.
The trigger gate is closed by applying the 0V level via a diode BAY 38 or equivalent type to the extender gate input EG and is opened by applying the positive level.
The gate is also open when the input EG is left floating.
When a trigger pulse is applied to the trigger input T the circuit generates a negative-going pulse at the output Q. This output pulse is particularly suitable for triggering and resetting flip-flops.
The duration of the output pulse can be increased by connecting an external capacitor between the terminals EC_1 and EC_2.
External trigger gates TG23 may be connected to the base input B to obtain additional triggering facilities.

Case temperature	T_C	max. 100 °C	(transistor TR_4 non-conducting)
Power supply currents (nominal)	I_{P1}	14 mA	
	I_{P2}	0 mA	
	I_{P1}	34 mA	(transistor TR_4 conducting)
	I_{P2} (R and Q interconnected)	20 mA	
	I_{P2} (R and Q not interconnected)	6 mA	

INPUT DATA

Extender gate input EG	$-I_G$	max. 3.5 mA
	$-Q_G$	max. 180 pC

The gate signal has to be applied via a diode BAY 38, IN 4009, IN 3604 or equivalent type; the anode connected to terminal EG.

Trigger input T		
input G at 0V level	$-I_T$	0 mA
	$-Q_T$	0 pC
input G at positive level or floating	$-I_T$	max. 3.5 mA
	$-Q_T$	max. 360 pC

Base input B

Capacitance (wiring plus output of TG23) max. 30 pF (absolute maximum)

Extender gate input EG and extender trigger input ET

Diodes BAY 38, IN 4009, IN 3604 or equivalent types may be used to increase the number of inputs.

Capacitance at EG and ET terminals together (wiring plus diode capacitance) max. 20 pF.

When this figure is exceeded, connect a resistor between terminal EG and the positive supply V_{P1} giving a time constant of 350 ns with the total capacitance.

OUTPUT DATA

Output Q

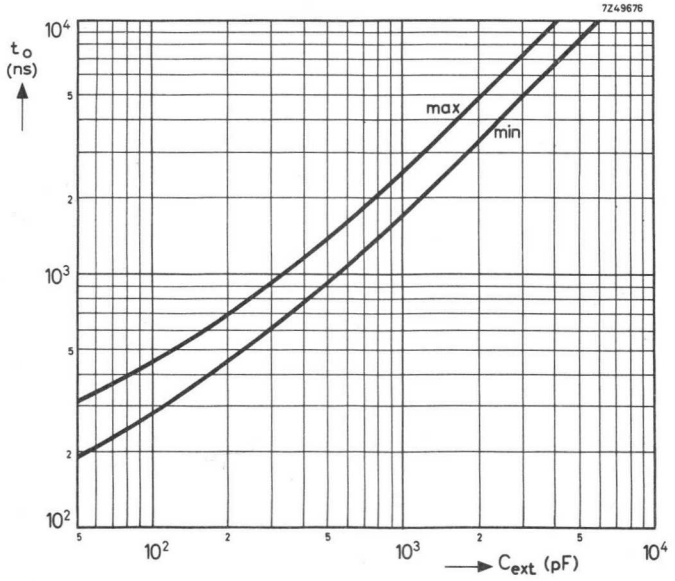
T_{amb} = min. 0 °C			
R and Q not interconnected	I_Q	min. 90 mA	
	Q_Q	min. 7500 pC	
R and Q interconnected	I_Q	min. 75 mA	
	Q_Q	min. 6700 pC	
T_{amb} = min. - 25 °C			
R and Q not interconnected	I_Q	min. 82 mA	
	Q_Q	min. 6800 pC	
R and Q interconnected	I_Q	min. 67 mA	
	Q_Q	min. 6000 pC	

Wiring capacitance

Unit used for triggering FF23 or resetting FF20		
R and Q not interconnected	C_w	max. 75 pF
R and Q interconnected	C_w	max. 250 pF
Unit used for resetting FF23	C_w	max. 250 pF

Time Data

Triggering edge duration + trigger pulse duration	t_e+t_p	min. 110 ns
Trigger gate charging time	t_{ch}	min. 500 ns
Trigger gate inhibiting time	t_{inh}	min. 800 ns
Output pulse duration		
Intrinsic value	t_o+t_e = 110 - 200 ns	
Increase with external capacitance	see figure below	
Maximum duration		1 ms
Recovery time	t_{rec}	min. 2 t_o with a minimum of 500 ns
Delay, full load	t_d	max. 90 ns



For larger capacitances log t_o is proportional to log C_{ext}

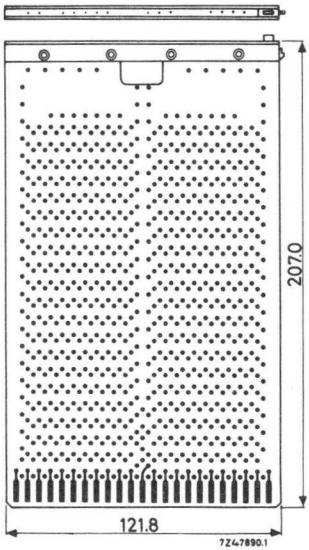
Stability of the output pulse duration

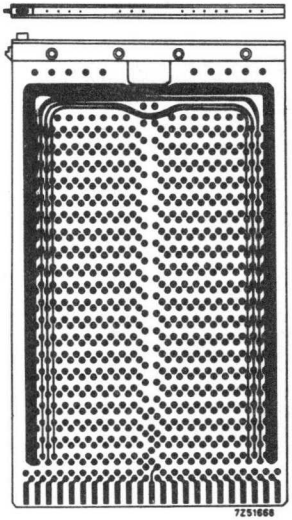
An increase in ambient temperature of 1 °C decreases the output pulse duration with less than 0.1% and vice versa.
An increase in leakage current of the external capacitor (C_{ext}) with 1 μA decreases the output pulse duration with less than 0.1% and vice versa.
There is practically no difference in duration between different output pulses at any combination of permitted supply voltage.

ACCESSORIES FOR CIRCUIT BLOCKS
20—SERIES

EXPERIMENTERS' PRINTED—WIRING BOARDS

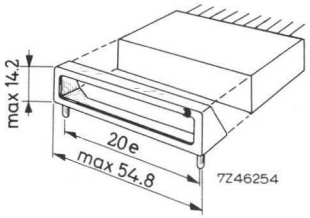
These printed-wiring boards (with extractor) for 20-Series circuit blocks can accommodate a maximum of 20 blocks mounted vertically or 6 to 12 blocks mounted horizontally at most (depending on how many of these are high and how many low). The boards fit the mounting chassis 4322 026 38240.





Catalogue number	4322 026 38660	4322 026 38670
Material	phenolic resin bonded paper	glass-expoxy
Holes	plated-through; 1.2 mm diameter	
Contacts	2x23, gold plated, pitch 0.2 inch	

LOCKING CAP



For better securing 10-Series and 20-Series circuit blocks mounted parallel to a printed-wiring board (horizontal mounting), window-shaped locking caps are available. They fit the top of a circuit block.
The locking caps are provided with two holes and recesses to lodge two soldering tags, with which the caps can be secured to the board.

description	catalogue number
locking cap	4322 026 32150
soldering tag	4322 026 32140

STICKERS

These are drawing symbols of circuit blocks printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings. The drawing symbols are as shown on the data sheets of the relevant circuit blocks.
The stickers are available in rolls, each containing 1000 drawing symbols of the same type of circuit block. Each sticker can be separately detached from the roll, without cutting.

for circuit block of type	catalog number of a roll with 1000 stickers
FF 20	4322 026 31450
FF 22	36800
FF 23	31460
2.TG 23	31490
2.GI 20	31470
2.GI 21	34670
2.GI 22	34680
OS 20	34650
PS 20	34660
PD 21	36810
2.LD 21	34690
2.LR 22	34700

Circuit blocks

40-Series

INTRODUCTION

In any analogue system for instrumentation and control there are a number of basic functions. The units of the 40-Series have been developed to perform basic analogue functions, thus to save the system designer considerable time and costs.
Great care has been taken to make them versatile so that a greater part of the required functions in analogue systems can be performed without needing complex external circuitry.
Being capable of handling signals down to d.c. they are very reliable and operate with a high degree of stability.

The 40-Series units find wide application in, for instance:

signal generating circuits
process and alarm circuits
closed-loop power control systems
A-D and D-A converters
electronic measuring instruments

Extensive information on the principles and applications can be found in the Application Book: "Measurement and control with the 40-Series modules".

The 40-Series comprises the following units:

DOA 40, Operational Amplifier
DOA 42, Differential Amplifier
DZD 40, Differential Zero Detector
PSM 40, Phase Shift Module

OPERATIONAL AMPLIFIER

GENERAL

The DOA40 is a high gain, wide band, low drift d.c. differential amplifier. Input voltage offset can be externally corrected.
A 6 dB/octave roll-off network is built-in. Terminals are available to connect an external roll-off network.

This unit is developed for use with power supplies of 15 V. As many control systems use 12 V supplies, some data are given for use at these voltages at the end of the specification.

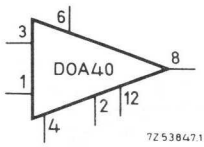


Fig.1. Drawing symbol

Dimensions in mm

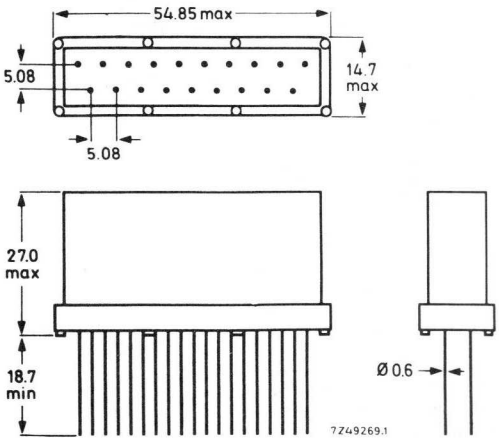


Fig.2.

The complete circuit is potted inside a metal can with 19 wire terminals. The can is internally connected to terminal 10 (0 V)

Circuit diagram and terminal location

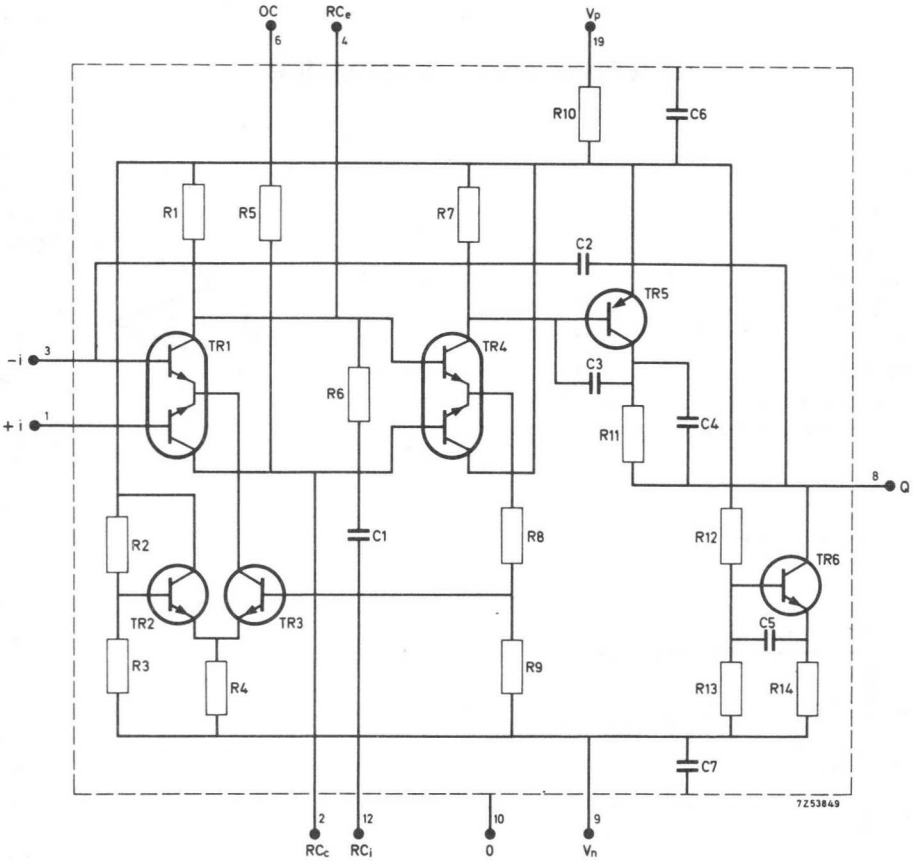


Fig.3. Circuit diagram

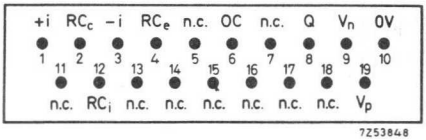


Fig.4. Terminal location

TECHNICAL PERFORMANCE

Ambient temperature range: operating	0 to +85 °C
storage	−40 to +85 °C
Max. case temperature	91 °C

Power supply

Supply voltages	V_P = +15 V ± 3% V_N = −15 V ± 3%
Supply currents	I_P = 10 mA + load current I_N = 10 mA + load current

Input data (ambient temperature +25 °C unless noted otherwise)

Open loop gain	minimum	typical
DC, max. load	25 000	60 000
DC, 100 kΩ load	100 000	150 000

Input voltage offset

Initial offset can be trimmed to zero by means of an external variable resistor of 15 kΩ between terminals OC and V_P

	maximum	typical
drift with temperature change (0 °C to +85 °C)	5 μV/deg C	3 μV/deg C
drift with supply voltage change		
for +15 V supply	7 μV/%	3 μV/%
for −15 V supply	3 μV/%	2 μV/%

Input current	maximum	typical
Each input: bias current	700 nA	300 nA
drift with temperature change (0 °C to +85 °C)	7 nA/deg C	3 nA/deg C
Differential: initial offset	35 nA	6 nA
drift with temperature change (0 °C to +85 °C)	1 nA/deg C	0.3 nA/deg C

Input impedance	minimum	typical
between inputs	75 kΩ	200 kΩ
common mode	60 MΩ	100 MΩ

Input voltage	
max. voltage between inputs	+5 and −5 V
max. common mode voltage	+10 and −10 V
common mode rejection	min. 20 000 typ. 60 000
Voltage noise (16 Hz - 16 kHz)	3 μV (rms)

Output data

Output voltage (at a load current of 6 mA)	min. +10 V to −10 V
Load resistance	min. 1.67 kΩ
Output resistance	< 5 kΩ

Frequency response

Unity gain bandwidth (small signal)	min. 8.5 MHz	typ. 9.5 MHz
Full output response (20 $V_{p\text{-}p}$)		
with 10 kΩ load	min. 40 kHz	typ. 60 kHz
with 1.67 kΩ load	min. 33 kHz	typ. 50 kHz
Slewing rate (R_{load} = 10 kΩ)	min. 2.5 V/μs	typ. 3.7 V/μs

Specifications for the DOA40 used with 12 V supply

If the DOA40 is used with 12 V supply, the specifications remain the same as those given for the 15 V supply, except those listed below.

Power supply voltages	V_P = +12 V ± 5% V_N = −12 V ± 5%
Power supply currents (load current and feedback current to be added)	I_P = 8 mA I_N = 8 mA
Input currents	multiply the data given for 15 V supply by 0.8
Common mode voltage	+8 V, −8 V
Output voltage at a load current of 5 mA	+9 V, −9 V
Load resistance	1.8 kΩ (min.)

APPLICATION INFORMATION

When used in a follower circuit, the DOA40 may exhibit instability. To avoid this, it is good practice to insert a 10 kΩ resistor between the signal source and the amplifier input.

The characteristics of the DOA40 are such that adaption circuitry is unnecessary for most applications. However, three special situations which are sometimes encountered - comparatively small input currents, comparatively large output capability, and the need to adjust input current to zero - can also be handled by the DOA40 with the simple adaption circuits described below.

Reduction of input current and increase of input impedance

The dual transistor BCY87 connected as an emitter-follower in the circuit of Fig.5 can be used to reduce the input current to 40 nA per input and increase the input impedance to 15 MΩ between inputs (typical values).

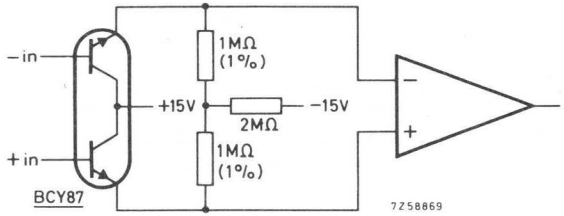


Fig.5. Configuration giving reduced input current and increased input impedance. The component values given are typical.

The characteristics of the circuit are given below. Other characteristics not listed are those of the DOA40 unit alone.

Supply voltage rejection (both supplies)	typical	80 μV/V
Input voltage, drift with temperature change	typical	5 μV/deg C
	maximum	10 μV/deg C
Input current / each input		
bias current	typical	40 nA
	maximum	60 nA
drift with temperature change / differential	typical	0.25 nA/deg C
initial offset	typical	4 nA
	maximum	6 nA
drift with temperature change	typical	0.1 nA/deg C
Input impedance between inputs,	typical	15 MΩ
	minimum	10 MΩ
common mode	typical	600 MΩ
Common mode rejection	typical	10 000
Unity gain bandwidth	typical	6.5 MHz
Full output frequency (20 V_{p-p})	typical	40 kHz

Increase of the output capability

The circuit of Fig.6 is capable of delivering 50 mA at +10 V and −10 V. The output can be short-circuited momentarily without causing damage to the circuit. Feedback networks if used should be connected to the circuit output, not the DOA40 output.

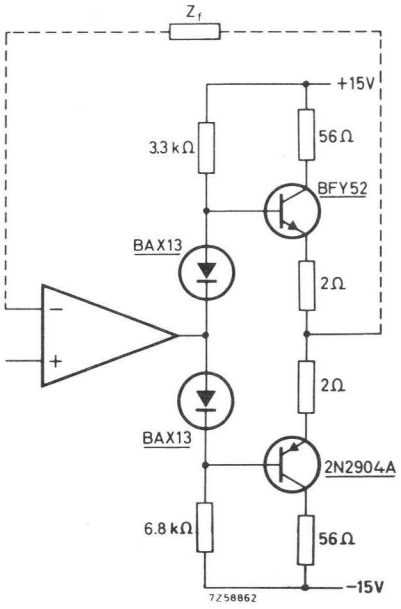


Fig.6. Configuration giving increased output capability.

Zero adjustment of input current

Each DOA40 input requires a bias current of 700 nA to give zero output voltage. By supplying this bias current from an external source, the DOA40 output can be made zero for a driving signal current equal to zero.

In Fig.7a the negative input (pin 3) is to be so adjusted. A 10 MΩ resistor should be connected between the output and pin 3, and the potentiometer adjusted so that the output voltage of the DOA40 becomes equal to zero. The 10 MΩ resistor should then be removed.

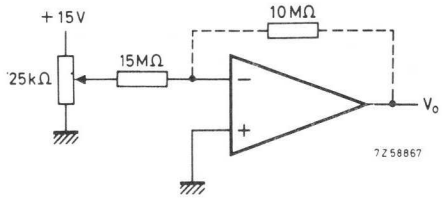


Fig.7a. External supply of bias current: adjustment of negative input.

The positive input (pin 1) may now be adjusted with the circuit of Fig.7b. Connect pin 3 to the DOA40 output, and the 10 MΩ resistor between pin 1 and ground. The potentiometer can now be adjusted so that the DOA40 output becomes zero. Disconnect the 10 MΩ resistor.

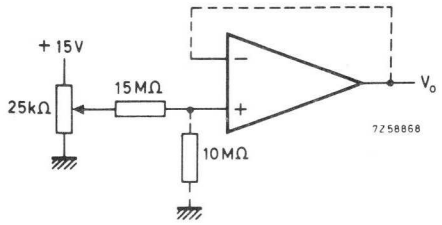


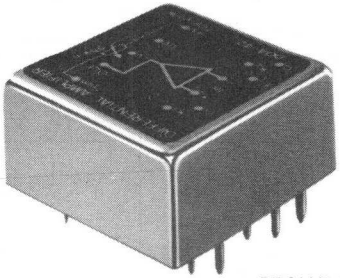
Fig.7b. External supply of bias current: adjustment of positive input.

Several publications are available which may be of further interest.

1. "Operational Amplifiers", Application Information.
   This publication gives an introduction to the use of operational amplifiers as engineering tools. The concepts and terminology of the general operational amplifier, and the properties and accuracy of a typical circuit are presented.
2. "Digital to Analogue and Analogue to Digital Conversion", Application Information.
   The publication gives detailed information on the construction of both types of converter.
3. "Flux Meter with Digital Read-out", Application Note (Print No. 9399 210 00601).
4. "Simple Process Control", Application Note (Print No. 9399 214 05501).
5. "Electronic Potentiometer", Application Note (Print No. 9399 260 00201).
6. "A level Detector Using the Operational Amplifier DOA40", Application Note (Print No. 9399 260 03101).

The Application Notes (3, 4, 5 and 6) give brief descriptions of practical applications of the DOA40.
Small discrepancies may be seen to exist in terminal location drawings in the above publications. The terminal locations as given in this Data Sheet are the ones to be followed.

DIFFERENTIAL AMPLIFIER



RZ 26449-1

GENERAL

The DOA42 is a high-gain, wideband, low-drift d.c. differential amplifier which may also be used as an operational amplifier. The input-voltage offset can be corrected externally.

A roll-off network is built in to ensure stable operation at feedback values between 100 and 60 dB (loop gain between 0 and 40 dB). Data on additional external compensating RC circuits to be used at lower gain values are given below under "Application information".

The unit, developed for use with power supplies producing +15 and −15 V, can also be operated from 12 V supplies if reduced output characteristics are acceptable. Some data are given for use at these voltages under "Technical Performance".

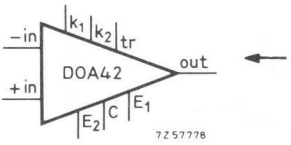


Fig.1
Drawing symbol

Dimensions (in mm) and terminal identification

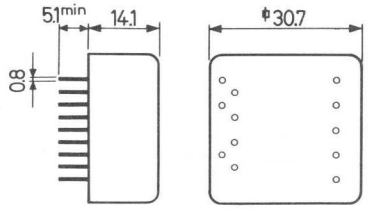
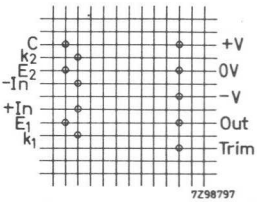


Fig.2



+V	= positive supply voltage
−V	= negative supply voltage
0 V	= earth and housing
+In	= non-inverting input
−In	= inverting input
k_1 }	= terminals for external
k_2 }	freq. compensation
Trim	= for external offset correction
Out	= amplifier output terminal
E_1	= emitter 1
E_2	= emitter 2
C	= collector

Fig.3. Terminal location (bottom view) on 0.1 in grid

Circuit diagram

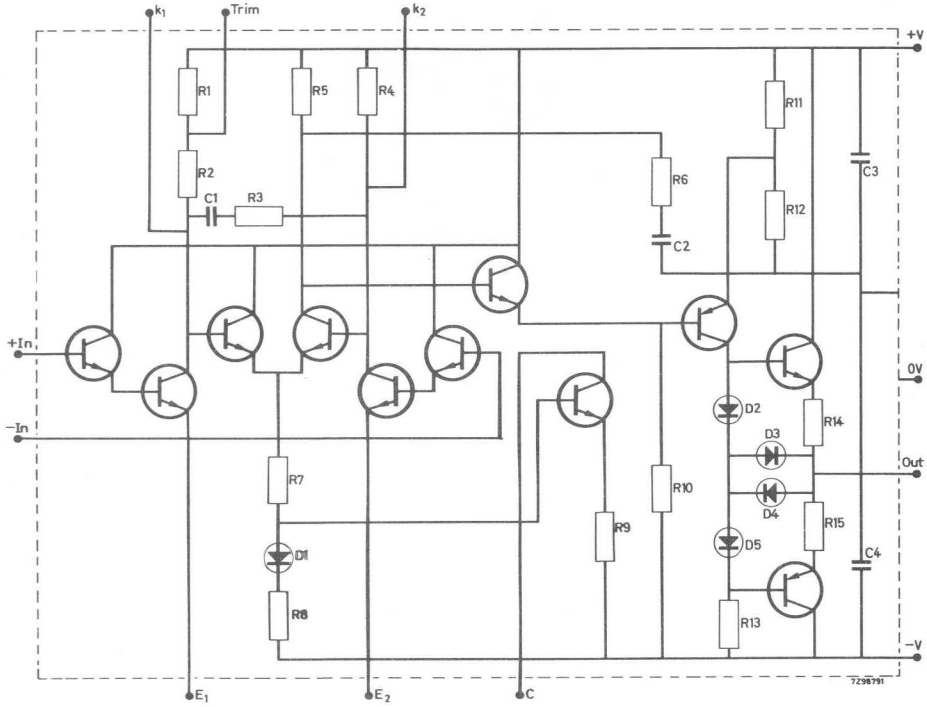


Fig.4

TECHNICAL PERFORMANCE

Ambient temperature range: operating	−25 °C to +85 °C
storage	−55 °C to +85 °C
Max. case temperature	85 °C
Power supply	+15 V ±3%, 3.7 mA (typ.)+load current −15 V ±3%, 1 mA (typ.)+load current

Input data (ambient temperature +25 °C unless stated otherwise)

Open loop gain	minimum	typical
DC, max. load		106 dB
DC, 10 kΩ load	100 dB	106 dB

Input voltage offset

Initial offset can be trimmed to zero by means of an external variable resistor of 25 kΩ between terminals Trim and +V.

	maximum	typical
Drift with temperature change (0 °C to +85 °C)		7 μV/degC
Drift with supply voltage change		
for +15 V supply	± 20 μV/V	± 10 μV/V
for −15 V supply	± 20 μV/V	± 10 μV/V

Input current	maximum	typical
Each input: bias current	20 nA	5 nA
drift with temperature change (0 °C to +85 °C)	0.5 nA/degC	0.1 nA/degC
Differential: initial offset	4 nA	1 nA
drift with temperature change (0 °C to +85 °C)	100 pA/deg C	30 pA/degC

Input impedance	minimum	typical
between inputs	5 MΩ	20 MΩ
common mode		1000 MΩ

Input voltage

Max. voltage between inputs	+5 and −5 V	
Max. common mode voltage	+5 and −5 V	
Common mode rejection	min. 80 dB	typ. 100 dB
Voltage noise (0 - 10 kHz)	max. 15 μV (rms)	typ. 8 μV (rms)

Output data

Output voltage (total current 5 mA)	min. +10 V to −10 V
Load resistance	min. 2 kΩ (short circuit proof)
Output resistance	typ. 150 Ω

Frequency response

Unity gain bandwidth (small signal)	typ. 5 MHz
Full output response (20 V_{p-p})	
with 10 kΩ load	typ. 45 kHz
with 2 kΩ load	typ. 40 kHz
Slewing rate (R_{load} = 10 kΩ)	typ. 2.5 V/μs

Specifications for the DOA42 used with 12 V supply.

If the DOA42 is used with a 12 V supply the specifications remain the same as those given for a 15 V supply except for the data given below:

Power supply	V_P = +12 V ± 5%, 2.9 mA(typ.) + load current V_N = -12 V ± 5%, 0.8 mA(typ.) + load current
Input currents	multiply the data given for 15 V supply by 0.8
Max. common mode voltage	+4 V, −4 V
Output voltage at a load current of 4 mA	+9 V, −9 V
Load resistance	min. 2.25 kΩ

APPLICATION INFORMATION

– Fig.5 gives the frequency response for various gain levels. When the amplifier is applied with a closed loop gain of less than 40 dB external compensation RC series circuits have to be connected between the pins k_1 and k_2.
The corresponding external correction networks are given in Fig. 6.

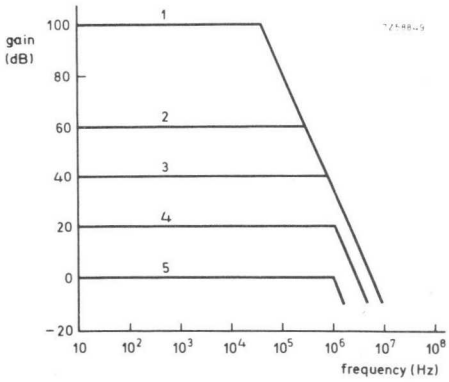


Fig.5

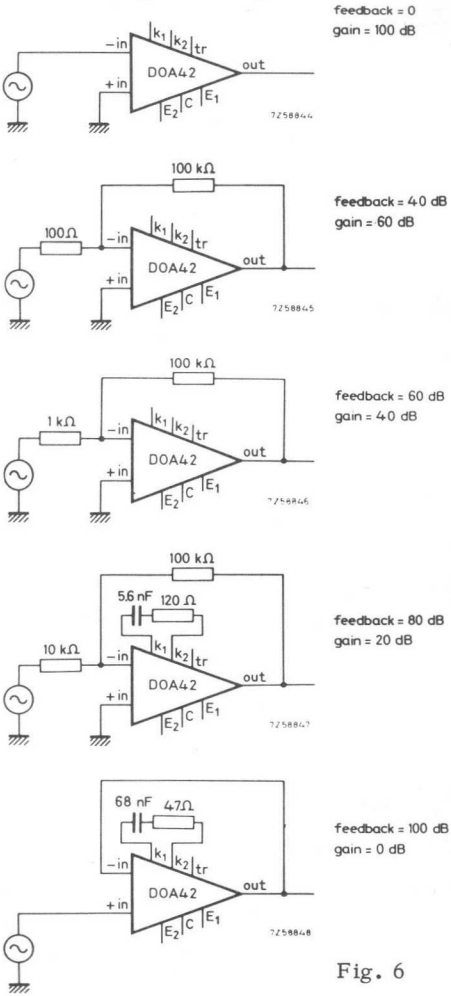


Fig. 6

– Use as an operational amplifier.

For use as an operational amplifier the terminals E_1, E_2 and C should be interconnected directly across the pins.

- Use as a differential amplifier with a high input impedance.

Operational amplifiers used as differential amplifiers have a rather low input impedance, because the input impedance of the negative input is equal to R1 (see Fig. 7), which is limited.

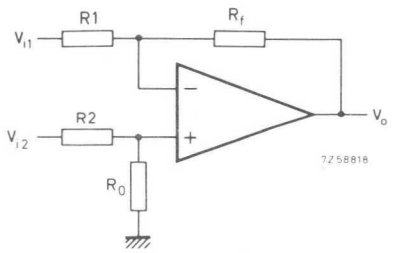


Fig. 7

Resistors R2 and R_0 give symmetry to the input. For high input impedance differential amplifiers a set-up with 3 operational amplifiers is often used (Fig. 8).

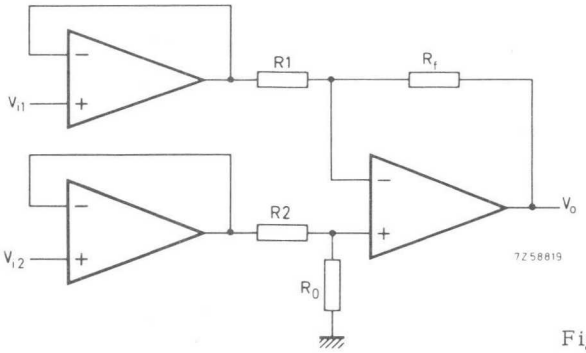


Fig. 8

With one DOA42 a high input impedance differential amplifier can be obtained as follows:

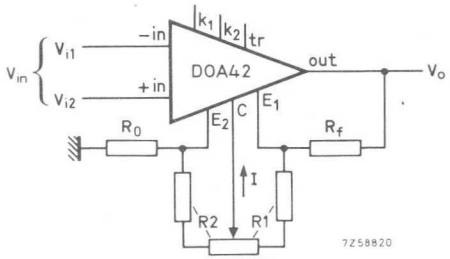


Fig. 9

The input impedance is high for both inputs. The transfer formula then is:

$$\frac{Vo}{Vin} = \left\{ \tfrac{1}{2} \left(1 + \frac{Rf}{R0}\right) + \frac{2Rf}{R1 + R2} \right\} - \frac{Rf\,(R1 - R2)}{R1 + R2} \cdot \frac{I}{Vin} + \left(\frac{Rf}{R0} - 1\right) \frac{Vcm - Vbe}{Vin}$$

where V_{cm} = common mode voltage, R_f = feedback resistance, V_{be} = base-emitter voltage.

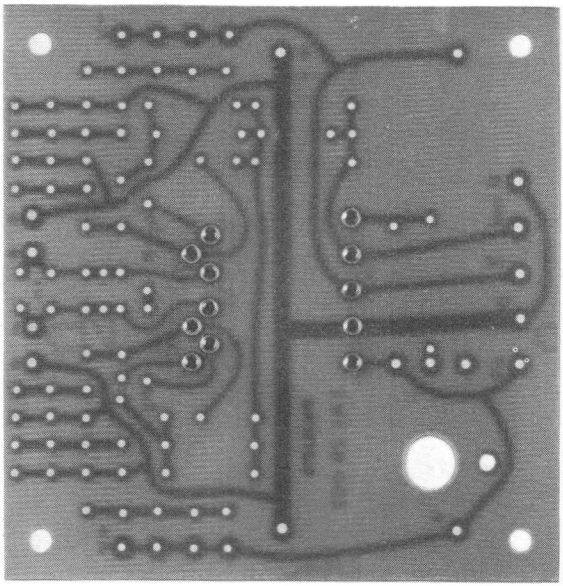
Thus, for R2 = R1 and R0 = Rf $\quad \dfrac{Vo}{Vin} = 1 + \dfrac{Rf}{R1}$

In this configuration $R_0 \geq 10$ kΩ.

The input impedance of this circuit is equal to the input impedance (min. 5 MΩ) of the normal DOA42 configuration without feedback (E1, E2, C shortcircuited). In those cases where a high input impedance differential amplifier is required, the DOA42 offers a unique solution.

ACCESSORIES

A printed-wiring board (see photograph) providing plug-in facilities for the DOA42 can be ordered separately under catalogue number 4332 000 00501.
This board will also accommodate a trimming potentiometer.



RZ 26423-5

DIFFERENTIAL ZERO DETECTOR

GENERAL

This unit can be used as a zero detector, voltage comparator, polarity detector, adjustable discriminator or differential amplifier.
Its feature of offering compatible signals for digital systems (e.g. composed of circuit blocks of the 10- or 20- Series) makes this unit a natural interface in hybrid systems.
The DZD 40 has been used succesfully in a wide range of instruments and control systems:

- digital to analogue and analogue to digital converters
- flux meter with digital read out
- automatic pH control system
- electronic potentiometer
- voice or no-voice detector
- automatic frequency characteristic testing
- over and under voltage detection
- over-dissipation switch in transmitter power stage
- servo control
- gas leak detector.

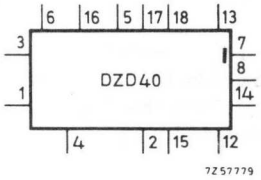
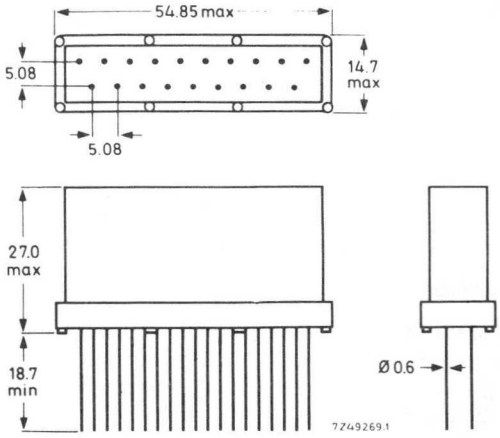


Fig.1 Drawing symbol

Dimensions in mm



The complete circuit is potted inside a metal can with 19 wire terminals.
The can is internally connected to the 0V supply (terminal 10).

Fig.2

Ambient temperature range

operating	0 to 70 °C
storage	−40 to +85 °C

Power supply
Supply voltages

V_P= + 12V ± 5%, V_N= - 12V ± 5%
or V_P= + 15V ± 1%, V_N= - 15V ± 1%
($V_V = V_B = V_{P'}$ = approx. V_P)

Nominal consumed current at nominal values of V_P and V_N

I_P = 6 mA, I_N = 8.3 mA

CIRCUIT DESCRIPTION

The differential zero detector comprises a two stage d.c. - coupled differential amplifier followed by an OR-gate and an inverting amplifier.
A voltage difference between the input terminals W_1 and W_2 is amplified about 1000 x by the two stage complementary differential amplifier (TR_1, TR_2, TR_3, TR_4). This amplified voltage difference is applied to the bases of TR_6 and TR_7.
As long as $|V_{A1} - V_{A2}|$ is less than a certain voltage, TR_5 is conducting.
If this voltage is exceeded TR_6 or TR_7 becomes conducting, the base current of TR_5 (via R_{10}) diminishes, the voltage across R_{14} goes up and TR_5 is cut off. So if the input voltage difference between W_1 and W_2 has a certain value either TR_6 or TR_7 are conducting (depending upon the polarity of $|V_{W_1} - V_{W_2}|$) and TR_5 is not conducting. From this it can be seen that V_{Q_1} and V_{Q_2} are in phase opposition with regards to V_{W_1} and V_{W_2}.

Truth table

inputs		outputs		
W_1	W_2	Q_1	Q_2	Q_3
high	high	high	high	low
high	low	low	high	high
low	low	high	high	low
low	high	high	low	high

High-high and low-low in the input rows indicate that signals applied to the inputs differ less than the trip value.

High-low and low-high in the input rows indicate that the voltage difference applied to the input exceeds the trip value.

In the output columns, high stands for +12 V and low for 0 V approximately.

It will be noticed that only one output terminal will be low for any input combination.

Current mode switching (no bottoming of transistors) is used to obtain high switching speeds and to reduce loading of the amplifier.
For this reason the terminals Q_1 and Q_2 should be connected to terminal 0 V if not used and they should be clamped with diodes (as for TR_5) if they are used.

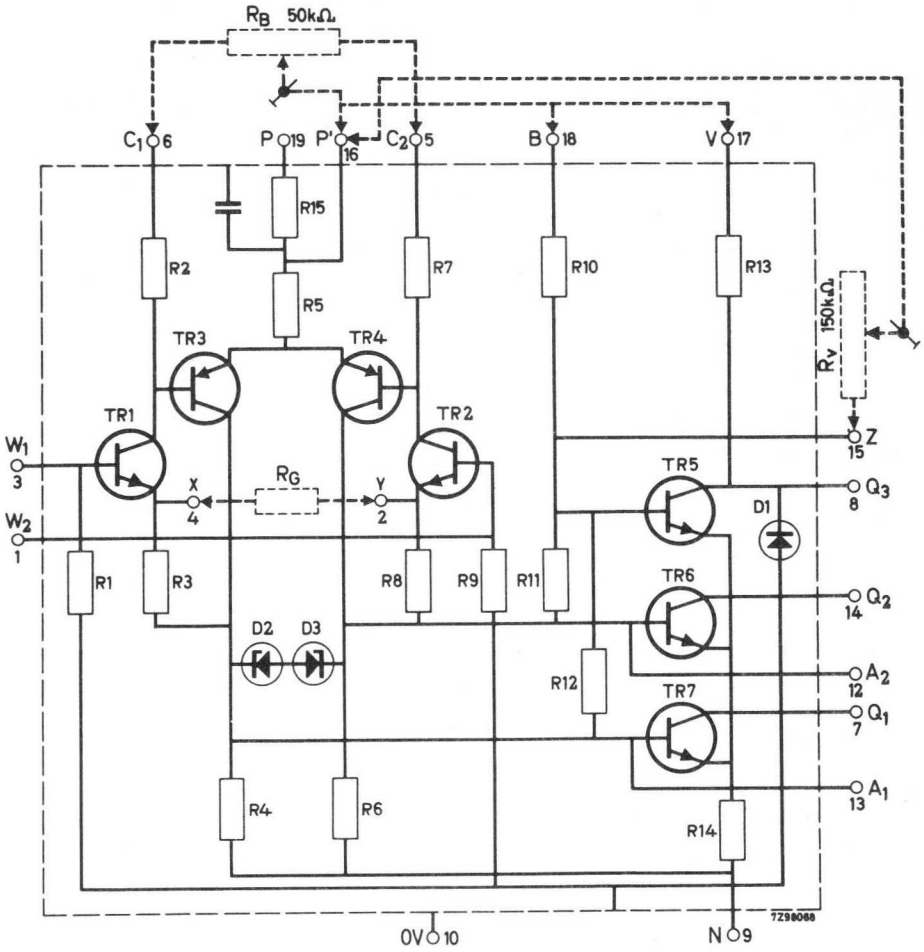


Fig.3. Circuit diagram

Terminal P' should be connected to terminal B for fixed bias or to variable resistor R_V for fine-gain adjustment.

Avoid a shortcircuit between terminals Q_3 and N, as this will damage diode D_1.

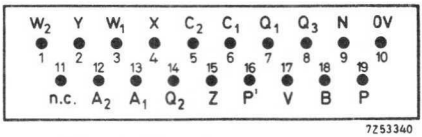


Fig.4. Terminal location

Oscillograms of some voltages with an input voltage of 8 mV_{p-p}, 100 kHz, are shown in the figures below.

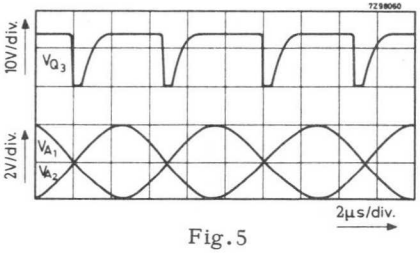


Fig.5

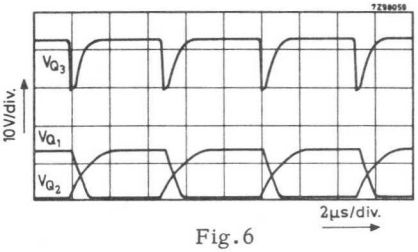


Fig.6

INPUT DATA

Differential off-set voltage after balancing (see "Initial adjustments")	0.1 mV
Voltage drift as a result of a change in temperature, measured at a source impedance of 10 kΩ	
typical value	3 µV / deg C
maximum value	5 µV / deg C
Differential sensitivity ($\lvert V_{W_1} - V_{W_2} \rvert$)	adjustable by means of gain control resistor R_G between X and Y; see graphs below

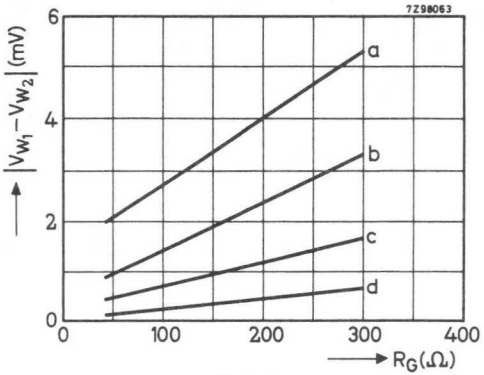
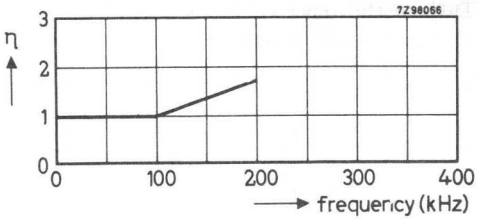


Fig. 7

The curves a and d are worst case limits at T_{amb} = 0 °C.
Curve a applies to the minimum input signal at which TR_5 or TR_6 is conducting (V_{Q_1} or V_{Q_2} is low) and TR_7 is not conducting (V_{Q_3} is high).
Curve d applies to the maximum input signal at which TR_5 or TR_6 is not conducting (V_{Q_1} and V_{Q_2} are high) and TR_7 is conducting (V_{Q_3} is low).
The curves b and c give typical values at T_{amb} = 25 °C.
Curve b : as a.
Curve c : as d.

η = input requirement factor for frequencies over 100 kHz (1.8 at 200 kHz, 1 up to 100 kHz)

Fig.8



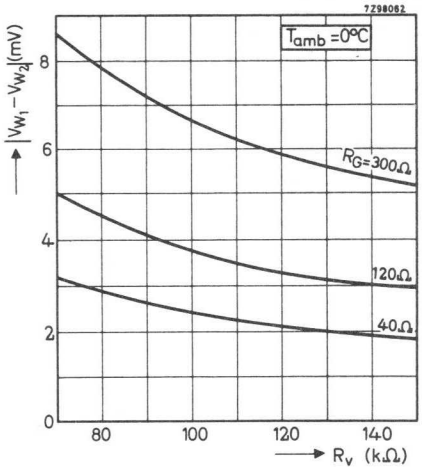


Fig. 9

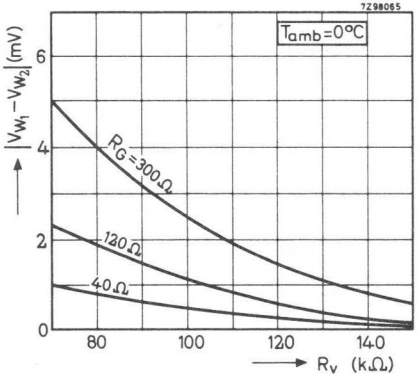


Fig. 10

The curves apply to the minimum input signal at which TR_5 or TR_6 is conducting (V_{Q1} or V_{Q2} is low) and TR_7 is not conducting (V_{Q3} is high).

The curves apply to the maximum input signal at which TR_5 and TR_6 are not conducting (V_{Q1} and V_{Q2} are high) and TR_7 is conducting (V_{Q3} is low).

Maximum value of $\lvert V_{W_1} - V_{W_2} \rvert$ to avoid extra delays	700 mV
Maximum voltage between input terminals	5 V
Frequency range	0-200 kHz. From 100 to 200 kHz the differential sensitivity reduces; the input voltage must be multiplied by the factor η (see Fig.8)
Maximum common mode voltage	$\pm$ 2V
Common mode rejection $\lvert V_{A1} - V_{A2} \rvert$ (typical value)	80 dB
Differential off-set current	< 30 nA
Current drift as a result of a change in temperature (typical value)	1 nA / deg C

Differential input resistance (R_i)	see Figs.11 and 12
Common mode impedance (typical value)	1.2 MΩ

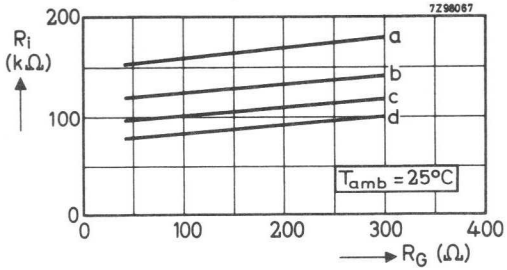


Fig.11

Curve a : typical differential input resistance
Curve b : typical input resistance between each input and 0 V
Curve c : minimum differential input resistance
Curve d : minimum input resistance between each input and 0 V

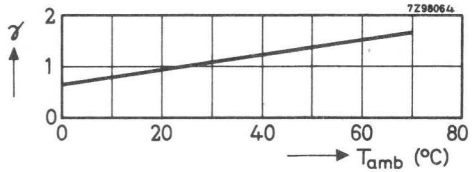


Fig.12. $\gamma = \frac{R_i \text{ at } T_{amb}}{R_i \text{ at } T_{amb} = 25\ ^oC}$

OUTPUT DATA

Outputs A_1 and A_2

Voltage gain	see Fig. 13
Maximum undistorted voltage $V_{A_1} = -V_{A_2}$	1 V
Band width at 3 dB	0 - 150 kHz
Minimum load resistance	100 kΩ

Outputs Q_1 and Q_2 *)

Maximum current at $V_Q > 0V$ **)	3.5 mA
Load resistance	3.6 kΩ

Output Q_3	V and P' interconnected	V and P' not interconnected
Maximum current	2.5 mA	3.5 mA
Load resistance	5 kΩ	3.6 kΩ

*) If the outputs Q_1 and Q_2 are not used these terminals should be connected to terminal 0 V.

**) Clamp diodes (e.g.BAX13, BAY38, 1N4009) must be externally connected to Q_1 and Q_2.

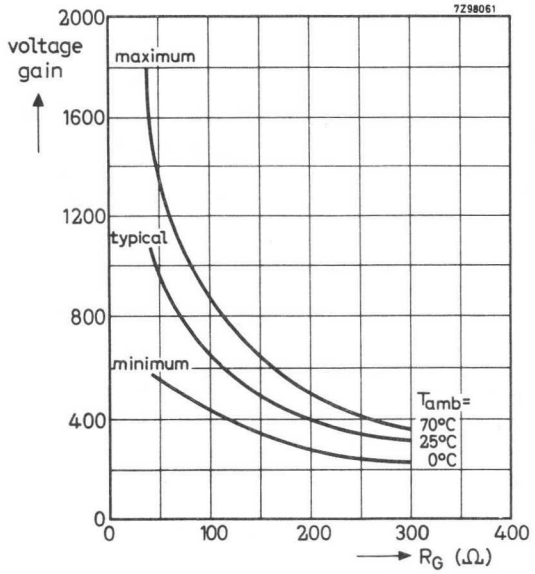


Fig.13

APPLICATION INFORMATION

Application hints

1. Avoid a shortcircuit between the terminals Q_3 and N as diode D_1 (see diagram) will be damaged.
2. In order to avoid instabilities due to transient switching voltages arising on supply lead inductance, the supply terminals N and P should be decoupled directly to terminal 0 V by means of low inductance capacitors.
3. For slowly diminishing voltages below the trip level the dv/dt of the zero going output at Q_3 will be approximately 10000 times as that of the input signal. In case a faster dv/dt is required, the voltage at Q_3 should be applied to a pulse shaper (e.g. PS10, PS20).
4. The terminals Q_1 and Q_2 provide signals that can in most cases directly be used to trigger units of the 10- and 20- Series or logic circuits having similar input requirements.
5. In circuits where high voltages might be detrimental, it is good practice to protect the inputs by an antiparallel diode circuit, thereby limiting the voltage.
6. If possible, arrange the circuit so as to avoid common mode voltage presence on inputs.
7. With a.c. input signals of over 10 kHz a capacitor of 2200 pF should be connected to the terminals Z and 0 V. Then only d.c. common mode voltage is allowed.
8. If terminal V is left unconnected the resistance load on Q_3 can be 3.6 kΩ.

Initial adjustments

Minimum off-set voltage

Connect a trimming potentiometer (R_B, see diagram) of 50 kΩ to the terminals C1 and C_2, slider to terminal P'. Place the slider in the centre position.
Short circuit the input terminals W_1 and W_2.
Connect a resistor to the terminals X and Y to obtain the desired gain (see "Sensitivity", next section).
Connect a d.c. millivoltmeter with high input impedance or an oscilloscope to the terminals A_1 and A_2; the meter or the oscilloscope must be floating.
Apply the supply voltages; allow a few minutes for block temperature distribution to reach a stable value of reading of the amplified off-set voltage on the millivoltmeter.
Correct the off-set voltage by turning the slider of the trimming potentiometer in such a way that minimum reading on the meter or the oscilloscope is obtained. When reading comes below 20% of full-scale value, switch to higher meter sensitivity. A correct adjustment will show a final value of a few millivolts, depending upon the actual gain.
Observe the voltmeter or oscilloscope for some time after balancing has been obtained; the reading should be stable.
Remove the shortcircuit of the input terminals and remove the voltmeter or the oscilloscope. Leave the slider of the potentiometer in optimum position.

Notes - In case no particular requirement for balance is to be met, the trimming potentiometer can be replaced by resistors having the value found during the balance procedure.

Un-balance will give unequal output wave shapes on Q_1 and Q_2 as well as an alternation of two forms on Q_3 with a sinusoidal input voltage.

Sensitivity

Coarse adjustment can be done by connecting a resistor (R_G, see diagram) to the terminals X and Y; if a trimming potentiometer of 500 Ω is used for this purpose the gain can be set over a wide range. The terminals P' and B must be interconnected. For the correct value of R_G, see Fig. 7. After the resistor between the terminals X and Y has been adjusted, fine adjustment can be done by disconnecting terminal P' from terminal B and by connecting a variable resistor (R_V) of 150 kΩ to the terminals Z and P' (without influencing the input impedance).

APPLICATION SUGGESTIONS

Low voltage zero detector giving zero output at zero input

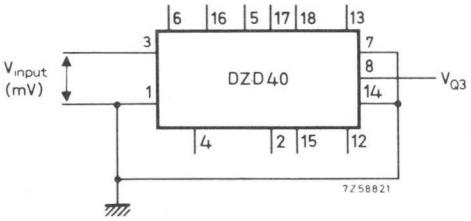


Fig.14

$V_{input} \ll 5\ V_{p-p}$ or $5\ V_{dc}$
$V_{Q3} = +V_{supply}$ as long as V_{input} is higher than the trip level.
$V_{Q3} = 0$ V as V_{input} has reached the trip level.
If V_{input} is an a.c. signal V_{Q3} will be high apart from the zero crossing points i.e. the unit acts as a bidirectional pulse shaper, see Fig.15.

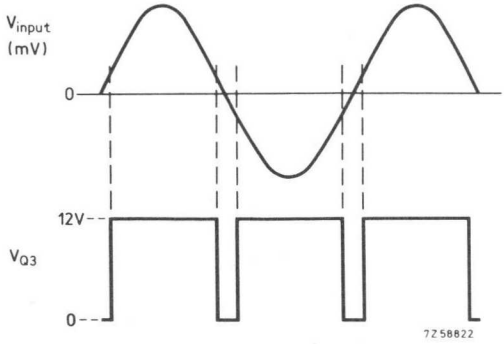


Fig.15

High voltage zero detector giving zero output at zero input

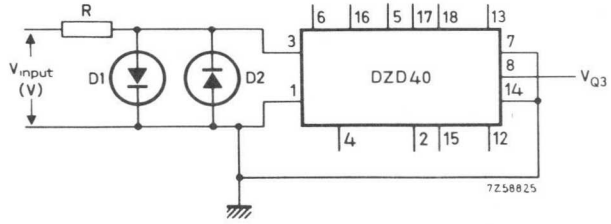


Fig.16

$V_{Q3} = +V_{supply}$ as long as V_{input} is higher than the trip level. $V_{Q3} = 0$ V as V_{input} has reached the trip level. If V_{input} is an a.c. signal V_{Q3} will be high apart from the zero crossing points i.e. the unit acts as a bi-directional pulse shaper (see Fig.15). D_1 and D_2 limit the input voltage. R serves to stay safely within diode current limits and loading of signal source possibilities.
If input frequency exceeds 10 kHz a capacitor of 2200 pF should be connected to the terminals Z and P' (see Figs.3 and 4).

Low voltage zero detector giving complementary outputs

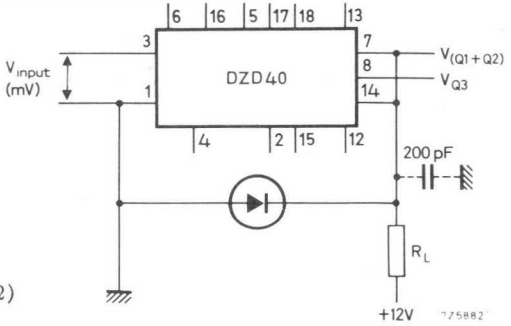


Fig. 17
(R_L = min. 3.6 kΩ)

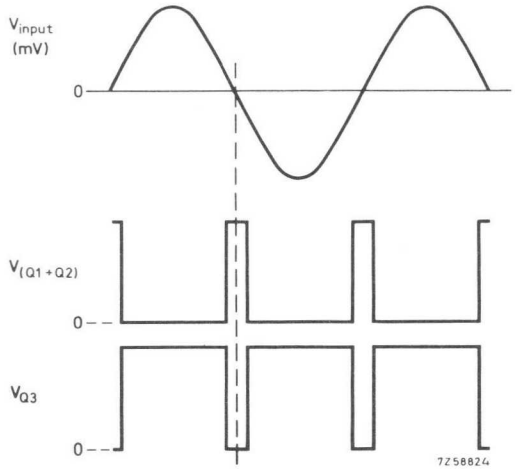


Fig. 18

V_{Q_3} may be obtained as well with this circuit, but then it is advisable to give Q_1 and Q_2 a capacitive load of 200 pF or more.

High voltage zero detector giving complementary outputs

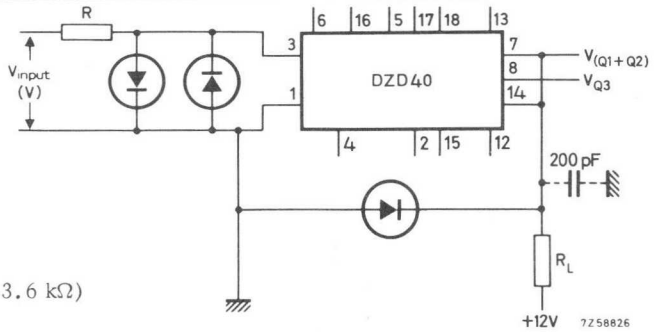


Fig. 19
(R_L = min. 3.6 kΩ)

Low voltage comparator giving zero output at zero difference input

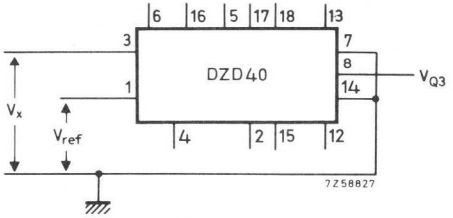


Fig. 20

V_X and $V_{ref} < 1$ V
$V_{Q_3} \approx 0$ V, if $|V_X - V_{ref}| <$ trip level

Low voltage comparator giving high output at zero difference input

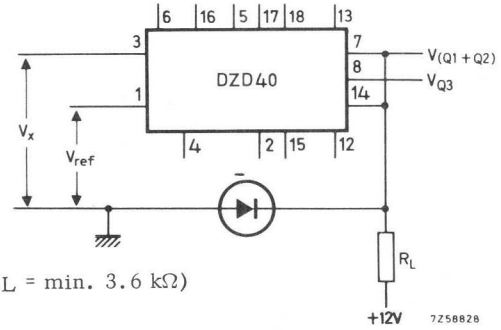


Fig. 21. (R_L = min. 3.6 kΩ)

$V_{(Q_1 + Q_2)}$ = high if $|V_X - V_{ref}| = 0$ V.

High voltage comparator for d.c. voltages

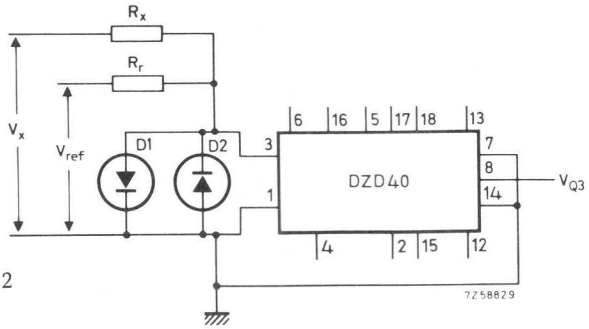


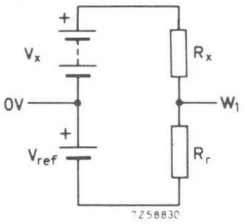
Fig. 22

The outputs can also be arranged as in Fig. 21.

This circuit avoids common mode difficulties. The clamping diodes D_1 and D_2 are to be used if the voltage between 3 and 1 could possibly exceed 5 V.

Note - V_{ref} and V_x are to be operating in series (i.e. not opposition).

Calculation of R_x and R_r.



The voltage between the terminals 0V and W_1 will be zero if

$$\frac{V_x}{V_{ref}} = \frac{R_x}{R_r}$$

R_x and R_r can be selected taking into account the loading of the sources V_r and V_x.

Fig. 23

Example - V_x is a potential between + 60 and + 95V with respect to the 0V line. V_r is a properly connected reference source of 5 V. Both sources can be loaded with 1mA max.

It is desired to produce a positive output signal whenever V_x = 80 V. As $V_x$max = 95V, the total voltage across $R_x + R_r$ is max. 100V. To stay within loading $R_x + R_r$ must be approx. 100 kΩ.

Furthermore $\frac{R_x}{R_r} = \frac{80}{5}$ for zero detection at 80 V, so $R_x = 16\ R_r$.

When R_r = 6.8 kΩ a trimming potentiometer of 150 kΩ can be used for R_x. The output can be taken from $(Q_1 + Q_2)$ as in Fig. 21.

Polarity detector

Use is made of the terminals Q_1 and Q_2, if desired terminal Q_3 can be used to indicate zero difference input.

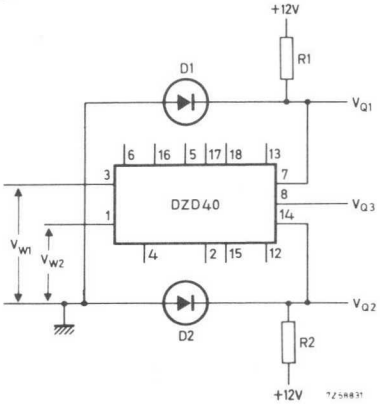


Fig. 24

V_{Q_1} is low, if W_1 (terminal 3) is high.
V_{Q_2} is low, if W_2 (terminal 1) is high.

Clamping diodes across the inputs can be omitted if the input voltages are $< 1\ V_p$.

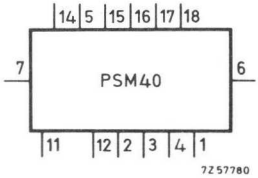
This circuit is extremely useful in servo control, direction determination and tolerance automation.

To avoid common mode influence V_{W_1} and V_{W_2} should be made lower than 2V (resistive step down).

PHASE SHIFT MODULE

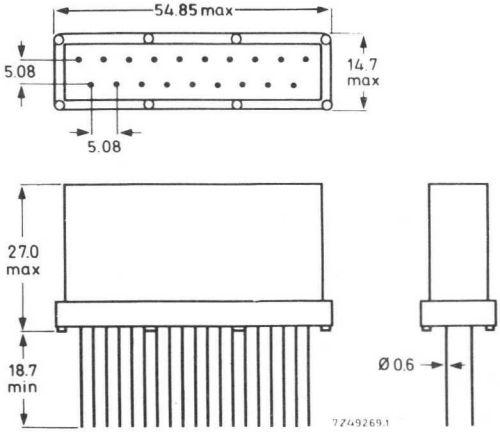
GENERAL

This phase shift module is designed for use in conjunction with a trigger source (e.g. TTM) for the control of the conduction angle of thyristors.
It can be used in single-phase, half- or full-wave applications for control of thyristors operating with an a.c. supply of 15 to 10 000 Hz. The control range is better than 10 to 170°. Three PSM's can be synchronised for 3-phase full-wave control.
An important feature is that one can make a choice between two operation modes, i.e. either linear control of conduction angle by means of a control voltage or linear control of the average voltage across the thyristor load (cosinusoidal control). In the latter case the average thyristor load voltage can be made independent of the a.c. supply voltage (see "CONTROL FACILITIES").



Drawing symbol

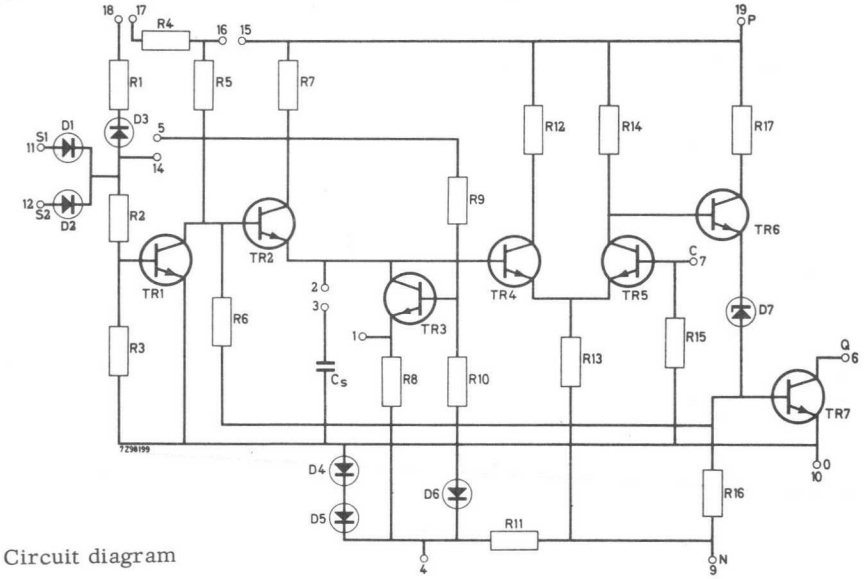
Dimensions in mm



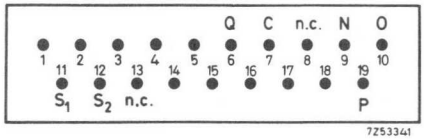
The complete circuit is potted inside a metal can with 19 wire terminals.

CIRCUIT DESCRIPTION

For operation on 50 Hz, terminals 2 and 3 have to be interconnected. Transistor TR_1 is conducting during most of the period that the synchronization voltages are present on S1 and S2. Thereby the collector of TR_1 will be at a low voltage, therefore TR_2 will be non conducting during the time that TR_1 conducts. As soon as the value of the synchronization voltage becomes lower than the diode forward voltage drop (around the zero crossing of the synchronization signal) TR_1 ceases to conduct, TR_2 rapidly charges C_S. A few electrical degrees after synchronization zero TR_1 becomes conducting again, TR_2 cuts off.
TR_3 discharges C_S during the half cycle to zero volts. TR_4 and TR_5 constitute a long tailed pair comparator. As long as the voltage to the base of TR_4 exceeds that applied to TR_5, TR_4 is conducting and TR_5 is off. Consequently base current will flow to TR_6 through R_{14} and TR_6 will conduct. The emitter current of TR_6 drives TR_7 into saturation so that the output Q will be at a low potential for the time that the voltage on point 2 is higher than that applied to the control input terminal C.
The discharge of C_S as a function of time can be made linear by means of TR_3 acting as a constant current discharger or cosinusoidal discharger by using different circuit connections.



Circuit diagram



Terminal location

TECHNICAL PERFORMANCE

Operating temperature range	−25 to +85 °C
Storage temperature range	−40 to +85 °C

Power supply

Supply voltage	V_p = + 12 V ± 5%, V_N = −12 V ± 5% or V_p = + 12 V + 10%, V_N = −12 V + 10% or V_p = + 12 V − 10%, V_N = −12 V − 10%
Consumed current	$I_p = I_N$ = approximately 10 mA (excluding load current)

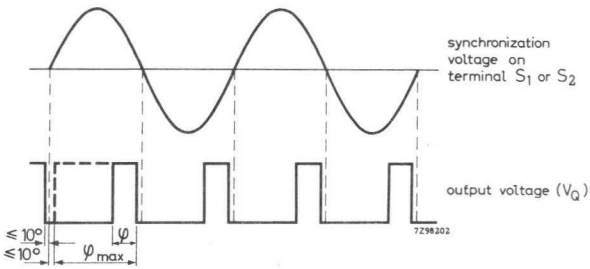
Note - As the output voltage V_Q is dependent upon switch on sequence and rise time of the supply voltages, it is recommended to short circuit terminal Q temporarily to terminal 0 when switching on.

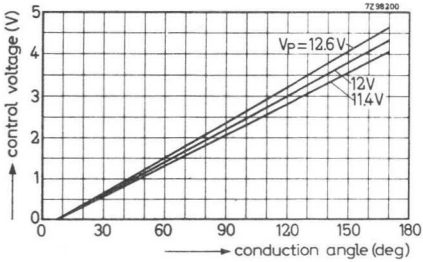
Input data

Control voltage (V_C)	
absolute maximum	5 V
absolute minimum	0 V
Control current (I_C)	0.5 to 0.33 mA
Maximum wiring capacitance at the control input (terminal C)	200 pF

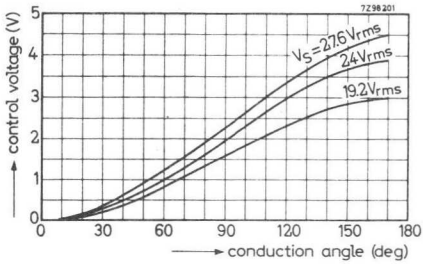
Output data

Output voltage (V_Q)	
high level (TR_7 non conducting)	max. 15 V
low level (TR_7 conducting)	max. 0.5 V min. 0 V
Output current (I_Q)	max. 25 mA at V_Q = max. 0.5 V (T_{amb} = −25 °C)
Minimum control range of conduction angle (φ)	10 − 170°





Linear control



Cosinusoidal control

Synchronization

Synchronization voltage (V_S)	24 V_{rms}, + 15%, -20%
Nominal synchronization current (I_S)	
at linear control	approx. 4 mA
at cosinusoidal control	approx. 8 mA

The synchronization voltage can be supplied by a transformer with or without a center tap and preferably provided with an electrostatic screen between the primary and the synchronization winding to avoid capacitive zero shift.

When a transformer with a center tap is used the outputs of the transformer have to be connected to the terminals S_1 and S_2, whereas the center tap is connected to terminal 0.

When a transformer without a center tap is used the outputs of the transformer have to be connected to the terminals S_1 and S_2. Furthermore two diodes OA200 or an equivalent type, have to be connected with the cathode to the terminals S_1 and S_2, whereas the anodes of these diodes have to be connected to terminal 0.

Synchronization frequency range 15 to 10 000 Hz

When the terminals 2 and 3 are interconnected the unit can be used at a synchronization frequency of 50 Hz.
For frequencies higher or lower than 50 Hz the terminals 2 and 3 have to be left disconnected and an external capacitor has to be connected between the terminals 2 and 0.
Capacitance as a function of the frequency: $C = \frac{11}{f}\ \mu F$

CONTROL FACILITIES

Linear conduction angle control

The conduction angle is proportional to the control voltage. The terminals 5, 15 and 16 have to be interconnected. The terminals 15 and 16 can also be interconnected by means of an adjustable resistor, in case of multi-phase operation.
The conduction angle can be controlled by a voltage level on the control input (terminal C).
When the control voltage is derived by a potentiometer from the d.c. voltage which supplies the conduction angle determining part of the circuit (terminal 16) the variations of the conduction angle, caused by supply voltage variations, are greatly reduced.

Cosinusoidal control of the conduction angle

The course of the conduction angle (φ) as a function of the control voltage (V_c) is given in the formula:

$\varphi = \arccos (1 - aV_c)$, in which

$a = \text{approx.} \frac{11}{V_{s_{rms}}}$

At a constant value of the control voltage the variations of the average voltage across the thyristor load, caused by the mains voltage variations, can be greatly reduced as follows.
The conduction angle determining part of the circuit has to be supplied by a full-wave rectified voltage (proportional to the mains voltage) and by a smoothed voltage derived from the mentioned voltage.
Therefore the terminals 14 and 5 have to be interconnected and the terminals 17 and 18 have to be interconnected directly or by means of an adjustable resistor (multi-phase operation). Furthermore an electrolytic capacitor of 100 μF, 40 V has to be connected between terminals 18 and 10.

ADJUSTMENT

1. Single-phase operation

To obtain a conduction angle of 0^{o} at a control voltage of 0 V, a resistor has to be connected between terminals 1 and 4. For determining its value the following procedure has to be done.
Connect an adjustable resistor with a control range up to 47 kΩ between the terminals 1 and 4, a resistor of 1 kΩ between the terminals Q and P and a d.c. voltmeter between the terminals Q and 0. The control input terminal C has to be connected to terminal 0. Furthermore the necessary interconnections for linear or cosinusoidal control have to be made. Apply the synchronization and d.c. supply voltages.
The output voltage will be about 0 V when the adjustable resistor has its maximum value. This resistor has to be decreased until the moment the output voltage starts to increase. The conduction angle is now close to 0^{o} at a control voltage of 0 V.
The unit is ready for use after the resistor of 1 kΩ and the voltmeter are removed.

Note - After the resistance value has been determined the variable resistor may be replaced by a fixed resistor of the same value as the inherent stability is such that no readjustment will be required.
Typical value of the resistor for linear control: 10 kΩ, for cosinusoidal control: 33 kΩ.

2. Multi-phase operation

To obtain equal conduction angles of two or more PSM's at a common control voltage within the whole control range the following has to be done.

a. Linear control

Interconnect the terminals 5, 15 and 16. Apply the d.c. supply voltages; the synchronization voltage is not applied. Measure the voltage on terminal 2. This voltage should be equal for all PSM's. If there is a difference between the voltages on terminals 2 a resistor has to be inserted between the terminals 17 and 18 of the unit with the highest voltage on terminal 2. The value of this resistor is approximately 1 Ω per mV voltage difference. For further adjustment, see 2c.

b. Cosinusoidal control

Connect terminal 5 to 15 and terminal 17 to 18. Apply the d.c. supply voltages to the terminals P and N and a d.c. voltage of 30 V to terminal 18; the synchronization voltage is not applied. The same measurements have to be done as for linear control.
If there is a difference between the voltages on terminal 2 of two PSM's a resistor has to be inserted between the terminals 17 and 18 of the unit with the highest voltage on terminal 2. The value of this resistor is approximately 3 Ω per mV voltage difference. For further adjustment, see 2c.

c. With the adjustments described in 2a and 2b the conduction angles of the units will be equal at high values of the control voltage (> 4 V). To obtain equal conduction angles at low values of the control voltage the following has to be done.

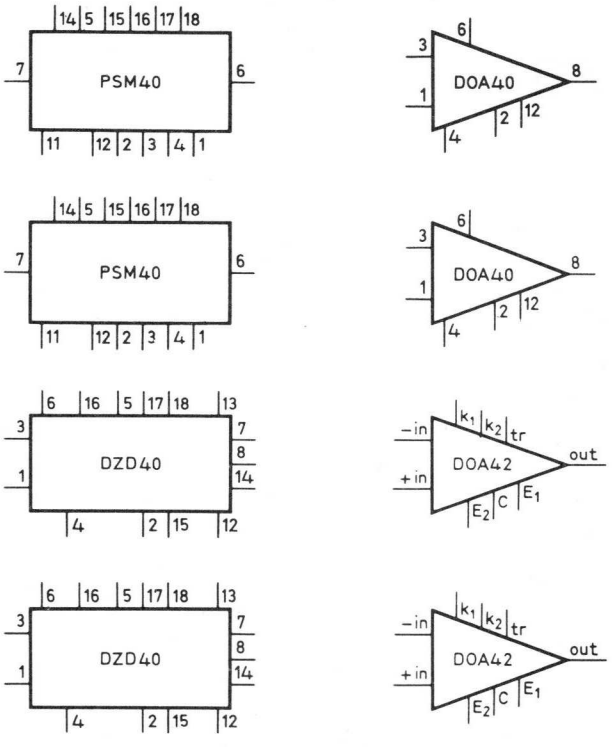
The units have to be connected for the desired mode of operation.

Adjust one unit so that a conduction angle of 0° at a control voltage of 0 V is obtained (see 1).

Apply a control voltage of 1 V to all units. Connect a d.c. voltmeter between output Q of the unit which has been adjusted and output Q of the unit to be adjusted. These outputs have to be connected via a resistor of 1 kΩ to terminal P. Vary the value of the resistor between the terminals 1 and 4 of the unit to be adjusted, until minimum reading on the voltmeter has been obtained. Now the conduction angles of both units will be equal within the whole control range.

STICKERS

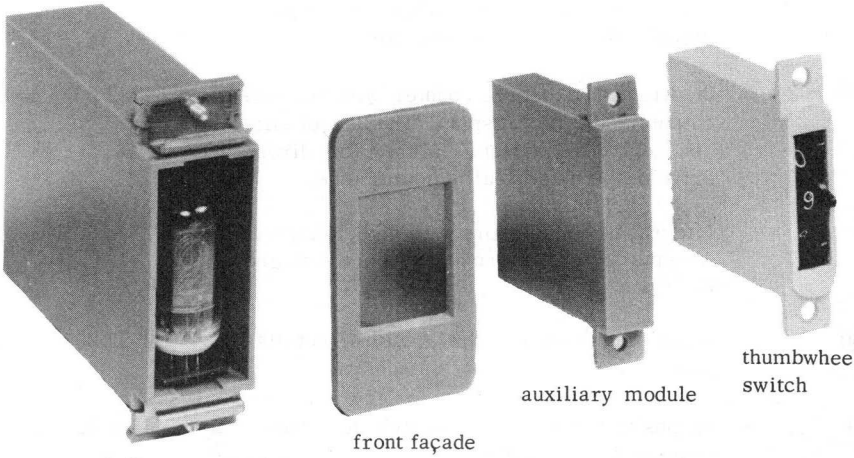
These are drawing symbols of 40-Series circuit blocks printed on self-adhesive, transparent material on which one can write. They can be used for fast preparation of system drawings.
The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 71951.



12NC 4322 026 71951

COUNTER MODULES
50-SERIES

INTRODUCTION



The 50-Series contains uni-directional and bi-directional decade counters with direct display and a number of auxiliary modules offering a complete range of building modules for industrial automation and control.
The use of silicon semiconductors, including silicon-controlled switches (SCS), ensures reliable operation over a wide temperature range.
The simple rules regarding electrical interconnections, mounting accessories and interwiring of the compact self-contained cases, make the 50-Series ideal for immediate installation and assembly in a large variety of applications. Preset programmed control with the aid of compatible preset switches and input/output devices offer excellent possibilities for:

- industrial batch counting
- automatic winding machines
- sequential control and timing
- numerical control systems
- automatic weighing and dosing
- speed control, etc.

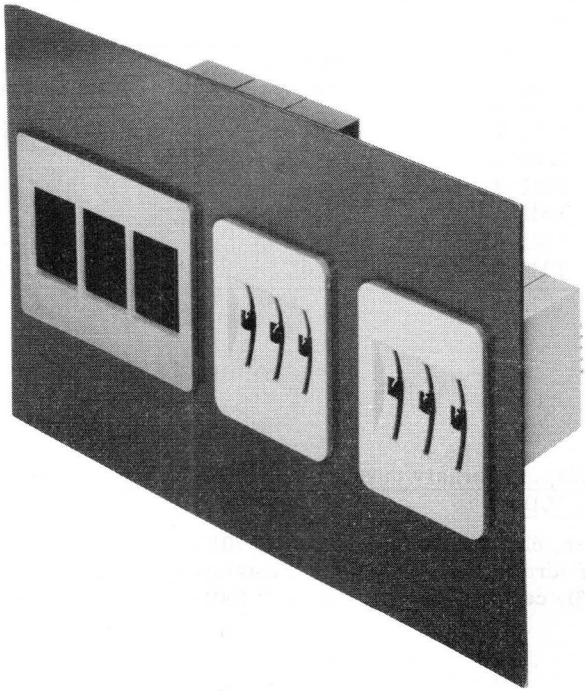
MODULES

The 50-Series comprises the following modules:

type	description	catalogue number
NIC50	Uni-directional decade counter with decimal outputs and direct display. The use of silicon controlled switches allows for direct drive of the numerical indicator tube.	2722 007 03001
RIC50	Bi-directional decade counter with decimal outputs and direct display. The use of silicon controlled switches allows for direct drive of the numerical indicator tube.	2722 007 04001
MID50	Integral buffer memory with direct display. Accepts decimal information from NIC50 and RIC50.	2722 007 05001
SID50	+ and - sign indicator driver with direct display.	2722 007 06001
SU50	10 position thumbwheel switch for preset counting (type 10P1C).	4311 027 82321
3.NOR50	Buffer adaptation stage and double NOR for sequential and combinational logic operations. The latter can be cross connected to form a d.c. memory function.	2722 007 00001
4.NOR51	Quadruple NOR for sequential and/or combinational logic operations. Two d.c. memory functions can be made from the four NOR's.	2722 007 00011
PSR50	Pulse shaper combined with an automatic/manual reset unit.	2722 007 01001
LRD50	300 mA, 30 V output stage for lamp and relay drive.	2722 007 02001
PDU50A and PDU50B	Printer drive units	2722 007 08001 2722 007 08011

type	description	catalogue number
PSU50	Power supply unit Input: 110, 220, 230, 240 V_{ac} ±10%, −15%; 45 to 65 Hz Output: a) 24 V_{dc}, ±5%, 250 mA (logic supply) b) 250 V_{dc}, ±18% (supply for 12 indicator tubes)	2722 151 00061
DCD50	General purpose decade counter and divider	2722 007 07001
ECA50	Empty case assembly	2722 007 89001

For detailed electrical information on the above-mentioned modules, see the relevant data sheets; for data on the SU50, see the data sheets of thumbwheel switches 4311 027 8.....
For detailed application information the Application Book "Design with 50-series modules", print number 9399 263 06001, should be consulted. ←



RZ 23932-1

→ MOUNTING ACCESSORIES

Front façades for indicator modules (NIC50, RIC50, MID50 and SID50)

Front façades are available for one up to and including six indicator modules. They are provided with a coloured polarised screen.

type	number of indicator modules	catalogue number
FIC 1	1	4322 026 70340
FIC 2	2	70350
FIC 3	3	70360
FIC 4	4	70370
FIC 5	5	70380
FIC 6	6	70390

Mounting façades for thumbwheel switches (SU50)

Mounting façades, giving facilities for mounting one up to and including six switches, are available.

type	number of switches	catalogue number
FMF 1	1	4311 027 80598
FMF 2	2	80608
FMF 3	3	80618
FMF 4	4	80628
FMF 5	5	80638
FMF 6	6	80648

Mounting aids for auxiliary modules (3.NOR50, 4.NOR51, PSR50, LRD50, PDU50A, PDU50B and DCD50)

Mounting bar, catalogue number 4322 026 70170
Self tapping screws (2 pieces), 4Nx$\frac{1}{4}$", catalogue number 2522 163 01005
Washer (M3), catalogue number 2522 600 16016

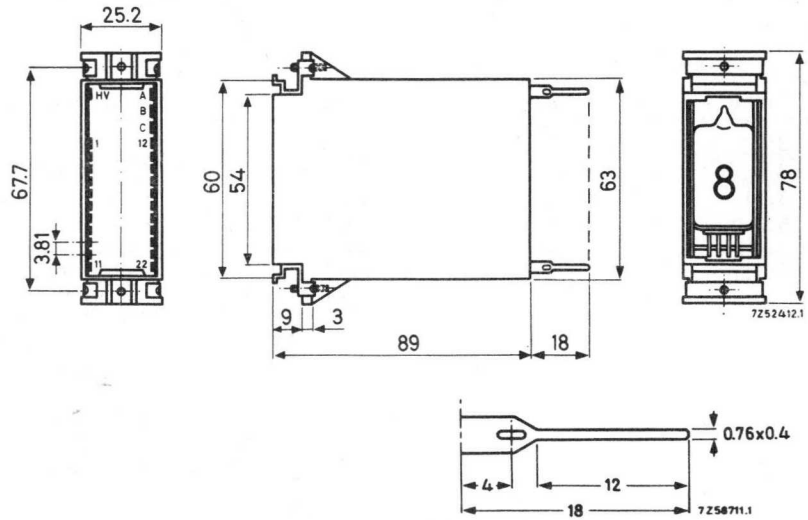
CONSTRUCTION

The various functions are housed in plastic cases, of which the dimensions and terminal locations are shown below.
Each module is provided with pins for soldering and wire-wrapping.

DIMENSIONS

The dimensions in the figures are given in mm; for inch values see the tables.

Indicator modules (NIC50, RIC50, MID50 and SID50)

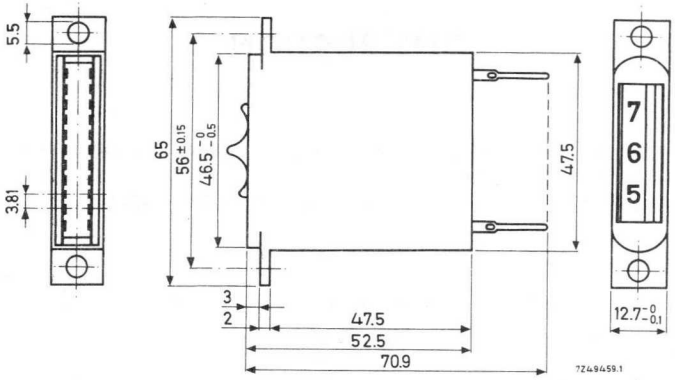


mm	inches
3	0.118
3.81	0.150
4	0.158
9	0.354
12	0.472
18	0.708
25.2	0.992
54	2.126

mm	inches
60	2.362
63	2.480
67.7	2.665
78	3.070
89	3.504

For detailed information on wire-wrapping, see the Application Book "Design with 50-Series modules, print number 9399 263 06001.

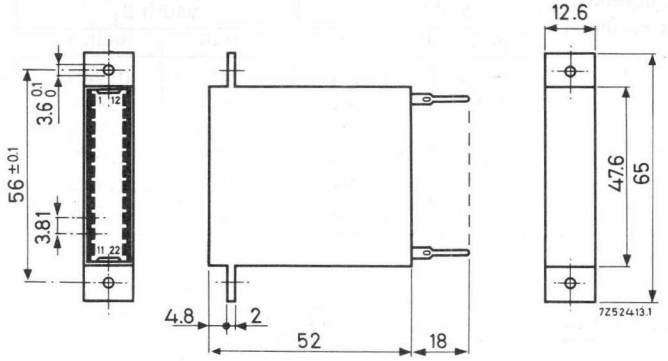
Thumbwheel switch (SU50)



mm	inches
2	0.078
3	0.118
3.81	0.150
5.5	0.216
$12.7^{-0}_{-0.1}$	$0.5^{-0}_{-0.004}$

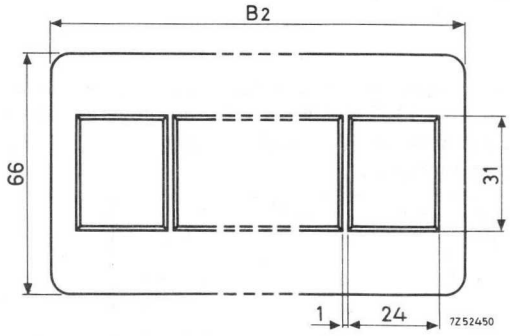
mm	inches
$46.5^{-0}_{-0.5}$	$1.831^{-0}_{-0.02}$
47.5	1.870
52.5	2.067
56 ± 0.15	2.205 ± 0.006
65	2.559
70.9	2.791

Auxiliary modules (3.NOR50, 4.NOR51, PSR50, LRD50, PDU50A, PDU50B and DCD50)

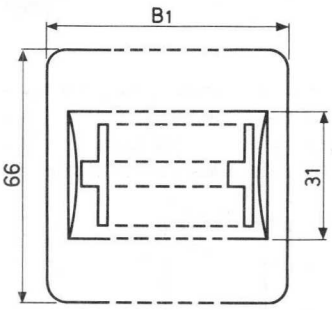


mm	inches	mm	inches
2	0.078	18	0.708
3.6 $^{0.1}_{0}$	0.142 $^{0.004}_{0}$	47.6	1.874
3.81	0.150	52	2.047
4.8	0.189	56 ± 0.1	2.205 ± 0.004
12.6	0.496	65	2.559

Façades



Front façade for indicator modules
(For B_2 see next page)



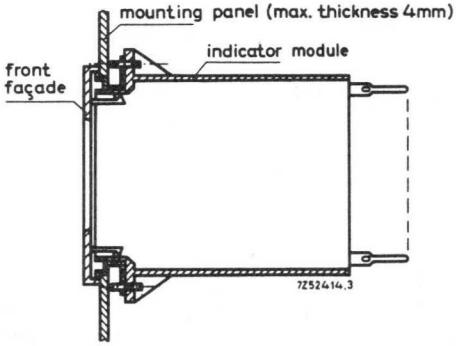
Mounting façade for thumbwheel switches
(For B_1 see next page)

mm	inches
1	0.039
24	0.945
31	1.220
66	2.598

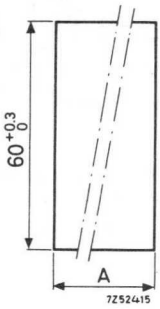
number of modules	indicator modules width B_2		thumbwheel switches width B_1	
	mm	inches	mm	inches
1	35.4	1.394	24	0.945
2	60.8	2.394	36.7	1.445
3	86.2	3.394	49.4	1.945
4	111.6	4.394	62.1	2.445
5	137.0	5.394	74.8	2.945
6	162.4	6.394	87.5	3.445

MOUNTING

Indicator modules (NIC50, RIC50, MID50 and SID50)



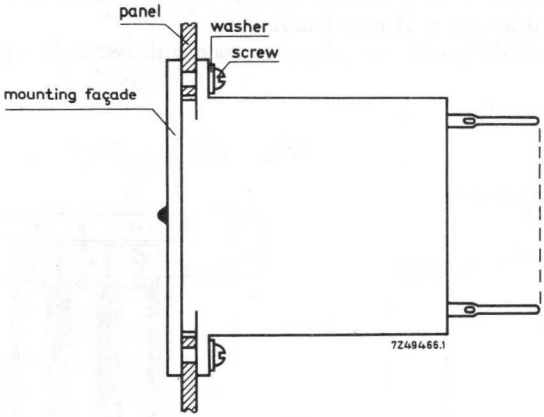
The module is fixed to a mounting panel by means of two screws. The maximum thickness of the mounting panel is 4 mm (0.157 inch). The aperture in the mounting panel is proportional to the number of indicator modules (see table below).
The front façades clip in to the indicator modules.



number of modules	width A	
	mm	inches
1	25.4 + 0.5	1 + 0.02
2	50.8 + 0.5	2 + 0.02
3	76.2 + 0.5	3 + 0.02
4	101.6 + 0.5	4 + 0.02
5	127.0 + 0.5	5 + 0.02
6	152.4 + 0.5	6 + 0.02

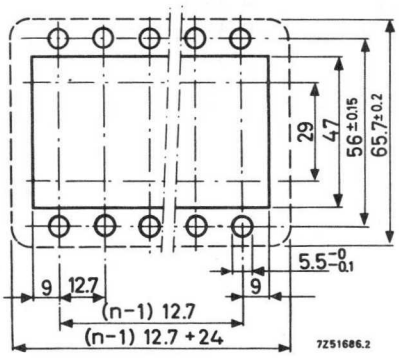
$(60^{+0.3}_{0}$ mm = $2.362^{+0.012}_{0}$ inch)

Thumbwheel switches (SU50)



The switches can be mounted in panels with a thickness up to 4 mm by means of mounting façades and the screws and washers supplied. When the panel thickness is less than 4 mm (0.157 inch), additional washers must be used between the panel and the switch.

The dimensions of the necessary apertures in the mounting panel are given in the drawing below; the outline of the mounting façade is indicated by a dash line.

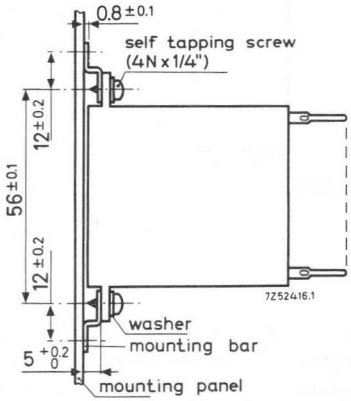


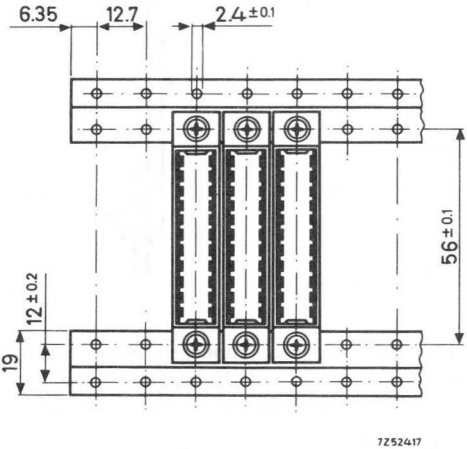
(n = number of switches)

mm	inches
$5.5^{-0}_{-0.1}$	$0.216^{-0}_{-0.004}$
9	0.354
12.7	0.5
24	0.945
29	1.142
47	1.851
56 ± 0.15	2.205 ± 0.004
65.7 ± 0.2	2.587 ± 0.008

Auxiliary modules (3.NOR50, 4.NOR51, PSR50, LRD50, PDU50A, PDU50B and DCD50)

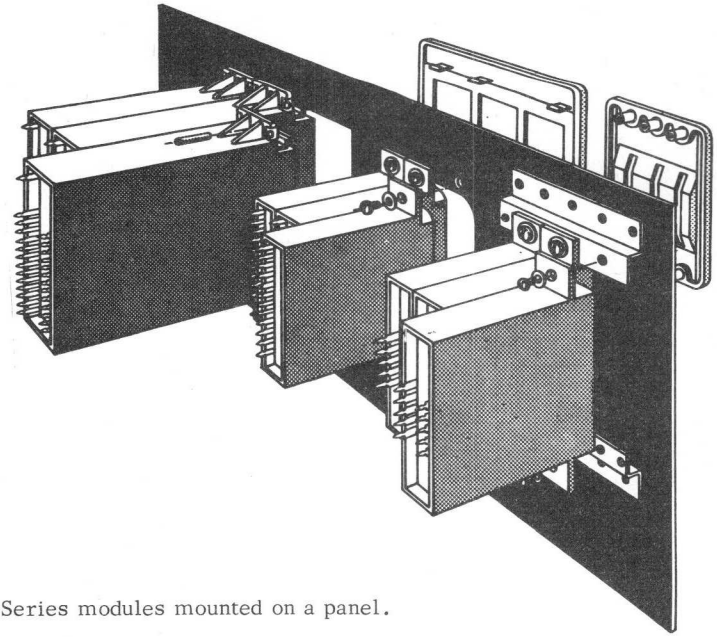
Auxiliary modules are to be fixed to a mounting panel with the aid of two metal bars (available in standard length of 21 positions).
The fixation of each module to the metal bar is done with two self tapping screws (4N x $\frac{1}{4}$inch).



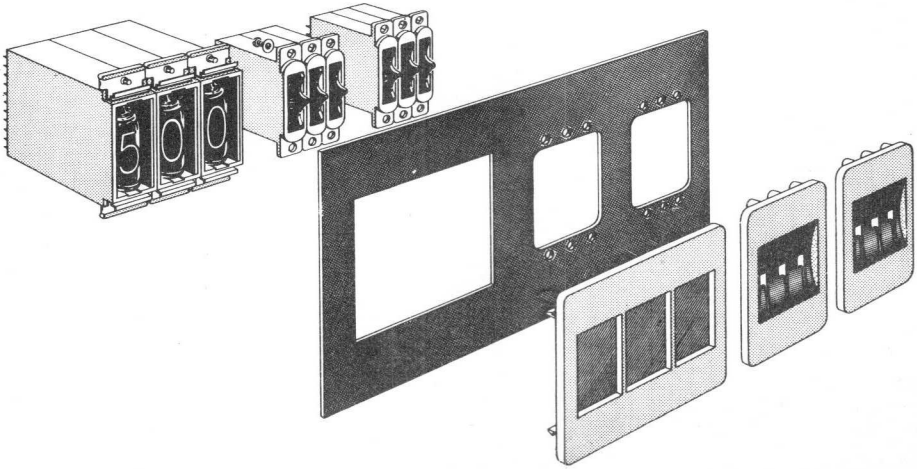


mm	inches
0.8 ± 0.1	0.032 ± 0.004
5 +0.2 0	0.197 +0.008 0
12 ± 0.2	0.472 ± 0.008
56 ± 0.1	2.205 ± 0.004

mm	inches
2.4 ± 0.1	0.094 ± 0.004
6.35	0.25
12 ± 0.2	0.472 ± 0.008
12.7	0.5
19	0.748
56 ± 0.1	2.205 ± 0.004



50-Series modules mounted on a panel.



CHARACTERISTICS

Ambient temperature range

Operating: -25 to +70 °C
-10 to +70 °C, for DCD50 at V_P = +24 V_{dc} ± 25%
Storage : -40 to +85 °C

Counting rate

Uni-directional: max. 50 kHz
Bi-directional : max. 12 kHz

Supply voltage

Logic supply: single rail, +24V_{dc} ± 10% [1)]
Tube supply : high voltage, +250V ± 18%

Fan out

Decade counter: the counter units can be loaded with 6 different programmes.

NOR gate : each output may be loaded with the inputs of six other NOR's. The NOR50 and NOR51 are fully compatible with NOR units of the 60-Series.

1) Note that output units may be operated from a supply voltage of +24V_{dc}, ± 25%.

TEST SPECIFICATIONS

All modules of the 50-Series are designed to meet the tests below. Before and during manufacture samples of modules are regularly subjected to these tests.

1. Shock test according to method 202B of MIL-STD-202C, 3 blows 50 g in 3 perpendicular directions.
2. Vibration test according to method 201A of MIL-STD-202C.
   Frequency 10-55 Hz, amplitude 0.76 mm max., cycle time 1 min, 2 hours in 3 perpendicular directions.
3. Temperature-cycling test according to method 102A of MIL-STD-202; 5 cycles from -40 to +100 °C.
4. Long-term humidity test according to I.E.C.68, test C.
   Duration 21 days at 40 °C and R.H. = 90-95%.
5. Solderability according to method 210 of MIL-STD-202.

LOADING TABLE

NOTES

By expressing the input requirements and output capabilities of most modules in "DRIVE UNITS (D.U)", system design is greatly simplified.
Moreover input requirements of all modules are additive.

*) Also suitable for driving 2 x C_F/C_R of RIC50.

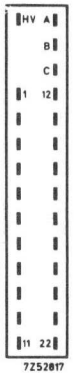
**) Two inputs in parallel or one input always floating.

type	function	input		output	
		terminal	required	terminal	available
NIC50	Uni-directional direct display counter	R	To be driven from Q_R of PSR50	Q_0-Q_9	To drive 6 x buffer NOR's + 1 x T-NIC50 + I_0-I_9 of 6 x MID50 + PDU50
		T	To be driven from Q_T of PSR50 or Q_0-Q_9 of NIC50		
RIC50	Bi-directional direct display counter	R	To be driven from Q_R of PSR50	Q_0-Q_9	To drive 6 x buffer NOR's + 1 x T-RIC50 + I_0-I_9 of 6 x MID50 + PDU50
		T_F/T_R	To be driven from Q_T of PSR50 or Q_0-Q_9 of RIC50		
		C_F/C_R	To be driven from Q of LRD50 or Q of NOR50/51		
MID50	Buffer memory with direct display	I_0-I_9	To be driven from Q_0-Q_9 of NIC50, RIC50 or MID50	Q_0-Q_9	To drive decimal input of PDU50 + I_0-I_9 of 3 x MID50
		T_C	To be driven from Q_R or Q_T of PSR50		
SID50	Driver plus and minus indicator tube	+ and - character	1 D.U.	none	Not applicable
3.NOR50	6 Input buffer NOR	G_1-G_6	To be driven from Q_0-Q_9 of NIC50 or RIC50	Q_1	2 D.U.
	Dual 4 input NOR	G_7-G_{14}	1 D.U.	Q_2/Q_3	6 D.U.*)
4.NOR51	Quadruple 4 input NOR	G_1-G_{16}	1 D.U.	Q_1-Q_4	6 D.U.*)

type	function	input		output	
		terminal	required	terminal	available
PSR50	Pulse shaper	B (via R = 39 kΩ)	2 D.U.	Q_T	2 x (T_R + T_F) - RIC50 + 2 D.U. or 4 x T-NIC50 + 2 D.U. or 6 x T_C-MID50
	Reset	T	1 D.U.	Q_R	6 x R-NIC50/RIC50 or 6 x T_C-MID50
		G	1 D.U.	Q_L	4 D.U.
LRD50	Lamp/relay driver	G_1-G_3	1 D.U.	Q	300 mA, 30V (abs.max.) or 6 x C_F/C_R -RIC50
PDU50A	Printer drive unit	I_0-I_9	To be driven from Q_0-Q_9 of NIC50, RIC50 or MID50	Q_0-Q_9	2 D.U.
		L	To be driven from L_1-L_3 of PDU50B		
PDU50B	Printer drive unit	C	To be driven from: -Q_T of PSR50 or -NOR unit**)	L_1-L_3	To drive input L of PDU50A
		S_1-S_3	To be driven from: -Q_0-Q_9 of NIC50 or RIC50 -DCD50 -NOR unit**)		
DCD50	Decade counter and divider	$T_A/T_C/T_D$ T_{B_1}/T_{B_2} S	0 D.U. 1 D.U. 1.5 D.U.	Q_A, $\overline{Q_A}$, Q_B, $\overline{Q_B}$, Q_C, $\overline{Q_C}$, Q_D, $\overline{Q_D}$	To drive 1 x T-NIC50/RIC50
		C_S	6 D.U.	Q_A, Q_B, $\overline{Q_B}$, Q_C, $\overline{Q_C}$	6 D.U. + 1 x T-DCD50 or 4 D.U. + 1 x B-PSR50
				$\overline{Q_A}$, Q_D, $\overline{Q_D}$	see data sheet

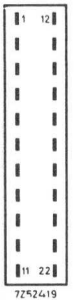
Survey of terminal location

terminals	indicator modules (Fig.A)				auxiliary modules (Fig.B)						
	NIC50	RIC50	MID50	SID50	3.NOR50	4.NOR51	PSR50	LRD50	PDU50A	PDU50B	DCD50
HV	V_{p3}	V_{p3}	V_{p3}	V_{p3}	not provided	not provided	not provided	not provided	not provided	not provided	not provided
A	not provided	not provided	LS	X	not provided	not provided	not provided	not provided	not provided	not provided	not provided
B	not provided	not provided	T_C	Y	not provided	not provided	not provided	not provided	not provided	not provided	not provided
C	not provided	not provided	I_0	Z	not provided	not provided	not provided	not provided	not provided	not provided	not provided
1	V_{p1}	V_{p1}	V_{p1}	V_{p1}	V_{p1}	V_{p1}	V_{p1}	not provided	I_1	V_{p1}	V_{p1}
2	0	0	0	0	0	0	0	0	I_2	0	0
3	not provided	C_F	I_1	not provided	G_1	G_1	Q_R	V_{p2}	I_3	K_1	$\overline{Q}_D$
4	not provided	C_R	I_2	not provided	G_2	G_2	Q_L	not provided	I_4	K_2	Q_D
5	F	F	I_3	not provided	G_3	G_3	Q_T	Q	I_5	L_1	Q_C
6	not provided	not provided	I_4	+	G_4	Q_2	i.c.	not provided	L	L_2	$\overline{Q}_C$
7	Q_5	Q_5	Q_5	-	G_5	Q_1	B	not provided	Q_1	L_3	T_{D_2}
8	Q_4	Q_4	Q_4	not provided	G_6	G_5	Z	G_1	Q_2	S_1	T_{D_1}
9	Q_3	Q_3	Q_3	not provided	D_1	G_6	A	G_2	Q_3	S_2	T_C
10	Q_2	Q_2	Q_2	not provided	D_2	G_7	G	G_3	Q_4	S_3	S_C
11	Q_1	Q_1	Q_1	not provided	Q_1	G_8	T	not provided	Q_5	C	S_D
12	not provided	not provided	I_9	~	G_7	G_9	not provided	not provided	Q_6	not provided	S_B
13	not provided	not provided	I_8	not provided	G_8	G_{10}	not provided	not provided	Q_7	not provided	$\overline{Q}_B$
14	R	R	I_7	not provided	G_9	G_{11}	not provided	not provided	Q_8	not provided	$\overline{Q}_B$
15	not provided	T_R	I_6	not provided	G_{10}	G_{12}	not provided	not provided	Q_9	not provided	S_A
16	T	T_F	I_5	not provided	Q_3	Q_4	not provided	not provided	Q_0	not provided	Q_A
17	DP	DP	DP	not provided	Q_2	Q_3	not provided	not provided	L	not provided	$\overline{Q}_A$
18	Q_6	Q_6	Q_6	not provided	G_{11}	G_{13}	not provided	not provided	I_6	not provided	T_{B_1}
19	Q_7	Q_7	Q_7	not provided	G_{12}	G_{14}	not provided	not provided	I_7	not provided	T_{B_2}
20	Q_8	Q_8	Q_8	not provided	G_{13}	G_{15}	not provided	not provided	I_8	not provided	K
21	Q_9	Q_9	Q_9	not provided	G_{14}	G_{16}	not provided	not provided	I_9	not provided	T_A
22	Q_0	Q_0	Q_0	not provided	R_1	G_4	not provided	not provided	I_0	not provided	C_S



7Z52417

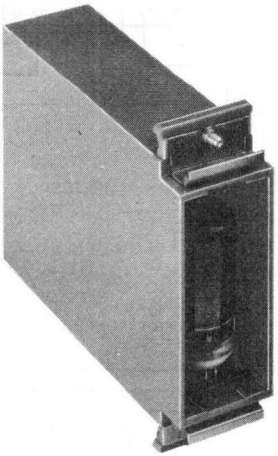
Fig.A.



7Z52419

Fig.B.

NUMERICAL INDICATOR COUNTER

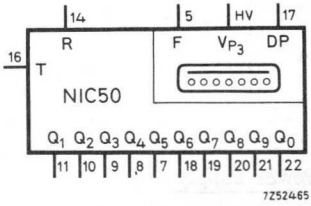


RZ 23932-3

Function	Uni-directional decade counter with direct numerical display for preset programmed control systems. Maximum counting rate: 50 kHz.

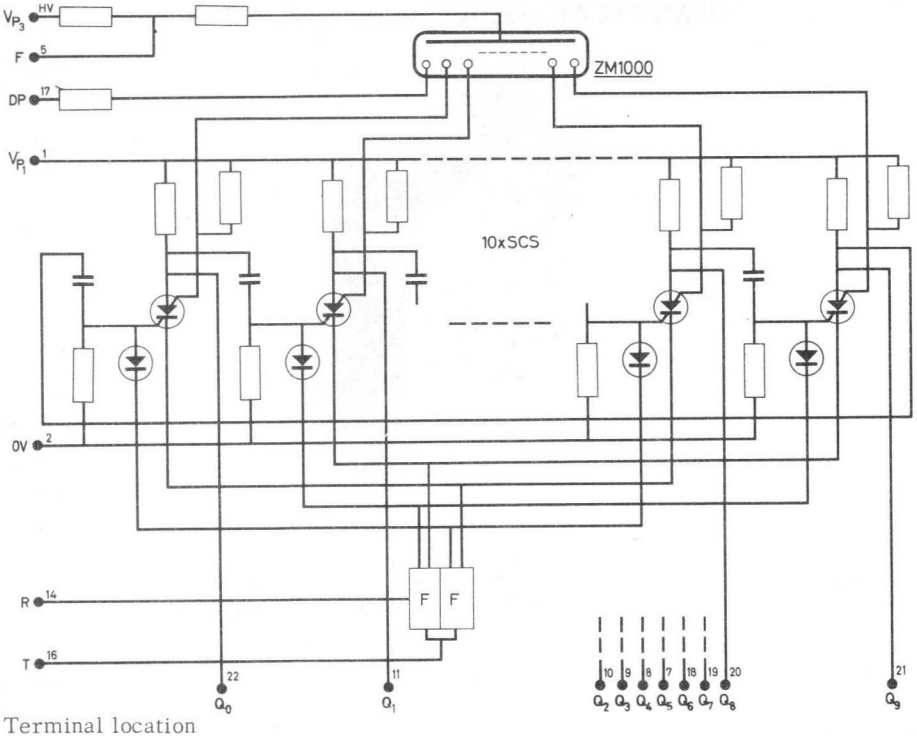
DESCRIPTION

The NIC50 is a uni-directional decade counter coupled to the numerical indicator tube ZM1000, assembled in one plastic case. The ZM1000 is mounted at the front of the case, the input and output terminals are found at the rear.
Ten decimal outputs enable connection to other units for active counting operations. There is also a terminal for display of the decimal point in the ZM1000 at the left of any numeral.
Use is made of silicon controlled switches featuring a direct drive of the ZM1000.
Carry pulses to trigger a succeeding counter NIC50 are obtained from output Q_0 (terminal 22) at the nine to zero transition.
The trigger (counting) pulse and the reset pulse are delivered by the pulse shaper/reset unit PSR50.
Filtering of the high voltage from transients can be obtained by connecting a capacitor of approximately 0.1 μF between terminal F and the central earth point.

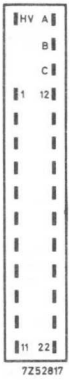


Drawing symbol

CIRCUIT DATA



Terminal location



HV = V_{p_3} = +250 V supply for numerical indicator tube
A = not provided
B = not provided
C = not provided
1 = V_{p_1} = +24 V supply
2 = 0 = common 0 V
3 = not provided
4 = not provided
5 = F = connection for filtering purposes
6 = not provided
7 = Q_5 = decimal output 5
8 = Q_4 = decimal output 4
9 = Q_3 = decimal output 3
10 = Q_2 = decimal output 2
11 = Q_1 = decimal output 1
12 = not provided
13 = not provided
14 = R = reset input
15 = not provided
16 = T = counting trigger input
17 = DP = input decimal point
18 = Q_6 = decimal output 6
19 = Q_7 = decimal output 7
20 = Q_8 = decimal output 8
21 = Q_9 = decimal output 9
22 = Q_0 = decimal output 0

Power supply	voltage	current
Tube supply	+250 V ± 18%	3 mA
Logic supply	+ 24 V ± 10%	12 mA

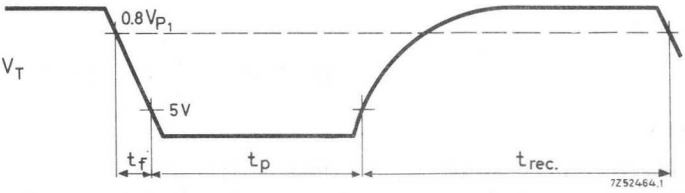
INPUT DATA

Trigger (counting) input T (terminal 16)

This input is to be driven by a negative going pulse, delivered by output Q_T of the unit PSR50, or by a preceding counter unit.

Voltage	V_T = from 0.8 V_{P_1} to 5 V
Required direct current	$-I_T$ = max. 1.5 mA (at V_T = 5 V)
Required transient charge when V_T changes from 0.8 V_{P_1} to 5 V in 1 μs	$-Q_T$ = max. 6.3 nC

Time data



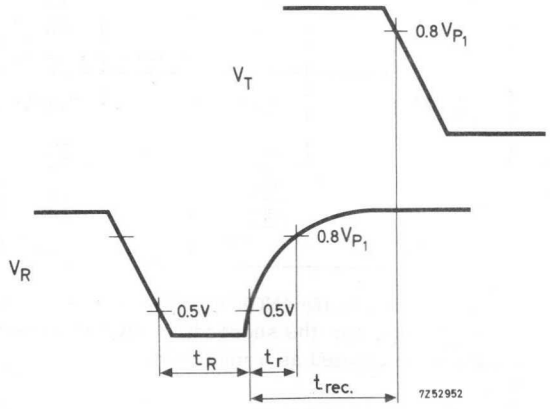
Fall time	t_f = max. 1 μs
Pulse duration	t_p = min. 4 μs
Recovery time	t_{rec} = max. 10 μs

Reset input R (terminal 14)

This input is to be driven by a LOW voltage level, delivered by output Q_R of the unit PSR50.

Required voltage	V_R = max. 0.5 V
Required direct current	I_R = max. 8.5 mA

Time data



Input pulse duration	t_R = min. 15 μs
Recovery time	t_{rec} = max. 50 μs
Trailing edge	t_r = max.1.2 μs

Decimal point input DP (terminal 17)

This input is to be driven by a LOW voltage level with the following requirements:

Decimal point ON

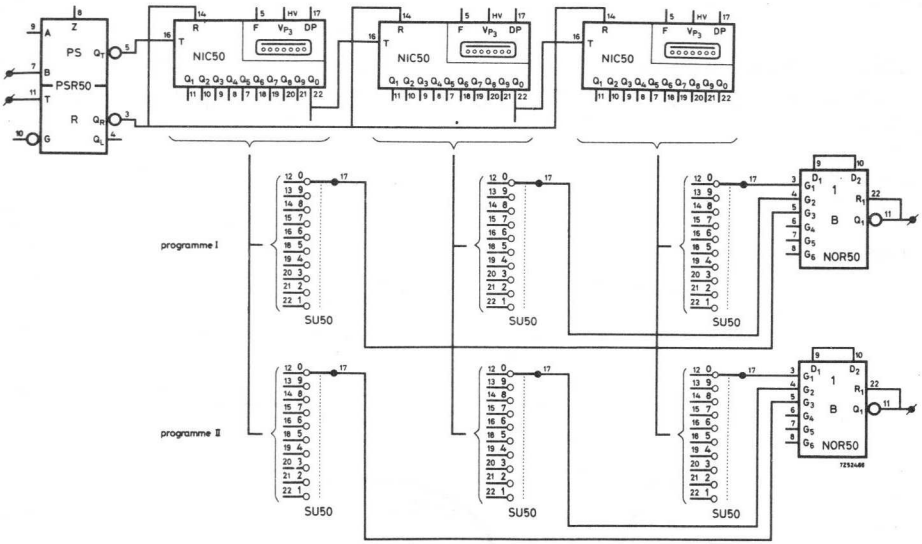
Voltage	V_{DP} = max. 0.5 V
Direct current	I_{DP} = 165 μA (typical)

Decimal point OFF

Voltage	V_{DP} = min. 50 V or terminal 17 floating

OUTPUT DATA

The digits 0-9 are available at the output terminals Q_0-Q_9.
These outputs are primarily intended to drive the buffer NOR in the unit 3.NOR50, in most cases via the 10 position preset switch SU50 as indicated below.



Each Q-output can be loaded with 6 buffer NOR's of the 3.NOR50 units simultaneously in excess of the carry pulse for the succeeding NIC50 counter. This means that 6 preset programmes can be applied as a maximum.

Output voltage LOW (SCS conducting)

Voltage	V_Q = max. 5 V
Available direct current	I_Q = max. 1.5 mA
Available transient charge when V_Q changes from 0.8 V_{P_1} to 5 V in 1 μs	Q_Q = max. 9.5 nC

Output voltage HIGH (SCS non conducting)

Voltage	V_Q = 0.8 V_{P_1} to V_{P_1}
Available direct current	$-I_Q$ = max. 0.32 mA

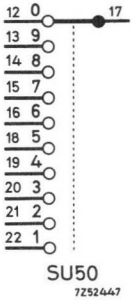
Wiring capacitance C_w = max. 200 pF

Time data

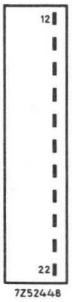
Delay between trigger input and positive going output t_{d_1} = max. 3 μs
Delay between trigger input and negative going output t_{d_2} = max. 4 μs

10 position preset switch

In the 50-Series for preset programmed counting, use is made of the 10 position thumbwheel switch SU50, which is identical to the existing type 10P1C, catalogue number 4311 027 82321.



Drawing symbol



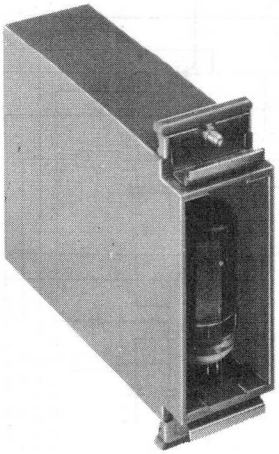
Terminal location

12 = input 0
13 = input 9
14 = input 8
15 = input 7
16 = input 6
17 = output (pole)
18 = input 5
19 = input 4
20 = input 3
21 = input 2
22 = input 1

The ten input terminals 0-9 have to be connected directly to the ten decimal output terminals Q_0-Q_9 of the decade counter NIC50.
The output terminal 17 has to be connected to one of the inputs of the buffer NOR in the unit 3.NOR50.

Note - For more specific data of the thumbwheel switch 10P1C, see data sheets of thumbwheel switches 4311 027 8.....

REVERSIBLE INDICATOR COUNTER



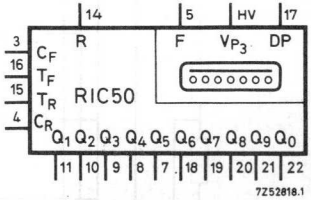
RZ 23932-3

Function

Bi-directional decade counter with direct numerical display for preset programmed control systems.
Maximum counting rate: 12 kHz.

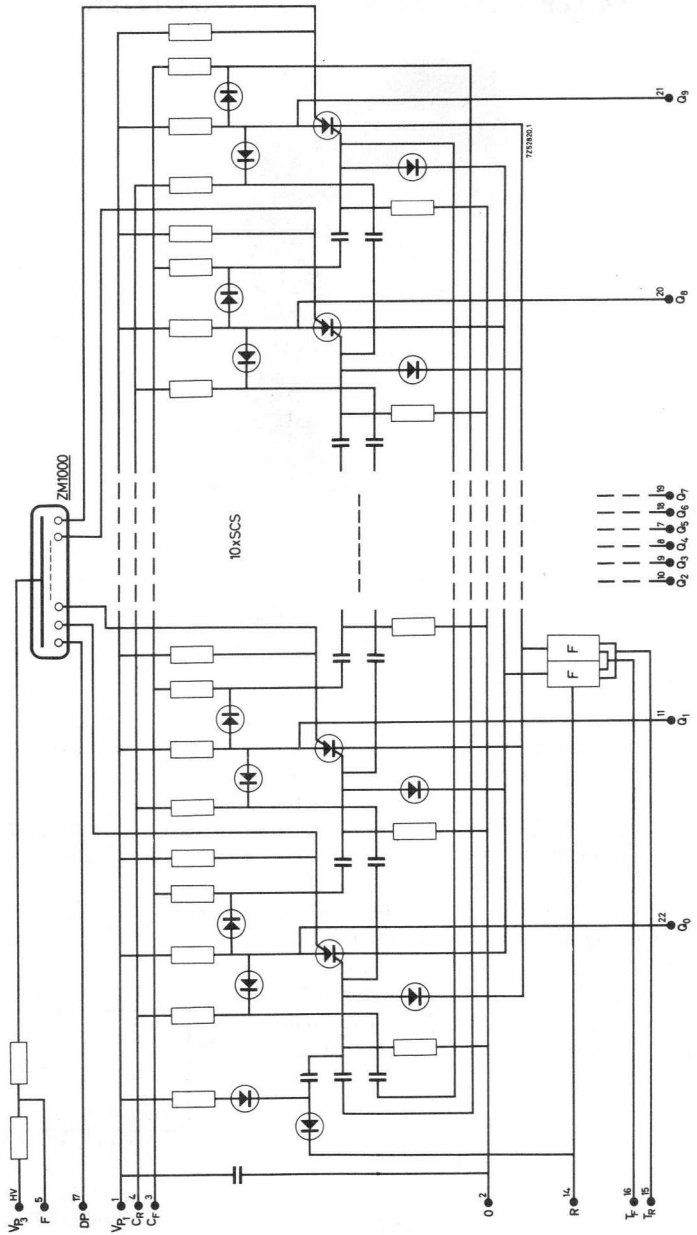
DESCRIPTION

The RIC50 is a bi-directional decade counter coupled to the numerical indicator tube ZM1000, assembled in one plastic case. The ZM1000 is mounted at the front of the case, the input and output terminals are found at the rear.
Ten decimal outputs enable connection to other units for active counting operations. There is also a terminal for display of the decimal point in the ZM1000 at the left of any numeral.
Use is made of silicon controlled switches featuring a direct drive of the ZM1000. The trigger (counting) pulses and the reset pulse are delivered by the pulse shaper/reset unit PSR50.
Filtering of the high voltage from transients can be obtained by connecting a capacitor of approximately 0.1 μF between terminal F and the central earth point.

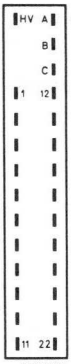


Drawing symbol

CIRCUIT DATA



Terminal location



7Z52817

HV = V_{p3} = +250 V supply for numerical indicator tube
A = not provided
B = not provided
C = not provided
1 = V_{p1} = +24 V supply
2 = 0 = common 0 V
3 = C_F = control forward direction
4 = C_R = control reverse direction
5 = F = connection for filtering purposes
6 = not provided
7 = Q_5 = decimal output 5
8 = Q_4 = decimal output 4
9 = Q_3 = decimal output 3
10 = Q_2 = decimal output 2
11 = Q_1 = decimal output 1
12 = not provided
13 = not provided
14 = R = reset input
15 = T_R = trigger input reverse counting
16 = T_F = trigger input forward counting
17 = DP = input decimal point
18 = Q_6 = decimal output 6
19 = Q_7 = decimal output 7
20 = Q_8 = decimal output 8
21 = Q_9 = decimal output 9
22 = Q_0 = decimal output 0

Power supply

	voltage	current
Tube supply	+250 V ± 18%	3 mA
Logic supply	+ 24 V ± 10%	23 mA

INPUT DATA

Counting conditions

The counting direction is determined by the voltage levels applied to C_F (terminal 3) and C_R (terminal 4).

Forward counting

V_{CF} = max. 1.6 V I_{CF} = max. 7.5 mA
V_{CR} = 0.95 V_{p1} to V_{p1}
} Each input to be driven by LRD50 or NOR unit

Counting pulse from PSR50 - Q_T to be applied to input T_F (terminal 16).

Reverse counting

V_{CR} = max. 1.6 V I_{CR} = max. 7.5 mA
V_{CF} = 0.95 V_{p1} to V_{p1}
} Each input to be driven by LRD50 or NOR unit

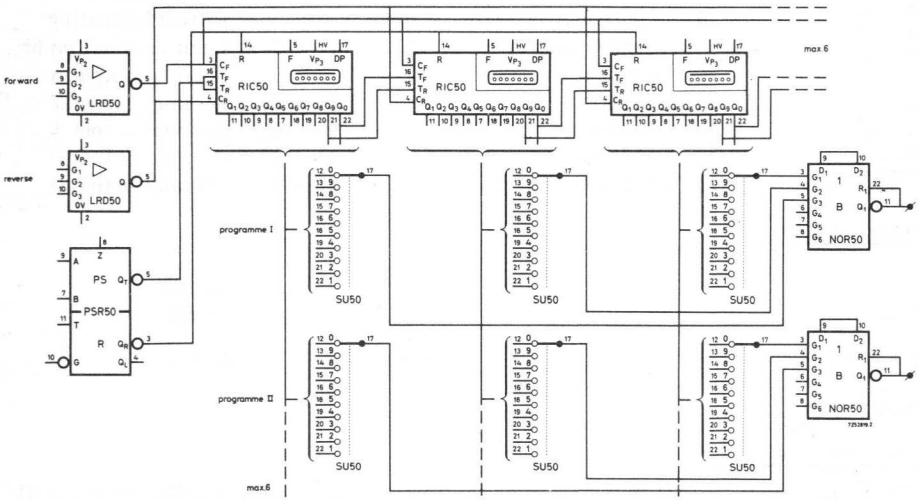
Counting pulse from PSR50 - Q_T to be applied to input T_R (terminal 15).

Note - When both control inputs C_F and C_R are HIGH the RIC50 is blocked for counting pulses.

When two units RIC50 are operating in series the following interconnections have to be made (see figure below).

For forward counting: Q_0 (terminal 22) of the preceding RIC50 has to be connected to T_F (terminal 16) of the succeeding RIC50.

For reverse counting: Q_9 (terminal 21) of the preceding RIC50 has to be connected to T_R (terminal 15) of the succeeding RIC50.



When the levels of the control voltages at C_F or C_R are changed a recovery time t_{rec} = min. 100 μs is to be observed.

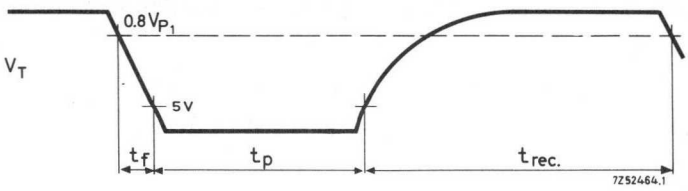
Trigger (counting) inputs T (terminals 16 and 15)

These inputs are to be driven by the negative going pulse, delivered by output Q_T of the unit PSR50 or by the corresponding output Q_0 (forward) or Q_9 (reverse) of the preceding counting decade RIC50.

Triggering edge	V_T = 0.8 V_{p_1} to 5 V
Required direct current	I_T = max. 1.5 mA (at V_T = 5 V)
Required transient charge when V_T changes from 0.8 V_{p_1} to 5 V in 1 μs	Q_T = max. 6.3 nC

When two trigger inputs are interconnected the above I_T and Q_T requirements have to be doubled.

Time data



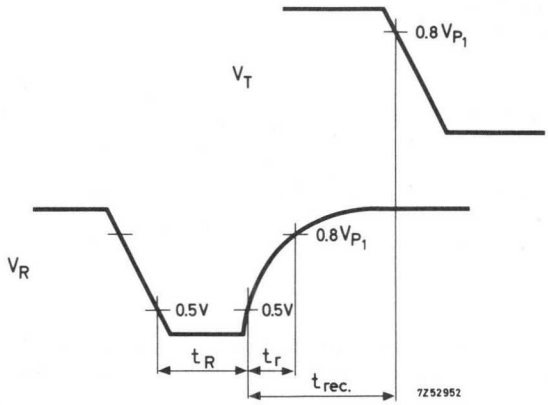
Fall time	t_f	= max. 1 μs
Pulse duration	t_p	= min. 4 μs
Recovery time	t_{rec}	= min. 15 μs
Time between two successive pulses		min. 85 μs

Reset input R (terminal 14)

This input is to be driven by a LOW voltage level, delivered by output Q_R of the unit PSR50.

Required voltage	V_R	= max. 0.5 V
Required direct current	I_R	= max. 8.5 mA

Time data



Pulse duration	t_R	= min. 15 μs
Recovery time	t_{rec}	= max. 80 μs
Trailing edge	t_r	= max. 1.2 μs

Decimal point input DP (terminal 17)

This input is to be driven by a LOW voltage level with the following requirements:

Decimal point ON

Voltage	V_{DP} = max. 0.5 V
Direct current	I_{DP} = 165 μA (typical)

Decimal point OFF

Voltage	V_{DP} = min. 50 V or terminal 17 floating

OUTPUT DATA

The digits 0-9 are available at the output terminals Q_0-Q_9.
These outputs are primarily intended to drive the buffer NOR in the unit 3.NOR50, in most cases via the 10 position preset switch SU50.
Each Q-output can be loaded with 6 buffer NOR's of the 3.NOR50 units simultaneously in excess of the carry pulses for the succeeding RIC50 counter. This means that 6 preset programmes can be applied as a maximum.

Output voltage LOW (SCS conducting)

Voltage	V_Q = max. 5 V
Available direct current	I_Q = max. 1.5 mA
Available transient charge when V_Q changes from 0.8 V_{p1} to 5 V in 1 μs	Q_Q = max. 9.5 nC

Output voltage HIGH (SCS non conducting)

Voltage	V_Q = 0.8 V_{p1} to V_{p1}
Available direct current	I_Q = max. 0.32 mA

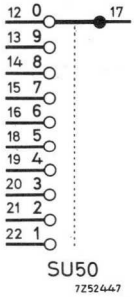
Wiring capacitance	C_W = max. 200 pF

Time data

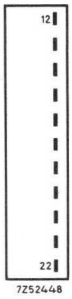
Delay between trigger input and positive going output t_{d_1} = max. 3 μs.
Delay between trigger input and negative going output t_{d_2} = max. 4 μs.

10 position preset switch

In the 50-Series for preset programmed counting, use is made of the 10 position thumbwheel switch SU50, which is identical to the existing type 10P1C, catalogue number 4311 027 82321.



Drawing symbol



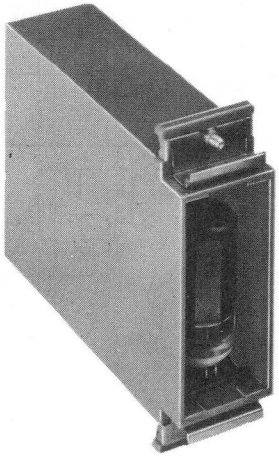
Terminal location

12 = input 0
13 = input 9
14 = input 8
15 = input 7
16 = input 6
17 = output (pole)
18 = input 5
19 = input 4
20 = input 3
21 = input 2
22 = input 1

The ten input terminals 0-9 have to be connected directly to the ten decimal output terminals Q_0-Q_9 of the reversible decade counters RIC50.
The output terminal 17 has to be connected to one of the inputs of the buffer NOR in the unit 3.NOR50.

Note - For more specific data of the thumbwheel switch 10P1C, see data sheets of thumbwheel switches 4311 027 8.....

MEMORY INDICATOR DRIVER



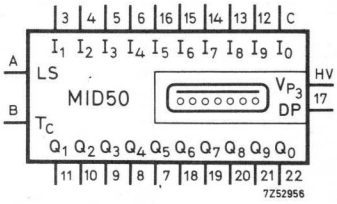
RZ 23932-3

Function

Integral buffer memory with direct numerical display for storage of information from decade counters NIC50 or RIC50.
Apart from numerical display, decimal output is available for e.g. printer drive.

DESCRIPTION

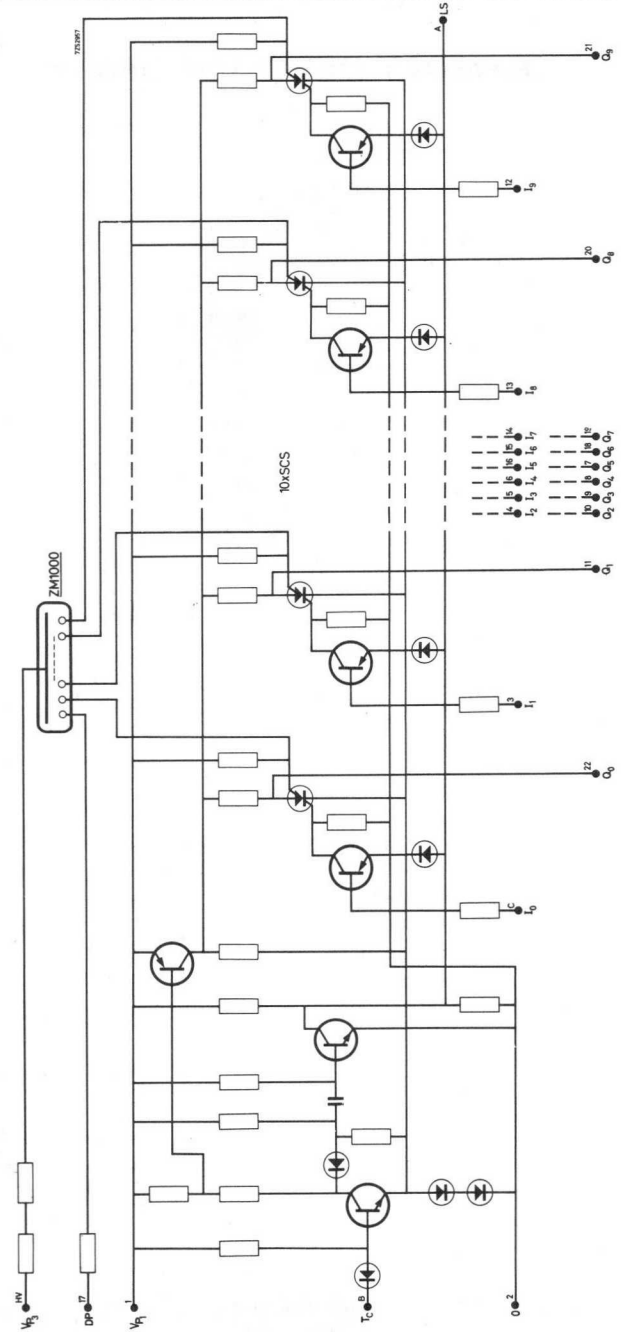
The MID50 is a buffer memory coupled to the numerical indicator tube ZM1000, assembled in one plastic case. The ZM1000 is mounted at the front of the case, the input and output terminals are found at the rear.
Use is made of silicon controlled switches featuring a direct drive of the ZM1000.
The ten decimal inputs (I_0-I_9) can be connected directly to the 10 corresponding outputs (Q_0-Q_9) of either the uni-directional decade counter NIC50 or the bi-directional decade counter RIC50, without influencing the output capability (fan out) of both types of counters.
By applying one single pulse to input T_C (terminal B) the decimal information is transferred from the decade counter into the buffer memory MID50 and remains there steadily displayed.
The MID50 is also provided with 10 decimal outputs for e.g. printer read-out *).
There is a terminal for display of the decimal point in the ZM1000 at the left of any numeral.



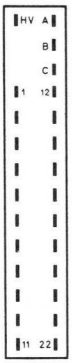
Drawing symbol

*) For this purpose printer drive units PDU50A and PDU50B are available.

CIRCUIT DATA



Terminal location



HV = V_{p3} = +250 V supply for numerical indicator tube
A = LS = level shift facility
B = T_C = shift pulse input
C = I_0 = decimal input 0
1 = V_{p1} = +24 V supply
2 = 0 = common 0 V
3 = I_1 = decimal input 1
4 = I_2 = decimal input 2
5 = I_3 = decimal input 3
6 = I_4 = decimal input 4
7 = Q_5 = decimal output 5
8 = Q_4 = decimal output 4
9 = Q_3 = decimal output 3
10 = Q_2 = decimal output 2
11 = Q_1 = decimal output 1
12 = I_9 = decimal input 9
13 = I_8 = decimal input 8
14 = I_7 = decimal input 7
15 = I_6 = decimal input 6
16 = I_5 = decimal input 5
17 = DP = input decimal point
18 = Q_6 = decimal output 6
19 = Q_7 = decimal output 7
20 = Q_8 = decimal output 8
21 = Q_9 = decimal output 9
22 = Q_0 = decimal output 0

Power supply

	voltage	current
Tube supply	+250 V ± 18%	3 mA
Logic supply	+ 24 V ± 10%	20 mA

INPUT DATA

Decimal inputs I_0-I_9

These inputs are to be fed by the decimal outputs Q_0-Q_9 of either the uni-directional decade counter NIC50 or the bi-directional decade counter RIC50.
One of the ten inputs must be fed with a LOW voltage level, the remaining nine inputs with a HIGH voltage level. By applying one transfer pulse to T_C (terminal B) that output Q becomes LOW of which the corresponding input I carries the LOW voltage, while simultaneously the corresponding figure of the indicator tube is lit. The other nine outputs of the MID50 will be HIGH. The decimal information of a NIC50 or RIC50 is transferred into the MID50 at the positive going edge of the transfer pulse

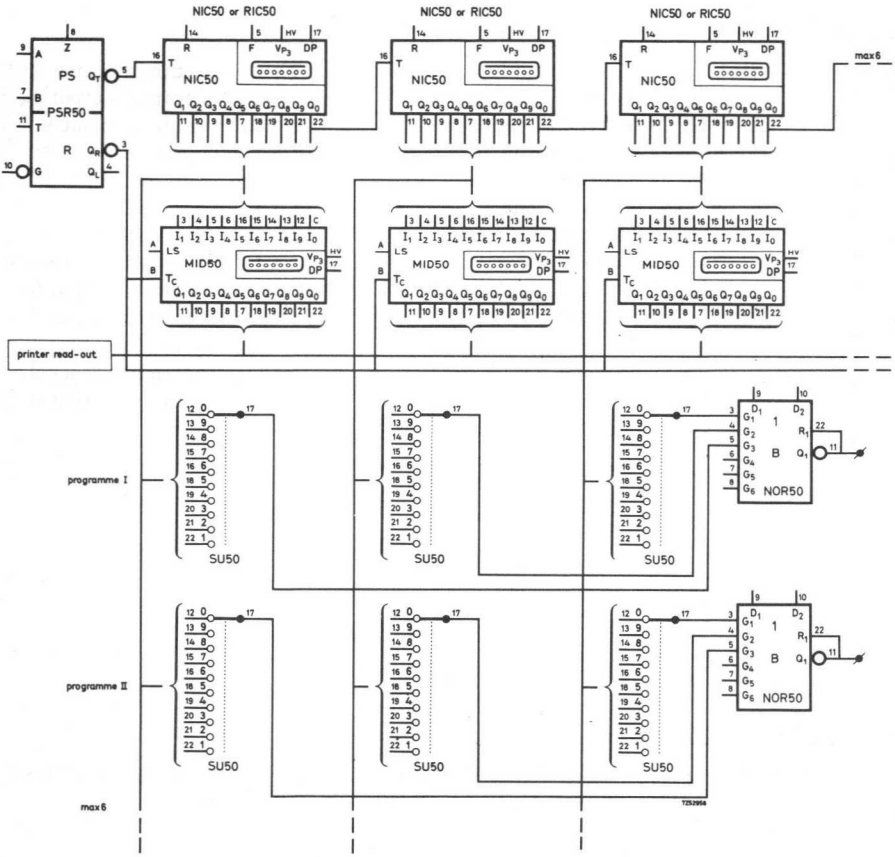
Voltage LOW

V_I = max. 5 V

I_I = max. 0.06 mA

Voltage HIGH

V_I = 0.8 V_{p1} to V_{p1}



Level shift input LS (terminal A)

By connecting a suitable zener diode between LS and 0 V and a resistor between LS and V_{P1}, the correct functional behaviour of the MID50 can be accomplished also when the inputs I_0-I_9 are fed with non-standard voltage levels (not derived from NIC50 or RIC50).

Transfer pulse input T_C (terminal B)

This input is driven by a pulse generated at output Q_R or Q_T of the unit PSR50. The transferring action takes place at the positive going edge. Maximum 6 inputs T_C can be driven simultaneously by output Q_R or Q_T of the PSR50.

Voltage LOW

V_B = max. 0.5 V

I_B = max. 0.5 mA

Voltage HIGH

V_B = 0.62 V_{p1} to V_{p1}

Decimal point input DP (terminal 17)

This input is to be driven by a LOW voltage level with the following requirements:

Decimal point ON

Voltage	V_{DP} = max. 0.5 V
Direct current	I_{DP} = 165 μA (typical)

Decimal point OFF

Voltage	V_{DP} = min. 50 V or terminal 17 floating

OUTPUT DATA

The digits 0-9 are available at the output terminals Q_0-Q_9. These outputs are primarily intended for either printer read-out purposes or shift register configurations.

Output voltage LOW (SCS conducting)

Voltage	V_Q = max. 3.5 V
Available direct current	I_Q = max. 0.2 mA *)

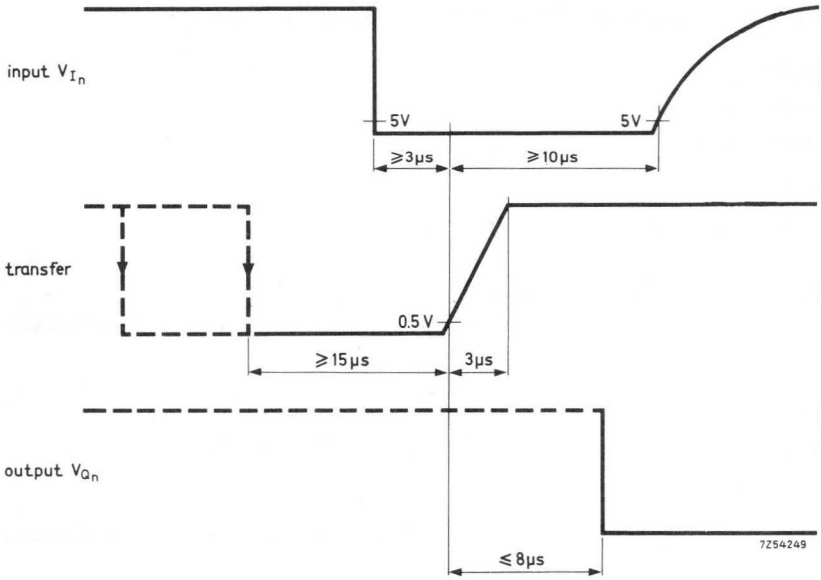
Output voltage HIGH (SCS non conducting)

Voltage	V_Q = 0.8 V_{p1} to V_{p1}
Available direct current	$-I_Q$ = max. 0.84 mA

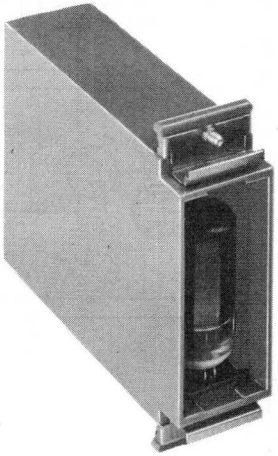
Wiring capacitance	C_W = max. 200 pF

*) The sum of the output currents I_{Q0}-I_{Q9} may not exceed 200 μA.

Time data


input V_{I_n}
5V
5V
≥3μs
≥10μs
transfer
0.5 V
≥15μs
3μs
output V_{Q_n}
≤8μs
7Z54249

SIGN INDICATOR DRIVER

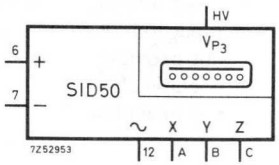


RZ 23932-3

Function	Driver of plus and minus character indicator tube. Characters ~, X, Y and Z are accessible

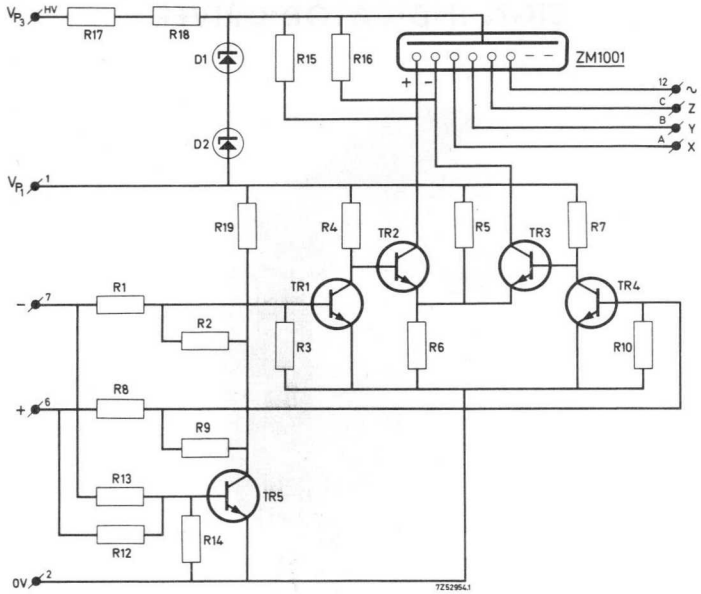
DESCRIPTION

The SID50 contains the plus and minus indicator tube ZM1001 and its driver stages in one plastic case. The ZM1001 is mounted at the front of the case, the connecting terminals are found at the rear.
A dark position of the ZM1001 can be obtained when both plus and minus inputs are driven by equal voltage levels.
The characters ~, X, Y and Z provided in the ZM1001 are also accessible.

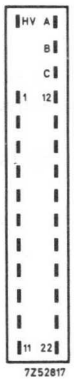


Drawing symbol

CIRCUIT DATA



Terminal location



HV = V_{p3} = +250 V supply for numerical indicator tube
A = X = X character
B = Y = Y character
C = Z = Z character
1 = V_{p1} = +24 V supply
2 = 0 = common 0 V
3 = not provided
4 = not provided
5 = not provided
6 = + = input driving + character
7 = – = input driving – character
8 to 11 = not provided
12 = ~ = ~ character
13 to 22 = not provided

Power supply

	voltage	current
Tube supply	+250 V ± 18%	2.8 mA
Logic supply	+ 24 V ± 10%	5.0 mA

INPUT DATA

Input terminals characters + and –

These inputs are to be driven by a HIGH voltage level to illuminate the corresponding character. A LOW level extinguishes the character.

HIGH voltage

V_+/V_- = 0.62 V_{pl} to V_{pl}

I_+/I_- = 0.17 mA (V = 13.4 V); EQUALS ONE D.U.*).

LOW voltage

V_+/V_- = max. 0.3 V

Characters ~, X, Y and Z

Visible : $V\sim/V_X/V_Y/V_Z$ = 0 to 10 V

Not visible: $V\sim/V_X/V_Y/V_Z$ = 60 to 120 V or floating

Dark : $V\sim/V_X/V_Y/V_Z$ = 80 to 120 V or floating

*) See also loading table.

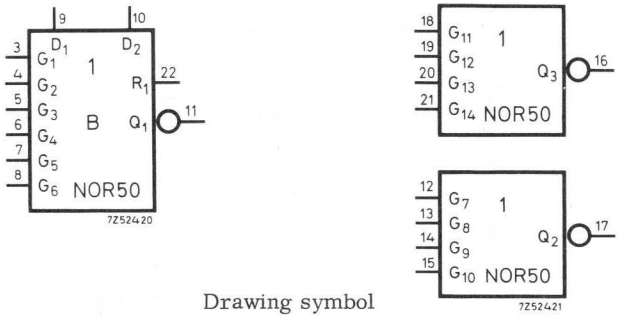
TRIPLE NOR GATE

Function

- 6 input buffer NOR for adapting the output levels of the NIC50 and the RIC50 to standard logic levels and
- dual 4 input NOR for logic purposes e.g. to form a memory function.

DESCRIPTION

The 3.NOR50 is intended to be used to memorize the count when the content of the unit(s) NIC50 or RIC50 corresponds with the preset position of the 10 position thumb-wheel switch SU50.



Drawing symbol

6 input buffer NOR

The 6 input buffer NOR is intended to adapt the output levels of the NIC50 or the RIC50 to the standard logic levels of the 4 input NOR's.
To this end each input of the 6 input buffer NOR is to be connected, directly or via the switch SU50, to one of the decimal outputs of the units NIC50 or RIC50.

Simplified truth table:

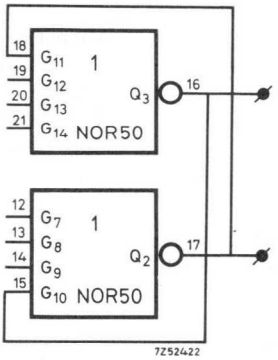
G_1	G_2	Q_1
H	H	L
L	H	L
H	L	L
L	L	H

All inputs (G_1 to G_6) must be LOW or floating for Q_1 is HIGH.

The 6 input buffer NOR can be provided with an intentional delay by interconnecting D_1 (terminal 9) and D2 (terminal 10) (see Time data). This intentional delay cancels hazardous (false) pulses that can occur during e.g. the transition from 499 to 500 at the transit counts 490 and 400, if preset programs have been set at these counts. The maximum delay can be decreased (the maximum counting rate increased) when an external capacitor is connected between D_1 and D_2.

Dual 4 input NOR

The 4 input NOR is intended for logic operations, such as memorizing the preset counts. To this end a memory function can be formed by cross connecting the two NOR's.

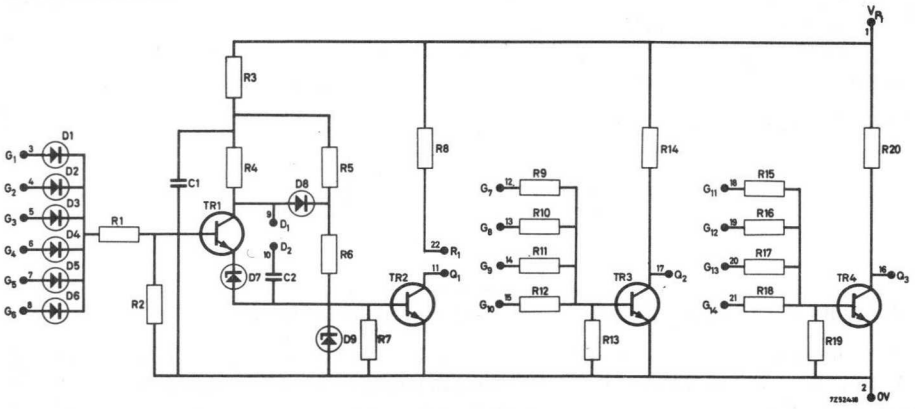


Simplified truth table:

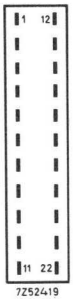
$G_7(G_{11})$	$G_8(G_{12})$	$Q_2(Q_3)$
H	H	L
H	L	L
L	H	L
L	L	H

All inputs G of a NOR must be LOW or floating for Q is HIGH.

CIRCUIT DATA



Terminal location



1 = V_{p_1} = +24 V supply
2 = 0 = common 0 V
3 = G_1 = input buffer NOR1
4 = G_2 = input buffer NOR1
5 = G_3 = input buffer NOR1
6 = G_4 = input buffer NOR1
7 = G_5 = input buffer NOR1
8 = G_6 = input buffer NOR1
9 = D_1 = } when interconnected
10 = D_2 = } providing built-in delay
11 = Q_1 = output buffer NOR1
12 = G_7 = input NOR2
13 = G_8 = input NOR2
14 = G_9 = input NOR2
15 = G_{10} = input NOR2
16 = Q_3 = output NOR3
17 = Q_2 = output NOR2
18 = G_{11} = input NOR3
19 = G_{12} = input NOR3
20 = G_{13} = input NOR3
21 = G_{14} = input NOR3
22 = R_1 = collector resistor buffer NOR1

Power supply

Voltage V_{p_1} = 24 V ±10%

Current I_{p_1} = 10.5 mA

INPUT DATA

6 input buffer NOR

Input HIGH: V_G = 0.8 V_{p_1} to V_{p_1}

I_G = 53 μA (V_G = 18.35 V)

Input LOW: V_G = 0 to 5.5 V

4 input NOR

Input HIGH: V_G = 0.62 V_{p_1} to V_{p_1}

I_G = 0.17 mA (V_G = 13.4 V); EQUALS ONE D.U.*)

Noise immunity: a voltage shift of 2 V on the minimum high level will not cause a change of the output voltage.

Input LOW: V_G = 0 to 0.3 V

Noise immunity: a voltage of +1 V with respect to the 0 V line applied to any one input (the other inputs at low level or floating) will not cause a change of the output voltage. The noise immunity can be increased by connecting unused inputs to 0 V.

*) See also loading table.

OUTPUT DATA

6 input buffer NOR

Output current: I_{Q_1} = 0.35 mA (V_{Q_1} = 13.4 V); EQUALS TWO D.U.*)

4 input NOR

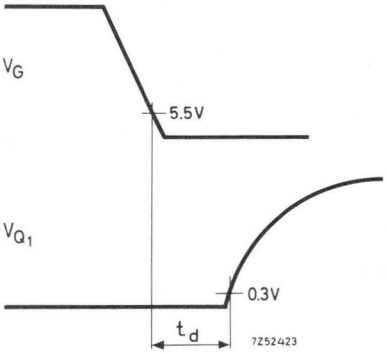
Output current: I_{Q_2/Q_3} = 1.02 mA (V_{Q_2/Q_3} = 13.4 V); EQUALS SIX D.U.*)

Time data

6 input buffer NOR

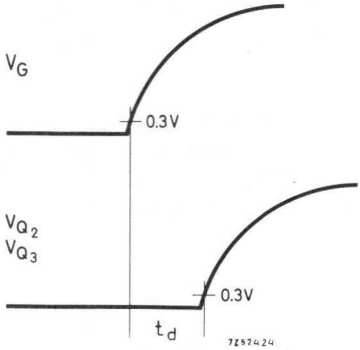
D_1 and D_2 interconnected: t_d = 7-18 μs

D_1 and D_2 not connected : t_d = 4 - 9 μs



4 input NOR

Delay, measured over two stages: t_d = max. 12 μs.
The delay is specified for C_w = 200 pF and worst input and output conditions.



*) See also loading table.

QUADRUPLE NOR GATE

Function

Quadruple 4 input NOR for logic operations e.g. to form memory functions.

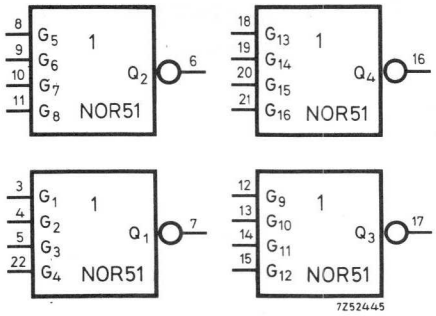
DESCRIPTION

The 4 input NOR is intended for logic operations. A memory function can be formed by cross connecting two NOR's.

Simplified truth table:

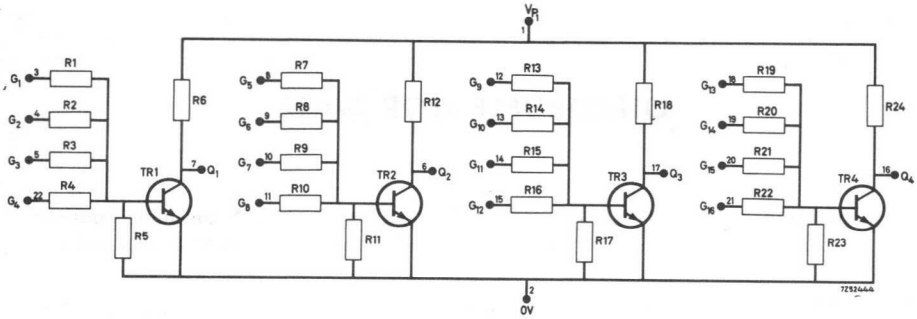
$G_1(G_5, G_9, G_{13})$	$G_2(G_6, G_{10}, G_{14})$	$Q_1(Q_2, Q_3, Q_4)$
H	H	L
H	L	L
L	H	L
L	L	H

All inputs G of a NOR must be LOW or floating for Q is HIGH.



Drawing symbol

CIRCUIT DATA



Terminal location

1 = V_{p1} = +24V supply
2 = 0 = common 0 V
3 = G_1 = input NOR 1
4 = G_2 = input NOR 1
5 = G_3 = input NOR 1
6 = Q_2 = output NOR 2
7 = Q_1 = output NOR 1
8 = G_5 = input NOR 2
9 = G_6 = input NOR 2
10 = G_7 = input NOR 2
11 = G_8 = input NOR 2
12 = G_9 = input NOR 3
13 = G_{10} = input NOR 3
14 = G_{11} = input NOR 3
15 = G_{12} = input NOR 3
16 = Q_4 = output NOR 4
17 = Q_3 = output NOR 3
18 = G_{13} = input NOR 4
19 = G_{14} = input NOR 4
20 = G_{15} = input NOR 4
21 = G_{16} = input NOR 4
22 = G_4 = input NOR 1

Power supply

Voltage $V_{p1} = 24\ V \pm 10\%$

Current $I_{p1} = 8\ mA$

INPUT DATA

Input HIGH: V_G = 0.62 V_{p1} to V_{p1}

I_G = 0.17 mA (V_G = 13.4 V); EQUALS ONE D.U.*)

Noise immunity: a voltage shift of 2 V on the minimum high level will not cause a change of the output voltage.

Input LOW: V_G = 0 to 0.3 V

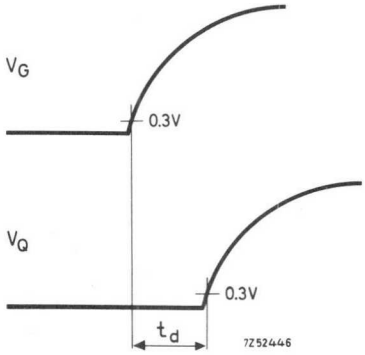
Noise immunity: a voltage of +1 V with respect to the 0 V line applied to any one G input (the other inputs at low level or floating) will not cause a change of the output voltage. The noise immunity can be increased by connecting unused inputs to 0 V.

OUTPUT DATA

Output current: I_Q = 1.02 mA (V_Q = 13.4 V); EQUALS SIX D.U.*)

Time data

Delay, measured over two stages: t_d = max. 12 μs
The delay is specified for Cw = 200 pF and worst input- and output conditions.



*) See also loading table.

PULSE SHAPER AND RESET UNIT

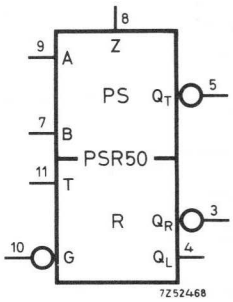
Function

Pulse shaper for converting input signals into counting pulses for the NIC50 and the RIC50, and

reset unit for generating pulses for resetting the NIC50 and the RIC50, generating pulses for resetting memories formed by cross-connected 4 input NOR's, generating transfer pulses for the MID50.

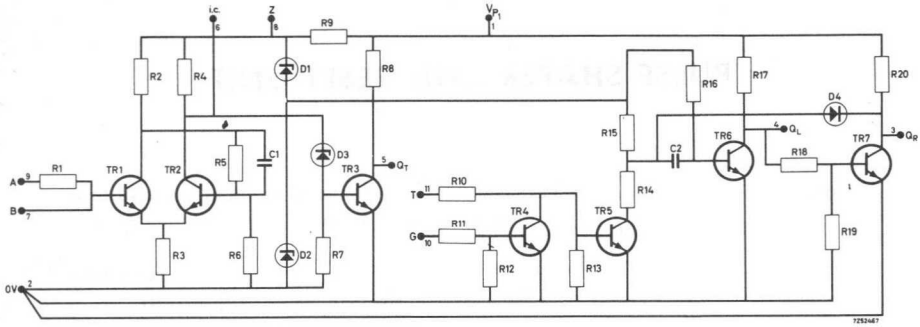
DESCRIPTION

The unit PSR50 contains a pulse shaper and a reset unit. The pulse shaper circuit consists of a Schmitt trigger followed by an inverting amplifier.
The circuit of the reset unit is a monostable multivibrator with one condition input and one trigger input.

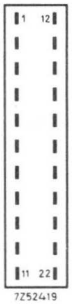


Drawing symbol

CIRCUIT DIAGRAM



Terminal location



1 = V_{p_1} = +24 V supply
2 = 0 = common 0 V
3 = Q_R = counter reset output
4 = Q_L = logic reset output
5 = Q_T = pulse shaper output
6 = internally connected
7 = B = direct base input pulse shaper
8 = Z = internally connected
9 = A = resistor input pulse shaper
10 = G = gate input reset unit
11 = T = trigger input reset unit
12 to 22 = not provided

Power supply

Voltage	V_{p_1} = +24 V ± 10%
Current	I_{p_1} = 23 mA nominal

PULSE SHAPER

A HIGH level at input B (terminal 7) produces a LOW level at output Q_T (terminal 5), a LOW level at input B produces a HIGH level at output Q_T.

The pulse shaper can be used as follows:

- as a pulse shaper driven by an external source (input transducers)
- as a pulse shaper driven by NOR's of the 50- or 60-Series
- in a relaxation oscillator circuit

INPUT DATA

Pulse shaper driven by an external source

The input voltage has to be applied to B (terminal 7).

HIGH level (operating)

Voltage	V_B = min. 4.0 V
Current	I_B = max. 0.06 mA

LOW level (operating)

Voltage	V_B = max. +1.36 V

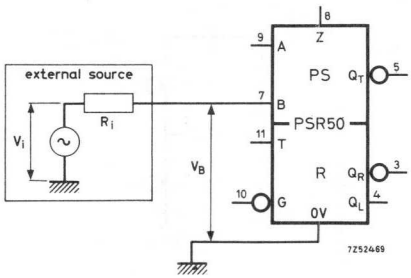
Limiting values

Voltage	V_B = max. +7.0 V min. −2 V
Current	I_B = max. 16 mA

Internal resistance of the driving external source

R_i = max. 33 kΩ

Hysteresis (difference between ON and OFF thresholds)



The hysteresis is affected by the R_i of the external source.
The relation is given by the following formula:

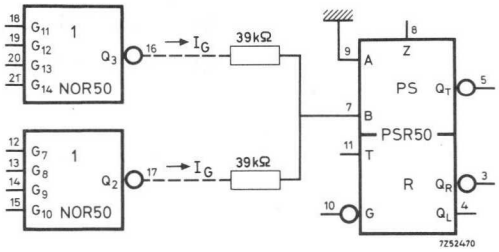
$$\Delta V_i = \text{min. } (1.5 - 0.0455\, R_i)\ V$$

$$\Delta V_B = \frac{\Delta V_i}{1 + 0.046\, R_i}\ V$$

R_i in kΩ and V in volt

Pulse shaper driven by a standard NOR

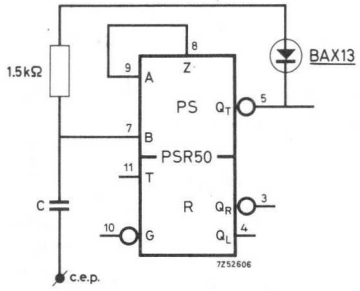
A (terminal 9) has to be connected to 0 (terminal 2).
The input voltage has to be applied to B (terminal 7), via a resistor of 39 kΩ (nominal).
I_G = max. 0.34 mA; EQUALS TWO D.U.*)



The maximum number of driving NOR's is two as shown in the diagram above.

Pulse shaper used in a relaxation oscillator circuit

For this application the connections must be made as shown in the circuitry below.



OUTPUT DATA

Available output suitable for driving three decade counters NIC50 or RIC50 simultaneously

Output voltage LOW

Voltage	V_{QT} = max. 0.5 V
Direct current	I_{QT} = max. 25 mA (V_{QT} = 0.5 V); max. 10 mA (V_{QT} = 0.3 V)
Transient charge	Q_{QT} = max. 30 nC
Wiring capacitance at Q_T	C_W = max. 200 pF

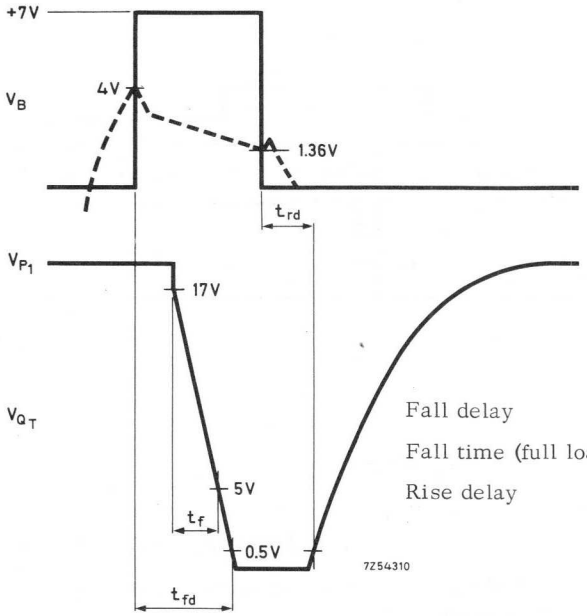
*) See also loading table.

Output voltage HIGH

Voltage	V_{QT} =	0.62 V_{p1} to V_{p1}
Direct current	$-I_{QT}$ =	max. 0.34 mA; EQUALS TWO D.U.*)

Wiring capacitance C_w = max. 200 pF

Time data (when the PSR50 is used in combination with 50-Series units)



Fall delay	t_{fd} = max.	2 μs
Fall time (full load)	t_f = max.	1 μs
Rise delay	t_{rd} = max.	2 μs

RESET UNIT

Reset pulses are only generated when:

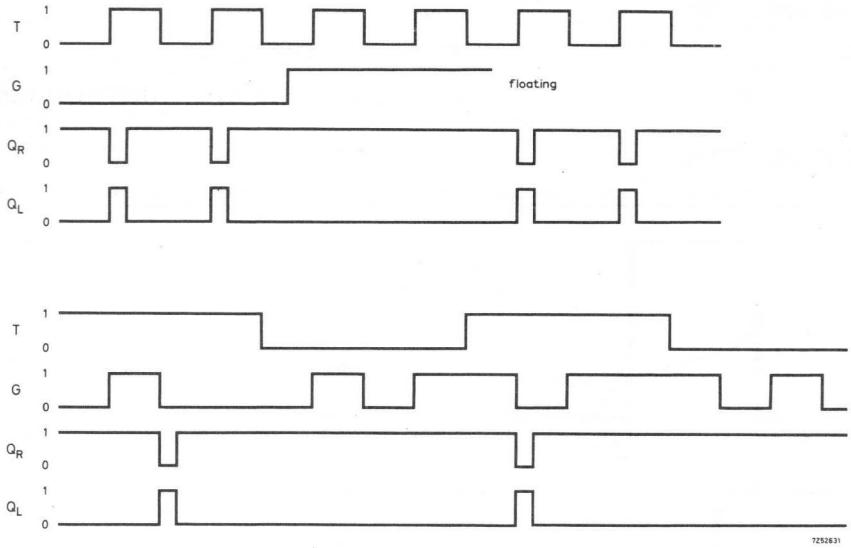
the HIGH level is applied to the trigger input T (terminal 11), and
the gate input G (terminal 10) is kept at the LOW level or left floating.

The unit generates two reset pulses simultaneously, namely:

from the logic reset output Q_L (terminal 4) for resetting d.c. memories built with NOR's
from the counter reset output Q_R (terminal 3) for resetting decade counters NIC50 and RIC50.

Note - A reset pulse is also generated when the G-input changes from the HIGH to the LOW level, whilst the T-input is at the HIGH level.

*) See also loading table.



INPUT DATA

Input HIGH

Voltage	$V_{T(G)} = 0.62\ V_{P_1}$ to V_{P_1}
limiting value	$V_{T(G)} = +100$ V
Current	$I_{T(G)} = 0.17$ mA ($V_{T(G)} = 13.4$ V); EQUALS ONE D.U.*)

Noise immunity: a voltage shift of 2 V on minimum HIGH level will not cause a change of the output voltage.

Input LOW

Voltage	$V_{T(G)}$ = max. 0.3 V
limiting value	$V_{T(G)}$ = −15 V

Noise immunity: a voltage of +1.25 V with respect to the 0 V terminal applied to either the T- or the G-input will not cause a change of the output voltage.

OUTPUT DATA

Output Q_L: capable of driving max. 4NOR's; EQUALS FOUR D.U.*)

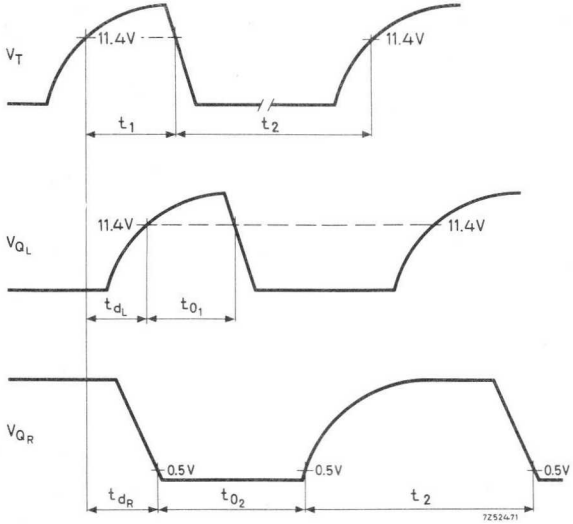
Voltage	V_{QL} = min. $0.53\ V_{P_1}$
Direct current	$-I_{QL}$ = max. 0.55 mA ($V_{QL} = 11.4$ V)

*) See also loading table.

Output Q_R: capable of driving the reset input of 6 decade counters NIC50 or RIC50 simultaneously

Voltage	V_{QR} = max. 0.5 V
Direct current	I_{QR} = max. 51 mA
Wiring capacitance	C_w = max. 200 pF at Q_R and Q_L

Time data



Input pulse duration	t_1	= min. 20 μs
Recovery time *)	t_2	= min. 20 μs
Output pulse duration	t_{0_1}	= min. 15 μs max. 45 μs
	t_{0_2}	= min. 15 μs max. 50 μs
Delay between V_T and V_{Q_L}	t_{d_L}	= max. 3 μs
Delay between V_T and V_{Q_R}	t_{d_R}	= max. 7 μs
Rise time at T	t_r	= max. 100 μs (between 0.5 V and 11.4 V)
Fall time at G	t_f	= max. 100 μs (between 11.4 V and 0.5 V)

*) The recovery time starts at the trailing edge of V_T when $t_1 > t_{0_2}$ or starts at the trailing edge of V_{Q_R} when $t_{0_2} > t_1$.

LAMP/RELAY DRIVER

Function — Low-power amplifier for driving lamps and relays

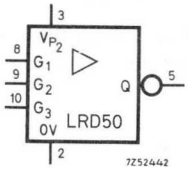
DESCRIPTION

The circuit consists of an inverting amplifier preceded by a 3 input OR-gate.
The load has to be connected between output Q and the unstabilised +24 V supply voltage (abs. max. 30 V).
The load is energised when one or more inputs are HIGH (Q is LOW).
The output transistor is protected against voltage transients which occur when inductive loads are driven.

Simplified truth table:

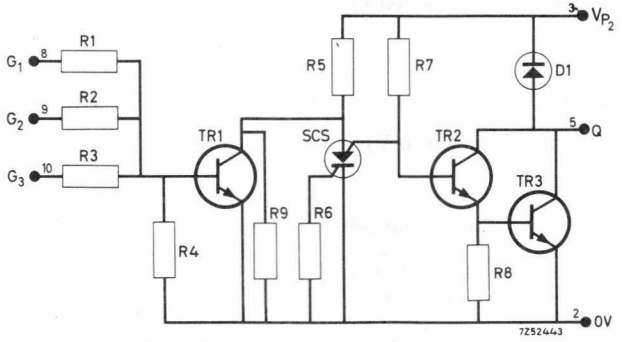
G_1	G_2	Q
H	H	L
H	L	L
L	H	L
L	L	H

All inputs G must be LOW or floating for Q is HIGH.

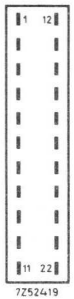


Drawing symbol

CIRCUIT DATA



Terminal location



1 = not provided
2 = 0 = common 0 V
3 = V_{p_2} = +24 V supply
4 = not provided
5 = Q = output
6 = not provided
7 = not provided
8 = G_1 = input
9 = G_2 = input
10 = G_3 = input
11 = not provided
12 to 22 = not provided

Power supply

Voltage	V_{p_2} = +24 V ±25%
Current	I_{p_2} = (4.4 + I_Q) mA

INPUT DATA

Output transistor ON

Input HIGH: : V_G = 0.62 V_{p_1} to V_{p_1}
I_G = max. 0.17 mA (V_G = 13.4 V); EQUALS ONE D.U.*)

Noise immunity: A voltage shift of 2 V on the minimum high level will not cause a change of the output voltage.

Output transistor OFF

Input LOW : V_G = max. 0.3 V

Noise immunity: A voltage of 1.25 V with respect to the 0 V line applied to any one input (other inputs at low level or floating) will not cause a change of the output voltage. The noise immunity can be increased by connecting unused inputs to 0 V.

OUTPUT DATA

Output transistor ON

I_Q = abs. max. 300 mA ($V_Q \leq$ 1.6 V)

Output transistor OFF

I_Q = max. 0.5 mA at V_Q = abs. max. 30 V.

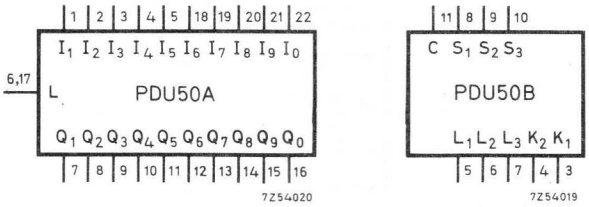
*) See also loading table.

PRINTER DRIVE UNIT

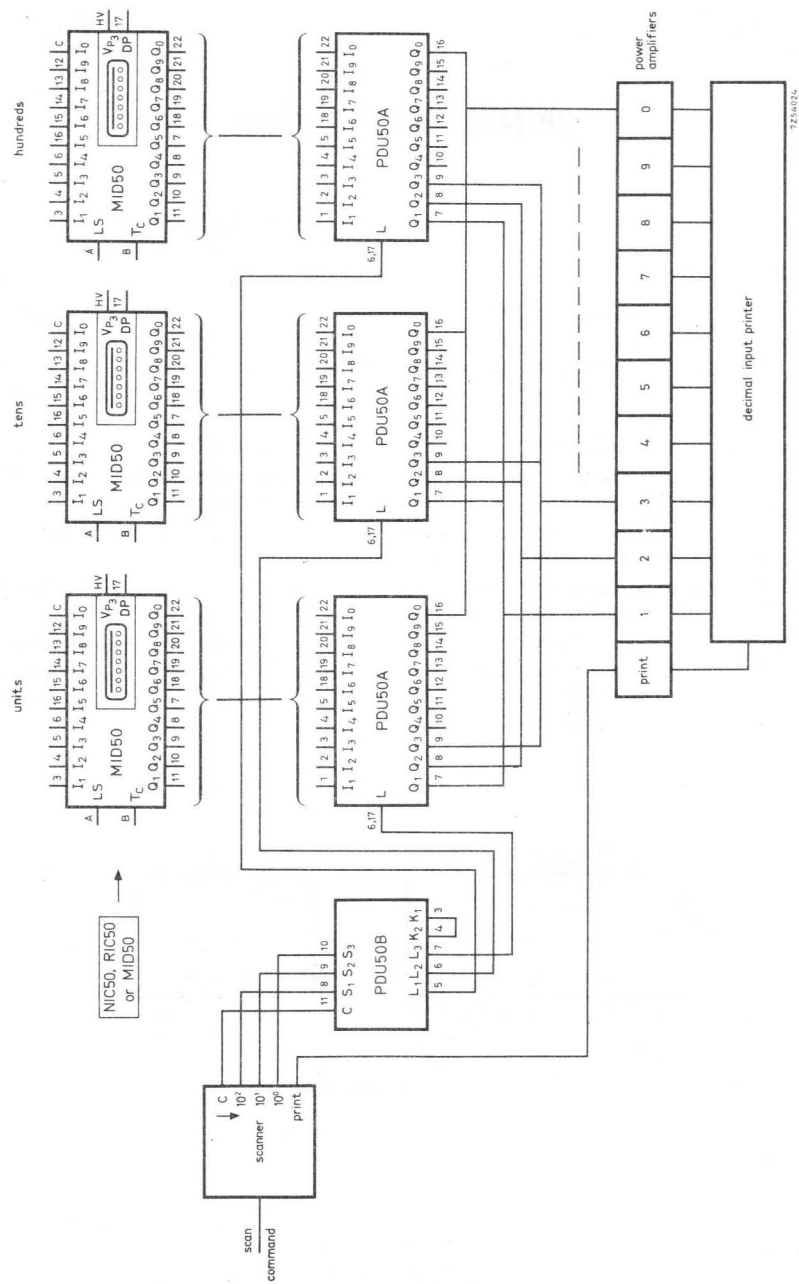
Function — Intermediate stages to drive decimal input printers

DESCRIPTION

With the units PDU50A and PDU50B a complete printer drive circuit is formed.
This circuit is intended to be used in combination with the NIC50, RIC50 or MID50 and a printer which requires decimal information at its inputs. A diagram for driving such a printer is given on the next page. One PDU50A unit, which contains ten inverter stages, must be used per decade.
The ten decimal inputs I_0 to I_9 can be connected directly to the ten corresponding outputs Q_0 to Q_9 of either the uni-directional decade counter NIC50 or the bi-directional decade counter RIC50 or the buffer memory MID50.
When a positive voltage is applied to control input L, that particular output Q will become HIGH, which has a LOW level at its input.
The PDU50B contains one clock control and three scan control circuits suitable to operate with a three decade counting system.
When simultaneously both the clock control input C and one of the scan control inputs S_1 to S_3 are at LOW level a positive voltage is available at the corresponding control output L_1 to L_3 of the PDU50B. Each control output of the PDU50B is connected to the control input L of the PDU50A.



Drawing symbols


hundreds
tens
units
MID50
PDU50A
PDU50B
NIC50, RIC50 or MID50
scanner
scan command
print
power amplifiers
decimal input printer
725024

Summarising the functions of the PDU50A and PDU50B it becomes clear that a particular output Q of the PDU50A is at a HIGH level only, when the three following conditions are fulfilled:

- the corresponding input I of the PDU50A at a LOW level,
- the clock control input C of the PDU50B at a LOW level,
- the corresponding scan control input S_1 to S_3 of the PDU50B at a LOW level.

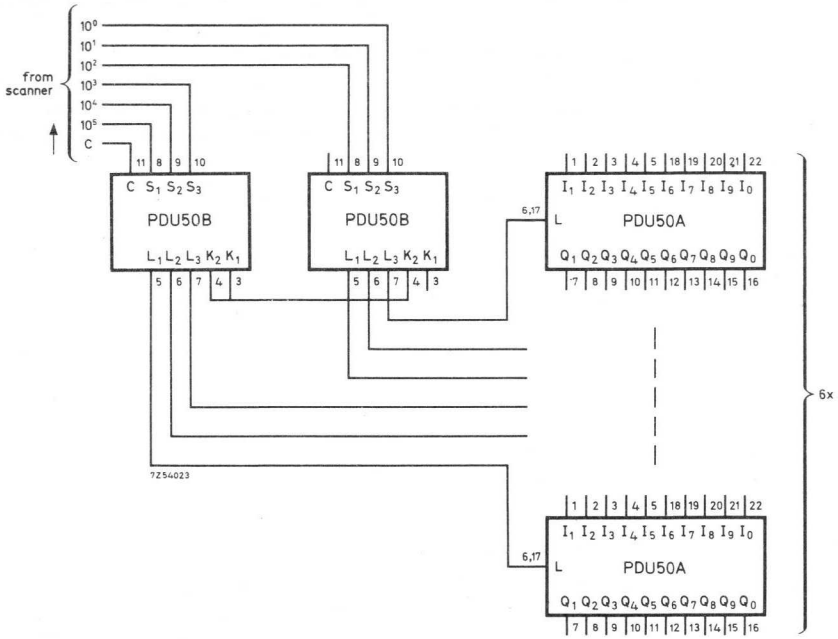
Note that only one output Q of the PDU50A is HIGH at a time as shown in the truth table below.

Truth table:

inputs			output
PDU50B		PDU50A	
C	S	I	Q
H	H	H	L
L	H	H	L
H	L	H	L
L	L	H	L
H	H	L	L
L	H	L	L
H	L	L	L
L	L	L	H

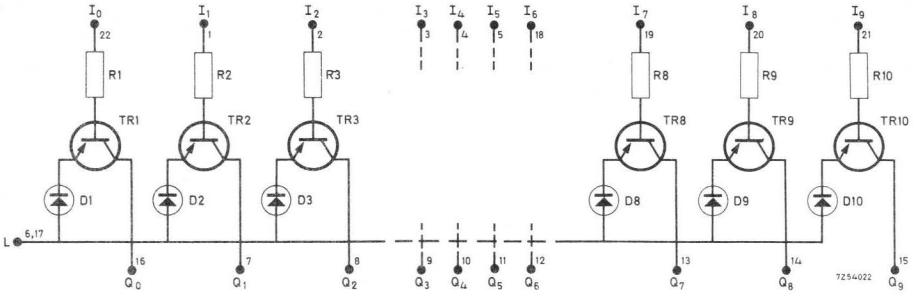
As the positive voltage derived from the PDU50B is fed to terminal L of only one PDU50A at a time it is permissible to common the corresponding outputs of all PDU50A units without any feedback consequences. These ten commoned PDU50A outputs are to be connected to ten power stages, of which the output power depends on the driving input requirements of the decimal input printers, e.g. the LRD50 supplies 300 mA/30V.

The description above holds for systems up to three decades, for which the terminals K_1 and K_2 of the PDU50B have to be interconnected.
When however more than three decades are required another PDU50B unit must be added to the system.
In this case terminals K_1 and K_2 need be interconnected for only one PDU50B.
For the other units PDU50B the terminals K_1 and K_2 are left open.
An interconnection diagram is given on the next page.

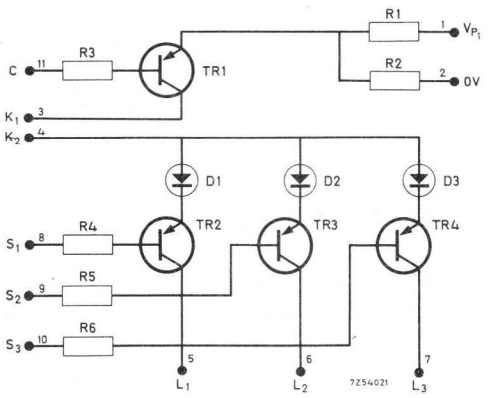


Note - When the input signal for the PDU50A is obtained from a MID50 unit either the clock pulse input C or all the scan inputs of the PDU50B must be at the HIGH level during the time the shift pulse input T_C of the MID50 is at the LOW level.

CIRCUIT DATA



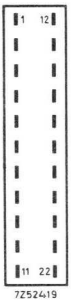
PDU50A



PDU50B

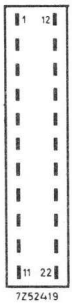
Terminal location

PDU50A



1 = I_1 = decimal input 1
2 = I_2 = decimal input 2
3 = I_3 = decimal input 3
4 = I_4 = decimal input 4
5 = I_5 = decimal input 5
6 = L = control input
7 = Q_1 = decimal output 1
8 = Q_2 = decimal output 2
9 = Q_3 = decimal output 3
10 = Q_4 = decimal output 4
11 = Q_5 = decimal output 5
12 = Q_6 = decimal output 6
13 = Q_7 = decimal output 7
14 = Q_8 = decimal output 8
15 = Q_9 = decimal output 9
16 = Q_0 = decimal output 0
17 = L = interconnected with 6
18 = I_6 = decimal input 6
19 = I_7 = decimal input 7
20 = I_8 = decimal input 8
21 = I_9 = decimal input 9
22 = I_0 = decimal input 0

PDU50B



1 = V_{p_1} = +24 V supply
2 = 0 = common 0 V
3 = K_1 = interconnecting point
4 = K_2 = interconnecting point
5 = L_1 = control output 1
6 = L_2 = control output 2
7 = L_3 = control output 3
8 = S_1 = scan control input 1
9 = S_2 = scan control input 2
10 = S_3 = scan control input 3
11 = C = clock control input
12 to 22 = not provided

Power supply PDU50B

Voltage V_{p_1} = 24 V ± 10%

Current I_{p_1} = 1 mA

INPUT DATA

PDU50A

Decimal inputs I_0 to I_9

These inputs are to be driven from decimal outputs Q_0 to Q_9 of either NIC50, RIC50 or MID50.
By applying a suitable, positive voltage to input L derived from output L_1, L_2 or L_3 of the PDU50B, that output Q becomes HIGH which has a LOW level at its input.

Voltage LOW:
V_I = max. 5 V
I_I = max. 35 μA

Voltage HIGH:
V_I = min. 0.8 V_{p_1}

PDU50B

Clock control input C (terminal 11)

Voltage LOW:
V_C = max. 5 V
I_C = max. 35 μA

Voltage HIGH:
V_C = min. 0.9 V_{p_1}

Scan control inputs S_1, S_2, S_3 (terminals 8, 9, 10)

Voltage LOW:
V_S = max. 5 V
I_S = max. 35 μA

Voltage HIGH:
V_S = min. 0.9 V_{p_1}

OUTPUT DATA

PDU50A

Output voltage LOW:
V_Q = max. 0.3 V

Output voltage HIGH:
I_Q = max. 0.34 mA (V_Q = 13.4 V); EQUALS TWO D.U.

PDU50B

Available output at the HIGH and LOW level (terminals L_1 to L_3) are adapted to the input requirements of the input terminal L of units PDU50A.

DECADE COUNTER AND DIVIDER

Function	Divider of 2, 3, 4, 5, 6, 8, 9, 10, 12 and 16
Ambient temperature range	
operating	−25 to +70 °C (at Vp = 24 V ±10%) −10 to +70 °C (at Vp = 24 V ±25%)
storage	−40 to +85 °C

DESCRIPTION

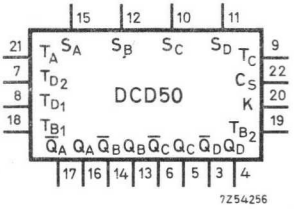
The DCD50 consists of four flip-flops. By correctly interconnecting the terminals a divider of 2, 3, 4, 5, 6, 8, 9, 10, 12 or 16 can be obtained. Each flip-flop is driven by a positive-going pulse. The flip-flops have one common reset input and four separate preset inputs, their condition being governed by a positive-going pulse applied to the appropriate terminal(s). When setting or presetting the DCD50 one sometimes has to apply a HIGH level signal to one of the trigger inputs of the second flip-flop (input K, via a diode).

Truth table (decade counter configuration):

	FF-A	FF-B	FF-C	FF-D
pulse	$\overline{Q_A}$	$\overline{Q_B}$	$\overline{Q_C}$	$\overline{Q_D}$
initial state	1	1	1	1
1	0	1	1	1
2	1	0	1	1
3	0	0	1	1
4	1	1	0	1
5	0	1	0	1
6	1	0	0	1
7	0	0	0	1
8	1	1	1	0
9	0	1	1	0

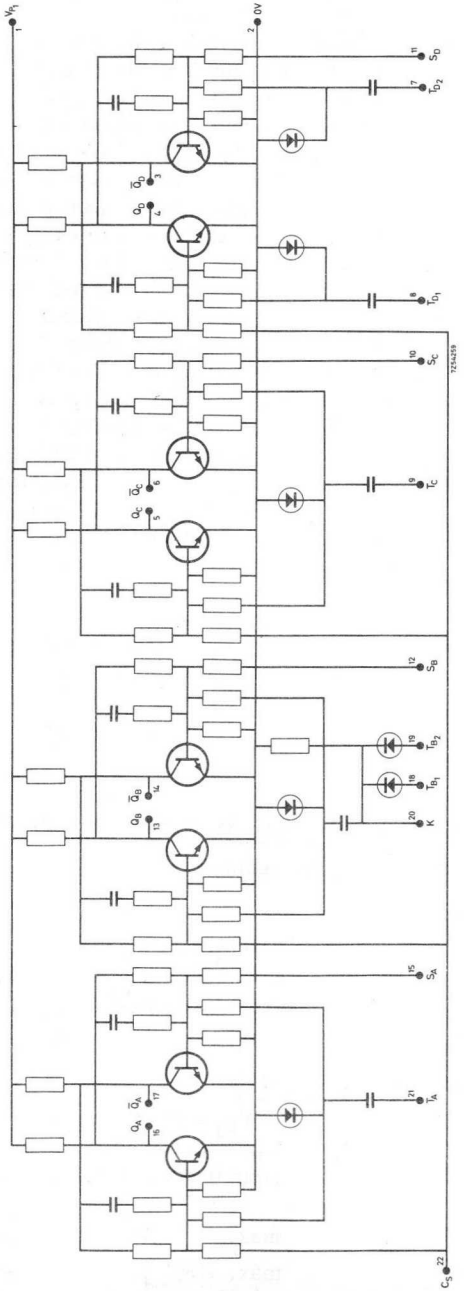
The table below shows the interconnections to be made externally for the various dividers:

divider	input	interconnection	output
2	8	7-8	$\overline{Q_D}$
	9	–	$\overline{Q_C}$
	18	–	$\overline{Q_B}$
	21	–	$\overline{Q_A}$
3	18	4-19, 7-14, 8-18	$\overline{Q_D}$
4	9	6-7-8	$\overline{Q_D}$
	21	17-18	$\overline{Q_B}$
5	18	4-19, 6-7, 8-18, 9-14	$\overline{Q_D}$
6	21	4-19, 7-14, 8-17-18	$\overline{Q_D}$
8	21	6-7-8, 9-17	$\overline{Q_D}$
9	18	4-19, 6-7, 8-18, 9-17, 14-21	$\overline{Q_D}$
10	21	4-19, 6-7, 8-17-18, 9-14	$\overline{Q_D}$
12	9	4-19, 6-21, 7-14, 8-17-18	$\overline{Q_D}$
16	21	6-7-8, 9-14, 17-18	$\overline{Q_D}$

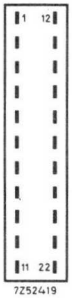


Drawing symbol

CIRCUIT DIAGRAM



Terminal location



1 = V_{p_1} = +24 V supply
2 = 0 = common 0 V
3 = $\overline{Q_D}$ = output $\overline{Q}$ of flip-flop D
4 = Q_D = output Q of flip-flop D
5 = Q_C = output Q of flip-flop C
6 = $\overline{Q_C}$ = output $\overline{Q}$ of flip-flop C
7 = T_{D2} = trigger input T of flip-flop D
8 = T_{D1} = trigger input T of flip-flop D
9 = T_C = trigger input T of flip-flop C
10 = S_C = preset input of flip-flop C
11 = S_D = preset input of flip-flop D
12 = S_B = preset input of flip-flop B
13 = Q_B = output Q of flip-flop B
14 = $\overline{Q_B}$ = output $\overline{Q}$ of flip-flop B
15 = S_A = preset input of flip-flop A
16 = Q_A = output Q of flip-flop A
17 = $\overline{Q_A}$ = output $\overline{Q}$ of flip-flop A
18 = T_{B1} = trigger input T of flip-flop B
19 = T_{B2} = trigger input T of flip-flop B
20 = K = extender input of flip-flop B
21 = T_A = trigger input T of flip-flop A
22 = C_S = common reset input

Power supply

Voltage: V_{p_1} = +24 V ±10% (at T_{amb} = −25 to +70 °C)
V_{p_1} = +24 V ±25% (at T_{amb} = −10 to +70 °C)

Current: I_{p_1} = 25 mA nominal

INPUT DATA

Trigger inputs T_A, T_{B1}, T_{B2}, T_C, T_{D1} and T_{D2} (terminals 21, 18, 19, 9, 8 and 7)

The trigger inputs require a positive-going pulse.

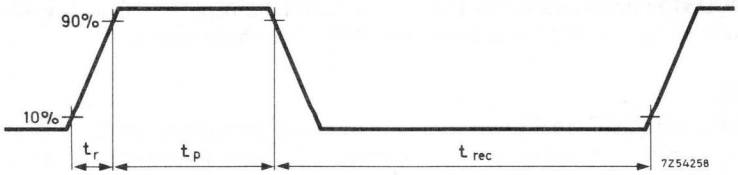
From another DCD50

	V_{p_1} = 24 V ±10%	V_{p_1} = 24 V ±25%
Triggering edge	from 0.3 V to 0.7 V_{p_1}	from 0.3 V to 0.8 V_{p_1}
Wiring capacitance C_w	C_w = max. 150 pF	

From a PSR50 (output Q_T) or from a NOR unit

	V_{p_1} = 24 V ±10%	V_{p_1} = 24 V ±25%
Triggering edge	from 0.3 V to 0.91 V_{p_1}	from 0.3 V to 0.83 V_{p_1}
Permissible load at output of driving unit	max. 1 D.U.	max. 2 D.U.
Wiring capacitance C_w	max. 150 pF	max. 50 pF

Time data



Fall time of negative-going input pulse to NOR-unit	t_f	= max.	2 μs
Rise time of input pulse to trigger input T of DCD50 from another unit than those mentioned above	t_r	= max.	1 μs
Pulse duration	t_p	= min.	4 μs
Recovery time for inputs T_A, T_C, T_{D1}, T_{D2}	t_{rec}	= min.	10 μs
	t_p+t_{rec}	= min.	30 μs
for inputs T_{B1}, T_{B2}	t_{rec}	= min.	80 μs, required at input: 1 D.U.
	t_{rec}	= min.	40 μs, with external resistor of 82 kΩ between K and 0; required at input: 2 D.U.
	t_{rec}	= min.	27.5 μs, with external resistor of 43 kΩ between K and 0; required at input: 3 D.U.

Noise margin 1.5 V

Common reset input C_S (terminal 22) and preset inputs S_A, S_B, S_C and S_D (terminals 15, 12, 10 and 11)

Voltage LOW

V_S, V_{CS} = max. 0.3 V

Voltage HIGH

V_S, V_{CS} = min. 0.62 V_{P_1}

I_S = min. 0.24 mA (V_S = 13.4 V); EQUALS 1.5 D.U.

I_{CS} = min. 0.96 mA (V_{CS} = 13.4 V); EQUALS 6 D.U.

Resetting

When a DCD50 is used as a divider of 3, 5 or 9 an inhibit pulse (HIGH level) must be applied to K (terminal 20) via a diode type BAX13 (cathode to K).

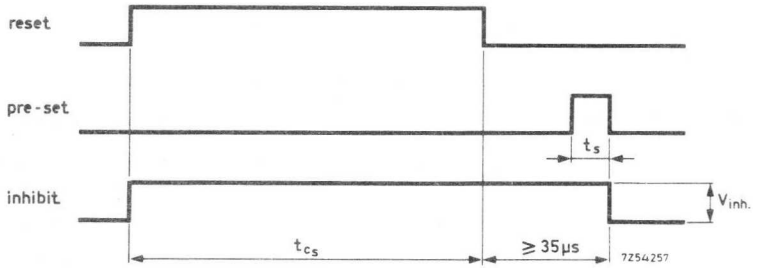
Presetting

When a DCD50 is used as a divider of 3, 5 or 9 and presetting via S_D (terminal 11) is required, an inhibit pulse must be applied to K (terminal 20) via a diode BAX13 (cathode to K).

When a DCD50 is used as divider of 6, 10 and 12 and presetting via S_A and S_D (terminals 15 and 11) is required, an inhibit pulse must be applied to K (terminal 20) via a diode BAX13 (cathode to K).

Time data

The reset pulse and the preset pulse must not be applied at the same time.



Reset pulse duration t_{cs} = min. 20 μs per flip-flop

Preset pulse duration t_s = min. 5 μs

Time delay between reset (preset) pulse and trigger input signal t_{r-t} = min. 30 μs

Time delay between end of reset pulse and end of preset pulse t_{r-p} = min. 35 μs

Inhibit pulse:

Voltage HIGH: $V_{inh} \geq V_{TB1\ (TB2)} - 1.5$ V

When inhibit pulses are applied the total reset time in a chain of dividers, built with the DCD50, can be reduced to t = (n + 1) 20 μs, where n = maximum number of flip-flops between two inhibited flip-flops.

OUTPUT DATA

The outputs of the four flip-flops are Q_A, $\overline{Q_A}$, Q_B, $\overline{Q_B}$, Q_C, $\overline{Q_C}$, Q_D and $\overline{Q_D}$.

Voltage LOW

V_Q = max. 0.3 V

Voltage HIGH

	V_{p1} = 24 V ±10%	V_{p1} = 24 V ±25%
Loadability	6 D.U.	4 D.U.

Loadability at V_{p1} = 24 V ±10%

- Each output can be loaded with one trigger input of a NIC50.
- The outputs Q_A, Q_B, $\overline{Q_B}$, Q_C and $\overline{Q_C}$ can be loaded with 6 D.U. plus one trigger input of a next DCD50 (except T_{B_1}, and T_{B_2}) or with 4 D.U. plus one base input of a PSR50.
- For further output data and maximum pulse repetition frequency, see table on next page.

Wiring capacitance at each output: C_W = max. 150 pF

Note - For proper inhibiting of the trigger gate of the second flip-flop in the DCD50 the load at the inhibiting output must not exceed the load at the trigger input by more than 2 D.U.

divider of	input		max. p.r.f. (kHz)			available output (D.U.)							
	terminal	required (D.U.)	without resistor *) **)	with 43 kΩ *) **)	with 82 kΩ *) **)	Q_A	$\overline{Q_A}$	Q_B	$\overline{Q_B}$	Q_C	$\overline{Q_C}$	Q_D	$\overline{Q_D}$
2	21	–	30			6	6						
	9	–	30							6	6		
	7-8	–	30									6	6
	18	3		30 18				6	6				
		2			22 12.5			6	6				
		1	12 6					6	6				
3	8-18	3		30 18				6	6			3	6
		2			22 12.5			6	6			4	6
		1	12 6					6	6			5	6
4	9	–	30							6	6	6	6
	21	–		30		6	3	6	6				
					24	6	4	6	6				
			12			6	5	6	6				
5	8-18	3		30 18				6	6	6	6	3	6
		2			22 12.5			6	6	6	6	4	6
		1	12 6					6	6	6	6	5	6
6	21	–		30		6	3	6	6			3	6
					24	6	4	6	6			4	6
			12			6	5	6	6			5	6
8	21	–	30			6	6			6	6	6	6
9	8-18	3		30 18		6	6	6	6	6	6	3	6
		2			22 12.5	6	6	6	6	6	6	4	6
		1	12 6			6	6	6	6	6	6	5	6
10	21	–		30		6	3	6	6	6	6	3	6
					24	6	4	6	6	6	6	4	6
			12			6	5	6	6	6	6	5	6
12	9	–			30	6	4	6	6	6	6	4	6
			24			6	5	6	6	6	6	5	6
16	21	–	30***)			6	6	6	6	6	6	6	5
				30		6	3	6	6	6	6	6	6
					24	6	4	6	6	6	6	6	6
			12			6	5	6	6	6	6	6	6

*) Input pulses according to "Time data".

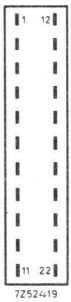
**) Input pulses with $\frac{1}{2}$ T wave form.

***) Second flip-flop (B) is last in chain.

Preset switch

For decoding the DCD50 in preset programmed counting systems use has to be made of the decoding switch 1248N, catalogue number 4311 027 82221.

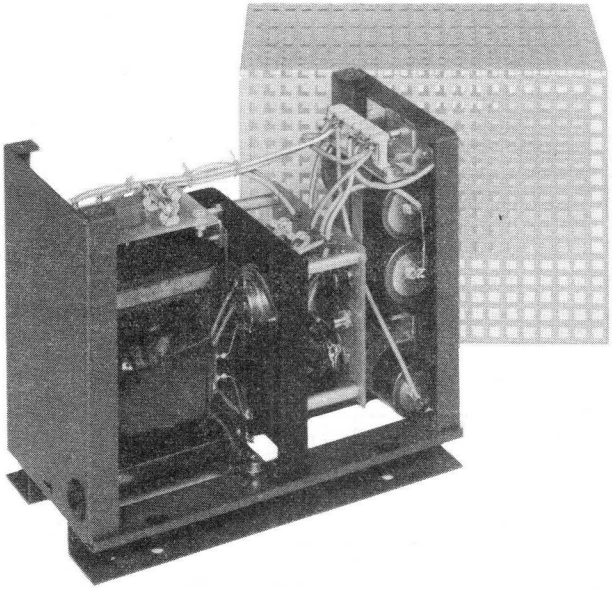
Note that:
- the outputs of the DCD50 have to be connected to the switch inputs as given below
- the internal resistance of the switch (terminal 12) has to be left floating.



1 = not connected	12 = floating
2 = not connected	13 = not connected
3 = not connected	14 = not connected
4 = $\overline{Q_D}$	15 = $\overline{Q_A}$
5 = Q_D	16 = Q_A
6 = output (pole)	17 = output (pole)
7 = Q_B	18 = Q_C
8 = $\overline{Q_B}$	19 = $\overline{Q_C}$
9 = not connected	20 = not connected
10 = not connected	21 = not connected
11 = not connected	22 = not connected

Note - The output (pole) of the decoding switch may directly be connected to one of the inputs of a NOR in the 4.NOR51 unit.

POWER SUPPLY UNIT
for 50-Series direct display counters



RZ 24599-2

TECHNICAL PERFORMANCE

Operating ambient temperature range	−25 to +65 °C

The unit is provided with a temperature fuse (F1).

Input data

Input voltage	110, 120, 130, 220, 230, 240 V_{ac}, +10%, −15%
Input frequency	45 to 65 Hz

Output data

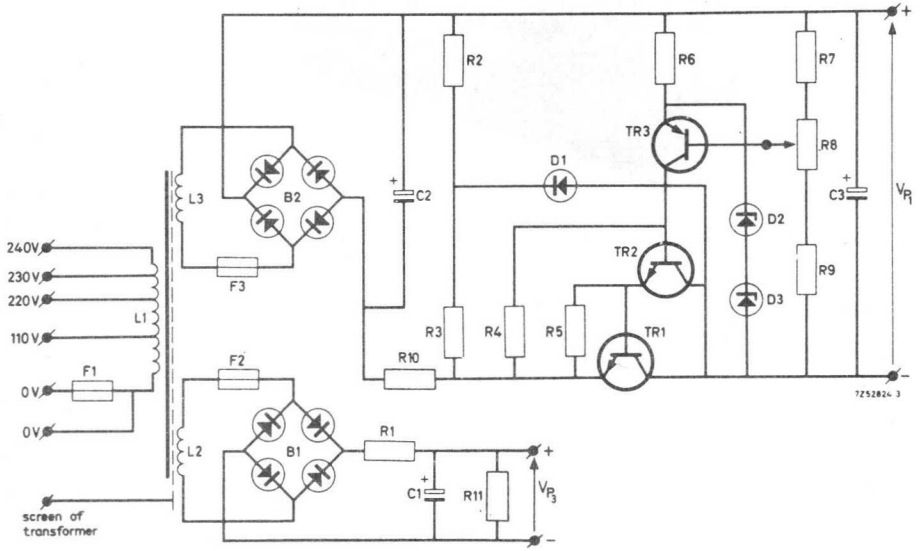
Logic supply (V_{P1})

Output voltage	+24 V ± 5%
Output current	0 to 250 mA
Internal resistance	0.5 Ω
Ripple voltage	10 mV_{rms}
Temperature coefficient	1 mV/deg C (typical value)
Fusing	easy replaceable fuse (630 mA slow, F3)

Provided with automatic short-circuit protection

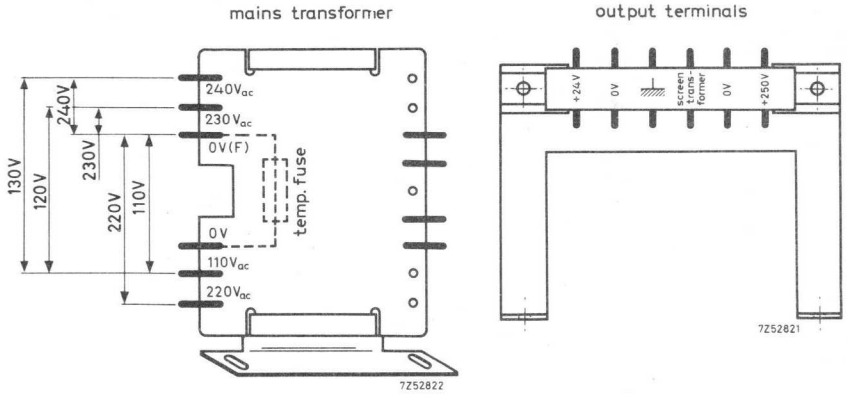
Numerical indicator tube supply (V_{P3})

Output voltage	+250 V ± 18%
Output current	max. 40 mA
Fusing	easy replaceable fuse (100 mA slow, F2)



Circuit diagram

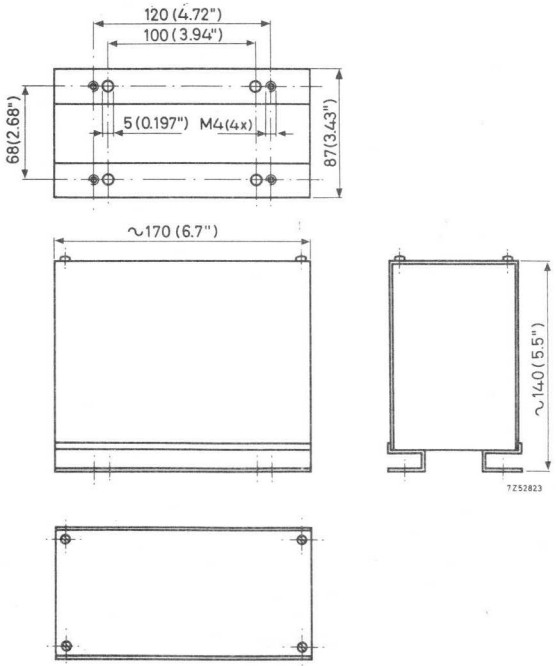
Terminal location



Note - Both input and output terminals are suitable for direct soldered connections.

MECHANICAL DATA

Housing	steel
Cover	perforated steel



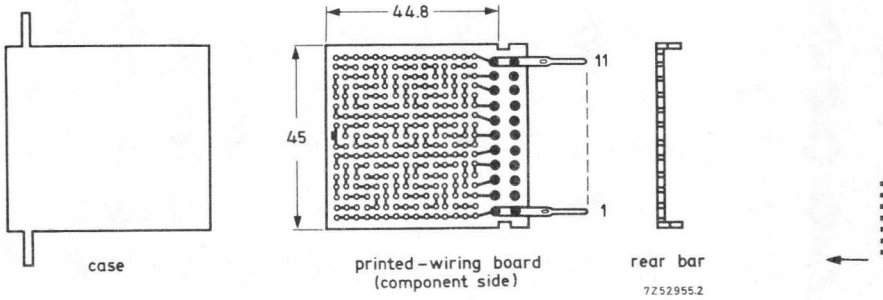
Dimensions in mm, inch values between brackets

EMPTY CASE ASSEMBLY

Function	Empty case assembly for non-standard circuits

DESCRIPTION

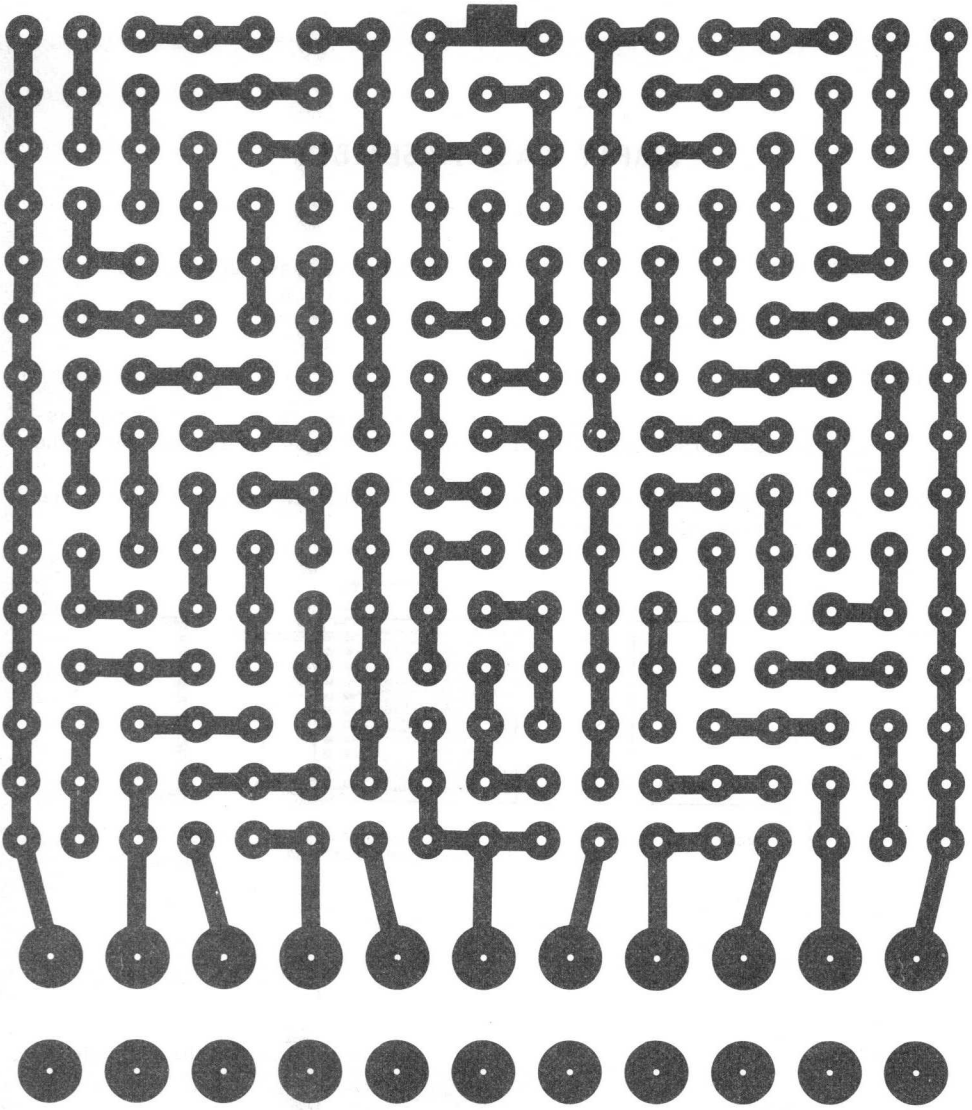
For non-standard circuit configurations an empty case assembly comprising a plastic case, a general purpose printed-wiring board and a rear bar is available in the 50-Series.
With these items non-standard circuits can be built in a technology similar to that of all auxiliary modules in the range.



Dimensions in mm

Printed-wiring board material	glass-epoxy with 254 plated-through holes
hole diameter	$0.8\ ^{+0.2}_{-0.05}$ mm
grid pitch	2.54 mm (0.1 inch)
contacts	11; similar to those of all other 50-Series modules

Note: On the next page the lay-out of the printed wiring (component side) is shown on a scale 3:1, which can be used as an aid for the designer.



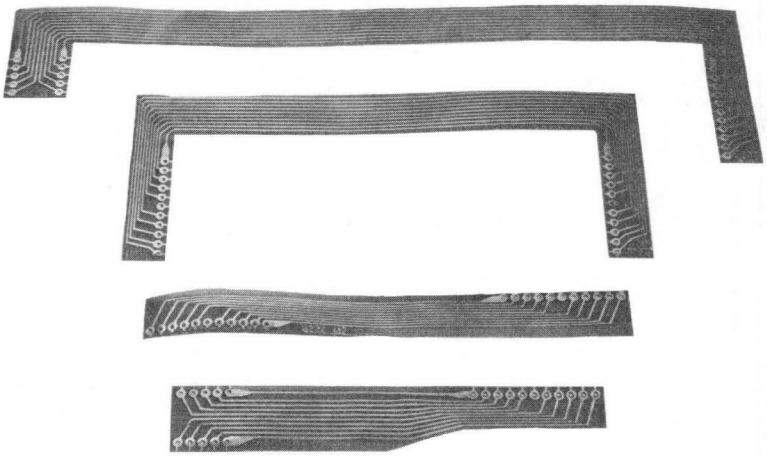
Lay-out of printed wiring (component side); scale 3 : 1

ACCESSORIES FOR COUNTER MODULES
50-SERIES

MOUNTING ACCESSORIES

For mounting accessories the sections "INTRODUCTION" and "CONSTRUCTION" of 50-Series, General should be consulted.

FLEXIBLE PRINTED WIRING



RZ 28179-3

The use of flexible printed wiring considerably shortens the time required to wire the modules, while allowing a neat and simple construction. Four types are available:

- Type HCS50, catalogue number 8222 412 10291, for interconnecting the ten output terminals of counters NIC50 or RIC50 to the corresponding terminals of the thumbwheel switches, when the modules are mounted on a horizontal axis
- Type HSS50, catalogue number 8222 412 10301, for interconnection between thumbwheel switches mounted on a horizontal axis
- Type VCS50, catalogue number 8222 412 10310 for interconnecting counters NIC50 and RIC50 and the thumbwheel switches, when these modules are mounted on a vertical axis
- Type VSS50, catalogue number 8222 412 10320 for interconnection between thumbwheel switches mounted on a vertical axis.

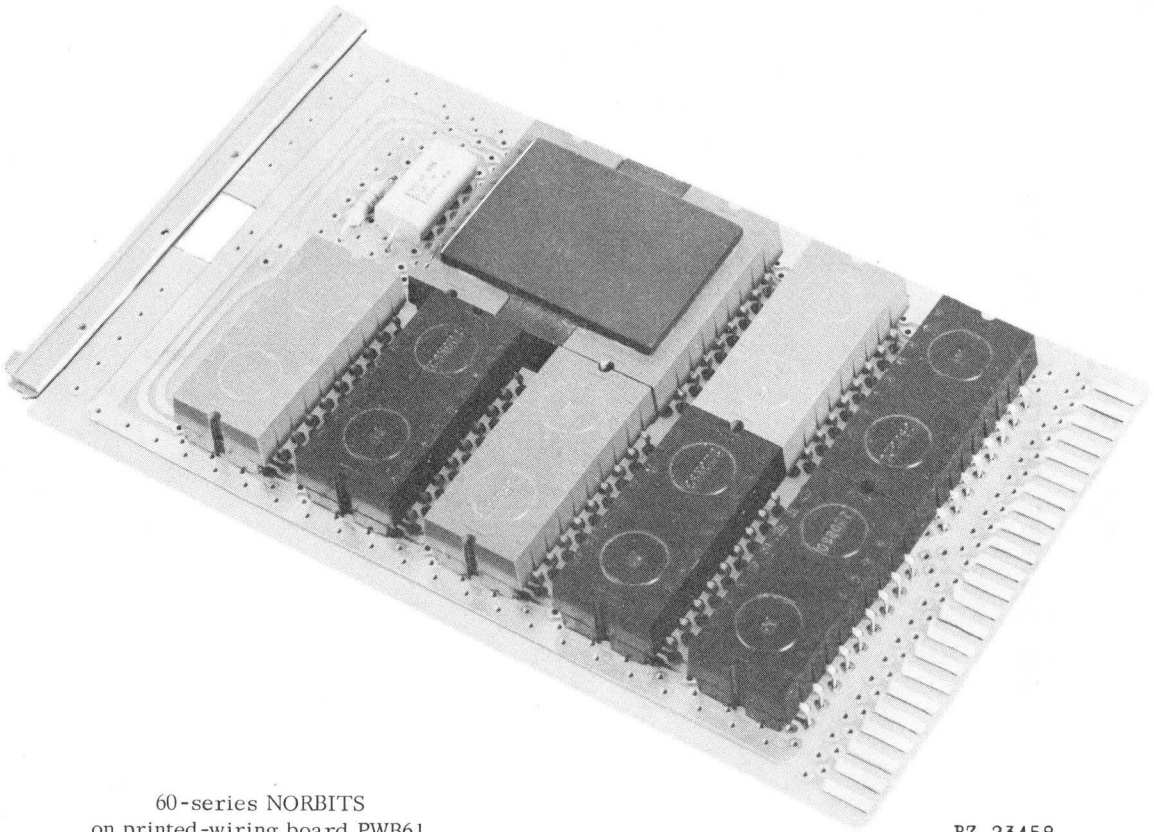
More complex installations, with combinations of vertical and horizontal mounting can be covered with the above four types of flexible printed wiring.

STICKERS

Stickers are drawing symbols of 50-Series modules printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings.
The stickers are available in sheets. Each sticker can be separately detached from the sheet, without cutting.

sheet with modules of type	catalogue number for 50 sheets
NIC50 (4x) + SU50 (8x)	4322 026 70260
LRD50 (3x) + PSR50 (2x) + 3.NOR50 (3x)+ 4.NOR51 (2x)	70270
RIC50 (4x) + SU50 (8x)	70430
MID50 (8x) + SID50 (4x)	70440
PDU50A (9x) + PDU50B (3x)	71910
DCD50	71920

NORBITS
60-Series and 61-Series



60-series NORBITS
on printed-wiring board PWB61

RZ 23458

60-SERIES NORBITS

INTRODUCTION

The 60 series, which uses NOR logic as a basis of operation, represents an important advance in static switching devices for industrial control systems. It comprises 7 circuit blocks having the following features in common:

- Single rail 24 V ± 25% supply, allowing the use of an inexpensive power supply - which helps to keep the cost down, particularly in small systems.
- Transfer moulded cases, giving optimum protection.
- Rigid terminals spaced at 0.2 in. pitch, permitting a variety of interconnection methods to be used (dip soldering, hand soldering, miniwire wrapping).
- Exceptionally good noise immunity.
- Easy to understand level logic, making it possible to carry out system tests with only a d.c. voltmeter.
- Silicon semiconductors throughout, ensuring reliable operation down to −10 °C and up to +70 °C.
- Low price.

Compatible input and output devices as well as a full range of mounting accessories are available.

The 60 series comprises the following types:

2.NOR 60	Dual 4-input NOR gate
4.NOR 60	Quadruple 2x2 + 2x3 input NOR gate
2.IA 60	Dual Inverter Amplifier
2.LPA 60	Dual Low Power Amplifier
TU 60	Timer Unit
2.SF 60	Dual input Switch Filter
PA 60	Power Amplifier

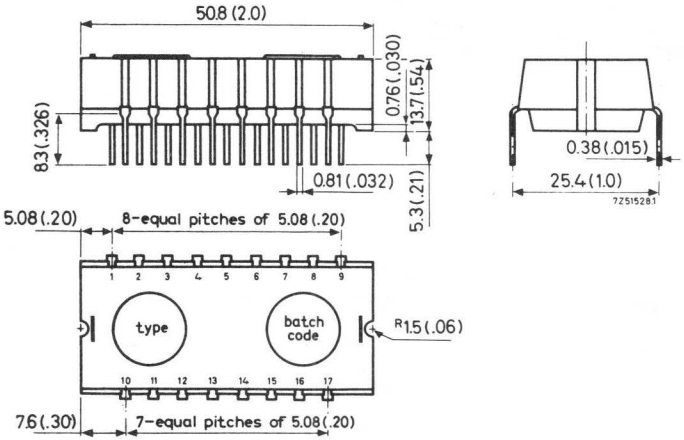
CONSTRUCTION

The circuit elements are housed in a transfer moulded encapsulation. The dimensions are as shown below. The pin connections for each unit are shown on the relevant data sheets. Pin numbering is moulded on both top and bottom of the unit. All pins are also accessible from the top of the unit to facilitate test requirements.

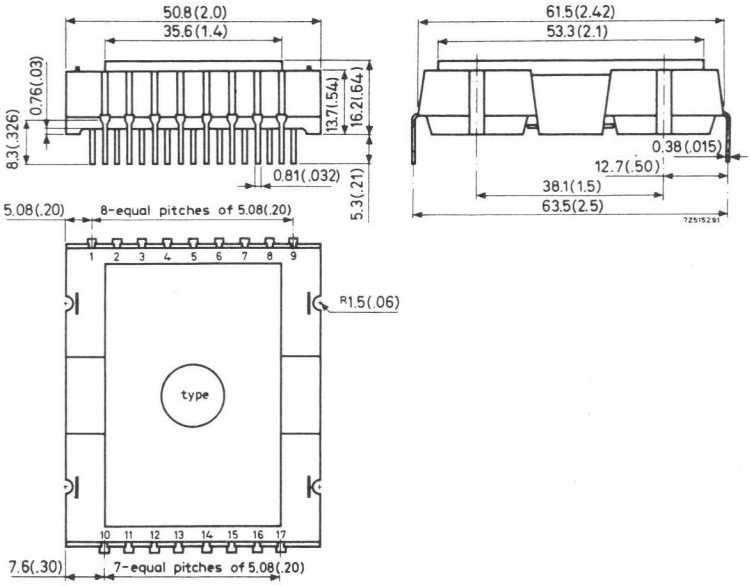
Mounting

The units may be mounted on printed-wiring boards, and a range of these is available with suitable metal mounting chassis. They may also be clamped in the moulded Universal Mounting Chassis UMC 60 or fixed with 3 mm screws.

Dimensions in mm (inch equivalents within brackets)



Size A (types 2.NOR 60, 4.NOR 60, 2.IA 60, 2.LPA 60, 2.SF 60, TU 60)



Size B (type PA 60)

Terminals	suitable for soldering and Miniwrap
Wrap tool	Gardner Denver, bit number 506633
Wrap wire size	0.3 mm (0.012" = 28 U.S. gauge = 30 s.w.g.)
Weight, size A	30 g approx.
size B	85 g approx.
Colour coding	see data sheets of the units

TEST SPECIFICATIONS

All units meet the following test specifications:

Test	IEC 68	MIL-STD-202C
Dry heat life test	56 days at max. diss. max. temp. check at: 0-10/14d-56d.	Meth. 108A, Cond. D; check at 0-10/ 14d-56d.
Long-term damp heat non operating	Test C, 56 days check at 0-10/14d-56d.	Meth. 103B, Cond. D; check at 0-10/ 14d-56d.
Long-term damp heat operating	Test C, 56d. min., diss., check at 0-10/14d-56d.	ditto
Temp. cycle-test	Test Na, 30 min., 2-3 min in between; preferred: -40 °C; +85 °C and +125 °C.	Meth. 107B, Cond. A: moderate temp.
Vibration	Test Fb; 10-500-10 Hz 1 octave/min ; ampl. 0.75 mm max.; 10 g max. 3 x 3 hrs.	Meth. 204A, Cond. A: 10-500-10 Hz: 15 min ampl. 0.75 max; 10 g max., 3 x 3 hrs.
Shock	-	Meth. 202B, 3 blows 50 g.
Robustness of terminations	Test $U_A + U_B$	Meth. 211A + (B or C)
Solderability + solder heat	Test T; at 0 hr and at 56d; no electr. test	Meth. 210, at 0 hr and at 56d; no electr. test

CHARACTERISTICS AND DEFINITIONS

AMBIENT TEMPERATURE LIMITS

Storage	T_{amb} = -40 °C to +85 °C
Operating	T_{amb} = -10 °C to +70 °C

SUPPLY VOLTAGE (V_S)

Single rail, +24 $V_{d.c.}$ ± 25% (18 to 30 V) or
+12 $V_{d.c.}$ ± 5% (11.4 to 12.6 V) at reduced ratings

LOGIC LEVELS

The operation of the "60"-series is based on positive logic, i.e. "1" level is a positive voltage that is more positive than "0" level, and "0" level is independent of supply voltage.
Logic "1" depends upon supply and loading of the output of the logic functional block.

Levels with V_S = 24 V ± 25%	Levels with V_S = 12 V ± 5%
0 V < "0" < +0.3 V	0 V < "0" < +0.3 V
11.4 V < "1" < V_S	8.3 V < "1" < V_S

D.C. NOISE IMMUNITY

"0" level Immunity: A d.c. voltage of +1 V with respect to the 0-volt line, applied to any one input (the other inputs floating) will not cause a change of output voltage.

"1" level Immunity:

a. With a supply voltage of 24 V ± 25%:
A variation of 2 V of the "1" input level will not cause a unit to change its output voltage.

b. With a supply voltage of 12 V ± 5%:
A variation of 0.25 V of the "1" input level will not cause a unit to change its output voltage.

DRIVE UNIT: Drive required on one input of a NOR 60 (with all other inputs returned to 0-volt line) to bring the output at "0" level (less than +0.3 V).

FAN OUT: Number of drive units that can be delivered by a logic function without exceeding the "1" level limits as defined above.
The fan out actually indicates the number of NOR gates that can be driven into saturation (thereby bringing the respective outputs at "0" level).

INPUT AND OUTPUT DATA

EXTENSION OF THE DRIVE UNIT CONCEPT

System design is greatly simplified by expression of the input requirements and fan out capabilities of the various units in integral multiples of the D.U. To check that the loadability of a particular unit is not exceeded, simply add the number of D.U.'s present at its output.

LOADING TABLE

The loading table shows the input requirements and output capability of the various units expressed in D.U.'s.

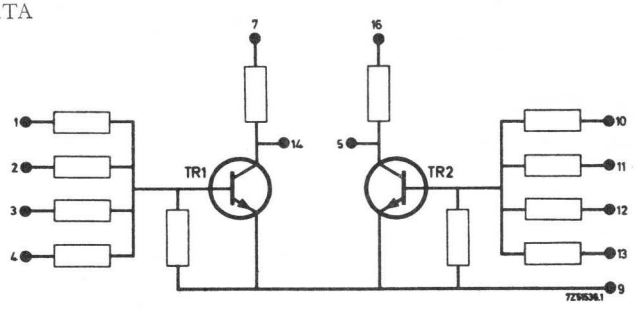
unit	input	V_S = 24 V ±25% output	V_S = 12 V ±5% output
2.NOR 60, per function	1 D.U.	6 D.U.	4 D.U.
4.NOR 60, per function	1 D.U.	6 D.U.	4 D.U.
2.IA 60, per function	2 D.U.	20 D.U.	13 D.U.
2.IA 60, connected as Low Power Amp.	2 D.U.	$R_{load} \geq 300\ \Omega$	$R_{load} \geq 150\ \Omega$
2.LPA 60 per function	2 D.U.	$R_{load} \geq 300\ \Omega$	$R_{load} \geq 150\ \Omega$
PA 60	1 D.U.	$R_{load} \geq 30\ \Omega$	$R_{load} \geq 13\ \Omega$
TU 60	1 D.U.	5 D.U.	3 D.U.
2.SF 60, per filter	100 $V_{d.c.}$	2 D.U.	2 D.U.

For matching non standard input signals to 60-series inputs as well as matching non standard loads, the data sheets of the units give impedances and current requirements.

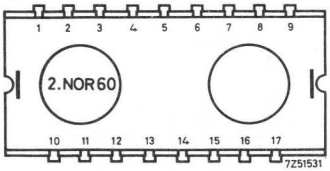
DUAL FOUR INPUT NOR GATE

Function	dual NOR (positive logic)
Case	size: A; colour: black

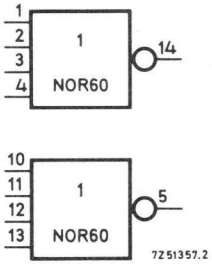
CIRCUIT DATA



Circuit diagram



Terminal location



Drawing symbols

1, 2, 3, 4	= input NOR 1
5	= output NOR 2
6	= n.c.
7	= for supply NOR 1 (V_S)
8	= n.c.
9	= 0 V common
10, 11, 12, 13	= input NOR 2
14	= output NOR 1
15	= n.c.
16	= for supply NOR 2 (V_S)
17	= n.c.

The unit contains two identical transistor-resistor NOR circuits. Each circuit has 4 inputs. If any input of a NOR is at "1" level the output of that NOR will be at "0" level.

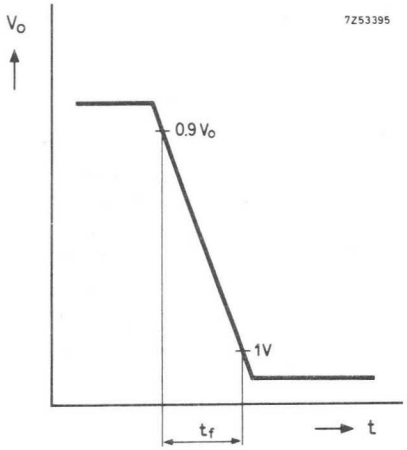
CHARACTERISTICS

	at V_S = 24 V ±25%	at V_S = 12 V ±5%
Supply current at $V_{S\,nom}$	3.2 mA	1.6 mA
at $V_{S\,max}$	≤ 4.2 mA	≤ 1.8 mA
Input requirement	1 D.U.	1 D.U.
Output capability	6 D.U.	4 D.U.

	single input	two paralleled inputs	three paralleled inputs	four paralleled inputs
Input impedance [1]	100 kΩ	62 kΩ	40 kΩ	30 kΩ
Input current for "0" output [1][2]	0.13 mA	0.125 mA	0.11 mA	0.1 mA

Switching speed

Fall time defined below	$t_f \leq 1.25\ \mu s$
Fall delay time defined below	$t_{fd} \leq 6\ \mu s$



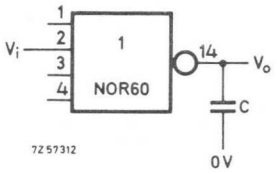


Fig.A

The fall time t_f is defined as the time required for the output voltage V_O to change from 90% of its full value to 1 V after application of a step input, the output being loaded with C = 200 pF (see Fig.A).

1) Not used inputs returned to 0-volt line.
2) At V_S = 30 V.

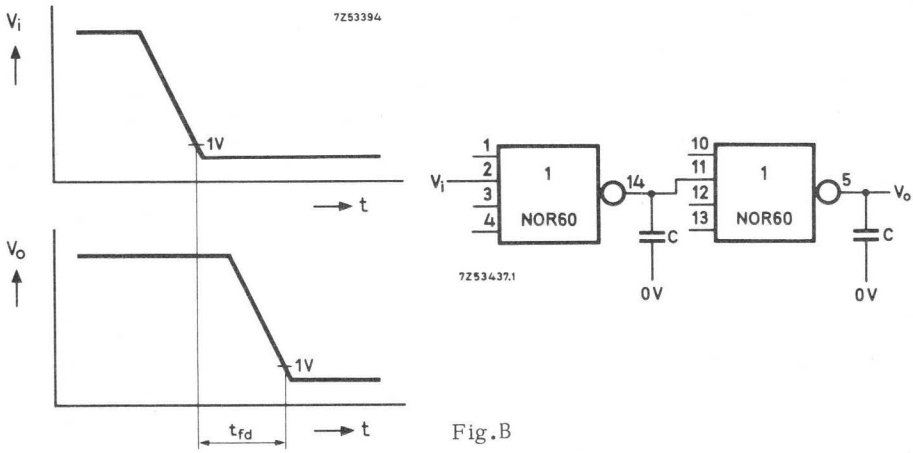


Fig.B

The fall delay time t_{fd} is defined as the time between the 1 V points of the negative-going input and output voltages of two cascaded NORs, each being loaded with C = 200 pF (see Fig.B).

LIMITING VALUES (Destruction may occur when these values are exceeded)

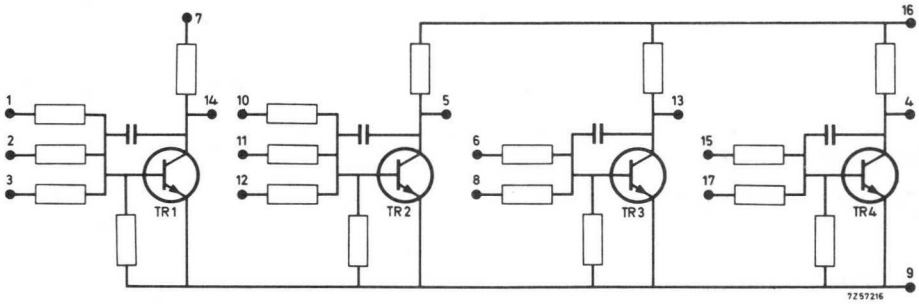
Supply voltage	V_S	max. 30	$V_{d.c.}$
		min. 0	V
Positive transient on V_S		max. 10	V during 10 μs
Positive input voltage	$+V_i$	max. 90	V
Negative input voltage	$-V_i$	max. 18	V

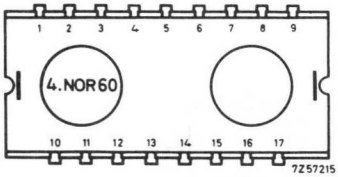
QUADRUPLE 2×2 + 2×3 INPUT NOR GATE

Function: quadruple NOR (positive logic)

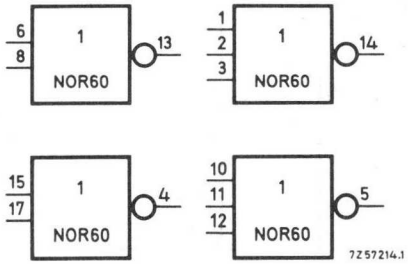
Case: size: A; colour: black

CIRCUIT DATA





Terminal location



Drawing symbols

1, 2, 3 = input NOR 1
4 = output NOR 4
5 = output NOR 2
6, 8 = input NOR 3
7 = for supply NOR 1 (V_S)
9 = 0 V common
10, 11, 12 = input NOR 2
13 = output NOR 3
14 = output NOR 1
15, 17 = input NOR 4
16 = for supply NOR 2, 3, 4 (V_S)

The unit contains two identical 2-input and two identical 3-input NOR circuits. If any input of a NOR is at "1" level the output of that NOR will be at "0" level.

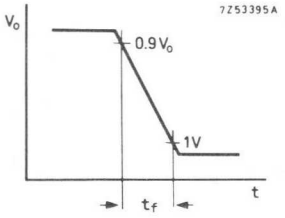
CHARACTERISTICS

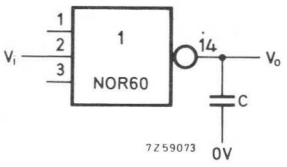
	at V_S = 24 V ±25%	at V_S = 12 V ±5%
Supply current at $V_{S\,nom}$	3.2 mA	1.6 mA
at $V_{S\,max}$	≤ 4.2 mA	≤ 1.8 mA
Input requirement	1 D.U.	1 D.U.
Output capability	6 D.U.	4 D.U.

	single input	two paralleled inputs	three paralleled inputs
Input impedance [1])	90 kΩ	50 kΩ	35 kΩ
Input current for "0" output [1])[2])	0.13 mA	0.125 mA	0.11 mA

→ Switching speed

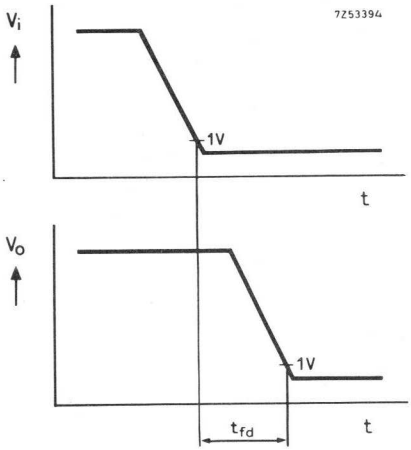
Fall time defined below	t_f	≤ 14 μs
Fall delay time defined below	t_{fd}	≤ 26 μs





The fall time t_f is defined as the time required for the output voltage V_O to change from 90% of its full value to 1 V after application of a step input, the output being loaded with C = 200 pF (see Fig. A).

[1]) Not used inputs returned to 0-volt line.
[2]) At V_S = 30 V.



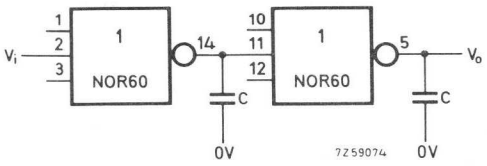


Fig.B

The fall delay time t_{fd} is defined as the time betweeb the 1 V points of the negative-going input and output voltages of two cascaded NORs, each being loaded with C = 200 pF (see Fig.B).

LIMITING VALUES (Destruction may occur when these values are exceeded)

Supply voltage	V_S	max. 30 V min. 0 V	$V_{d.c.}$
Positive transient on V_S		max. 10 V for 10 μs	
Positive input voltage	$+V_i$	max. 90 V	
Negative input voltage	$-V_i$	max. 24 V	

DUAL INVERTER AMPLIFIER

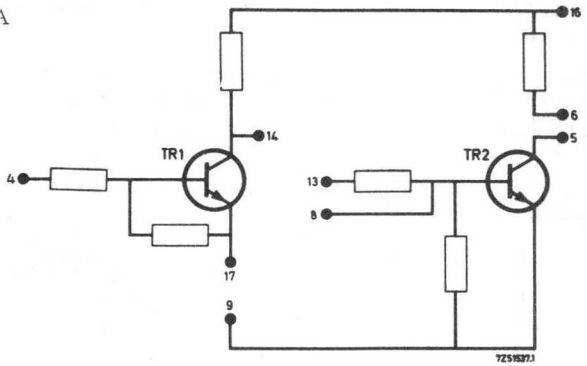
Function

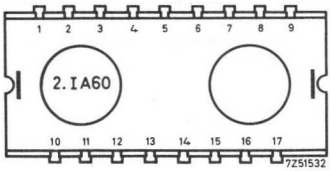
The unit comprises two identical Inverter Amplifiers. Use as a single inverting Low Power Amplifier is feasible.

Case

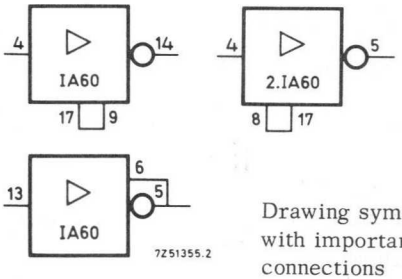
Size: A; colour: blue

CIRCUIT DATA





Terminal location



Drawing symbols with important connections

1, 2, 3 = n.c.
4 = input IA 1
5 = output IA 2
6 = collector resistor IA 2
7 = n.c.
8 = base of IA 2 transistor
9 = 0 V common
10, 11, 12 = n.c.
13 = input IA 2
14 = output IA 1
15 = n.c.
16 = for supply (V_S)
17 = emitter of IA 1 transistor

To obtain the dual I.A., pin 17 should be connected to pin 9 and pin 6 to pin 5.
A "1" level input (pin 4 or 13) will cause a "0" level output (pin 14 or 5-6 respectively).
To obtain the inverting L.P.A., pin 17 should be connected to pin 8 and the load connected between pins 5 and 16. When pin 4 is at "1" level, pin 5 will be at "0" level.

Notes to the load of the L.P.A.

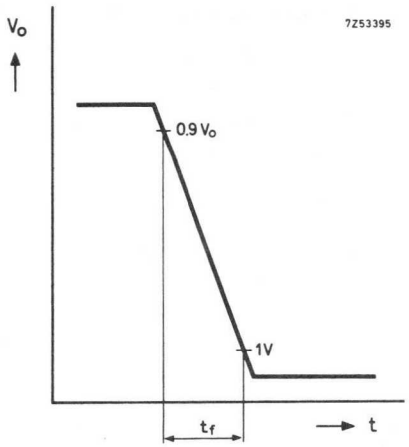
1. Care should be taken that the value of a varying load should not drop below the specified minimum.
2. Incandescent lamps have a "cold" resistance that is only a fraction of the value calculated from nominal voltage and current, so that turning on of the lamp may cause a surge current. It is advisable to use a pre-heating quiescent current to eliminate destructive surge currents.
3. Inductive loads will cause large voltage peaks upon switching off. To avoid destruction the load should be provided with a flywheeling diode, type BY126. The anode should be connected to pin 5, the cathode to pin 16 (positive supply).

CHARACTERISTICS

	at V_S = 24 V ±25%		at V_S = 12 V ±5%	
	per I.A.	as L.P.A.	per I.A.	as L.P.A.
Supply current at $V_{S\,nom}$	10.9 mA	10.9 mA I_{load} = 0 mA	5.5 mA	5.5 mA I_{load} = 0 mA
Supply current at V_S max and "1" input	≤ 14.0 mA	≤ 114 mA R_{load} = 300 Ω	≤ 5.9 mA	≤ 89.9 mA R_{load} = 150 Ω
Input requirement	2 D.U.	2 D.U.	2 D.U.	2 D.U.
Output capability	20 D.U.	140 D.U. [1]	13 D.U.	
Minimum load resistance		300 Ω [1]		150 Ω [1]

Input impedance		45 kΩ
Input current for "0" output of I.A. at V_S = 30 V		0.285 mA
Switching speed		
Fall time defined below	t_f	≤ 1 μs
Fall delay time defined below	t_{fd}	≤ 3 μs

[1]) This load is permissible only if the input switched between "0" and "1" levels by a preceding 60 Series unit or other true digital input, avoiding excessive dissipation during transitions.



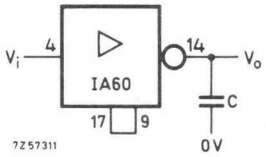
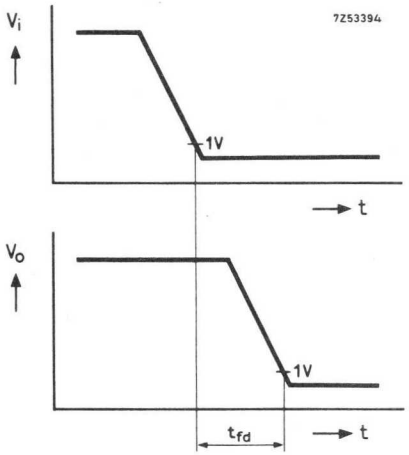


Fig.A

The fall time t_f is defined as the time required for the output voltage V_o to change from 90% of its full value to 1 V, after application of a step input, the output being loaded with C = 200 pF (see Fig.A).



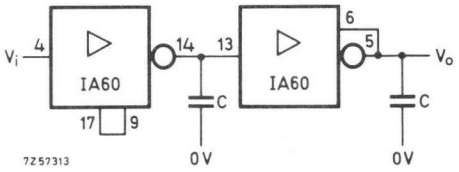


Fig.B

The fall delay time t_{fd} is defined as the time between the 1 V points of the negative-going input and output voltages of two cascaded Inverter Amplifiers, each being loaded with 200 pF (see Fig.B).

LIMITING VALUES (Destruction may occur if these values are exceeded)

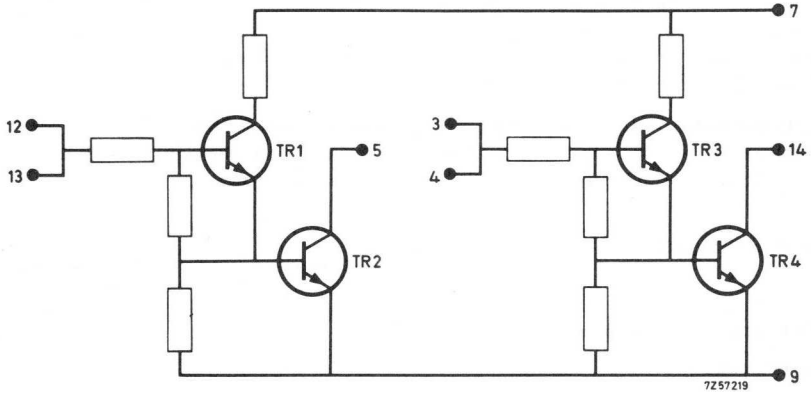
Supply voltage	V_s	max. min.	30 0	$V_{d.c.}$ V
Positive transient on V_s		max.	10	V during 10 μs
Positive input voltage	$+V_4$, $+V_{13}$	max.	70	V
Negative input voltage	$-V_4$, $-V_{13}$	max.	16	V
Positive voltage at pin 8	$+V_8$	max.	1	V via min. 500 Ω
Negative voltage at pin 8	$-V_8$	max.	5	V

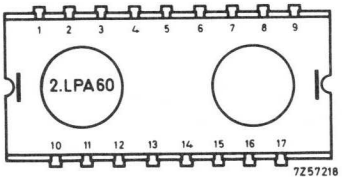
DUAL LOW POWER AMPLIFIER

Function — The unit comprises two identical inverting Low Power Amplifiers

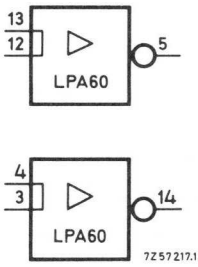
Case — size: A; colour: blue

CIRCUIT DATA





Terminal location



Drawing symbols

1, 2	=	n.c.
3, 4	=	input LPA2
5	=	output LPA1
6	=	n.c.
7	=	for supply (V_S)
8	=	n.c.
9	=	0 V common
10, 11	=	n.c.
12, 13	=	input LPA1
14	=	output LPA2
15, 16, 17	=	n.c.

The load should be connected between pins 5 and 7 for LPA1 and between pins 14 and 7 for LPA2.
When the input (12/13 or 3/4) is at "1" level, the output (5 or 14) will be at less than 1 V. This being no true "0" level, it is not recommended to use an LPA as a logic operator.

Notes to the loading

1. Care should be taken that the value of a varying load should not drop below the specified minimum.
2. Incandescent lamps have a "cold" resistance that is only a fraction of the value calculated from nominal voltage and current, so that turning on of the lamp may cause a surge current. It is advisable to use a pre-heating quiescent current to eliminate destructive surge currents.
3. Inductive loads will cause large voltage peaks upon switching off. To avoid destruction the load should be provided with a flywheeling diode, type BAX12. The anode should be connected to pin 5 (14), the cathode to pin 7 (positive supply).

CHARACTERISTICS

	at V_S = 24 V ±25%	at V_S = 12 V ±5%
Supply current at $V_{S\,nom}$, I_{load} = 0 mA	8 mA	4 mA
Supply current at $V_{S\,max}$ and "1" input,		
R_{load} = 300 Ω	≤ 108 mA	–
R_{load} = 150 Ω	–	≤ 89.9 mA
Input requirement	2 D.U.	2 D.U.
Output capability	100 mA	80 mA
Min. load resistance	300 Ω	150 Ω

Input impedance			45 kΩ
Input current for "0" output at V_S = 30 V			0.285 mA
Output voltage at "1" input			< 1 V
→ Switching speed			
Fall time (Fig.A)	t_f	≤	0.4 μs
Rise time (Fig.B and Fig.C)	t_r	≤	2 μs
Storage time (Fig.B and Fig.C)	t_s	≤	10 μs

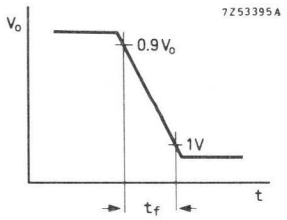


Fig.A

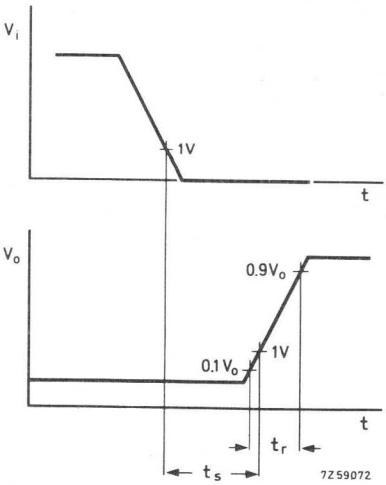


Fig.B

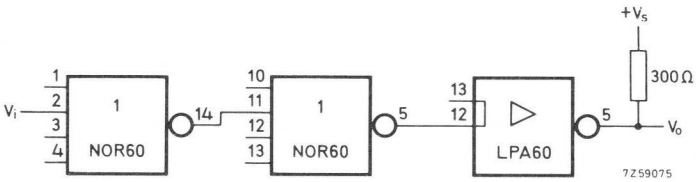


Fig.C

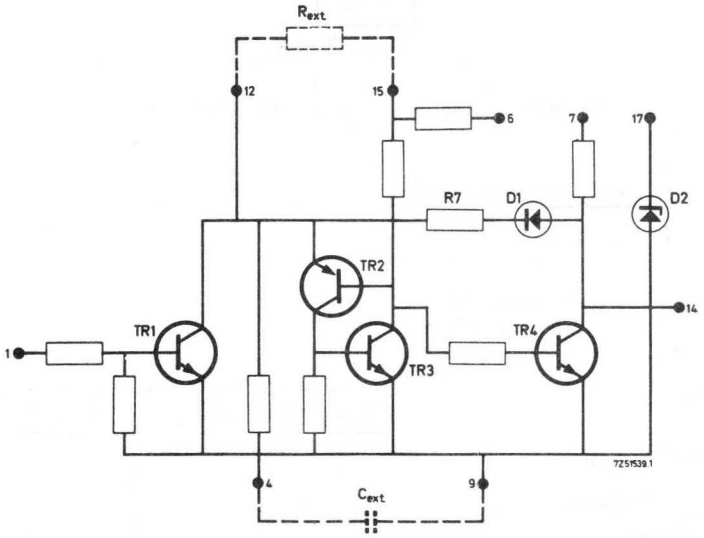
LIMITING VALUES (Destruction may occur if these values are exceeded)

Supply voltage	V_S	max. 30 V min. 0 V	$V_{d.c}$
Positive transient on V_S		max. 10 V	for 10 μs
Positive input voltage	$+V_i$	max. 70 V	
Negative input voltage	$-V_i$	max. 16 V	

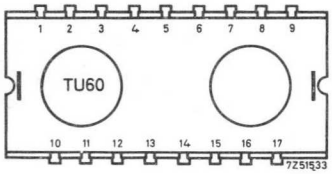
TIMER

Function	Gives an inverted output. The output of a "1" is delayed following a "0" input. No delay occurs when the input returns to "1"
Case	Size: A; colour: red

CIRCUIT DATA

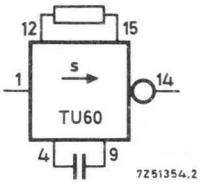


With the input at "1" the capacitor (C_{ext}) is discharged. When the input goes to "0", TR_1 ceases to conduct so that the capacitor is allowed to slowly charge until the base potential of TR_2 is exceeded. TR_2 starts to conduct and provides base current for TR_3, which speeds the turn-on of TR_2. TR_4 ceases to conduct and the output level changes from "0" to "1". Positive feedback is provided via D_1 and R_7.



Terminal location

1	= input	10, 11	= n.c.
2, 3	= n.c.	12	= for external resistor
4	= for external capacitor	13	= n.c.
5	= n.c.	14	= output
6	= see instructions below	15	= for external resistor
7	= positive supply	16	= n.c.
8	= n.c.	17	= see instructions below
9	= 0 V common		



Drawing symbol with significant connections

Instructions for connection of the supply

When V_S = 24 V ±25% : connect 6 and 7, connect 15 and 17.

When V_S = 12 V ±5% : connect 15 and 7, do not connect 6 and 17.

CHARACTERISTICS

	at V_S = 24 V ±25%	at V_S = 12 V ±5%
Supply current at $V_{S\,nom}$	6.9 mA	1.9 mA
at $V_{S\,max}$	10.1 mA	2.1 mA
Input requirement	1 D.U.	1 D.U.
Output capability	5 D.U.	3 D.U.

Input impedance	90 kΩ
Input current for "0" output, at V_S = 30 V	0.125 mA
External resistance	R_{ext} min. 100 kΩ, max. 1 MΩ
External capacitance	C_{ext} requirement: leakage current max. 100 nA at 10 V (or leakage resistance min. 100 MΩ at 10 V)

Delay time (see Fig.A)	t_{delay}	about $R_{ext}\ C_{ext}$ seconds ($M\Omega \times \mu F$)
Max. change of delay time with temperature		-0.14 %/deg C
Switching speed		
Fall time as defined below	t_f	$\leq$ 1 μs
Rise time as defined below	t_r	$\leq$ 6 μs
Timing requirements (see Fig.A)		
Set time	t_{set}	min. 11.9 C_{ext} ms (C_{ext} in μF)
Recovery time	t_{sec}	min. 11.9 C_{ext} ms
Start inhibit before end of delay	$t_{st\ inh}$	min. 18.9 C_{ext} ms
Inhibit duration	t_{inh}	min. 18.9 C_{ext} ms (A shorter t_{inh} gives a shorter delay)

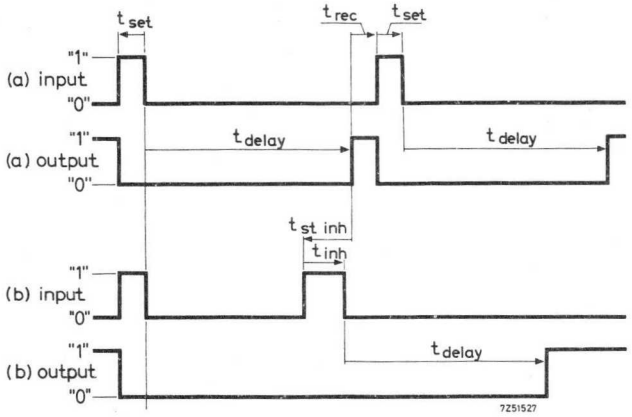


Fig.A

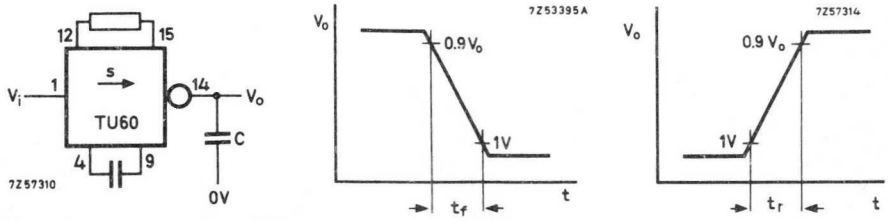


Fig.B

The fall time t_f is defined as the time required for the output voltage V_o to change from 90% of its full value to 1 V, after application of a step input and being loaded with C = 200 pF (see Fig.B).

The rise time t_r is defined as the time required for the output voltage V_o to change from 1 V to 90% of its full value, after application of a step input and being loaded with C = 200 pF (see Fig.B).

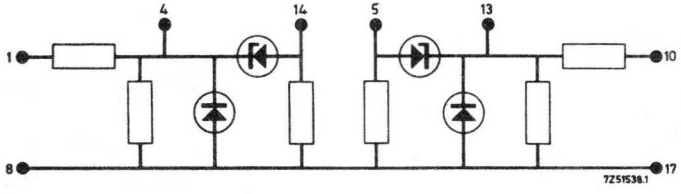
LIMITING VALUES (Destruction may occur if these values are exceeded)

Supply	V_s	max. 30 $V_{d.c.}$ min. 0 V
Positive transient on V_s		max. 10 V during 10 μs
Positive input voltage	$+V_1$	max. 70 V
Negative input voltage	$-V_1$	max. 16 V

DUAL SWITCH FILTER

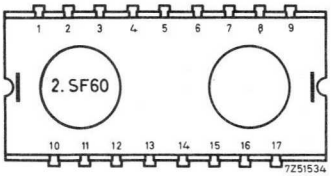
Function	Dual switch filter for eliminating the effects of contact bounce of mechanical switches
Case	size: A; colour: green

CIRCUIT DATA



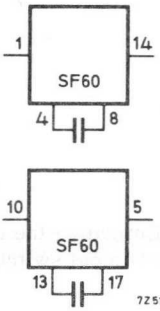
The circuit consists of two identical filters for minimising the effects of contact bounce and spurious interference on long leads between switch and system input. The switch filter also has the facility that 100 V are applied across the switch contacts, thus ensuring reliable switching.

The voltage divider enables the input to be presented with a high impedance load whilst the internal circuitry is presented with a lower impedance source. The time for which contact bounce is eliminated is determined by an external capacitor. The zener diode provides a threshold. The diode prevents that excessive base current is drawn from any driven NORBIT if a large negative voltage appears on the filter input. It also prevents that a reverse voltage is presented to the capacitor, which thus may be of a polarised type.



Terminal location

1	= input SF1	10	= input SF2
2, 3	= n.c.	11, 12	= n.c.
4	= for external capacitor of SF1	13	= for external capacitor of SF2
5	= output SF2	14	= output SF1
6, 7	= n.c.	15, 16	= n.c.
8	= 0 V common	17	= 0 V common (to be taken to central earth point)
9	= n.c.		



Drawing symbols with capacitor

Instructions

a. Capacitor working voltage ≥ 100 $V_{d.c.}$

b. Mount the unit as close as possible to the logic system input.

c. The common 0-volt line (8 or 17) must be returned to the central earth point of the system to avoid common impedance coupling.

CHARACTERISTICS (per filter)

Input voltage for "1" out	+100 V ±25%
Input current	< 3.3 mA
Input surge current peak	< 4.8 mA
Output capability	2 D.U.
Contact bounce elimination time	1.7 C ms (C in μF)

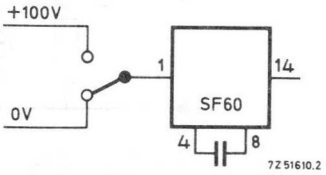


Fig.a

Switching speed (C in μF):	
Turn-on time	41 C ms
Max. operating frequency with 1 : 1 mark to space ratio for circuit Fig.a	$\frac{6.3}{C}$ Hz
Ditto for Fig.b	$\frac{11.08}{C}$ Hz

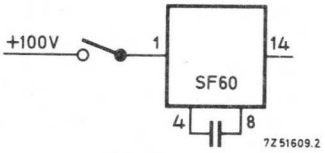


Fig.b

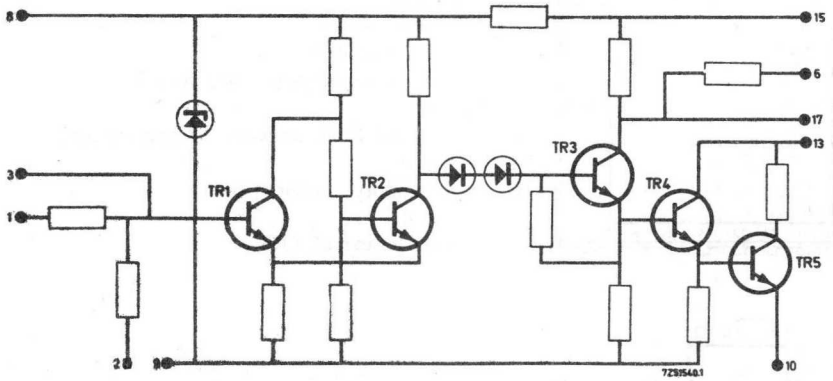
LIMITING VALUES (Destruction may occur if these values are exceeded)

Positive input voltage	$+V_1$, $+V_{10}$	max. 125 V
Negative input voltage	$-V_1$, $-V_{10}$	max. 100 V

POWER AMPLIFIER

Function	Power amplifier for load switching
Case	size: B; colour: blue

CIRCUIT DATA



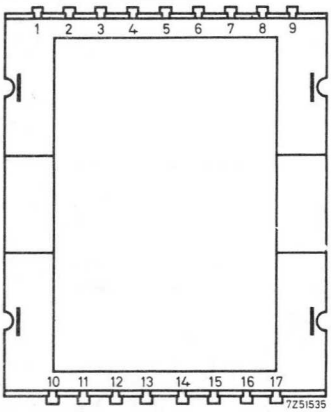
The power amplifier consists of a Schmitt trigger followed by a buffer + driver stage, which provides adequate drive to the power transistor under all conditions of permissible supply voltage and input signal. The load should be connected between pin 13 and + of power supply. A "1" input will switch on the load current.

Notes

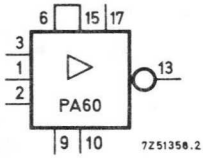
1. Observe rules for $R_{load\,min.}$
2. Incandescent lamps have a "cold" resistance that is only a fraction of the value calculated from voltage and current so that turning on of a lamp may cause a current surge. It is often advisable to use a preheating quiescent current to eliminate destructive surge currents.
3. Inductive loads will cause large voltage peaks at switching off. To avoid destruction of the output transistor the load should be shunted by a damping diode. By using diode type BAX12 a max. current of 1 A at 30 V in a load of 10 H can be switched off, while secondary breakdown is avoided.
   (Connection of the diode: anode to pin 13, cathode to supply).

4. Pin 10 facilitates the connection of a 0 V load supply line which is separated from the 0 V logic supply line up to the power supply unit, by which means common wire impedance is avoided. Also, if a second power supply unit is used for the PA 60, common impedance with the 0 V logic supply line should be avoided in the connecting wire necessary between pin 9 (0 V logic supply) and pin 10 (0 V supply of PA 60).

Terminal location



1 = input
2 = base resistor of input transistor
3 = base of input transistor
4, 5 = n.c.
6 = +supply, connect to 15
7 = n.c.
8 = zener diode
9 = 0 V common
10 = 0 V output stage, see note 4
11, 12 = n.c.
13 = output (load between 13 and supply)
14 = n.c.
15 = +supply, connect to 6
16 = n.c.
17 = collector of TR3



Drawing symbol with one of the necessary connections

Additional instructions

a. If the input (pin 1) is driven by a standard "1" level from NOR 60, etc., connect pins 2 and 9.

b. If the supply voltage is 12 V ±5%, connect a resistor of 330 Ω between pin 6 and 8, and a resistor of 1.5 kΩ between 15 and 17; both resistors ±5%, $\frac{1}{4}$ W.

c. The metal centre part of the case is a heatsink connected to the collector of TR5; it should not be touched by electrical conductors.

CHARACTERISTICS	at V_S = 24 V ±25%	at V_S = 12 V ±5%
Supply current at $V_{S\,nom}$ excluding I_{load}	18.8 mA	15.1 mA
Supply current at $V_{S\,max}$ excluding I_{load}	< 26.2 mA	< 28.8 mA
Required load resistance	> 30 Ω	> 13 Ω
Required input	1 D.U.	1 D.U.
For switching on load current	at pin 1	at pin 3
input voltage	8 V	1.6 V [1]
input current, 2-9 connected	75 μA	75 μA
2-9 not connected	-	30 μA
For switching off load current		
input voltage	< 2.5 V	< 0.65 V
On-off input voltage difference,		
R_{source} < 56 kΩ	-	> 0.32 V

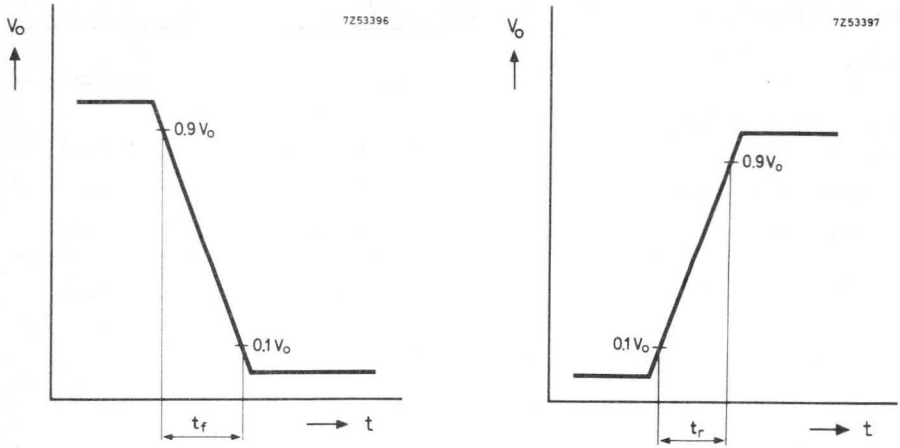
Switching speed

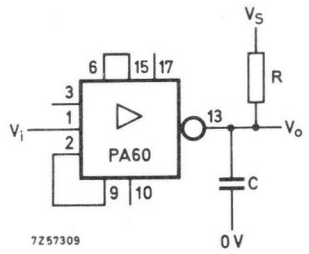
Fall time as defined below	$t_f \leq 1\ \mu s$
Rise time as defined below	$t_r \leq 5\ \mu s$

The fall time t_f is defined as the time required for the output voltage to change from 90% to 10% of its full value, after application of a step input, at a supply voltage V_S = 30 V and a load resistance R = 30 Ω shunted by C = 200 pF (see Figure).

The rise time t_r is defined as the time required for the output voltage to change from 10% to 90% of its full value, after application of a step input, at a supply voltage V_S = 30 V and a load resistance R = 30 Ω shunted by C = 200 pF (see Figure).

1) Via min. 500 Ω.





LIMITING VALUES (Destruction may occur if these values are exceeded)

Supply voltage(s)	V_S	max. 30	$V_{d.c.}$
		min. 0	V
Positive transient on V_S driver stage		max. 10	V during 10 μs
Positive transient on V_S power stage		max. 5	V during 10 μs
Voltage at pin 1 (pins 2 and 9 connected)			
positive	$+V_1$	max. 100	V
negative	$-V_1$	max. 15	V
Voltage at pin 3			
positive	$+V_3$	max. 5	V via min. 500 Ω
negative	$-V_3$	max. 4.5	V

61-SERIES NORBITS

INTRODUCTION

The units of the 61-Series have been designed as an extension to the NORbit range in order to facilitate using NORbits in thyristorized power control circuits. By doing so, designers can cut system costs considerably: for one thing, the number of external components necessary will be reduced to a bare minimum, for another, mounting costs can be kept low as all units are housed in the NORbit size A encapsulation, and thus fit into a UMC60 chassis or can be fixed on the special printed-wiring boards for the 60-Series.
Furthermore, all units in the 61-Series offer the same outstanding features as those of the 60-Series, the chief ones being:

- high noise immunity
- rugged encapsulation with rigid terminals
- ample accessories
- single-rail 24 V $\pm$ 25% supply (except the DOA61)

Comprising the following units:

2.NOR61	Dual NOR-gate with diode-resistor networks
RSA61	Rectifier and synchronization assembly
UPA61	Universal power amplifier
DOA61	Differential amplifier
TT61	Dual thyristor trigger transformer,

the Series may well be expected to find a large number of applications.

An important accessory to this range is the supply transformer ST61.

Wiring Layout Stickers for the 61-Series are available under catalogue number 4322 026 71981.

UNIVERSAL POWER AMPLIFIER

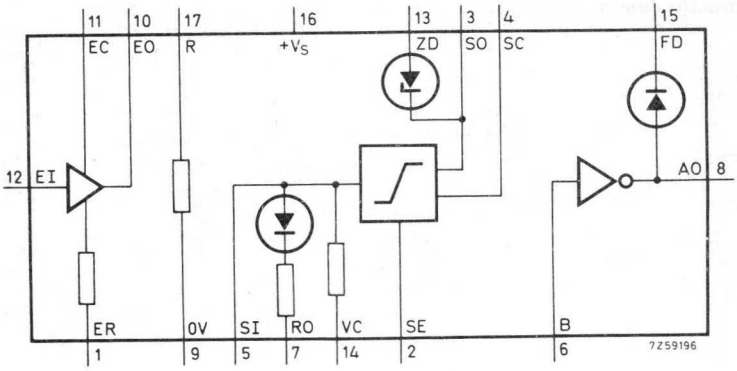
Function

1. D.C. switching amplifier.
2. Power oscillator for driving thyristor trigger transformers.
3. Phase shift module.
4. Current source for linear capacitor discharging.

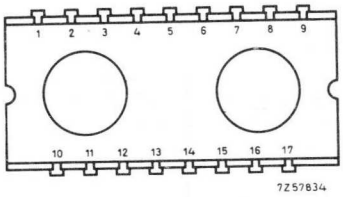
Case

Size: A; Colour: black.

CIRCUIT DATA



Quick reference circuit diagram

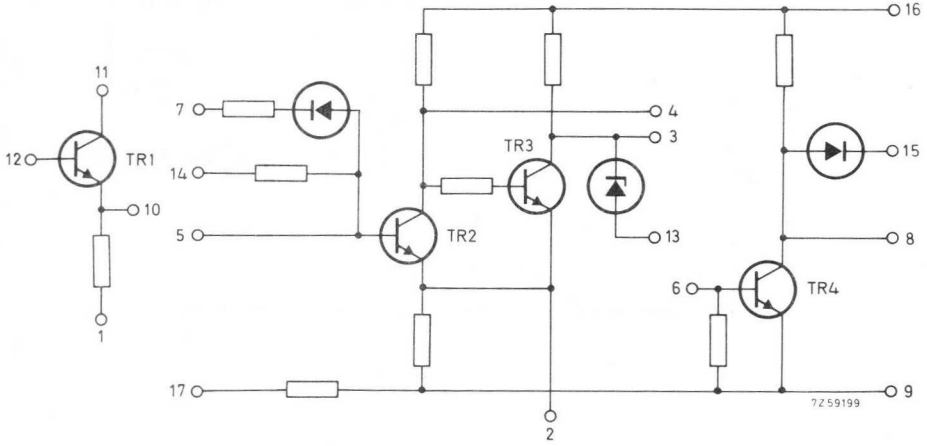


Terminal location

1 = emitter resistance follower
2 = emitter output Schmitt trigger
3 = output Schmitt trigger
4 = complementary output Schmitt trigger
5 = Schmitt trigger base input
6 = power stage base input
7 = oscillator feedback input
8 = power stage output
9 = 0 V common
10 = output emitter follower
11 = collector emitter follower
12 = base emitter follower
13 = restored "0" output Schmitt trigger
14 = input Schmitt trigger
15 = damping diode power stage
16 = supply voltage $+V_S$
17 = auxiliary resistor

Notes

1. For applications as a power amplifier with a min. permissible load resistance of 90 Ω, connect pin 13 to pin 6. A "1" at pin 14 will switch on the load between pins 8 and 16.
2. For applications as a power amplifier with a min. permissible load resistance of 48 Ω, connect pin 12 to 13, 17 and 1, connect pin 10 to 6 and pin 11 to 8. A "1" at pin 14 will switch on the load between pin 8 and 16.
3. The load should be connected between pins 8 and 16. To avoid destruction resulting from large voltage peaks occurring at switching off of inductive loads, the damping diode in the circuit block has to be connected across the load (15 to 16).
4. Incandescent lamps have a "cold" resistance that is only a fraction of the value calculated from nominal voltage and current, so that turning on of the lamp may cause a surge current. It is advisable to use a pre-heating quiescent current to eliminate destructive surge currents.



Circuit diagram

CHARACTERISTICS

Pins 6 and 13 connected, unless otherwise specified.

Supply	at V_S = +24 V ± 25%	at V_S = +12 V ± 5%
Supply current at I_{load} = 0 mA	≤ 25 mA	≤ 9 mA
Supply current at "1" input (pin 14) *) V_S = 30 V, R_{load} = 48 Ω	650 mA	

*) Connections as in Note 2 above.

Input	at V_S = +24 V ± 25%	at V_S = +12 V ± 5%
Drive at pin 14 for switching on load current	2 D.U.	2 D.U.
Input impedance at pin 14	92 kΩ	92 kΩ
Input voltage for switching on load current at pin 5 **)	≥ 8.2 V	≥ 4 V
at pin 14	≥ 11.4 V	≥ 5.3 V
Input voltage for switching off load current at pin 5 **)	≤ 1.6 V	≤ 1 V
at pin 14	≤ 1.8 V	≤ 1.2 V
On-off input voltage difference, R_{source} = 2200 Ω, at pin 5	≤ 4.8 V	≤ 2.0 V
at pin 14	≤ 4.9 V	≤ 2.1 V
Max. source resistance for pin 5	250 kΩ	
for pin 14	200 kΩ	
Output		
Min. load resistance - connections Note 1	90 Ω	
- connections Note 2	48 Ω	
Output voltage at "1" input at min. load resistance - connections Note 1	≤ 0.3 V	
- connections Note 2	≤ 1.3 V	

Switching speed.			
Switch off delay at 625 mA and 10 H with pin 15 connected to 16	t_d		480 ms
Fall time	t_f	≤	0.5 μs
Rise time	t_z	≤	10 μs

LIMITING VALUES

Supply voltage	V_S	max.	30 V
		min.	0 V
Positive transient on V_S, for 10 μs		max.	10 V
Input voltage at pin 14	$+V_{14}$	max.	70 V
	$-V_{14}$	min.	0 V
Input voltage at pin 5	$+V_5$	max.	30 V
via min. 2200 Ω	$-V_5$	min.	0 V
Output current for 20 ms		max.	5 A
for 20 ms each second		max.	2 A

*) Connections as in Note 2
**) Via min. 2200 Ω

DUAL TRIGGER TRANSFORMER

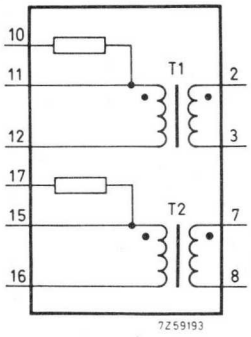
Function

Matching the pulse output from a power amplifier (e.g. UPA61) to thyristor gates.

Case

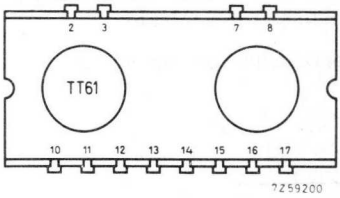
Size A; colour: black

CIRCUIT DATA



Circuit diagram

2. Secondary winding T_1 (cathode thyristor)
3. Secondary winding T_1 (gate thyristor)
7. Secondary winding T_2 (cathode thyristor)
8. Secondary winding T_2 (gate thyristor)
10. Resistance connected to primary winding T_1
11. Primary winding T_1 (driving source)
12. Primary winding T_1 ($+V_S$)
13. Not connected
14. Not connected
15. Primary winding T_2 (driving source)
16. Primary winding T_2 ($+V_S$)
17. Resistance connected to primary winding T_2



Terminal location

CHARACTERISTICS

Frequency range	3 to 12.5 kHz
Turns ratio primary: secondary	3 : 1
Inductance of primary winding	$\geq$ 2.2 mH
Leakage inductance referred to primary (secondary short-circuited)	$\leq$ 65 μH
Primary winding resistance at T_{amb} = 25 °C	$\leq$ 4 Ω
Primary series resistor	82 Ω
Secondary winding resistance at T_{amb} = 25 °C	$\leq$ 0.6 Ω
Output pulse in response to step input, circuit of Fig. A, R_{eq} = 15 Ω: rise time (from 0.3 to 3 V) pulse duration, V_{pulse} = 3 V [1])	 $\leq$ 0.6 μs $\geq$ 20 μs
Output current at pins 2/3 (7/8) at T_{amb} = 25 °C in response to step input at pins 10/12 (16/17) (see Fig. A);	
V_S = 18 V, V_{pulse} = 3 V [1]) R_{eq} = 15 Ω	$\leq$ 200 mA
V_{pulse} = 3.5 V [1]) R_{eq} = 22 Ω	$\leq$ 160 mA
V_S = 30 V, V_{pulse} = 4.25 V [1]) R_{eq} = 10 Ω	$\leq$ 425 mA
V_{pulse} = 5.0 V [1]) R_{eq} = 15 Ω	$\leq$ 335 mA

LIMITING VALUES

Primary switched voltage across pins 10/12 (17/16)	max. 30 V [2])
Primary switched current 82 Ω internal, duty cycle 1 : 3 max. 39 Ω external, duty cycle 1 : 2 max.	 max. 170 mA max. 200 mA
D.C. test voltage between any pair of windings for 1 minute	3 kV
Continuous working voltage	max. 500 V r.m.s.

---

[1]) V_{pulse} = Minimum mean pulse magnitude over 20 μs, over R_{eq}.

[2]) If the UJPA61 ceases to oscillate with the output transistor conducting, the primary series resistor may be damaged; circuit design must safeguard against this condition.

APPLICATION INFORMATION

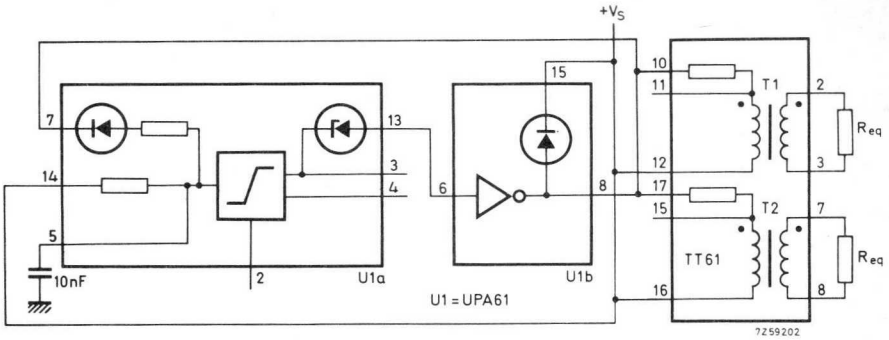


Fig.A. Relaxation oscillator circuit (10 kHz)

RECTIFIER AND SYNCHRONIZATION ASSEMBLY

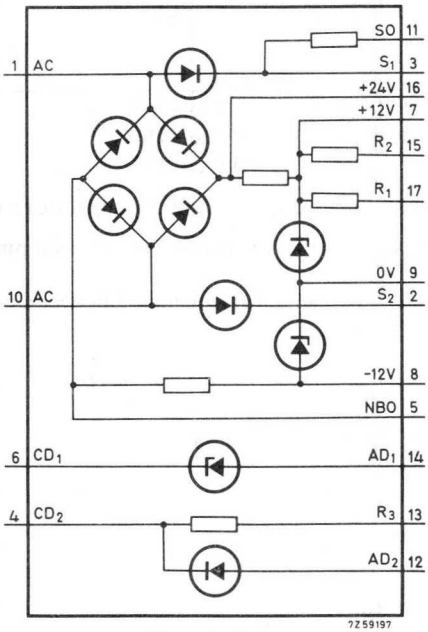
Function

- To provide an unregulated voltage of +24 V for Norbit systems
- To provide synchronization signals.
- To provide +12 V and −12 V (zener stabilized) for servo amplifiers.

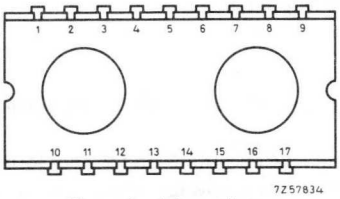
Case

Size: A; colour: black

CIRCUIT DATA



Circuit diagram



Terminal location

1 = A.C. input from supply transformer
2 = Synchronization voltage
3 = Synchronization voltage
4 = Cathode D_2
5 = Output rectifier bridge
6 = Cathode D_1
7 = +12 V output voltage
8 = −12 V output voltage
9 = 0 V from common supply
10 = A.C. input from supply transformer
11 = Synchronizing resistor output
12 = Anode D_2
13 = Resistor output cathode D_2
14 = Anode D_1
15 = +12 V, 150 kΩ source
16 = +24 V output voltage
17 = +12 V, 100 kΩ source

CHARACTERISTICS

Input

A.C. input voltage (r.m.s.)	2 x 20 V (+10, −15%)
A.C. input current	375 mA max.
Frequency	50 - 60 Hz
Source resistance	1 Ω min.
	4 Ω max.

Outputs

Pin number (9 connected to c.t. transformer)	Voltage	Current
16	+18 to +30 V	≤ 220 mA
7	+11 to +15 V	≤ 8 mA
8	−11 to −15 V	≤ 4 mA

In order to obtain the outputs specified, smoothing capacitors are required:

1. a 680 μF (−10, +50%), 40 V, capacitor connected between pins 16 and 9 to smooth the +24 V and +12 V.
2. a 100 μF (−10, +50%), 40 V, capacitor connected between pins 5 and 9 to smooth the −12 V.

Additional components

R : 2.2 kΩ; max. voltage 30 V r.m.s.

D_2 : max. reverse voltage 30 V;
max. forward current 200 mA

D_1 : nom. zener voltage 6.8 V;
max. dissipation 60 mW

LIMITING VALUES

Input voltage 2 x 22 V r.m.s.

APPLICATION INFORMATION

1. The output current of the −12 V output can be increased to 7 mA by connecting pin 4 to 5 and pin 8 to 13.
2. A mains synchronization signal is available at pin 11 when pins 3 and 2 are joined. The output at pins 2 and 3 takes the form of a zero voltage when the a.c. driving voltage passes through zero. At all other times a positive voltage is present on pins 2 and 3.

DUAL NOR-GATE WITH DIODE-RESISTOR NETWORKS

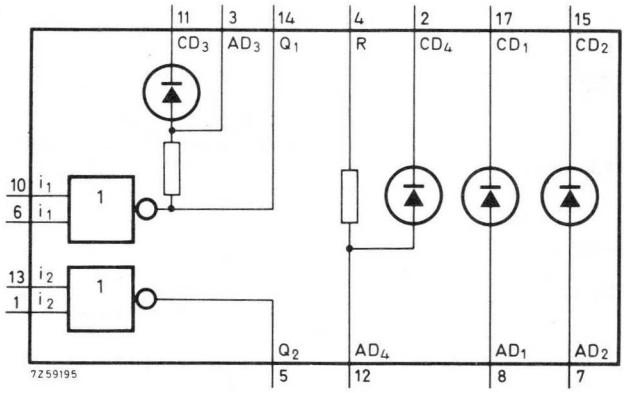
Function

Dual two-input transistor-resistor NOR-gate with diode gating facilities incorporated; specifically applicable as a d.c. counting/shifting stage.

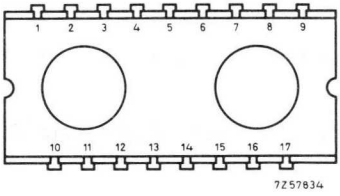
Case

Size: A; colour: black.

CIRCUIT DATA

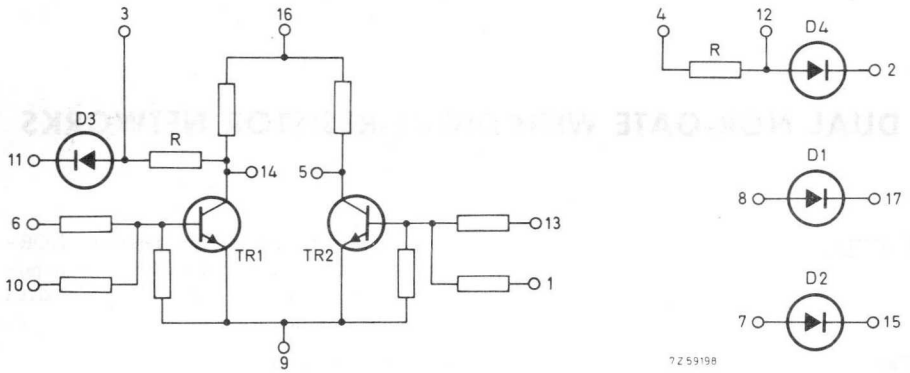


Quick reference circuit diagram



Terminal location

1 = Input NOR 2
2 = Cathode diode D_4
3 = Anode diode D_3
4 = Gate resistor
5 = Output NOR 2
6 = Input NOR 1
7 = Anode diode D_2
8 = Anode diode D_1
9 = 0 V common supply
10 = Input NOR 1
11 = Cathode diode D_3
12 = Anode diode D_4
13 = Input NOR 2
14 = Output NOR 1
15 = Cathode diode D_2
16 = $+V_s$ supply for NOR 1 and NOR 2
17 = Cathode diode D_1



Circuit diagram

CHARACTERISTICS

	at V_S = 24 V ±25%	at V_S = 12 V ±5%
Supply current at V_S nom	5.6 mA	2.8 mA
at V_S max	7.2 mA	3.1 mA
Input requirement	2 D.U.	2 D.U.
Output capability	10 D.U.	6 D.U.

	pins 6, 13	pins 10, 1	pins 6, 10 and 13, 1 in parallel
Input impedance [1]	63 kΩ	47 kΩ	32 kΩ
Input current for "0" output [1] [2]	92 μA	86 μA	75 μA

Switching speed

Fall time	$t_f \leq 1.5$ μs
Fall time	$t_{fd} \leq 6$ μs

Diode-resistor networks

Resistors R (22 kΩ) can be used as a load of 4 D.U. in a logic Norbit system.

[1]) Not used inputs returned to 0-volt line .
[2]) At V_S = 30 V

LIMITING VALUES

Supply voltage V_S	max.	+30	V
	min.	0	V
Positive transient on V_S	max.	10	V for 10 μs
Positive input voltage $+V_i$	max.	70	V
Negative input voltage $-V_i$	max.	15	V
Reverse voltage of diodes	max.	50	V
Forward current of diodes	max.	75	mA
Repetitive peak forward current of diodes	max.	150	mA
Dissipation of resistor R	max.	50	mW

DIFFERENTIAL AMPLIFIER

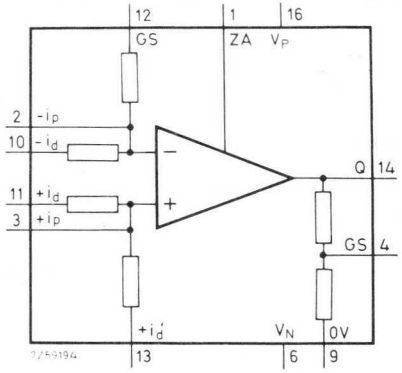
Function

Amplification, loop shaping and comparison with reference signals in analogue closed-loop systems. Many other applications are possible with the operational amplifier incorporated.

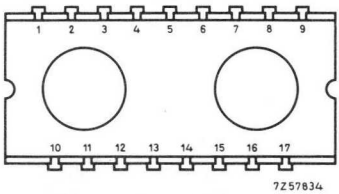
Case:

Size: A; colour: blue

CIRCUIT DATA



Quick reference circuit diagram



Terminal location

1 = zero output voltage adjustment
2 = inverting input operational amplifier
3 = non-inverting input operational amplifier
4 = gain selection (100 x)
5 = n.c.
6 = negative supply voltage V_N
7 = n.c.
8 = n.c.
9 = 0 V common
10 = inverting input difference amplifier
11 = non-inverting input difference amplifier
12 = gain selection (10 x)
13 = 100 kΩ non-inverting input operational amplifier
14 = output and gain selection
15 = n.c.
16 = positive supply voltage V_p
17 = n.c.

CHARACTERISTICS

Ambient temperature range

Operating	0 to +70 °C
Storage	−40 to +85 °C

Power Supply

Supply voltages	V_P = +12 V V_N = −12 V	V_P = +15 V V_N = −15 V
Supply currents for I load = 0 mA	I_P = 2.2 mA I_N = 2.2 mA	I_P = 2.7 mA I_N = 2.7 mA

The circuit has been protected against reverse connection of supply voltages.

Voltage gain

With feedback, from input (pin 10) to output (pin 14)		
a. pin 12 connected to pin 14	10 x	
b. pin 12 connected to pin 4	100 x	
Without feedback, from input (between pins 2 and 3) to output (pin 14) - typical	32 000	45 000

Frequency response

The operational amplifier has a frequency response of 6 dB/oct, with unity gain bandwidth (for small signals)	1 MHz
3 dB down frequency for gains of 10 and 100 (at rated output voltage swing)	10 kHz

Rejection ratio

Connected as a difference amplifier with gain of 10 (inputs pin 10 and 11)	
- of supply voltage variations	to be established
- of common mode signals	to be established

Input

Minimum input voltage range, when connected as a difference amplifier with a gain of 10 (input pins 10 and 11)	± 13 V	± 17 V

Circuit has been protected against too high voltages between the inputs of the operational amplifier.

Input resistance	
-inverting input (pin 10)	10 kΩ
-non-inverting input (pin 11)	110 kΩ

Input voltage offset

Initial offset can be adjusted to zero with a potentiometer of 100 kΩ connected between 0 V line and positive supply voltage and the wiper connected to pin 1.

Equivalent input voltage offset drift with temperature (typ.)	10 μV/degC

Output

Minimum output voltage swing		
at R_L = 10 kΩ	± 9 V	± 11 V
at R_L = 2 kΩ	± 7 V	± 9 V
Output current	≥ 5 mA	≥ 6 mA

Output resistance	
for a gain of 10	≤ 0.3 Ω
for a gain of 100	≤ 3 Ω
Maximum capacitive load	1 nF
Slewing rate (change of output voltage in response to step input voltage)	to be established

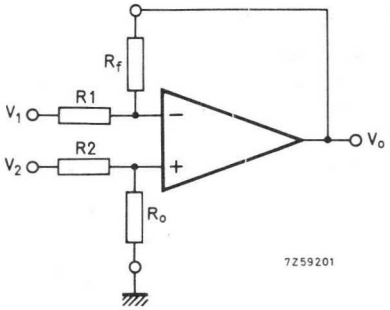
The output may be shorted to earth for any length of time.

APPLICATION INFORMATION

As shown, the DOA61 consists of an operational amplifier and feedback networks for closed loop gains of 10 and 100 times. Other gains can be obtained by applying one or more external resistors.

According to operational amplifier theory the transfer function of an amplifier with feedback networks as shown in the circuit diagram is given by

$$V_o = V_2 \frac{R_o}{R_1} \cdot \frac{R_1 + R_f}{R_o + R_2} - V_1 \frac{R_f}{R_1}$$ (See circuit below)

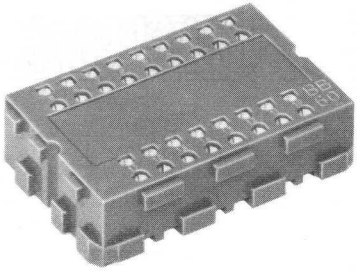


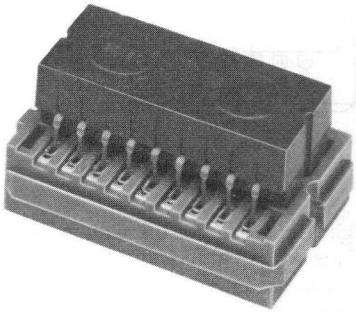
For $\frac{R_o}{R_2} = \frac{R_f}{R_1}$ the function can be simplified to: $V_o = \frac{R_f}{R_1} (V_2 - V_1)$

Networks incorporated into the circuit block are providing a difference amplifier, with a gain of 10 x.

ACCESSORIES FOR NORBITS

BREADBOARD BLOCK
for 60-series NORBITS



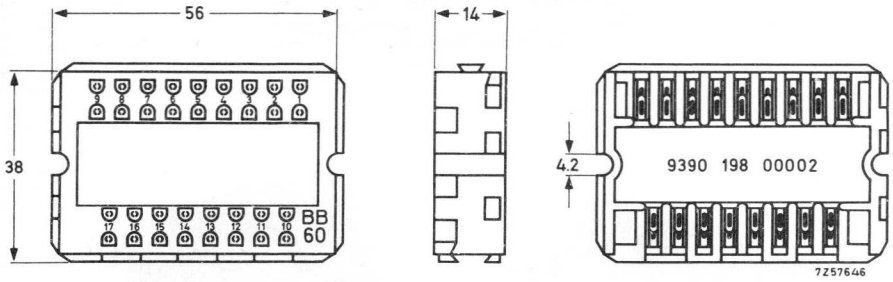


RZ 27447-18

APPLICATION

The "Breadboard Block", BB60, has been produced as an aid to 60-Series logic system design. Each block takes one size A unit from the 60-Series, and each block can be firmly locked on any of its edges to another BB60 block, thus a breadboard base can be built up to accommodate any size and complexity of logic circuit, interconnections being simply made with hook-up wire plugged into cup-shaped contacts. The BB60 blocks are ideal as experimenting and teaching aids. For instance, with four units 4. NOR60, one unit TU60 and one unit 2. LPA60 mounted on a base of six blocks BB60, it is easy to realize a large number of instructive logic circuits. Such a base of six blocks can be mounted in the Universal Mounting Chassis UMC60.

DESCRIPTION



(Dimensions in mm)

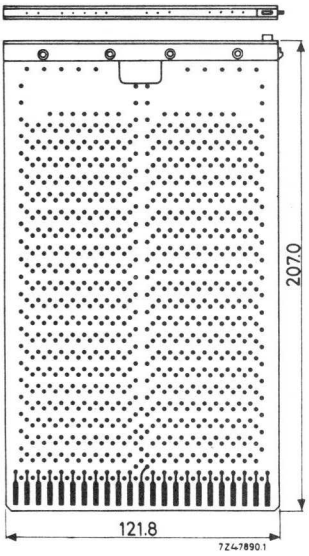
The right figure shows the underneath of the block with the 2 x 17 soldering lugs; the 60-Series units can be soldered directly onto these lugs. In the top view the cup-shaped contacts are visible; interconnecting wires or discrete components such as resistors can be plugged in on this side. There are two contacts for each terminal of a 60-Series unit, which facilitates multiple connections.

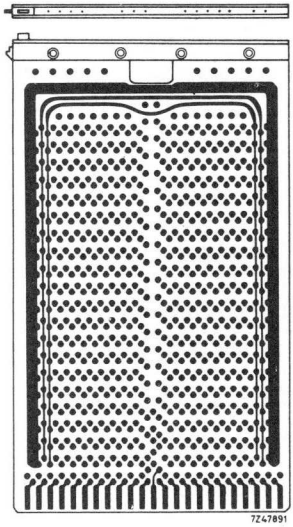
Body material	rigid grey plastic
Contacts	cup shaped, silver plated, suited for wires up to 1 mm diameter
Weight	20 g
Delivery	in packs of six, plus six sheets of wiring lay-out stickers for the 60-Series units.

The stickers are drawing symbols on self-adhesive transparent material, and they can be stuck to the top side of the breadboard blocks or be used for circuit drawings. The catalogue No. of a sheet is 9399 269 15301.

EXPERIMENTERS' PRINTED-WIRING BOARD

Experimenters' printed-wiring board (with extractor) with plated-through holes suitable for 60-series NORBITS. It fits mounting chassis 4322 026 38240.





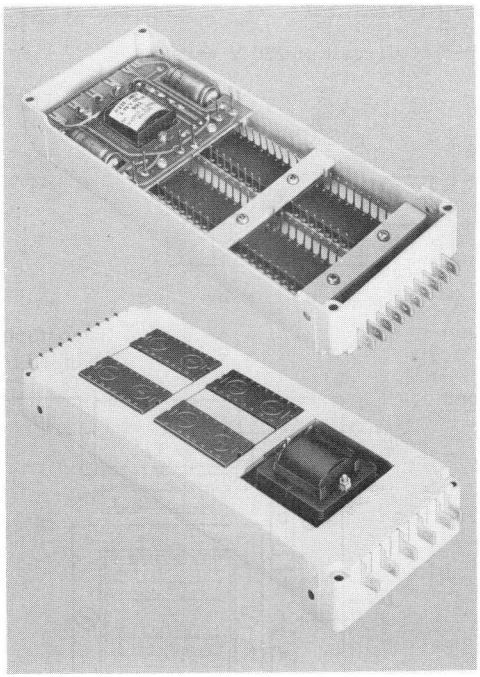
Accommodation of NORBITS

size A + size B (PA 60)	
10	0
8	1
6	2
3	3
0	4

Material of version GPB 60	glass-epoxy
of version GPB 60/P	phenol paper
Hole diameter	1.2 mm
Contacts	2x23, gold plated, pitch 0.2"
Mating connector	2422 020 52591 (type F045)

For more information, see Application Note "Printed-wiring boards for 60-series Norbit Assemblies", No. 32/522/BE.

LOGIC SUPPLY UNIT



RZ 27077-11
RZ 27077-8

LSU60 mounted in UMC60

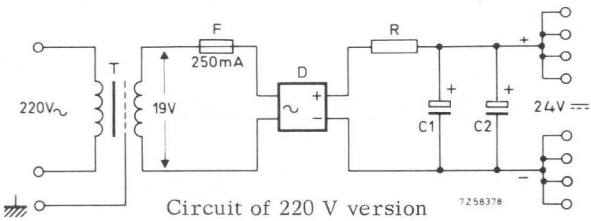
APPLICATION

The LSU60 is a power supply unit for small systems with 60-series Norbits. It is intended to be mounted in the universal mounting chassis UMC60. There is a version for 220 V mains (4332 000 01000) and one for 110 V mains (4332 000 01010).

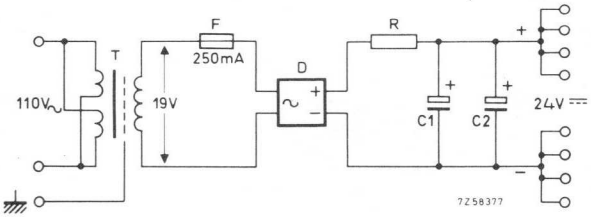
DESCRIPTION

The unit takes the same place as a size B Norbit block (PA60). To mount the unit in the UMC60, the material between the two adjacent size A holes in the chassis should be removed, after which the unit can be fixed with 4 self-tapping screws.
Slots in the board of the LSU60 facilitate the connection of the input voltage and the output voltage to the Fastons of the UMC60, for external connection to the chassis. The other three pairs of output terminals are soldering tags intended for connection to Norbit blocks on the chassis. A 250 mA fuse (F) is inserted in the secondary part of the circuit. Its catalogue number is 4822 253 20011.

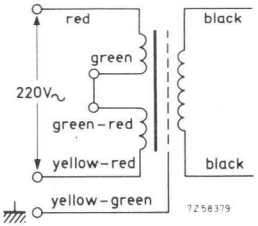
Circuit



Circuit of 220 V version



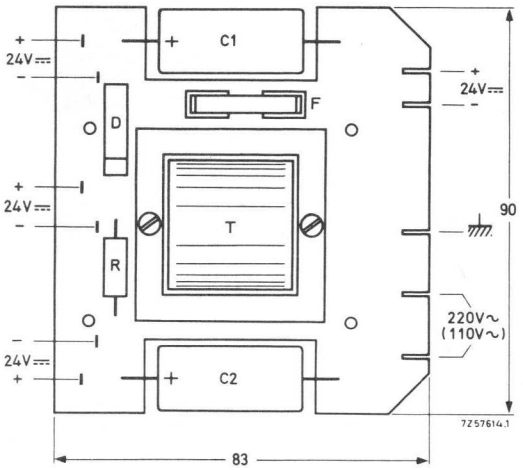
Circuit of 110 V version



Transformer of 110 V version changed for 220 V.

Outline and connections

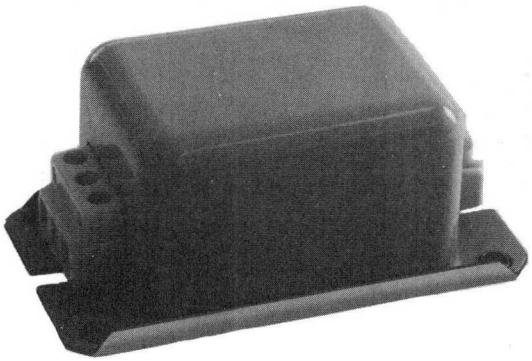
Dimensions in mm



ELECTRICAL DATA

Input voltage	
version 4332 000 01000	220 V a.c., +10%, −15%
version 4332 000 01010	110 V a.c., +10%, −15%
Input frequency	45 to 400 Hz
Output voltage at 0 mA	< 30 V d.c.
at 150 mA	> 18 V d.c.
Temperature range	−10 to +70 °C
Test voltage for 1 min,	
across input terminals and earth	2 kV r.m.s.
across output terminals and earth	2 kV r.m.s.

0.5 A MAINS FILTER



RZ 22748-2

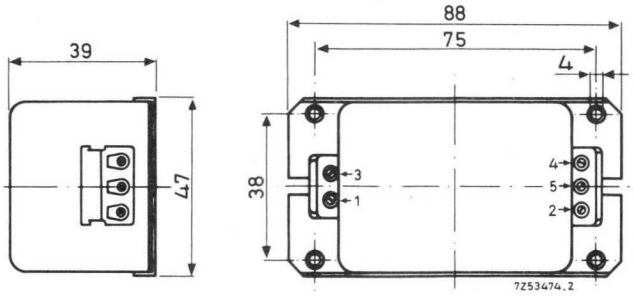
APPLICATION

This mains filter is intended for use between mains supply connection terminals and the mains inputs of control systems consuming less than 0.5 Amp. to provide an attenuation of minimum 50 dB for frequencies between 100 kHz and 10 MHz.

CONSTRUCTION

Unit is potted in a metal housing.

Dimensions in mm

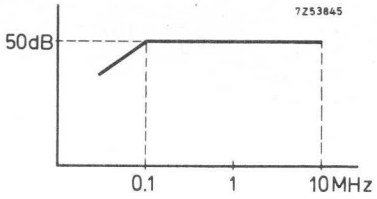


Weight: 280 g

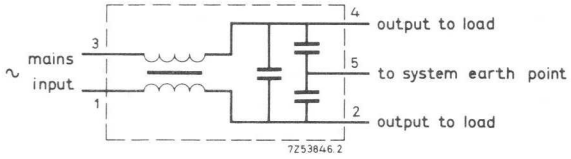
TECHNICAL PERFORMANCE

Attenuation	≥ 50 dB
Maximum a.c. input voltage	250 V
Maximum a.c. input current	0.5 A
Test voltage for 1 min	
a) across input terminals	2 kV
b) across input terminal and case	2 kV
Operating temperature range	−25 to +70 °C
Storage temperature range	−40 to +85 °C

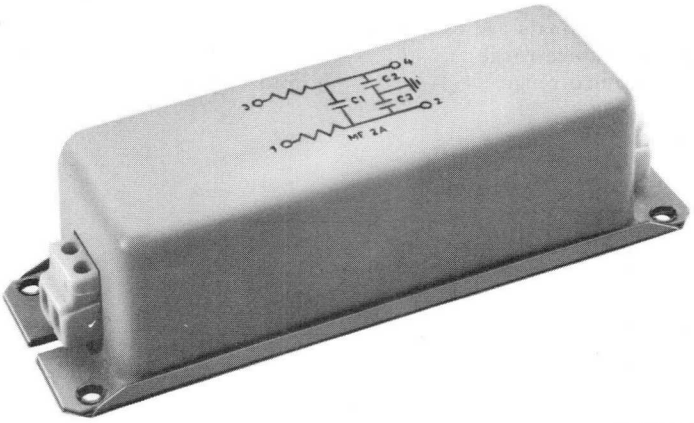
Minimum attenuation



Circuit diagram



2A MAINS FILTER



RZ 27208-8

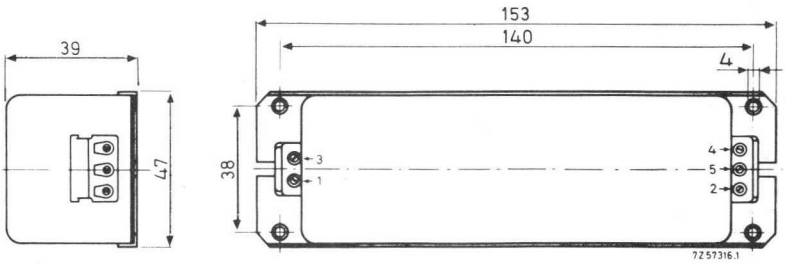
APPLICATION

This mains filter is intended for use between mains supply connection terminals and the mains inputs of control systems consuming less than 2 A to provide an attenua- of minimum 50 dB for frequencies between 300 kHz and 15 MHz.

CONSTRUCTION

Unit is potted in a metal housing.

Dimensions in mm

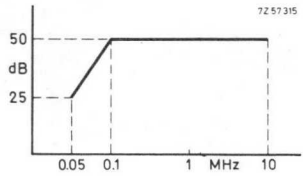


Weight: 570 g

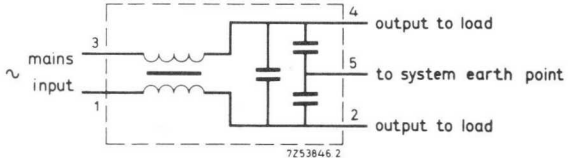
TECHNICAL PERFORMANCE

Attenuation	≥ 50 dB
Maximum a.c. input voltage	250 V
Maximum a.c. input current	2 A
Test voltage for 1 min	
a) across input terminals	2 kV
b) across input terminals and case	2 kV
Operating temperature range	−25 to +70 °C
Storage temperature range	−25 to +85 °C

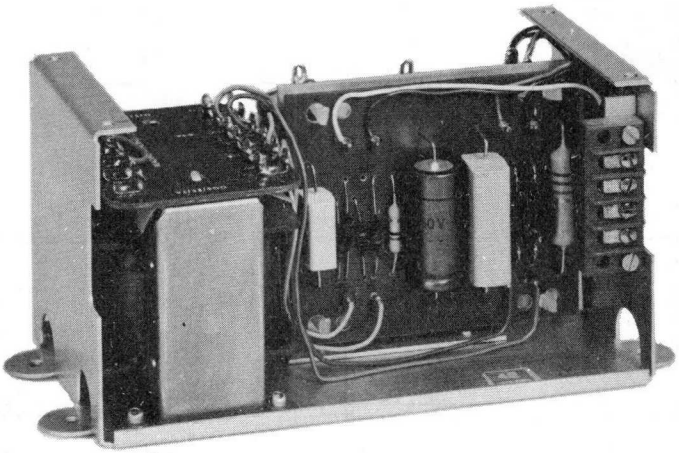
Minimum attenuation



Circuit diagram

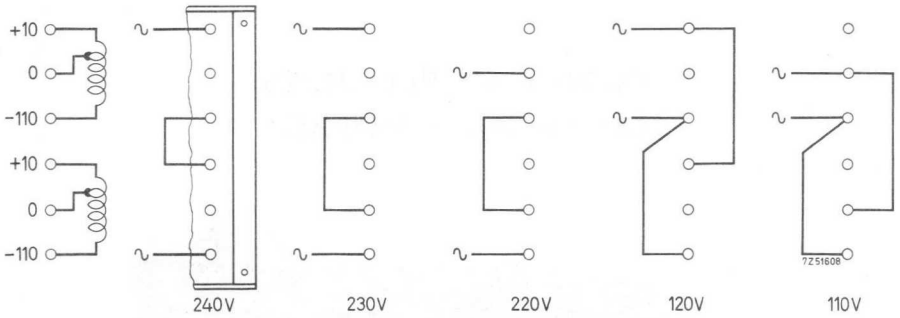


POWER SUPPLY UNITS
for 60-series NORBITS

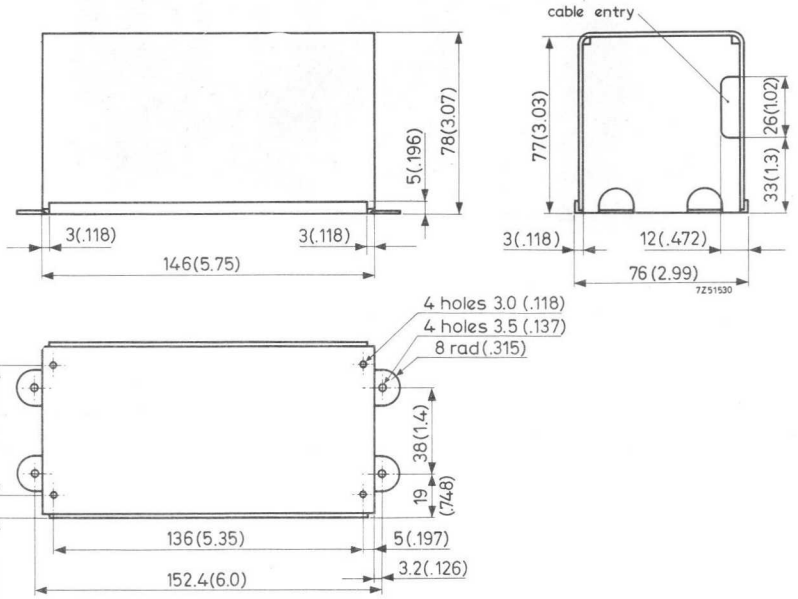


(Cap removed from unit.) RZ 23469-1

Input voltage	240, 230, 220, 120 or 100 V_{ac}, +10%, -15%
Input frequency	47 to 440 Hz
Output	< 30 V at 0 mA, > 18 V at 500 mA (for logic supply)
Additional output PSU 61	+100 V ±25% at 0 to 25 mA (for Switch Filters)
Operating ambient temperature	-10 to +60 °C



Input facilities of mains transformer

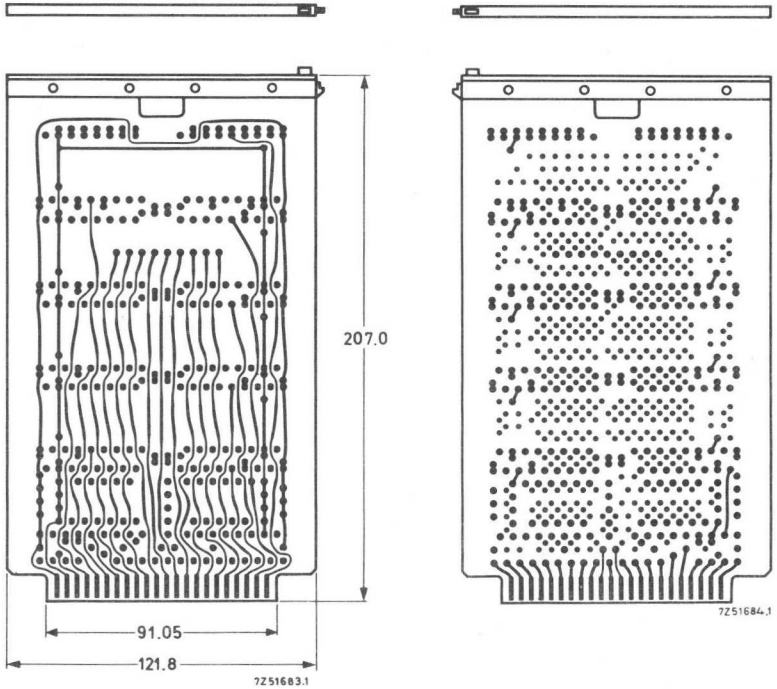


Dimensions in mm, inch values between brackets.

Case: aluminium

EXPERIMENTERS' PRINTED-WIRING BOARDS for 60-series NORBITS

Experimenters' printed-wiring boards (with extractor) with plated-through holes, and 0-volt supply line tracks for pins 9 and 16. They fit mounting chassis 4322 026 38230.

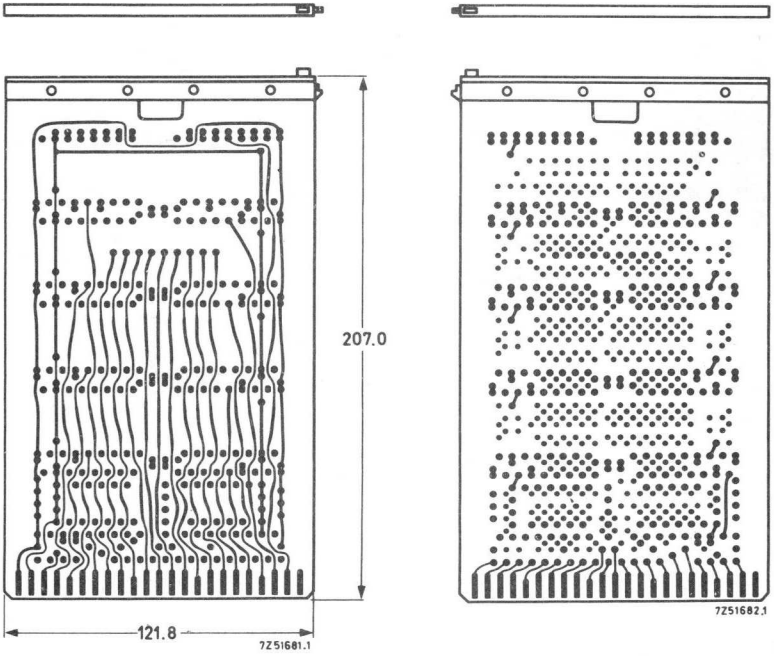


Accommodation	ten blocks size A
Material of version 4322 026 38790 of version 4322 026 38800	glass-epoxy (PWB 60) phenol paper (PWB 60/P)
Hole diameter	1.3 mm
Contacts	2x22, gold plated, pitch 0.156"
Mating connector	types F047, F050, F053

For more information, see Application Note "Printed-wiring boards for 60-series Norbit Assemblies", No. 32/522/BE.

EXPERIMENTERS' PRINTED-WIRING BOARDS
for 60-series NORBITS

Experimenters' printed-wiring boards (with extractor) with plated-through holes, and 0-volt supply line tracks for pins 9 and 16. They fit mounting chassis 4322 026 38240.

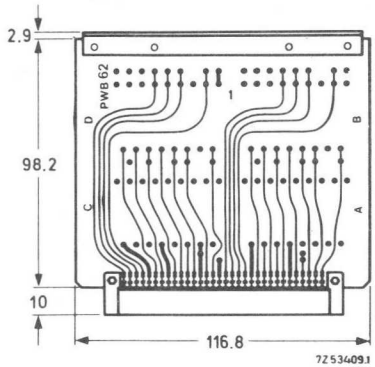


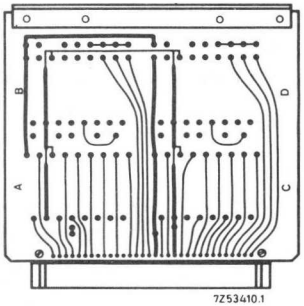
Accommodation	ten blocks size A
Material of version 4322 026 38810 of version 4322 026 38820	glass-epoxy (PWB 61) phenol paper (PWB 61/P)
Hole diameter	1.3 mm
Contacts	2x23, gold plated, pitch 0.2"
Mating connector	2422 020 52591 (type F045)

For more information, see Application Note "Printed-wiring boards for 60-series Norbit Assemblies", No. 32/522/BE.

PRINTED–WIRING BOARD
for 60–series NORBITS

Printed-wiring board with plated-through holes, extractor and complete F054 connector, of which the female part has been soldered to the board. All terminals of any Norbit mounted on the board are brought out. The 0-volt pins and the positive supply pins have been tracked together for all Norbits.
The board fits the miniature mounting chassis 4322 026 38250.
The board is especially useful for systems where a small number of types (board + blocks) is essential with a view to replacement.





Accommodation	size A + size B (PA60)
	4 | 0
	2 | 1
	0 | 2
Material	glass-epoxy
Hole diameter	1.2 mm
Connector	
type	F054 (2422 025 89082)
contacts	2 x 32
contact pitch	2.54 mm (0.1")
terminations	suitable for mini wire-wrapping

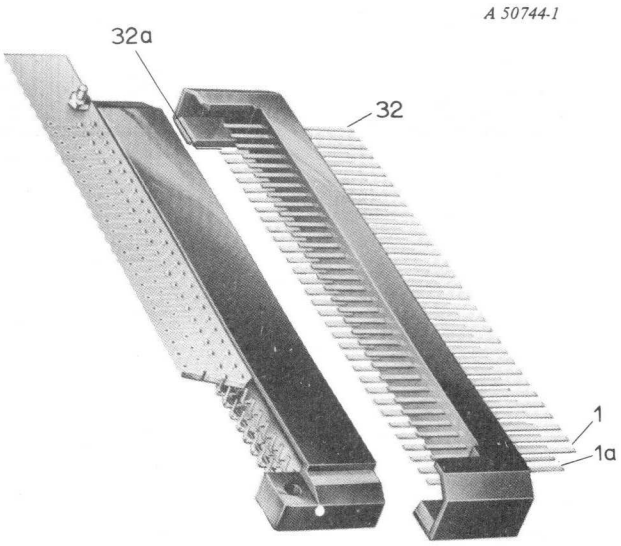
INTERCONNECTION DIAGRAM

The designer of an electronic circuit with Norbits mounted on PWB62 boards, can easily derive the necessary connecting instructions from the diagram depicted on the next page. With this diagram he can indicate the connections that are to be made. The diagram gives the numbers of the terminals of the circuit block, its position on the PWB62 and the numbers of the connector terminals (see photograph below).
The thin lines in the diagram represent the tracks of the printed circuit on the PWB62, so they indicate the interconnections between the Norbit terminals, and the connector pins.

All the designer has to do is to draw the connections which should be made by the wire man (see thick lines on the second diagram).

As an example we give an alarm circuit of which the designer has drawn the diagram in the upper part, and has indicated for the wire man on the lower part the external interconnections to be made. Moreover, outside the diagram the necessary connections to be made the supply with unit, the oscillator, switches, and so on, are indicated by the arrows.

In this way the design engineer can draw the electronic circuit and the associated assembly instructions in one diagram.

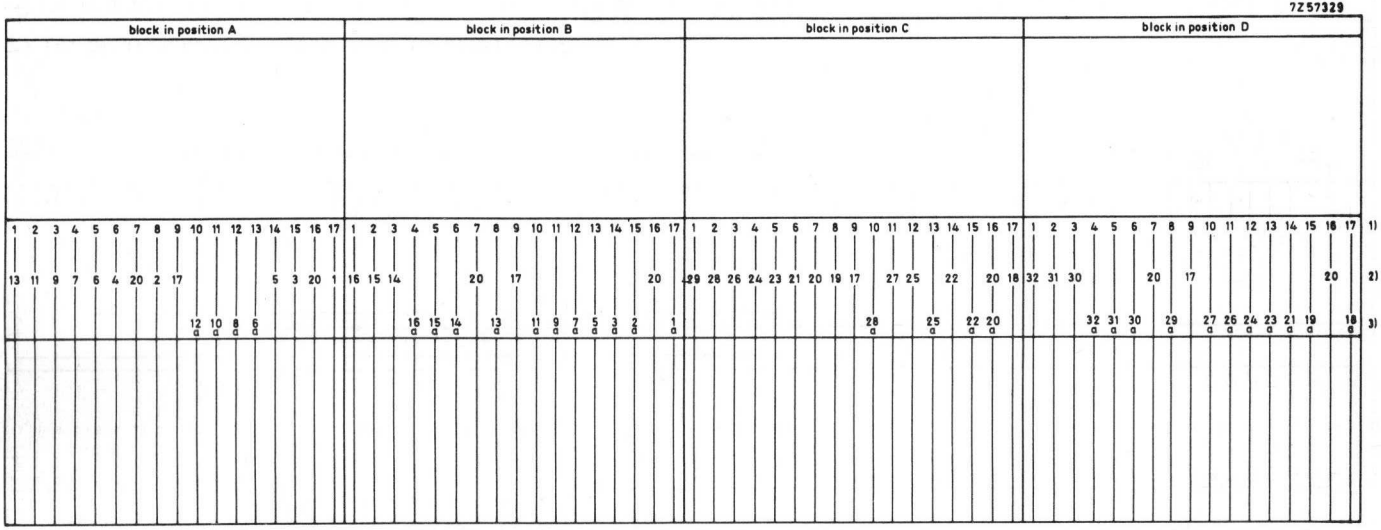


Connector pin numbering as used in Interconnection Diagram.

Interconnection diagram (containing track data)

See example next page.

7Z57329

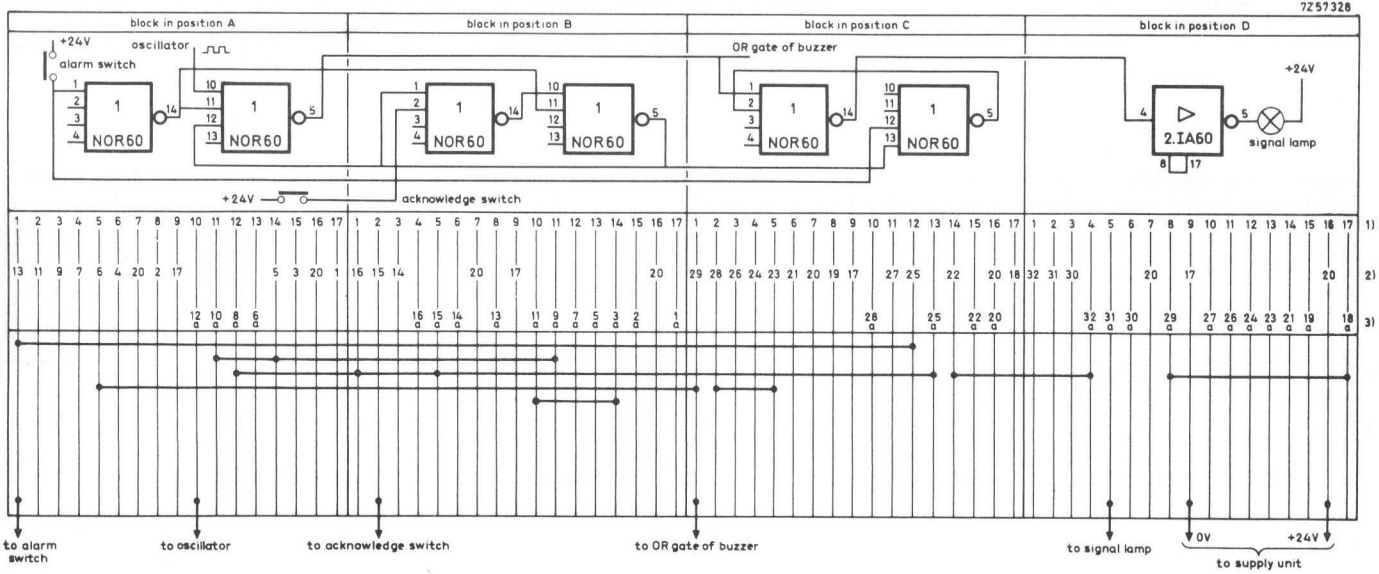


1) Terminal number of circuit block inserted in PWB62

2) Pin number of male F054 connector (see photograph) to which track on the "solder side" (bearing no type number) is connected.

3) Pin number of male F054 connector (see photograph) to which track on the "components side" (bearing type number) is connected.

Example

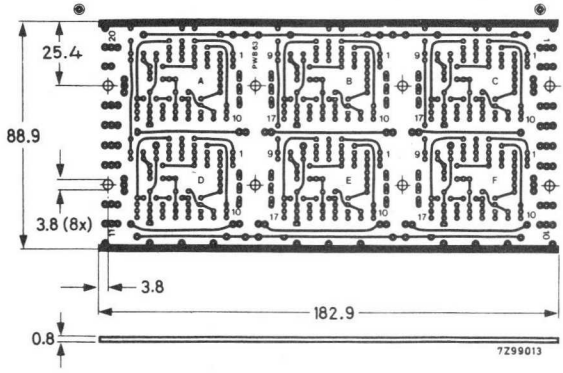


1) Terminal number of circuit block inserted in PWB62

2) Pin number of male F054 connector (se photograph) to which track on the "solder side" (bearing no type number) is connected

3) Pin number of male F054 connector (see photograph) to which track on the "components side" (bearing type number) is connected.

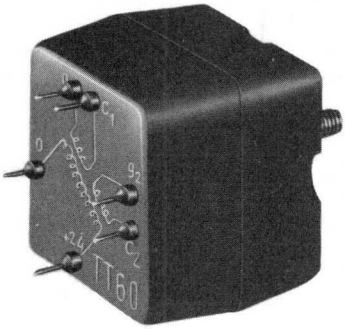
PRINTED-WIRING BOARD for UMC60



Single-sided printed-wiring board (with holes) intended for use in a Universal Mounting Chassis UMC 60.
Tracks have been laid such that only short jumpers need be used to obtain all kinds of logic functions with Norbits.

Accommodation (60-series blocks)	6 size A or 4 size A + 1 size B (PA60) or 2 size A + 2 size B or 3 size B
Material	glass-epoxy
Board thickness	0.8 mm
Hole diameter	1.2 mm

THYRISTOR TRIGGER TRANSFORMER



A 51993

APPLICATION

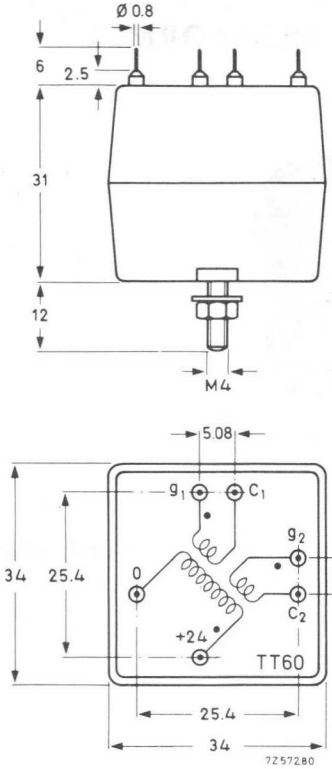
The TT60 can produce, in conjunction with the power amplifier PA60, two pulse currents of up to 400 mA. This is sufficient gate current to trigger a pair of practically any type of thyristor.

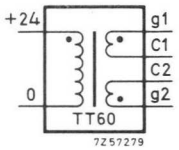
DESCRIPTION

The transformer has been encapsulated in a mould.
A threaded stud permits the unit to be fixed to a support (This may be the thyristor heat sink, to obtain short gate and cathode leads).

For the hand soldering of wires to the pins 7 wire spirals, catal.No. 4022 220 64781, are packed with the transformer.

Dimensions in mm





Drawing symbol

Weight: 80 g approx.

TECHNICAL PERFORMANCE

Turns ratio primary : sec_1 : sec_2	3 : 1 : 1
Inductance of primary winding	≥ 6 mH
Leakage inductance referred to primary (both secondaries short-circuited)	≤ 18 μH
Primary winding resistance at T_{amb} = 25 °C	≤ 0.5 Ω
Secondary winding resistance at T_{amb} = 25 °C	≤ 0.1 Ω
Test voltage between the windings for 1 minute	5 kV

Output pulse in response to step input, circuit of Fig.A, R_{eq} = 13 Ω:

rise time	≤ 0,75 μs
pulse duration	≥ 20 μs
Operating ambient temperature	−10 to +85 °C
Storage temperature	−40 to +85 °C

APPLICATION INFORMATION

Pulse amplifier circuit

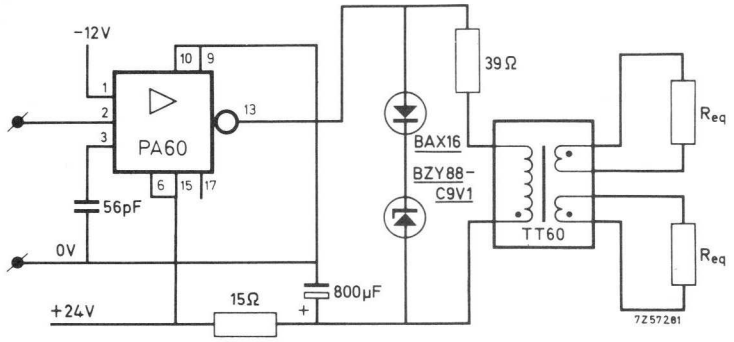


Fig.A

Note that terminal 2 of the PA60 is used for the pulse input.

Relaxation oscillator circuit

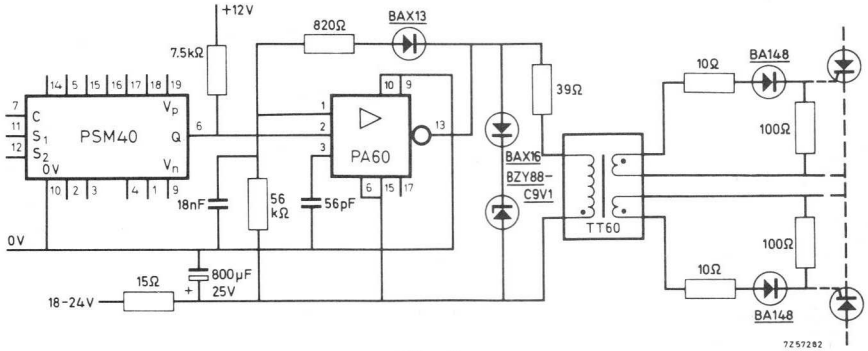
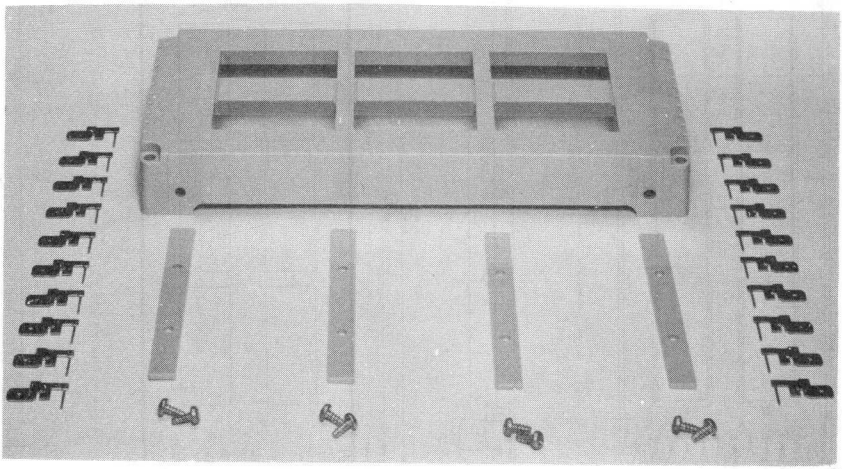


Fig.B

Fig.B shows the PA60 as a 10 kHz oscillator controlled by phase shift module PSM40. Oscillation commences with the level "high" (+12 V) on terminal 2 of the PA60, ceasing when it becomes "low" (0 V).

UNIVERSAL MOUNTING CHASSIS

for 60-series NORBITS



RZ 26441-7

APPLICATION

Low cost mounting facility for:

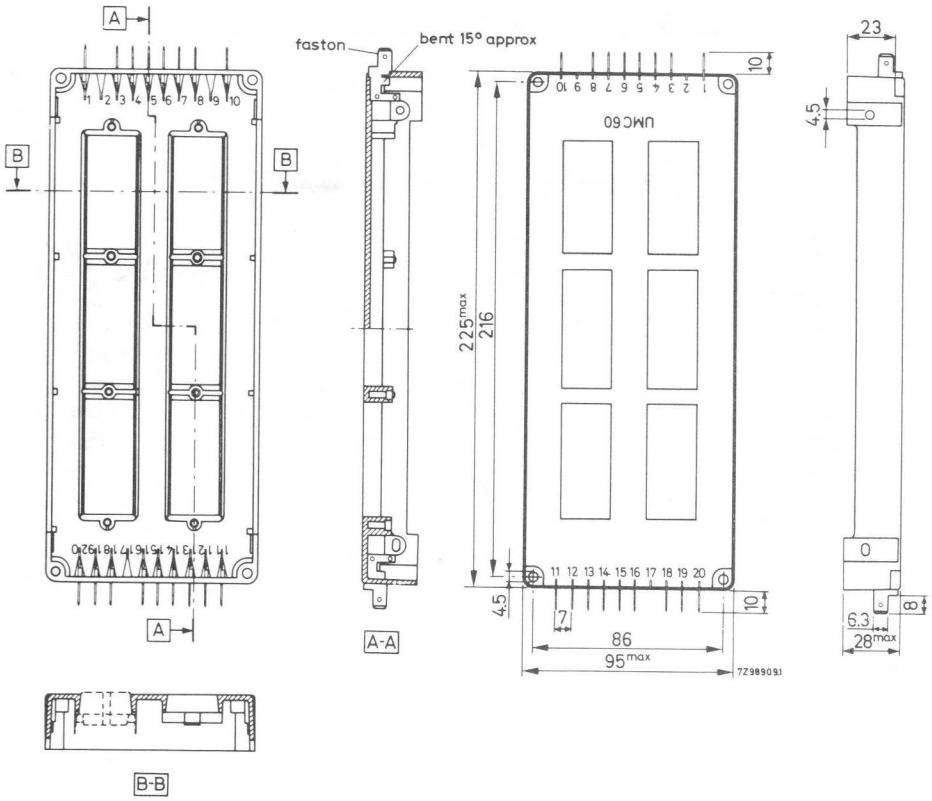
6 size A blocks,
or 4 size A blocks and 1 size B block (PA 60)
or 2 size A blocks and 2 size B blocks
or 3 size B blocks.

The chassis provides an alternative for mounting 60-series blocks on a printed-wiring board with connector.
Chassis can be bolted together side by side (Fig.4); they may also be stacked (Fig.5 and Fig.6) or hinged.

DESCRIPTION

The delivery includes a moulded polycarbonate chassis body, 4 moulded polycarbonate strips, 8 self-tapping screws and 20 standard 0.25 inch Fastons. Strips and screws are for clamping the circuit blocks into the holes in the chassis. The Fastons are for connections to the circuitry in the chassis.

To accommodate a size B block, it is necessary to remove the material between two size A holes, see Fig.1.
Interconnections between the terminal pins of the circuit blocks can be made by means of hand soldering or mini wire-wrapping; it is also feasible to use printed-wiring board PWB63 (catal. No. 4322 026 73750) in the chassis (see Fig.3).



Colour: grey

Dimensions in mm

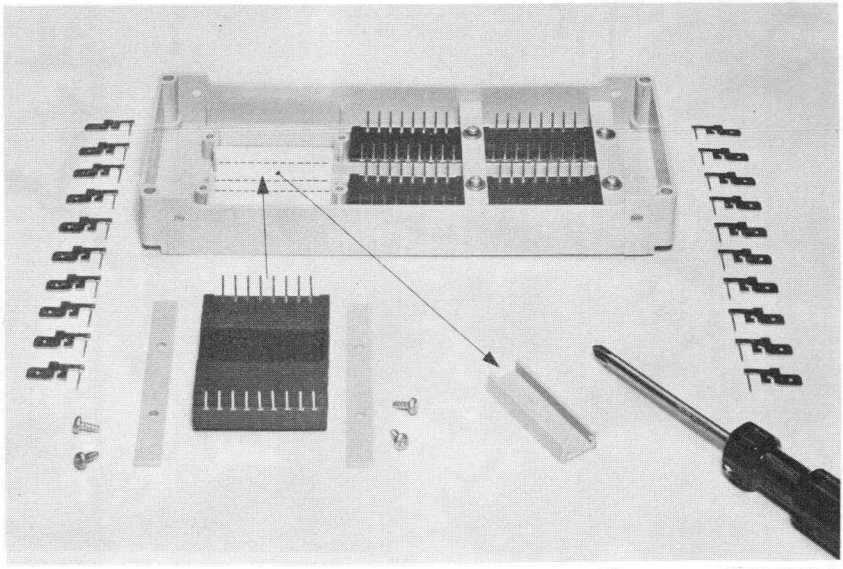
Weight: 150 g approx.

ASSEMBLY AND USE

The Fastons are brought in from the outside of a chassis and then fixed by bending the slotted part on the inside over about 15°

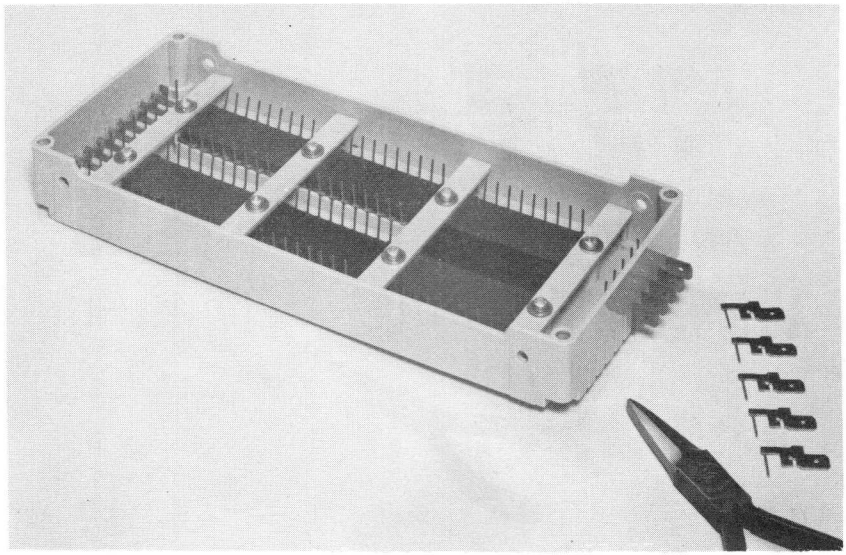
The blocks are clamped into the chassis with the strips and the self-tapping screws.

For fixing two or more chassis together, 4 mm bolts and nuts may be used.



RZ 26441-6

Fig.1



RZ 26441-3

Fig.2

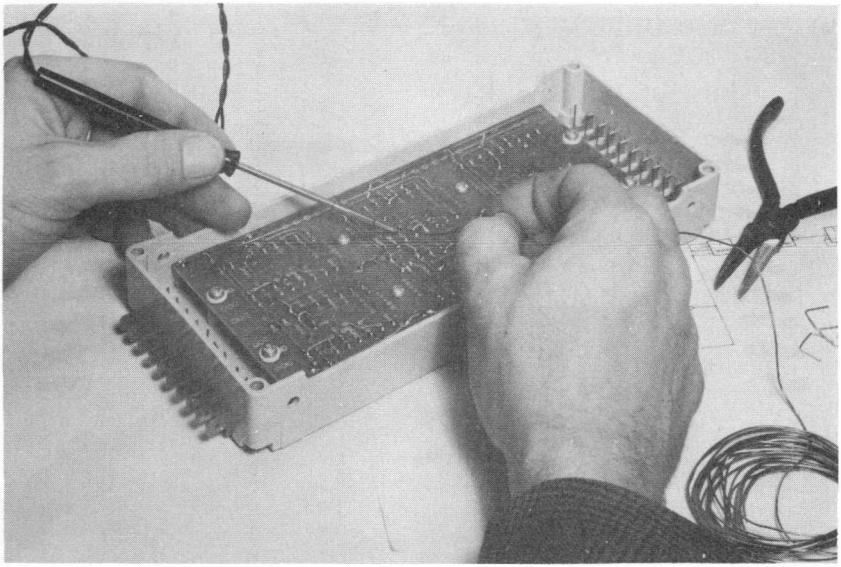


Fig.3 *RZ 26441-8*

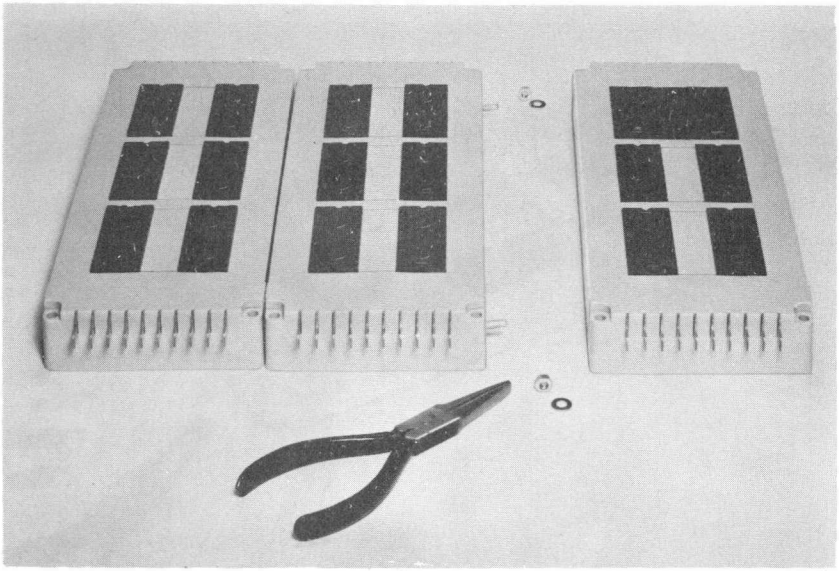


Fig.4 *RZ 26441-4*

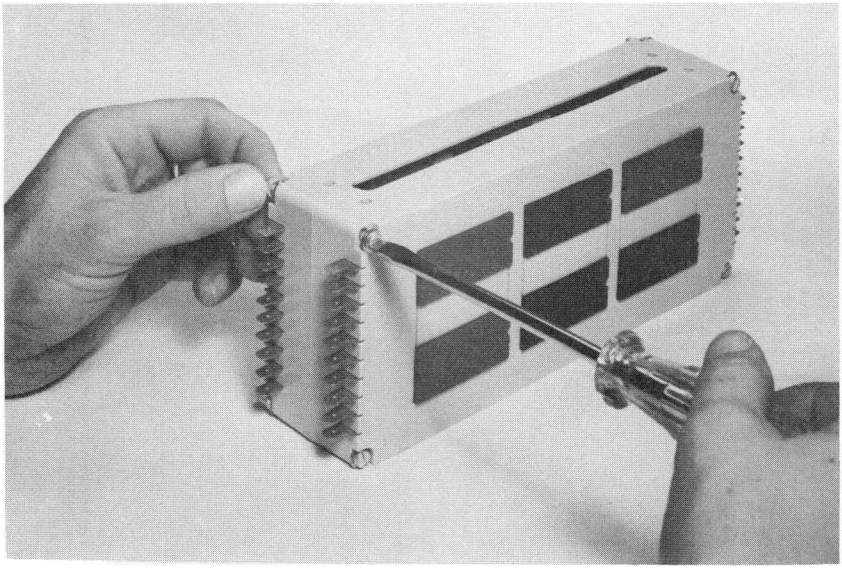


Fig.5 RZ 26441-9

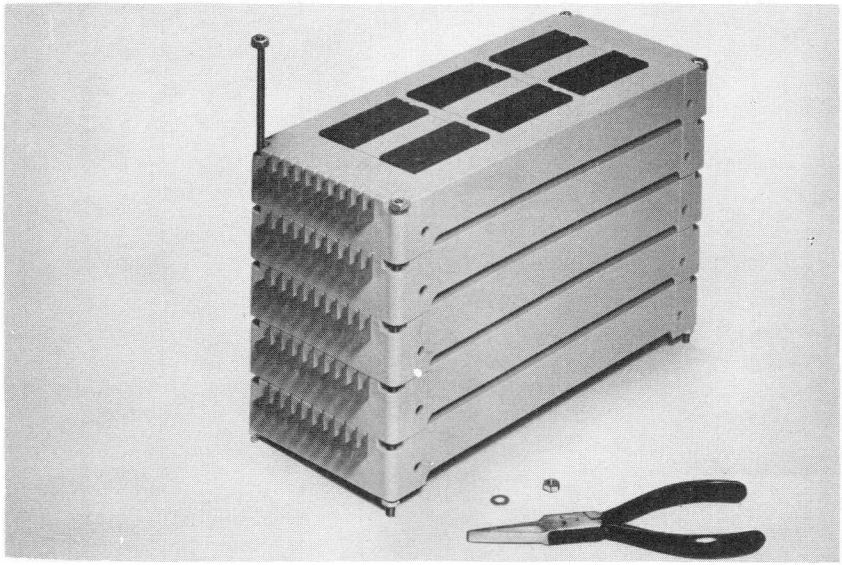
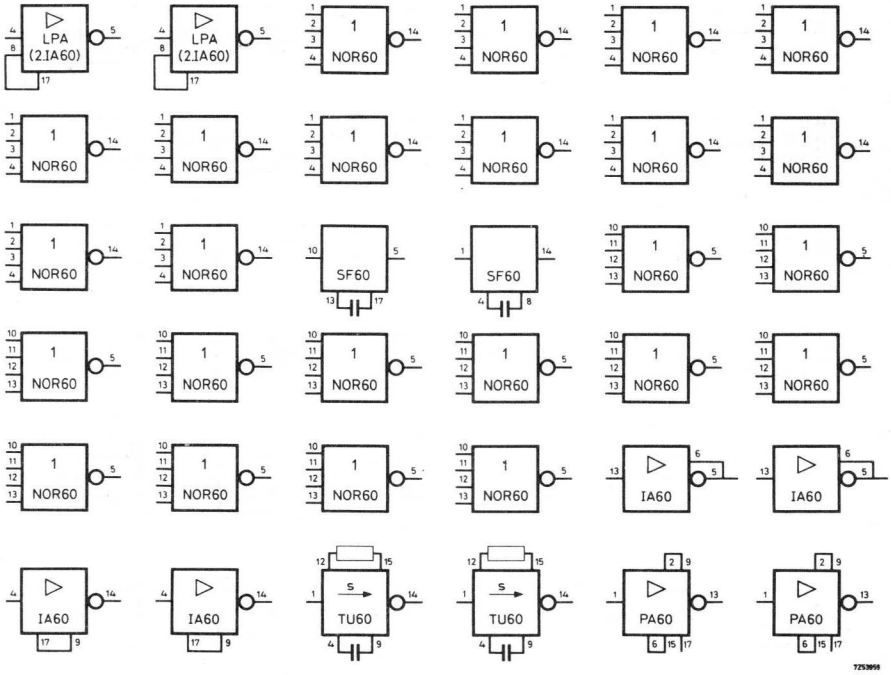


Fig.6 RZ 26441-10

STICKERS FOR THE 60-SERIES NORBITS

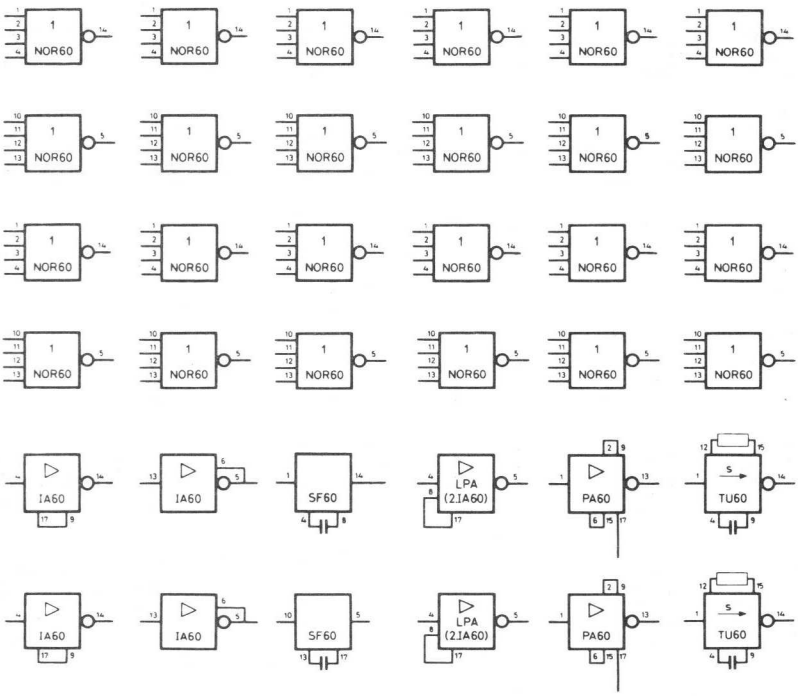
These are drawing symbols of NORBITS printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings.
The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number of 50 sheets: 4322 026 36481.



Sticker sheet without 4. NOR60 or TT60

STICKERS FOR THE 60-SERIES NORBITS

These are drawing symbols of NORBITS printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings.
The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 71941.

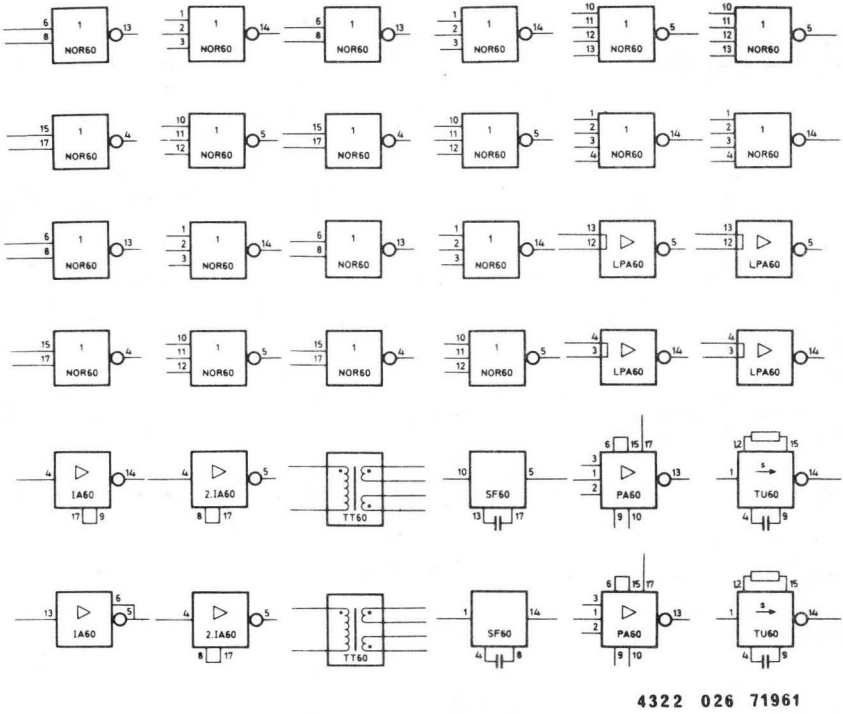


4322 026 71941

Sticker sheet without 4. NOR60 or TT60

STICKERS FOR THE 60-SERIES NORBITS

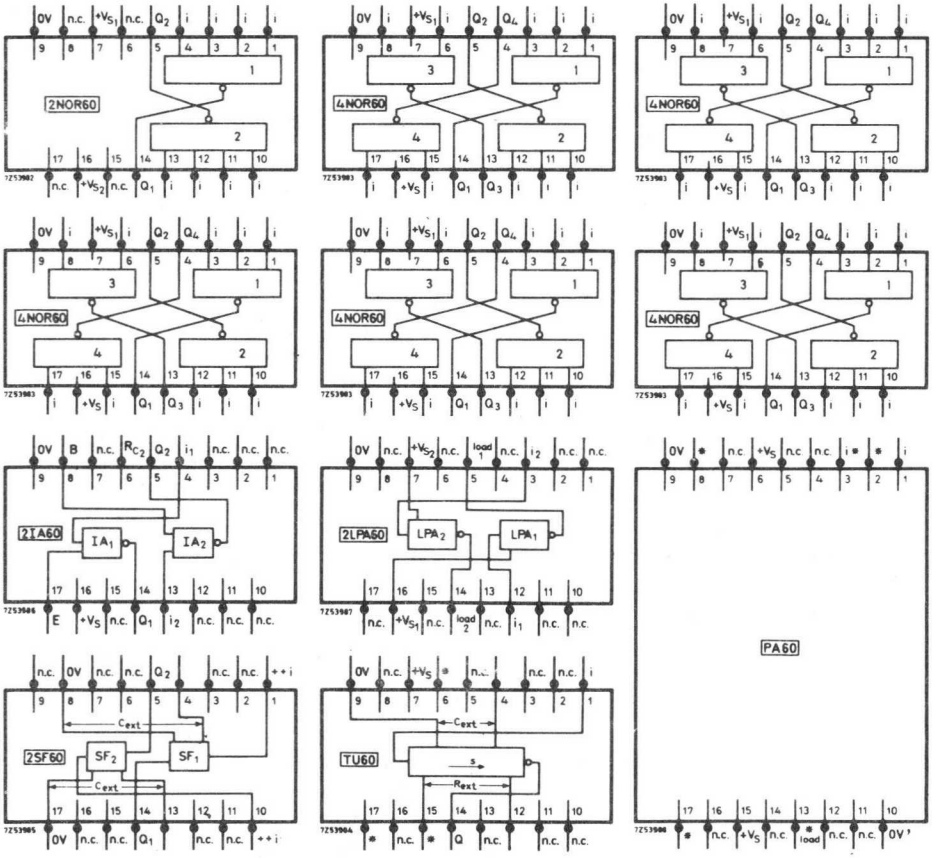
These are drawing symbols of NORBITS printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings.
The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 71961.



Sticker sheet with 4. NOR60 and TT60

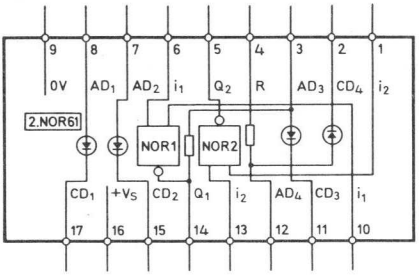
WIRING LAYOUT STICKERS
for the 60-series NORBITS

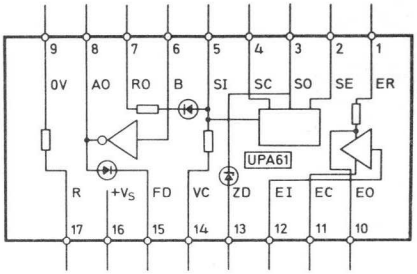
These are drawing symbols of 60-series blocks printed on self-adhesive, transparent material. They can be used for fast preparation of wiring layouts. All pin distances are actual size.
The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 71971.

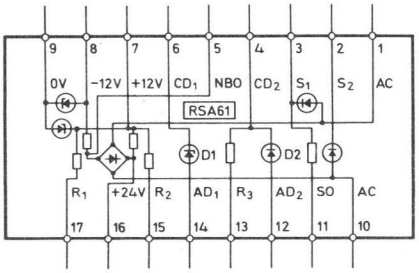


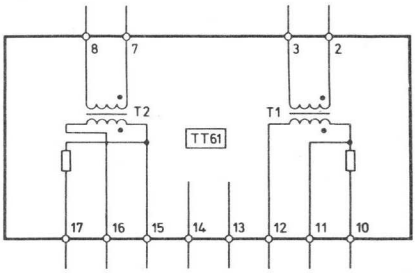
WIRING LAYOUT STICKERS
for the 61-Series NORBITS

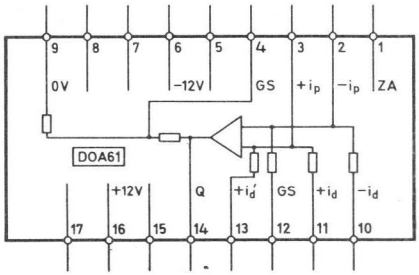
These are drawing symbols of 61-series blocks printed on self-adhesive,transparent material. They can be used for fast preparation of wiring layouts. All pin distances are actual size.
The stickers are available in sheets, each containing the five drawings shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 71981.











Circuit blocks
90-Series

INTRODUCTION

The "90-Series" comprises a number of circuit blocks eminently suitable for use in industrial control systems.

As far as the environmental specification, the supply voltage and the encapsulation are concerned, the circuit blocks in this series are compatible with those of the 60-Series and they can therefore be successfully combined.

Operating on the principle of trigger logic (that is: the units are driven by voltage transients in contrast with those of the 60-Series which respond to voltage level), the 90-Series units allow the building of assemblies such as counters and shift registers simply and economically. They are so designed as to have a high noise immunity. However, care must be taken to avoid capacitive and inductive cross-talk between connecting wires.

Briefly, the features of the 90-Series are:

- Single rail 24 V $\pm$ 25 % supply, allowing the use of an inexpensive power supply, which helps to keep the cost down, particularly in small systems.
- Transfer moulded cases, giving optimum protection.
- Rigid terminals spaced at 0.2 in pitch, permitting a variety of interconnection methods to be used (dip soldering, hand soldering, mini wire-wrapping).
- Good noise immunity.
- Silicon semiconductors throughout, ensuring reliable operation down to $-10\ ^{o}C$ and up to $+70\ ^{o}C$.
- Usable with the large number of accessories of the 60-Series.
- Easy-to-use loading table for system design.

The 90-Series comprises the following types:

FF90	Flip-flop
2.TG90	Twin-trigger gate
PS90	Pulse shaper

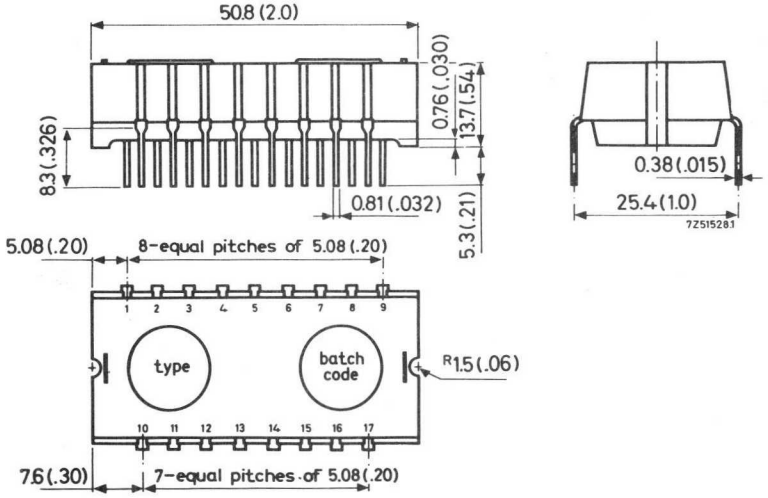
CONSTRUCTION

The circuit elements are housed in a transfer moulded encapsulation, which is identical to the "size A" block of the 60-series. The dimensions are as shown below. The pin connections for each unit are shown on the relevant data sheets. Pin numbering is moulded on both top and bottom of the unit. All pins are also accessible from the top of the unit to facilitate test requirements.

Mounting

The units may be mounted on printed-wiring boards, and a range of these is available with suitable metal housing chassis. They may also be clamped in the moulded Universal Mounting Chassis UMC 60 or fixed with 3 mm screws.

Dimensions in mm (inch equivalents within brackets)



TEST SPECIFICATIONS

All units meet the following test specifications:

Test	IEC 68	MIL-STD-202C
Dry heat life test	56 days at max. diss. max. temp. check at: 0-10/14d-56d.	Meth. 108A, Cond. D; check at 0-10/ 14d-56d.
Long-term damp heat non operating	Test C, 56 days check at 0-10/14 d-56d.	Meth. 103B, Cond. D; check at 0-10/ 14d-56d.
Long-term damp heat operating	Test C, 56d. min., diss., check at 0-10/14d-56d.	ditto
Temp. cycle-test	Test Na, 30 min., 2-3 min. in between; preferred: −40 °C; +85 °C and +125 °C.	Meth. 107B, Cond. A: moderate temp.
Vibration	Test Fb; 10-500-10 Hz 1 octave/min.; ampl. 0.75 mm max.; 10 g max. 3 x 3 hrs.	Meth. 204A, Cond. A: 10-500-10 Hz: 15 min. ampl. 0.75 max; 10 g max., 3 x 3 hrs.
Shock	-	Meth. 202B, 3 blows 50 g.
Robustness of terminations	Test $U_A + U_B$	Meth. 211A + (B or C)
Solderability + solder heat	Test T; at 0 hr and at 56d; no electr. test	Meth. 210, at 0 hr and at 56d; no electr. test

CHARACTERISTICS AND DEFINITIONS

AMBIENT TEMPERATURE LIMITS

Storage	T_{amb} = -40 °C to +85 °C
Operating	T_{amb} = -10 °C to +70 °C

SUPPLY VOLTAGE (V_S)

Single rail, +24 $V_{d.c.}$ ± 25% (18 to 30 V)

OUTPUT LEVEL

Logic '0'	0 to +0.3 V
Logic '1'	+12 to +30 V

TRIGGERING EDGE

The unit FF90 is driven by a negative-going transient (from "1" to "0" level). The maximum duration of the transient is, unless specified otherwise, 3 μs.

DRIVE UNIT (D.U.)

Drive required on Reset input of FF90 to bring output Q_1 to '1' level. [1])

ZERO UNIT (Z.U.)

Half the drive at '0' level required on one T terminal to trigger an FF90 unit.

FAN OUT

Number of drive units and zero units that can be delivered by a logic function, without exceeding the above defined limits for the logic levels.

[1]) This drive unit has also been specified as the drive required on one input of a NOR60 (with all other inputs returned to 0-volt line) to bring the output at '0' level.

INPUT AND OUTPUT DATA

System design is greatly simplified by expression of the input requirements and fan out capabilities of the various units in integral multiples of drive units (D.U.) and zero units (Z.U.). To check that the loadability of a particular unit is not exceeded simply add the number of D.U.'s or Z.U.'s present at its output.

FAN-OUT TABLE

The table shows the number D.U.'s and Z.U.'s, which can be delivered by the different units of the 90- and 60-series. The fan-outs are valid for a positive supply voltage of 24 V ± 25%.

unit	output capability		notes and instructions
	'1' level (D.U.)	'0' level (Z.U.)	
NOR of 2.NOR 60	6	12	2 inputs of the NOR must be connected in parallel. Signal must be derived from a chain of units that includes either a PS 90, an FF 90 or a TU 60.
2. IA 60; I.A. driven by an I.A.	20	50	Both the inverting and non-inverting connections can be used, but pins 5 and 6 must be interconnected. Signal must be derived from a chain of units that includes either a PS 90, an FF 90 or a TU 60.
NOR of 4.NOR 60	6	0	
LPA 60	-	0	No Z.U. available. Therefore, these units must not be used to drive an FF 90 or 2.TG90 directly.
PA 60	-	0	
TU 60	5	0	
SF 60	2	0	
PS 90	6	80	
FF 90	5	7	

FLIP-FLOP

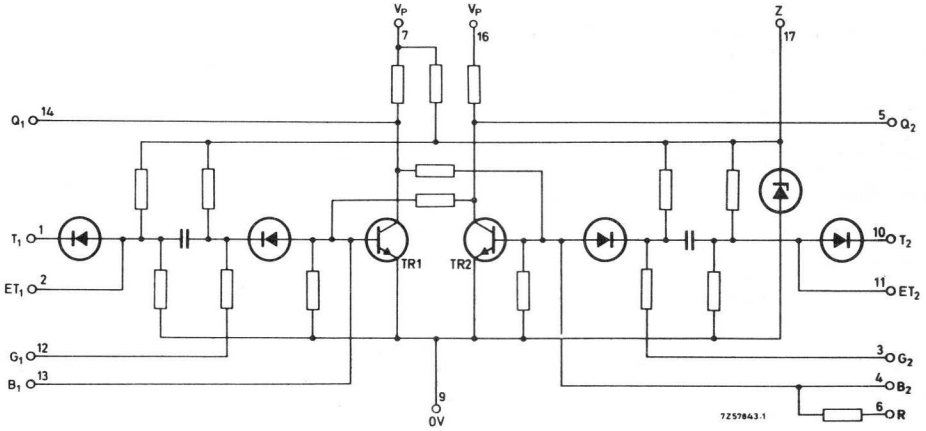
QUICK REFERENCE DATA	
Function	set-reset bistable multivibrator with trigger gates
Encapsulation	size: A block; colour: red
Max. counting speed (worst case)	5 kHz
Output capability	5 D.U., 7 Z.U.
Trigger input requirement	"1"-"0" edge of max. 3 μs; 2 Z.U.

APPLICATION

The FF90 has been intended to be used in counters, shift registers, etc.

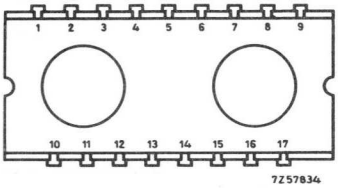
DESCRIPTION

Circuit

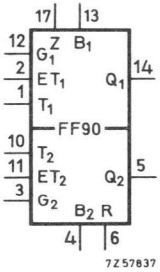


The unit comprises a set-reset bistable multivibrator which incorporates trigger gates. Switching is performed by applying a "1"-"0" edge of max. 3 μs at the trigger terminals (T_1 and T_2) which are controlled by gates (G_1 and G_2). The trigger inputs may be extended by the addition of external diodes to the extension terminals (ET_1 and ET_2) to provide an OR or inhibit facility. In addition, the circuit may be reset by applying a "1" level to the reset terminal (R) and may be set by applying a "1" level to the base of transistor 1 (B_1) via a resistor.

Terminal location



Drawing symbol



1 = T_1 = Trigger input 1
2 = ET_1 = Extension trigger input 1
3 = G_2 = Gate input 2
4 = B_2 = Transistor TR_2 base
5 = Q_2 = Output 2
6 = R = Reset
7 = V_p = For positive supply (connect to pin 16)
8 = Not connected
9 = 0 V = 0 V common
10 = T_2 = Trigger input 2
11 = ET_2 = Extension trigger input 2
12 = G_1 = Gate input 1
13 = B_1 = Transistor TR_1 base
14 = Q_1 = Output 1
15 = Not connected
16 = V_p = For positive supply (connect to pin 7)
17 = Z = Zener diode*

* Caution: With the supplies connected ensure that pin 16 is not accidentally connected to pin 17, otherwise the zener diode will be damaged.

ELECTRICAL DATA

Power supply

Voltage	+24 V ± 25%
Current	< 18 mA

Input requirements (see also "Switching times")

function	input terminal	input requirement		notes and instructions
		'1' level (D.U.)	'0' level (Z.U.)	
reset (put Q1 to '1')	R	1	0	The Set and Reset inputs may be expanded by using up to 3 suitable diodes at each input. Ensure that the cathode of each diode is connected to the input. If the Set or Reset facilities are used, inputs must be held at '0' (and not left open-circuited) except during the command period.
set (put Q2 to '1')	B1 via 82 kΩ resistor 2)	1	0	
gate	G_1, G_2	2	1	'1' or open-circuit closes gate. '0' opens gate.
gate	G_1, G_2 via a diode 1) 2)	0	1	'1' or open-circuit closes gate. '0' opens gate. Ensure that the anode of the diode is connected to the input.
trigger	T_1, T_2	0	2	Only a '1'-'0' edge occurring within 3 μs triggers the flip-flop. If T_1 and T_2 are interconnected, 4 Z.U. are required.
trigger	ET_1, ET_2 via a diode 1) 2)	0	2	Only a '1'-'0' edge occurring within 3 μs triggers the flip-flop. If ET_1 and ET_2 are interconnected, 4 Z.U. are required. Ensure that the anode of each diode is connected to the input.

1) Diodes type BAX 13, BAX 16 or BAX 78 can be used.

2) If external components are used, ensure that they are mounted as close as possible to the appropriate input.

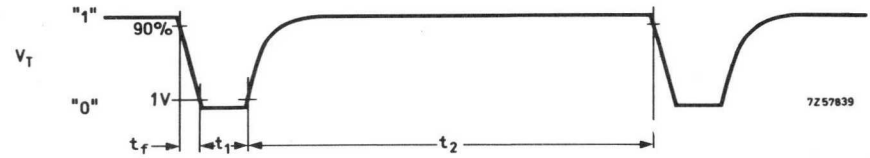
Output data

Output capability	5 D.U. and 7 Z.U.
Max. capacitive load	200 pF

Account must be taken of the load imposed by the gates when they are connected to the output terminals (Q_1, Q_2).

Switching times

Trigger



Max. fall time	t_{fmax}		3 μs
Min. pulse duration	t_{1min}		5 μs
Trigger recovery time	t_2	max.	99 μs
		typ.	73 μs

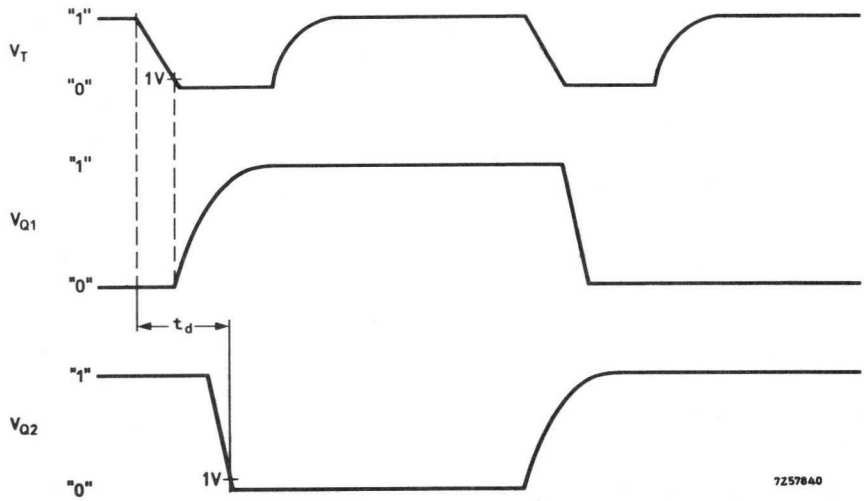
Gate

Gate recovery time	max.	137 μs
	typ.	100 μs

The signal at the gate must be present at least 137 μs (worst case) before the triggering edge is applied to T_1 or T_2. It is permitted to change the gate signal simultaneously with the triggering edge.

Switching delay

Delay between triggering edge and negative-going output.	t_d	max.	8 μs
		typ.	3 μs



Reset of Set: The appropriate terminal should be at a logical '1' for a minimum of 50 μs to reset or set the flip-flop.

Maximum Counting Speed (1 : 1 mark: space ratio) 5 kHz (worst case)

The worst case figure is related to the most disadvantageous connection or input condition that can be made.

TWIN-TRIGGER GATE

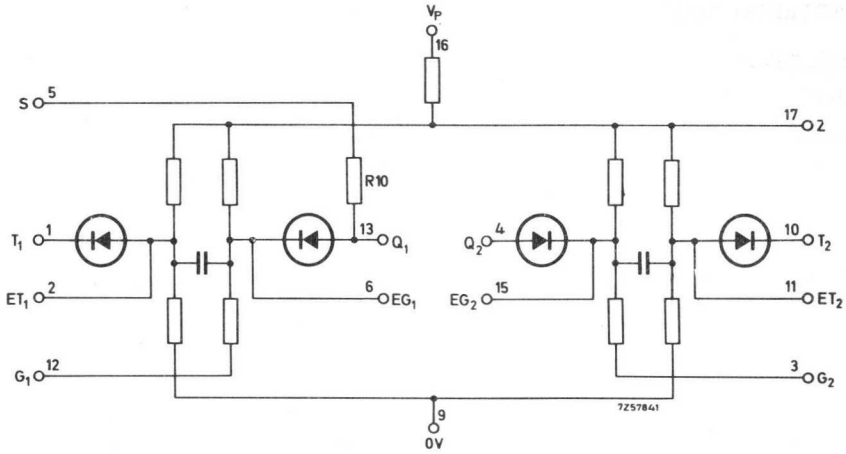
QUICK REFERENCE DATA	
Function	two trigger gates for use with FF90 only
Encapsulation	size: A block; colour: red
Output signal	suitable for triggering direct on transistor base of FF90 (B_1 and B_2)
Trigger input requirement	'1'-'0' edge of max. 3 μs; 2 Z.U.

APPLICATION

The 2.TG90 has been intended to provide two extra independent trigger gates for the FF90.

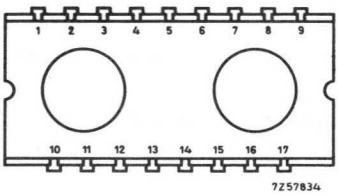
DESCRIPTION

Circuit

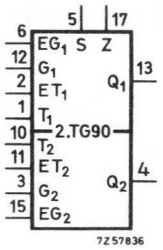


The unit comprises two gating circuits to perform extra independent trigger functions. The mode of operation is the same as for the trigger functions of the FF90. Switching is performed by applying a '1'-'0' edge of max. 3 μs at the trigger terminals (T1 and T2) which are controlled by gates (G_1 and G_2). The trigger inputs may be expanded by the addition of external diodes to the extension terminals (ET_1 and ET_2) to provide an OR or inhibit facility. The extra resistor (R_{10}), connected to terminal Q_1, provides the 'set' facility for the FF90.

Terminal location



Drawing symbol



1 = T_1 = Trigger input
2 = ET_1 = Extension trigger input 1
3 = G_2 = Gate input 2
4 = Q_2 = Output to B_2 (pin 4) of FF90
5 = S = Set terminal
6 = EG_1 = Extension gate input
8 = Not connected
9 = Not connected
9 = 0 V = 0 V common

10 = T_2 = Trigger input 2
11 = ET_2 = Extension trigger input 2
12 = G_1 = Gate input 1
13 = Q_1 = Output to B_1 (pin 13) of FF90
14 = Not connected
15 = EG_2 = Extension gate input
16 = V_P = For positive supply
17 = Z = Voltage reference terminal, connect to Z (pin 17) on FF90

ELECTRICAL DATA

Power supply

Voltage	+24 V ± 25%
Current	7.5 mA

Input requirements

function	input terminal	input requirement		notes and instructions
		'1' level (D.U.)	'0' level (Z.U.)	
set (put Q_2 of associated FF90 to '1')	S	1	0	The Set input may be expanded by using up to 3 suitable diodes on each input. Ensure that the cathode of each diode is connected to the input. If the Set facility is used, the input must be held at '0' (and not left open-circuited), except during the input period.
gate	G_1, G_2	2	1	'1' or open-circuit closes gate. '0' opens gate
gate	G_1, G_2 via diode 1) 2)	0	1	'1' or open-circuit closes gate. '0' opens gate. Ensure that the anode of the diode is connected to the input.
trigger	T_1, T_2	0	2	Only a '1'-'0' edge occurring within 3 μs triggers the flip-flop 3). If T_1 and T_2 are interconnected, 4 Z.U. are required.
trigger	ET_1, ET_2 via diode 1) 2)	0	2	Only a '1'-'0' edge occurring within 3 μs triggers the flip-flop 3). If ET_1 and ET_2 are interconnected, 4 Z.U. are required. A maximum of two diodes may be connected to each ET terminal. Ensure that the anode of each diode is connected to the input.

For notes see page 4.

Output data

The outputs Q_1, Q_2 are suitable only for use with one FF90; Q_1, Q_2 and Z of the 2.TG90 should be connected to B_1, B_2 and Z respectively of the FF90.
The inter-wiring capacitance should be limited at 50 pF (maximum). This capacitance will not be exceeded when a 2.TG90 is mounted next to an FF90.

1) Diodes type BAX 13, BAX 16 or BAX 78 can be used. Max. 2 diodes may be added.
2) If external components are used, ensure that they are mounted as close as possible to the appropriate input.
3) Switching times of the triggering signal are the same as for the FF90.

PULSE SHAPER

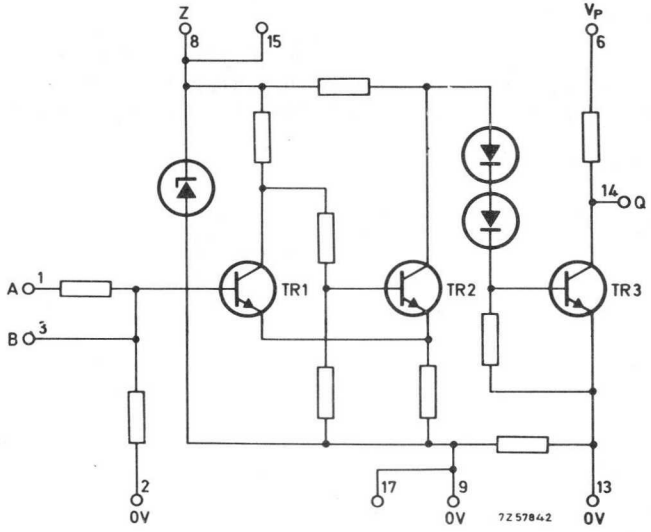
QUICK REFERENCE DATA	
Function	a. Driving the trigger inputs of one or more FF90 or 2.TG90 units b. Shaping signals to produce NORBIT 60 drive levels
Encapsulation	size: A block; colour: green
Output capability	6 D.U.; 80 Z.U.

APPLICATION

The PS90 has been intended to produce the triggering edge required for the FF90. The output levels are conforming to '1' and '0' of 60-Series logic.

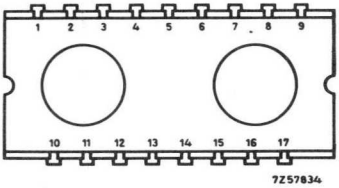
DESCRIPTION

Circuit

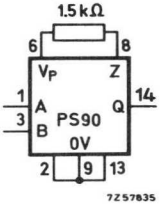


The unit contains a Schmitt trigger circuit followed by an inverting amplifier.

Terminal location



Drawing symbol



1 = A = Input via resistor
2 = 0 V = 0 V common (connect to pins 9 and 13)
3 = B = Input direct to base
4 = Not connected
5 = Not connected
6 = Vp = For positive supply (connect also to pin 8 via 1.5 kΩ resistor*)
7 = Not connected
8 = Z = Zener diode ** internally connected to pin 15 (connect to pin 6 via 1.5 kΩ resistor *)
9 = 0 V = 0 V common, internal connection to pin 17 (connect also to pins 2 and 13)
10 = Not connected
11 = Not connected
12 = Not connected
13 = 0 V = 0 V common (connect also to pins 2 and 9)
14 = Q = Output
15 = Z = Internally connected to pin 8
16 = Not connected
17 = 0 V = Internally connected to pin 9.

* The 1.5 kΩ ± 10% resistor connected between pins 6 and 8 (15) has a dissipation of 0.35 W maximum.

** When the PS90 is mounted on PWB60 or PWB61, pins 7 and 16 are connected to the positive supply VP. Ensure therefore, that neither pins 7 and 8 nor pins 15 and 16 are interconnected. Otherwise, the Zener diode will be damaged.

ELECTRICAL DATA

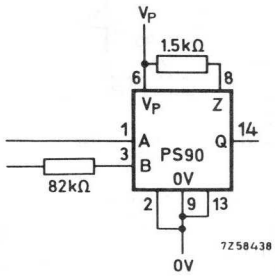
Power supply

Voltage	+24 V ± 25%
Current	< 21 mA

Input Data

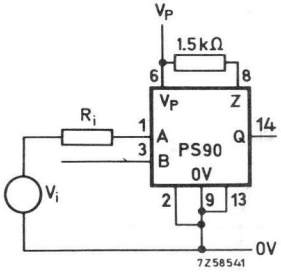
1. Unit driven by circuit block of 60 Series or 90 Series

The input requirement at pin 1 (pin 3 not connected) for '0' output is 1 D.U. One input may be added, namely an 82 kΩ resistor connected to pin 3 (input requirement is 1 D.U.). The circuit then performs as a 2-input NOR function. The 82 kΩ resistor should be mounted as close as possible to the unit.



2. Unit driven by any other circuit at pin 1 with pin 3 not connected.

	Operating	Limiting value
Input voltage to give '0' output	min. +6 V	+30 V
Input voltage to give '1' output	max. +1.5 V	−15 V



Hysteresis

ΔV_i min. = 0.55 + 0.003 Ri V (R_i in kΩ)

ΔV_i max. = 1.5 + 0.012 Ri V (R_i in kΩ)

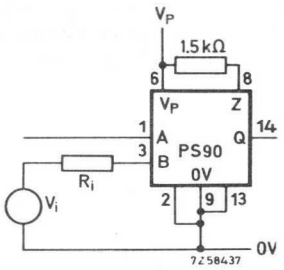
See also "Switching speed".

3. Unit driven by any other circuit at pin 3 with pin 1 not connected

	Operating	Limiting values
Input current to give '0' output	min. 50 μA	5 mA
Input current to give '1' output	max. 15 μA	0 mA

If driven by a voltage source, the source resistance should be minimum 500 Ω.

Max. positive voltage with R_i = 500 Ω +5 V
Max. positive voltage with R_i = 6.8 kΩ +30 V
With pin 2 not connected the max. source resistance is 50 kΩ and the max. negative voltage is 4 V.



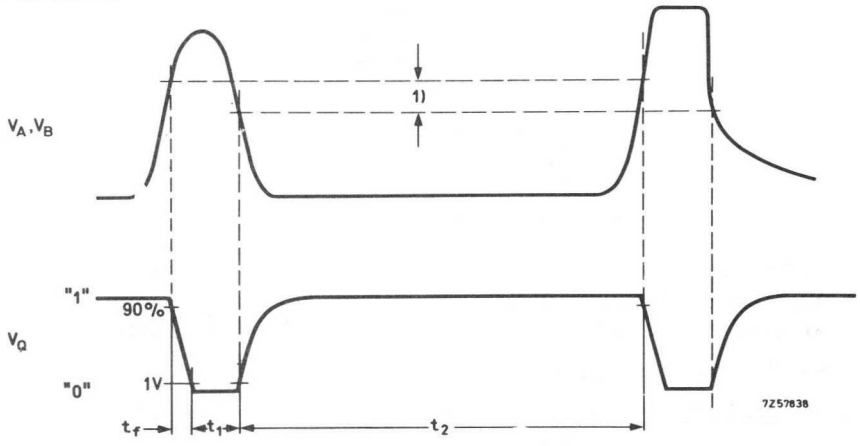
Hysteresis
ΔV_i min. = 0.32 + 0.003 R_i V (R_i in kΩ)
ΔV_i max. = 0.45 + 0.012 R_i V (R_i in kΩ)

See also "Switching speed".

Output Data

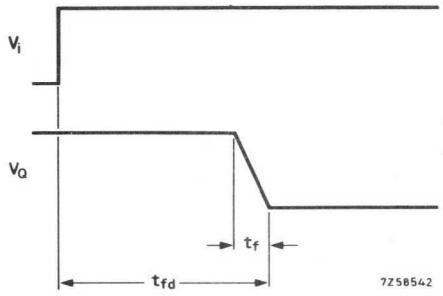
Output capability	6 D.U.
	80 Z.U.
Max. capacitive load	200 pF

Switching Speed



$t_f \leq 3\ \mu s$
t_1 and t_2 depend on input waveforms.
1) Hysteris ΔV_A or ΔV_B

If a step function is applied to the input and the output is loaded with 200 pF the output signal is given by:



Fall time	$t_f < 0.25\ \mu s$
Fall delay time	$t_{fd} < 2.5\ \mu s$

Input/output devices

INTRODUCTION

Input devices

Industrial control systems require compatible input devices that are capable of deriving signals representative of controlled or otherwise pertinent conditions. Though the information to be dealt with may take a variety of forms - e.g. presence, position, movement, rotation etc. - many different situations can be covered by a comparitively small selection of input devices.
The requirements of each situation determine the physical principle to be employed in the input device.
For reasons of speed and reliability it is preferable to avoid mechanical contact in deriving the input signal, and often an all-static method of derivation is required. Experience with input devices has made it clear that skilful use of them can greatly improve machine output and reliability.

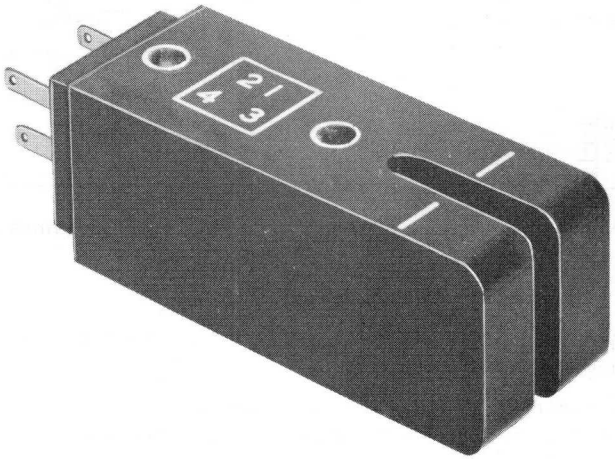
Output devices

At the output of a control system signals will often have to be amplified to obtain the necessary power for certain operations. In this respect the Thyristor Trigger Module will provide a useful way of bridging the gap from low signal voltage to high mains voltages. In connection with a Phase Shift Module PSM40 it makes possible a wide range of output control facilities.

In this series the following units are available:

VANE SWITCHED OSCILLATOR

RZ 19213-1



Supply voltage	12 V_{dc}
Operating-temperature range	−25 to +85 °C

APPLICATION

The vane switched oscillator can be applied as a static switching device, the switching action being determined by the position of a vane. For the vane any metal can be used.

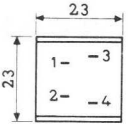
CONSTRUCTION

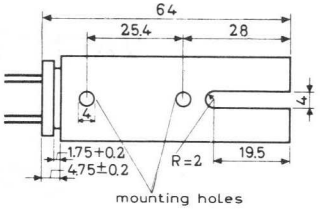
The vane switched oscillator consists of an oscillator and a diode rectifier. The latter is connected to a separate coupling winding of the oscillator coil, thus providing an isolated d.c. output.
The lay-out of the oscillator is such that upon inserting a suitable piece of metal (vane) in a gap between the oscillator coil windings, the oscillation stops and the d.c. output of the unit will drop to zero.
The complete circuit is encapsulated in epoxy resin.

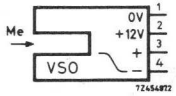
1 = −
2 = +
} supply

3 = +
4 = −
} output

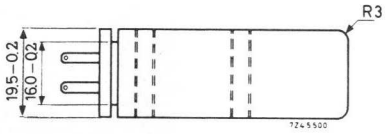
Terminal location







Drawing symbol

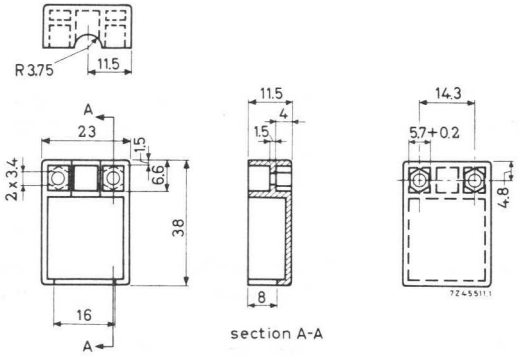


Dimensions in mm

The weight (without cable anchoring cover) is 42 g.

The unit may be mounted in any position. Two mounting holes allow the use of 4 mm bolts. Stacking of units is permitted.

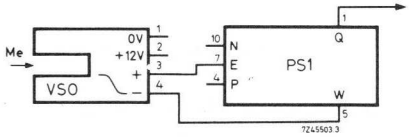
Connection can be made by 0.110 Fastons or by soldering.
A cable anchoring cover, consisting of two equal caps (as shown in the figure below), is supplied with each VSO.

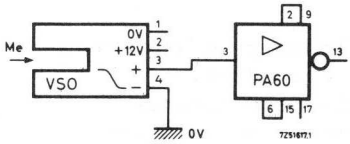


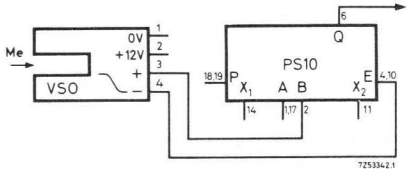
Cable anchoring cover

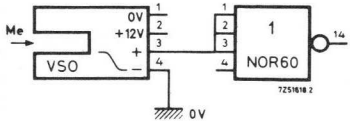
ELECTRICAL DATA

Supply voltage	12 V_{dc} ± 10% or +6 V_{dc} ± 10% and −6 V_{dc} ± 10% (with common 0 V)
Consumed current (in both oscillating and non-oscillating condition)	12 mA ± 10%
Output voltage	5.75 V ± 15% open circuit , isolated from the supply. Maximum permissible voltage between 1-2 and 3-4 is 100 V_p Suited for driving the pulse shaper types PS 1* and PS 10**, and for driving the Norbit PA60 and 2.NOR60 if three inputs are connected in parallel.









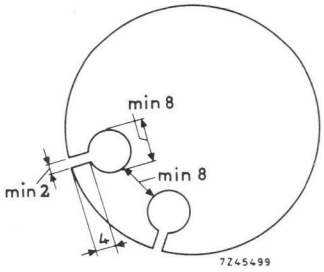
Output impedance (without vane)	4.1 kΩ ± 10%
Maximum detection frequency	1 kHz
Noise (over supply lines)	< 100 mV_{p-p}
Ambient temperature range operating storage	 −25 to +85 °C −40 to +85 °C

* circuit block 100 kHz series, catalog number 2722 001 11001
** circuit block 10-series , catalog number 2722 004 11001

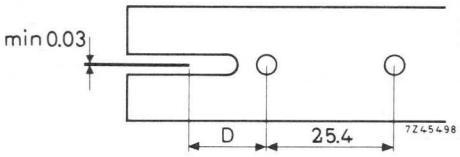
APPLICATION INFORMATION (typical values)

Vane material	any metal
Vane dimensions for aluminium:	
minimum width for a thickness of 2 mm	8 mm
minimum thickness	0.03 mm

Instead of a vane a disc with holes of indicated dimensions may be used.



The data given below are based on a movement of an aluminium vane 50 x 50 x 2 mm in longitudinal direction.
The operating distance D (see figure below) is the distance at which the output just drops to zero (measured from the centre of the hole nearest to the gap).
Hysteresis is defined as the distance between the vane position at which oscillation ceases and that at which oscillation starts.

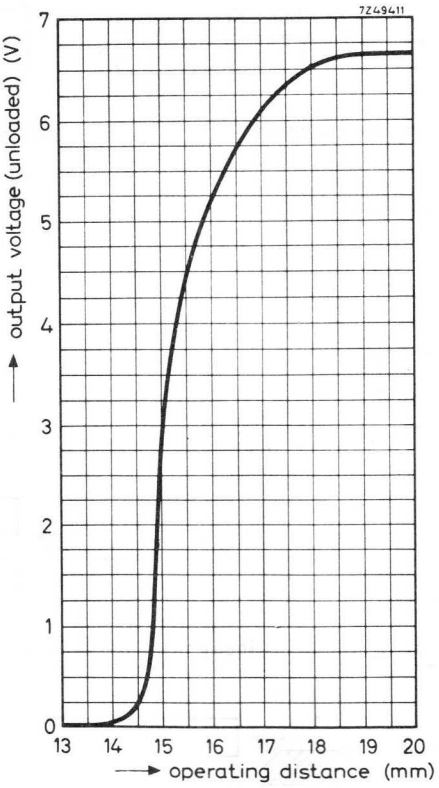


Operating distance D	
open circuit	14.6 ± 1.5 mm
with PS 1 or PS 10 (0 to 1)	15.3 ± 1 mm
Hysteresis	
open circuit	< 1 mm
with PS 1	0.03 mm
with PS 10	0.6 mm

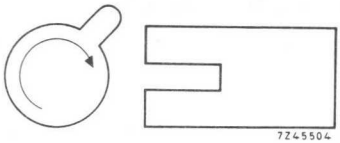
Variation of D with supply voltage

supply voltage	operating distance (mm)
nominal	D
nominal −5%	D +0.06
nominal +5%	D −0.06

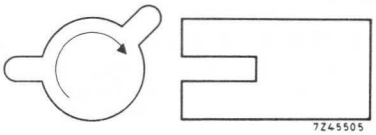
Variation of D with temperature (from −25 to +85 °C)	< 2.7 mm D is maximum at −25 °C
Variation of D with time (at T_{amb} = 25 °C and V_{supply} = 12 V ± 1%, reference point is half the unloaded output voltage of VSO without vane)	< 0.02 mm
Variation of output voltage with D	see typical curve, figure below. From the steep curve it can be seen that a switching point will be kept within very narrow mechanical tolerances.



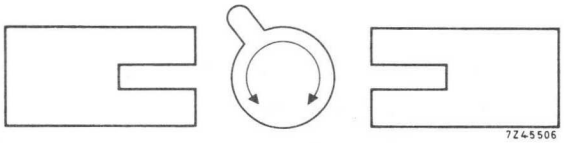
APPLICATION SUGGESTIONS



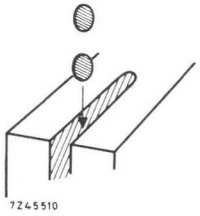
counting of revolutions



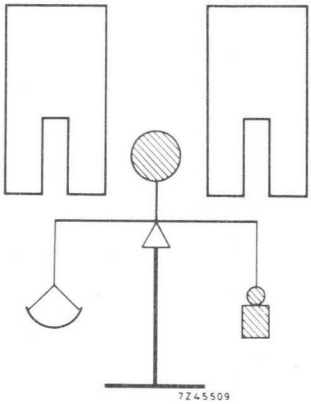
angular position switching (programming)



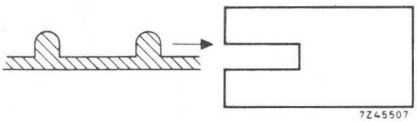
bidirectional counting



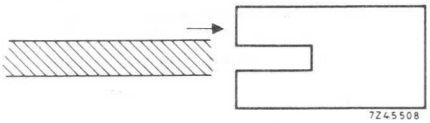
counting of small objects



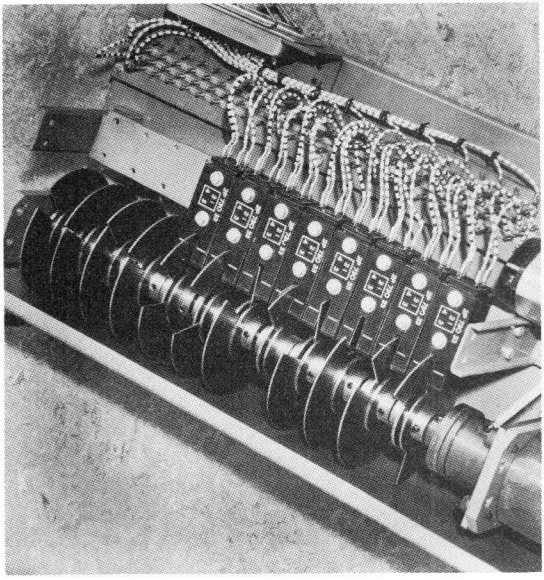
weighing or dosing



linear position switching (programming)

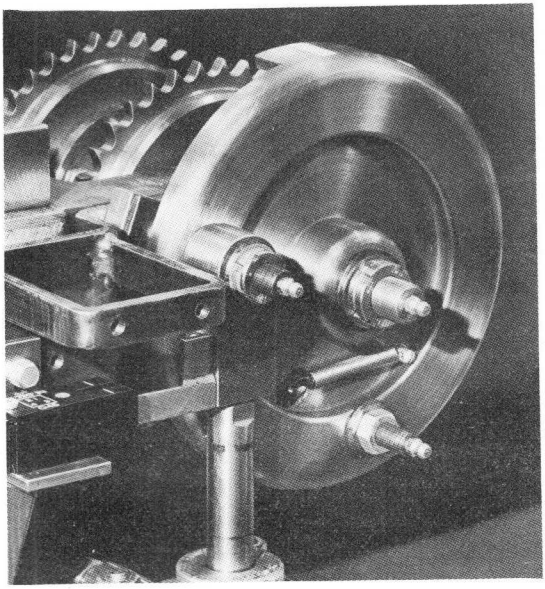


foil continuity check



Eight VSO's used in a disc programmer for control of a metal-working machine.

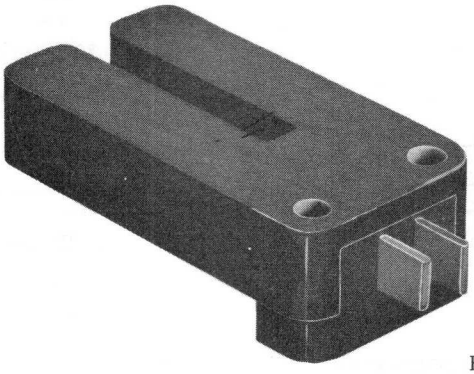
RK 9230-4



VSO control of pneumatic metal-forming machine.

RK 9230-5

IRON VANE SWITCHED REED



RZ 21773-3

Maximum switching frequency	100 Hz
Operating-temperature range	−25 to +70 °C

APPLICATION

The iron vane switched reed can be applied as a limit switch, position indicator or as a signal source for low counting speeds.
In conjunction with d.c. amplifiers or with the thyristor trigger module (TTM), the IVSR can be used for power switching.
As the IVSR is free from most of the difficulties encountered with mechanical switches, it can succesfully replace micro switches.

CONSTRUCTION

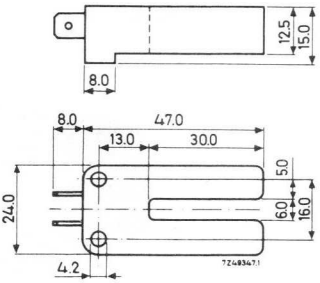
The IVSR consists of a magnet and a reed switch encapsulated in an U-shaped plastic housing.
When there is no piece of iron (vane) in the gap between the reed switch and the magnet, the reed switch is closed. Inserting a piece of iron of suitable dimensions in the gap reduces the magnetic flux through the reed to such an extent that the reed switch opens.
In this way it is possible to obtain signals that indicate the position of the iron vane.

The weight is approximately 20 g.

The IVSR can be mounted in any position. Two mounting holes allow the use of 4 mm bolts. When IVSR's are mounted on a common support, the minimum distance between the housings is 36 mm, to avoid interaction. For mounting IVSR's over each other, this distance is 60 mm.

Connection can be made by means of 0.250" Fastons or by soldering.

Drawing symbol



Dimensions in mm

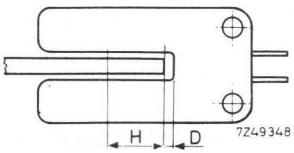
TECHNICAL PERFORMANCE

Load switching capacity (non inductive)	$\leq$ 1.2 VA
Voltage switching capacity	$\leq$ 32 V_{dc}
	$\leq$ 50 V_{ac}
Current switching capacity (non inductive)	$\leq$ 0.1 A_{dc}
Switching frequency	$\leq$ 100 Hz
Contact resistance, measured at 10 mV	
at open circuit	< 150 mΩ
Contact capacitance	$\leq$ 5 pF
Insulation resistance, measured at 250 V_{dc}	
at open circuit	$\geq 10^8$ Ω
Test voltage, measured at open circuit	
for 1 min	500 V_{dc}
Permissible operating-temperature range	-25 to +70 °C
Permissible storage-temperature range	-40 to +85 °C

APPLICATION INFORMATION (typical values)

Vane material	mild steel

The data given are based upon a movement of a mild steel vane 30 x 10 x 4 mm, placed centrally in the gap, in longitudinal direction.



The operating distance (D) is the distance between the front edge of the vane and the rear of the gap at which the reed switch opens.
The hysteresis (H) is defined as the distance between the vane position at which the reed switch opens and that at which the reed switch closes.

Operating distance	4 ± 3 mm
Hysteresis	10 ± 3 mm

APPLICATION SUGGESTIONS

As the reed switch is normally closed, the following two modes of operation can be distinguished:
- output voltage is present when there is no vane in the gap (Fig.a)
- output voltage is present when there is a vane in the gap (Fig.b)

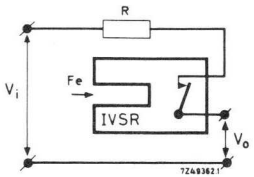


Fig.a

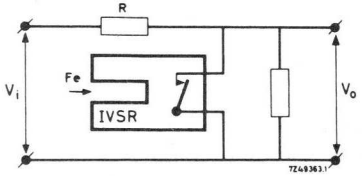
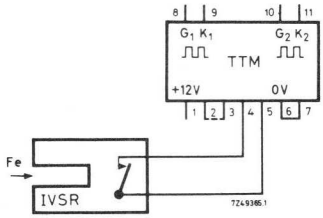
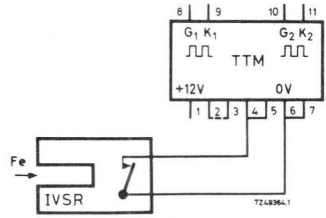


Fig.b

IVSR in conjunction with the thyristor trigger module (TTM)



Trigger pulses from the TTM only if there is no vane in the gap of the IVSR



Trigger pulses from the TTM only if there is a vane in the gap of the IVSR

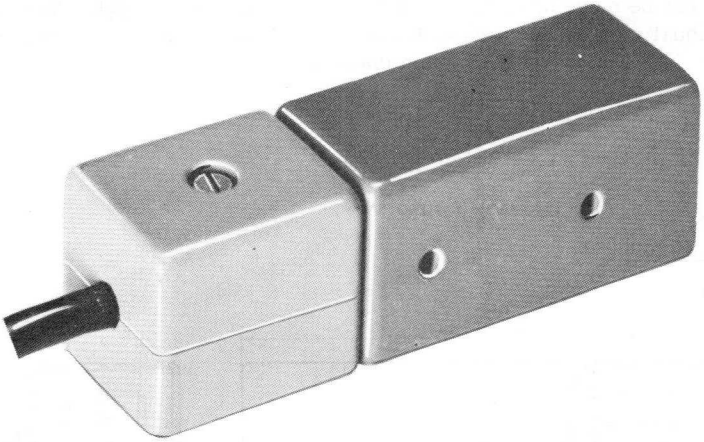
Notes

It is obvious that the IVSR should not be used in environments where iron dust or scraps might impair its operation.

It should be realised that capacitance directly across the switch terminals can be the cause of high currents through the switch at the moment of closing the contacts. This should be avoided by having sufficient resistance in the proper contact circuit.

In case the switch is used with electronic circuitry in which bounce might give rise to malfunctioning of the equipment, appropriate circuitry should be added to get rid of the bounce effect. The safe way out is the use of a one shot multivibrator.
Another solution that sometimes can be used, is applying a low pass RC network between the IVSR and the input of the equipment.

ELECTRONIC PROXIMITY DETECTOR



Supply voltage	12 V_{dc}
Maximum detection frequency	1 kHz
Operating-temperature range	−25 to +85 °C

GENERAL

The electronic proximity detector is a static switching device, the switching action being determined by the presence of a metallic object. The metal can be any electrically conducting material of rather arbitrary shape.
It can be applied as a detector for the presence, passage or position of metal parts and is a versatile tool in various industrial automation set-ups.

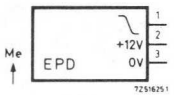
The EPD contains an oscillator which is link coupled to a detector. The detector is followed by an amplifier.
The oscillator coils and the coupling link are placed in a potcore half. In this way a well-defined field is set up in front of the open side of the potcore, located at the front side of the EPD. Bringing a piece of metal in this field the oscillator output and subsequently the output of the amplifier decreases, due to the loading effect of the eddy current losses in the metal.
When no piece of metal is near, the output voltage of the EPD is approximately 12 V. It will decrease in proportion to the reduction of the oscillator output, resulting from a metal object coming nearer.

The complete circuit is epoxy encapsulated in a polycarbonate housing.

The weight is approximately 120 g.

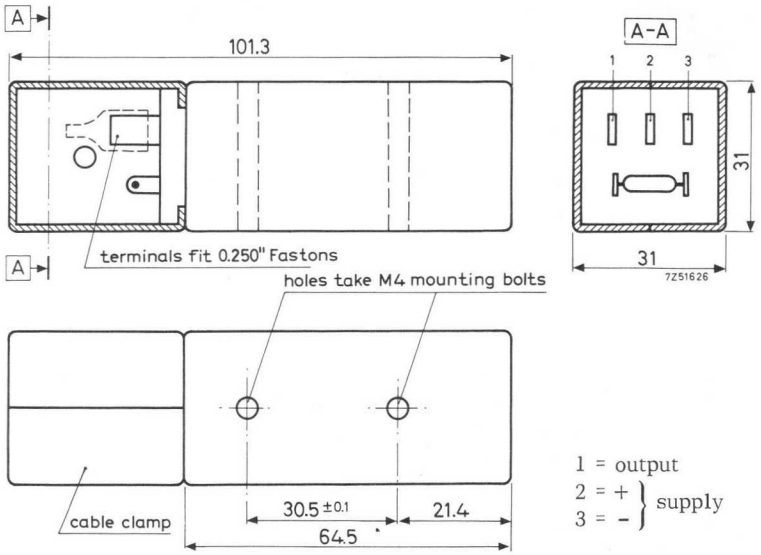
The unit may be mounted in any position. Two mounting holes allow the use of 4 mm bolts.

Connection can be made by 0.250" Fastons or by soldering. A cable clamp consisting of two equal caps is supplied with each EPD. This clamp permits either end or top entrance of a 3-core cable of 7 mm diameter.



Drawing symbol

Dimensions in mm



Note

The resistor between the two 0.110" Fastons is an adjustment resistor for the oscillator loop gain; it should not be changed.

TECHNICAL PERFORMANCE

Supply voltage (V_S)	12 V_{dc} ±5% or +6 V_{dc} ±5% and −6 V_{dc} ±5% (with common 0 V) or 24 V_{dc} via series resistor and 12 V zener diode, giving a stabilised supply voltage of 12 V. (See also APPLICATION SUGGESTIONS.)
limiting value	abs. max. 15 V *) (destructive at $T_{amb} \geq 40\ ^oC$)
Consumed current (nominal value)	16 mA
Output voltage, no object being detected	approximately V_S − 0.5 V
Output resistance	
no object being detected	680 Ω ±10%
object being detected	3.3 kΩ
Hysteresis for output voltages of 100 mV − 11 V	0 mm
Minimum load	1 kΩ
Maximum detection frequency	1 kHz
Noise (over supply lines)	< 10 mV
Ambient temperature range	
operating	−25 to +85 °C
storage	−40 to +85 °C

APPLICATION INFORMATION (typical values)

Detection graphs

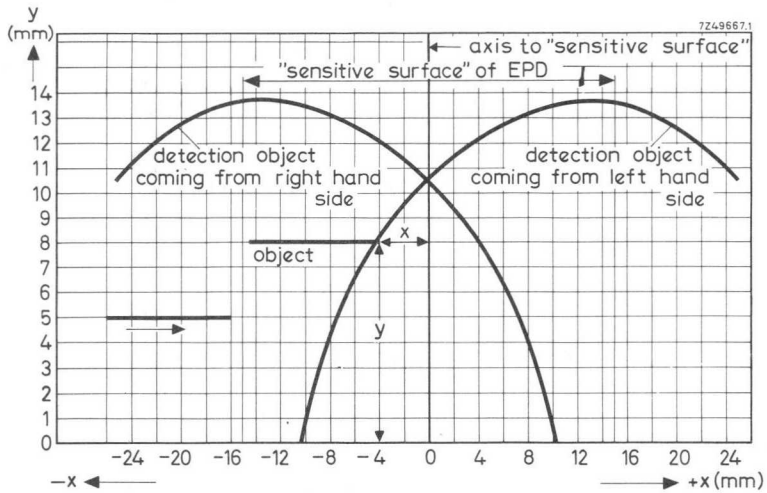
Detection of a rectangular mild steel reference object, 50 x 25 x 1 mm

Sensitive surface	surface of 31 x 31 mm at the opposite end of the EPD to the terminals
Axis	line perpendicular to the centre of the sensitive surface
Operating point	point at which the output voltage of the EPD is reduced to 100 mV (moment of detection)

*) Reversal of supply voltage will damage the detector.

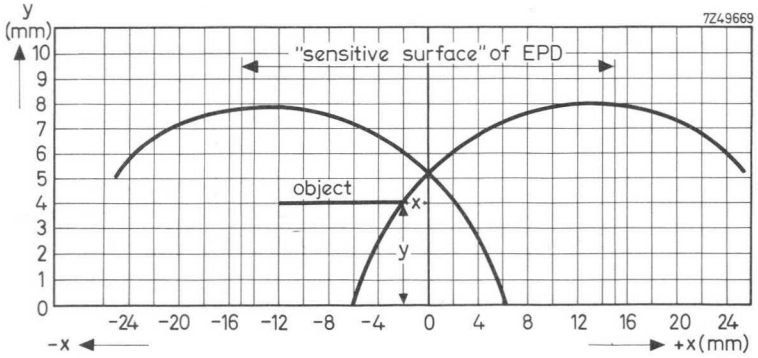
Operating distance — distance of the leading edge of the reference object to the axis at the operating point (x-operating distance)

Detection range — distance of the reference object to the sensitive surface (y-operating distance)



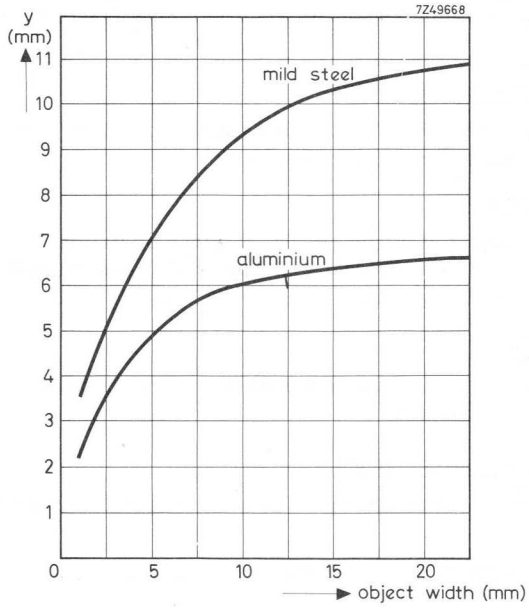
From the graph it can be seen that the object is detected before the axis is reached if it passes at a distance of < 10 mm from the sensitive surface. If it passes at a distance of e.g. 13.5 mm, the object is detected after the axis has been passed.

Detection of a rectangular aluminium reference object, 50 x 25 x 1 mm

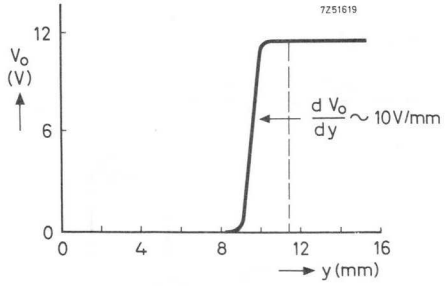


Detection of rectangular mild steel and aluminium reference objects (50 x 1 mm) with different widths

Object approaches the centre of the sensitive surface perpendicularly from in front.



Output voltage as a function of the position of a rectangular mild steel reference object, 50 x 25 x 1 mm



Upon frontal approach of the object to the sensitive surface, the output voltage of the EPD will change from over 11 V to 100 mV within 1 mm from the position in which the output voltage starts to change.
This characteristic is extremely important when the EPD is used as a position detector.

Notes:

The detection graphs may differ slightly from unit to unit.

Quite small objects can be detected when brought close to the sensitive surface. Thickness is relatively unimportant as eddy currents occur in penetration layer only.

Influence of supply voltage variations

A supply voltage variation of ±5% produces a change of ±0.1 mm in y-operating distance, at 10 mm from the sensitive surface.

Influence of temperature

With the reference object at a y-operating distance of 10 mm (at −25 °C) a change in temperature of both EPD and object will cause the y-operating distance to change less than 2 mm over the range from −25° to +85 °C.

Direction of approach

As the exterior field is rotation symmetrical the path along which the detection position is reached is immaterial.

Distance from metallic surroundings

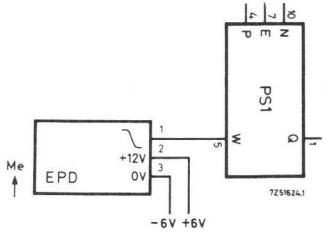
Clearance from metallic surrounding: 30 mm (this applies for sensitive front part of unit).

Spacing required between two detector axes with sensitive surface in the same plane: 60 mm.

Spacing required between two reference objects to give discrete detection: 50 mm. (This property can be put to use in feeder systems, a gap being used to initiate part supply restart.)

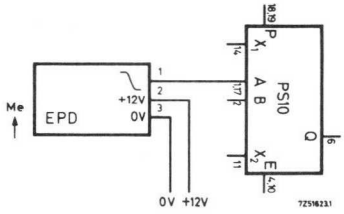
APPLICATION SUGGESTIONS *)

EPD in conjunction with 100 kHz-Series circuit blocks

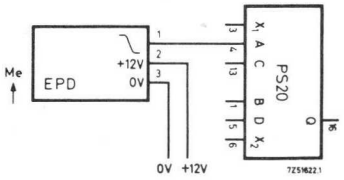


*) With long cables between EPD and subsequent electronics RC decoupling of interference can be employed.

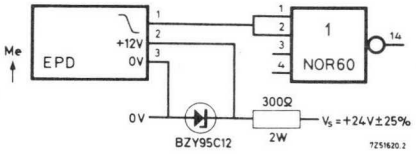
EPD in conjunction with 10-Series circuit blocks

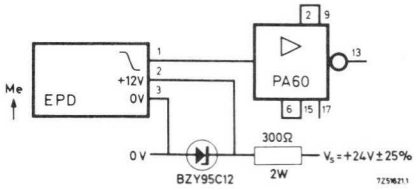


EPD in conjunction with 20-Series circuit blocks



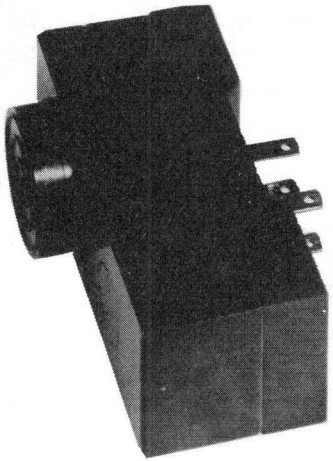
EPD in conjunction with 60-Series Norbits





MINIATURE ELECTRONIC PROXIMITY DETECTOR

QUICK REFERENCE DATA	
Supply voltage	24 V (d.c.) ±25%, or 12 V (d.c.) ± 5%
Maximum detection frequency	1 kHz
Operating temperature range	−25 to + 70 °C



RZ 2851 3-2

APPLICATION

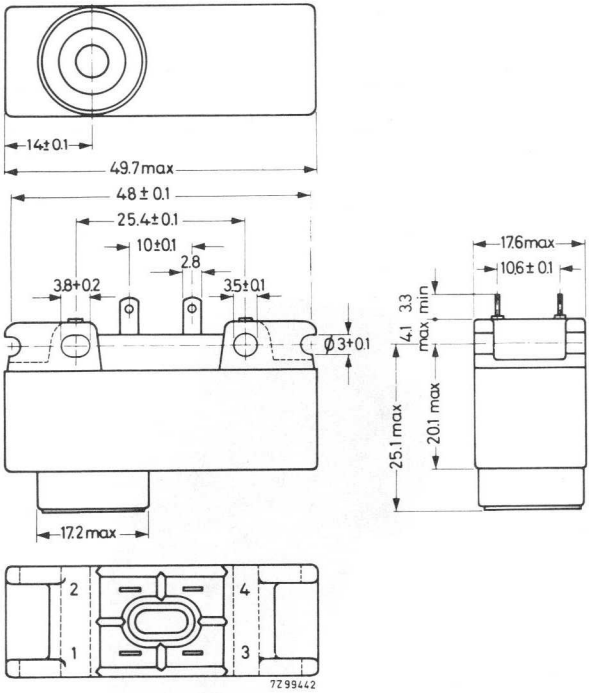
The EPD 60 can be applied as a static switching device, the switching action being determined by the position of a metal object. In this way a static equivalent for the well-known mechanical miniature switch is obtained.

DESCRIPTION

The circuit consists of an oscillator followed by a detector and an amplifier.
The oscillator coil, placed in a potcore half, which is located in the cylindrical part of the housing, sets up a well defined field.
If there is no metal object in the field of the coil the output is low, if a metal object of adequate size is brought far enough into the field, the oscillator will be damped in such a way that the output of the unit goes "high".
The unit is potted in a polydiallylphtalate resin housing, the dimensions of which are compatible with standard mechanical miniature switch housings, see photograph below. Connection to the unit can be made by means of 0.110 inch Fastons supplied with it.

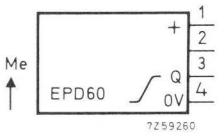
MECHANICAL DATA

Dimensions in mm



Terminal location

Terminal 1 = +24 V
2 = +12 V (connect 2 and 1)
3 = output (Q)
4 = 0 V common



Drawing symbol

Colour red

Weight 30 g approximately

Mounting

The unit may be mounted in any position. Two mounting holes allow the use of 3 mm bolts. Two grooves in the short sides are provided for bar mounting. Any number of units may be stacked side by side.

ELECTRICAL DATA

Supply voltage (V_S) *)	+24 V ±25%, or +12 V ± 5%
Consumed current (nominal)	15 mA
Max. permissible voltage for 1 s	
at V_S = +24 V	+35 V
at V_S = +12 V	+15 V
Ambient temperature range	
operating	−25 to +70 °C
storage	−40 to +85 °C
Maximum detection frequency	1 kHz

Output data

			V_S = +24 V		V_S = +12 V	
Output low	at I_Q	=	0	mA	0	mA
	max. V_Q	=	+ 0.3	V	+ 0.3	V
	R_Q	=	3	kΩ	3	kΩ
Output high	at − I_Q	=	0.41	mA	0.20	mA
	and at min. V_S	=	18.0	V	11.4	V
	at loading equivalent	=	3 D.U. in 24 V nom. 60-Series operation		2 D.U. in 12 V nom. 60-Series operation	
	V_Q	=	min.+11.4	V	min.+8.3	V
	max. V_Q	=	max.V_S		max.V_S	
	R_Q	=	15	kΩ	15	kΩ

External short-circuit is not destructive.

APPLICATION INFORMATION

The EPD 60 can be switched by moving either a ferrous or a non-ferrous metal object of any size and form in front of the detection head. If the object is ferrous the resulting damping on the oscillator is proportional to the volume of the object; in the case of a non-ferrous object it is governed by the conductivity of the material. Thus, a perfect conductor cannot be detected unless it is sufficiently thin and brought close to the detection head.

*) Accidental polarity reversal is not destructive.

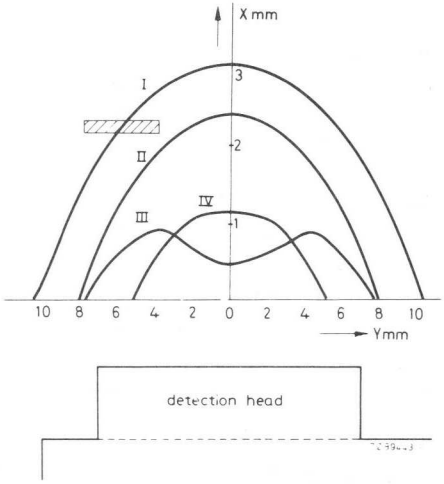
Operating distance

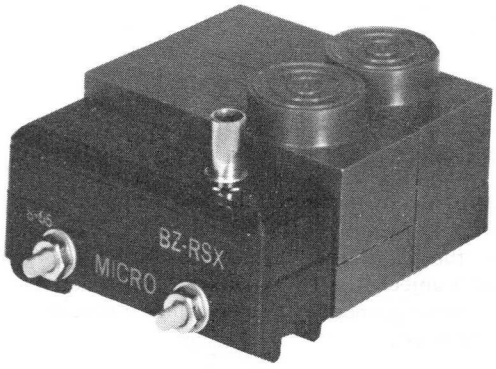
The operating distance (X) is the distance between the centre of an object and the centre of the detection head at which the output is about to go "high" (measured axially)

For reference purposes four standard objects are used:

Object I : mild steel, circular disc Ø 15 mm, thickness 0.2 mm
Object II : mild steel, circular disc Ø 10 mm, thickness 0.2 mm
Object III : copper, circular disc Ø 15 mm, thickness 0.04 mm
Object IV : copper, circular disc Ø 10 mm, thickness 0.04 mm

The graph below gives X for each of the four standard objects traversing the sensitive area of the detection head along a straight line which intersects the axis of the head, and runs parallel to the surface of the head.





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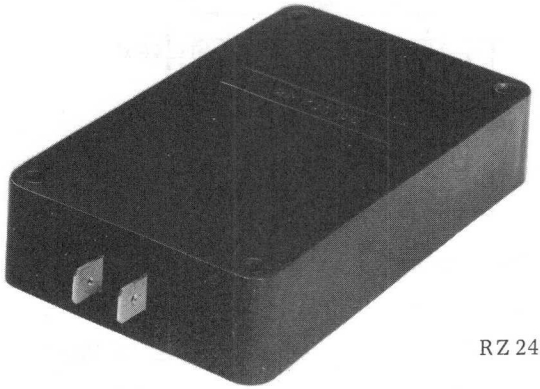
The photograph shows two EPD 60's together with a "Microswitch".

MAGNETIC PROXIMITY DETECTOR



RZ 24323-1

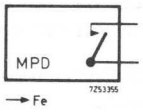
Maximum switching frequency	100 Hz
Operating temperature range	-25 to + 70 °C

GENERAL

The magnetic proximity detector can be applied as a detector for the presence, passage or position of ferreous parts. It is a versatile tool in industrial automation set-ups.

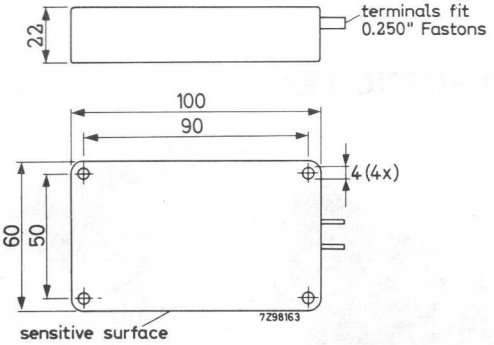
The MPD consists of two magnets and a reed switch, which are mounted in a high grade plastic housing. The reed switch is mounted between the magnets at a position where their fields are balanced (contacts normally open).
As a ferreous object approaches the sensitive surface of the MPD, unbalance occurs between the magnetic fields and the reed switches on. As the ferreous object is withdrawn the reed switches off.

Connection can be made by 0.250" Fastons. The terminals of the MPD are provided with receptacles and insulating covers.



Drawing symbol

Dimensions in mm



TECHNICAL PERFORMANCE

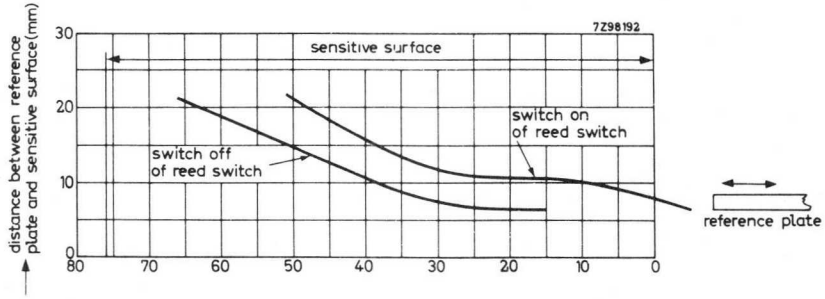
Load switching capacity	≤ 25 W
Voltage switching capacity	≤ 200 V_{dc}
Current switching capacity	≤ 1 A_{dc}
Switching frequency	≤ 100 Hz
Contact resistance, initially	≤ 100 mΩ
Operating temperature range	-25 to + 70 °C
Storage temperature range	-25 to + 85 °C

APPLICATION INFORMATION

The data given below are based upon the position of a mild steel (free cutting quality) reference plate 76 x 76 x 1.9 mm.

Detection range = distance between sensitive surface and front face of reference plate, at frontal approach	≥ 17 mm at 20 °C
Hysteresis = distance between "switch on" and "switch off" points, at frontal approach	< 6 mm at 20 °C
Repeatability with a supply voltage of 30V and a current of 7.5 mA flowing through the unit when the reed contacts are closed	
after 10 000 operations	detection range and hysteresis unchanged
after one million operations	detection range and hysteresis may decrease by approximately 0.4 mm

Change of "switch on" point with a temperature variation from +25 to +70 °C	≤ 0.5 mm
Change of hysteresis with a temperature variation from + 25 to + 70 °C	≤ 0.75 mm

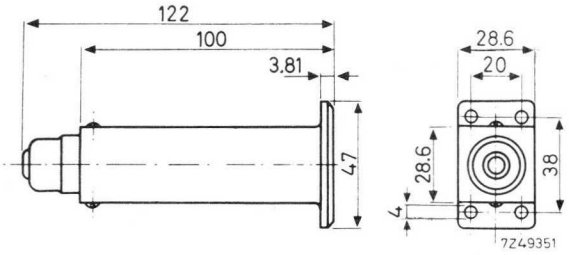


Typical detection graphs for passage of reference plate.
With the reference plate approaching from opposite end, the results are the same and the curves a mirror image of those shown.

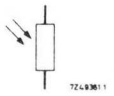
MOUNTING

Distance of ferreous metals from any point of the unit in order to avoid altering the detection range by more than 0.1 mm	≥ 200 mm
Distance between two units, mounted side by side giving a change in detection range of 0.1 mm	
sensitive surfaces in same direction	170 mm
sensitive surfaces in opposite direction	155 mm

PHOTO-ELECTRIC DETECTOR



Dimensions in mm



Drawing symbol

APPLICATION

This photo-electric detector has been developed to be used as an Input Device for systems composed of digital circuit blocks. However, it can also be used for other applications, see "APPLICATION SUGGESTIONS" on next page.
It is intended for use in conjunction with the lamp unit 1 MLU.
It can also be combined with other light sources, that meet the requirements of the particular situation.

CONSTRUCTION

The housing has been moulded of black acryl butyl styrene. In the housing a cadmium sulfide cell has been mounted. At the front side is a lens with a focal distance of 43.5 mm. The lens is protected by a glass disc. Connection to the circuitry can be made after unscrewing the cap at the rear.
The photo-electric detector can be mounted in any position by means of four bolts and nuts.

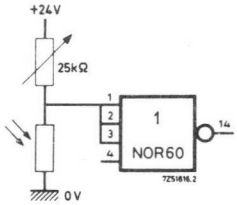
TECHNICAL PERFORMANCE

Dark value, measured in total darkness	> 10 MΩ
Light value, measured at 1000 lux	< 300 Ω
Recovery rate at falling light intensity	> 200 kΩ/s
Maximum permissible voltage	150 V_p
Maximum dissipation at 40 °C	0.2 W
Maximum capacitance	6 pF
Maximum switching frequency	6 Hz (typical value)
Maximum operating distance when used with the lamp unit 1 MLU	1 m

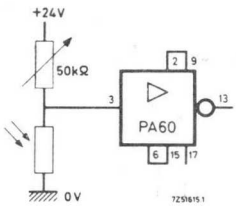
Permissible operating-temperature range	−10 to +40 °C For higher temperatures up to +50 °C, the maximum dissipation is 0.1 W
Permissible storage-temperature range	−20 to +60 °C
Weight	approximately 130 g

APPLICATION SUGGESTIONS (typical values)

a. Photo-electric detector CSPD in conjunction with 60-series Norbits.

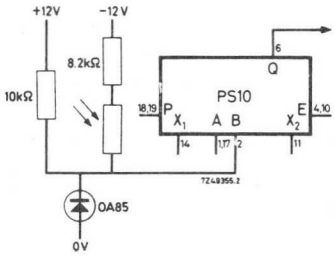


Output level state "1", when detector is illuminated

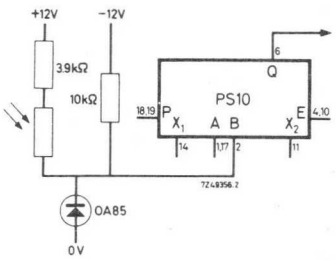


Output current is flowing, when detector is not illuminated.

b. Photo-electric detector CSPD in conjunction with 10-series circuit blocks.

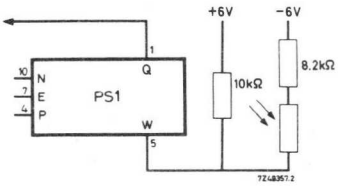


Output level state "1", when detector is illuminated

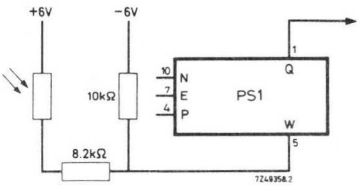


Output level state "1", when detector is not illuminated

c. Photo-electric detector CSPD in conjunction with 100 kHz-series circuit blocks.



Output level state "0", when detector is illuminated



Output level state "0", when detector is not illuminated

d. Twilight switch

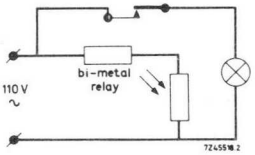
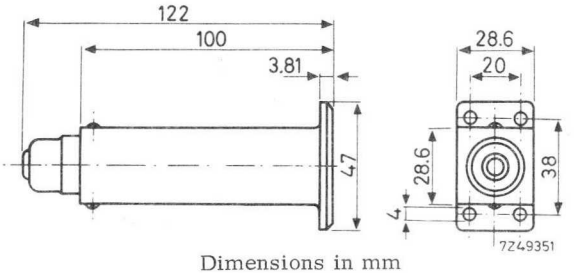
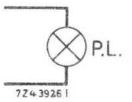


Photo-electric detector CSPD operates with a bi-metal relay so that incident light flashes have no influence.

LAMP UNIT



Dimensions in mm



Drawing symbol

APPLICATION

This lamp unit is intended for use in conjunction with the photo-electric detector CSPD

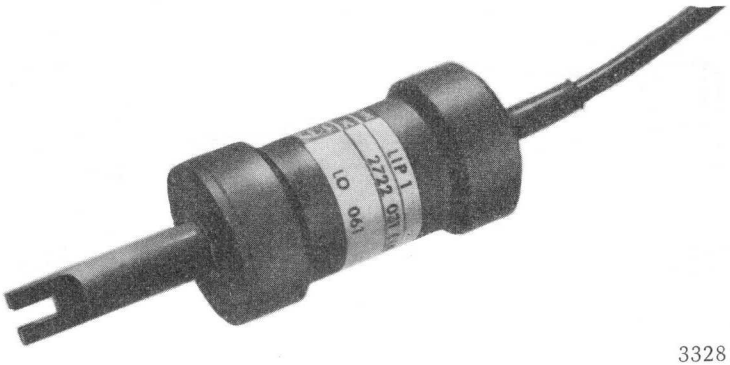
CONSTRUCTION

The housing has been moulded of black acryl butyl styrene. A 6 V, 3 W-lamp with bayonet base (type of lamp socket B15d) has been mounted inside the housing. At the front side is a lens with a focal distance of 43.5 mm. The lens is protected by a glass disc.
Connection to the supply voltage can be made after unscrewing the cap at the rear. The unit can be mounted in any position by means of four bolts and nuts.

TECHNICAL PERFORMANCE

Maximum supply voltage	6 V_{ac} or 6 V_{dc} For maximum life of the lamp it is advisable to use an a.c. or d.c. supply voltage of 5.4 V (I = 0.5 A). Variant supply voltages can be used for other lamps, provided the power consumption does not exceed 3 W.
Maximum operating distance when used with the photo-electric detector CSPD	1 m
Permissible operating-temperature range	−10 to +40 °C
Permissible storage-temperature range	−20 to +60 °C
Weight	approximately 130 g

LIGHT INTERRUPTION PROBE



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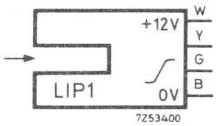
APPLICATIONS

The Light Interruption Probe can be used to detect the presence or passage of small objects. Major applications are envisaged in the field of machine tool control (accurate positioning and revolution counting).

DESCRIPTION

The unit houses a novel optical system, a lamp, a photo element, and an emitter follower output stage.

The light coming from the lamp is guided through an optical glass rod. The end of this glass rod at the probe side has been cut and polished at an angle of 45° to the axis of the rod. This provides a combination of a converging lens and prism, forming a focal line in the centre of the gap at the end of the probe. By means of a similar optical system the light that has passed the gap is guided to the photo element in the cylindrical housing.



Drawing symbol

The photo element has a low resistance when illuminated, thereby draining the base current to the emitter follower.

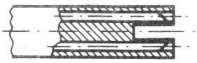
As a consequence the output of the unit will be a 'low' voltage. On the other hand if the light emerging from the lamp-side rod is intercepted the output of the unit will be a 'high' voltage.

As only a small object is necessary to intercept the light at the location of the focal line a high resolution is obtained. Though the unit essentially behaves in an analogue way only data pertaining to digital applications will be given.

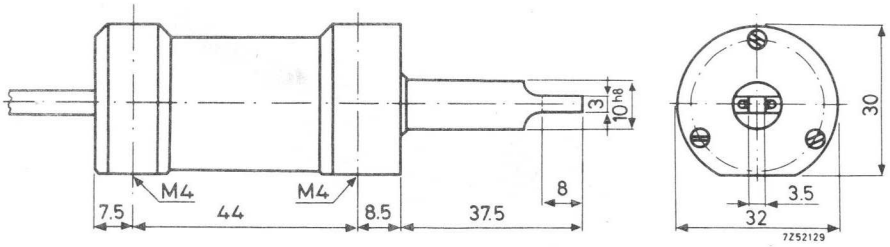
Electrical connections are made by means of a 4-core colour-coded shielded cable with a length of 2 m.

MECHANICAL DATA

Dimensions in mm



Housing material: brass
Finish: black

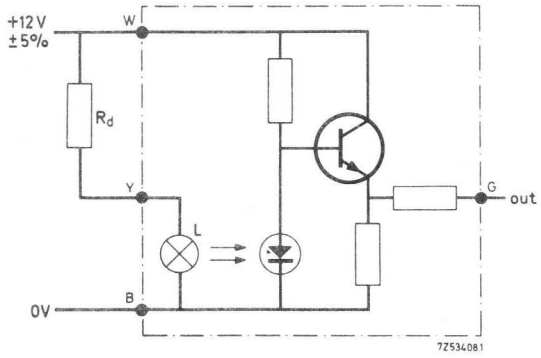


Weight: 170 g (ex cable)

Mounting

The unit can be mounted in any position either by means of two M4 bolts and a supporting bracket, or by entering the probe part into a 10 mm bore cylindrical hole.

CIRCUIT DATA



R_d = 36 Ω ± 2% (cat. no. 2112 100 10538) is supplied with unit,
L = 6 V, 1 W (cat. no. 9237 246 10181).
Cable shield is connected to probe housing.

Connections

W = white lead, to be connected to +12 V
Y = yellow lead, to be connected via R_d to +12 V
B = brown lead, common 0 V for power supply and load
G = green lead, to be connected to load.
Cable shield to be connected to system shield or to central earth point depending on system lay-out.

Notes

Interconnecting 0 volt and shield arbitrarily may cause difficulties as this introduces the possibility of feeding shield interference pick-up to the 0 volt line.

When the LIP is attached to a machine, which will generally have some earth connecnection provided for its metal structure, it is recommended that the probe housing and cable shield be properly insulated from the machine to eliminate extra interference pick-up due to capacitive and inductive coupling.

When considering to connect the load terminal to the input of a subsequent unit which is positive with respect to the 0 volt line, make sure that the LIP 1 output voltage is not raised as a result.

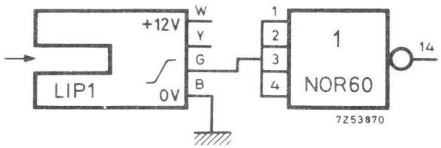
TECHNICAL PERFORMANCE

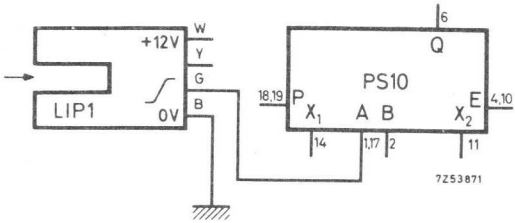
Ambient temperature range		
operating		0 to +50 °C
storage		−10 to +70 °C
Power supply	voltage (V_s)	+12 V_{dc} ± 5%
	current	180 mA
Output, unloaded [1]		
max. '0' level (no object)		+1.25 V
min. '0' level (no object)		0 V
min. '1' level (with object)		+4.8 V
max. '1' level (with object)		+ V_s
Output impedance, no object		max. 2.1 kΩ
, complete interception		max. 1.1 kΩ
Output is short circuit proof against 0 volt line		
Max. detection frequency		> 10 kHz
Lamp life		> 1000 h (spare lamp is supplied with the unit)

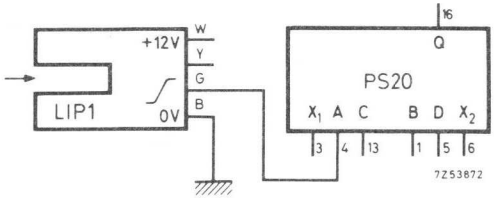
[1]) For specification purposes use is made of a glass disc carrying a (chromium) mark and space pattern.
Mark width and space width are each 1 mm.
Marks are arranged radially and have a length of 5 mm.
Disc is located in gap so as to bring mark in center of gap.
Actual length of focal line is 2 mm approximately.

APPLICATION INFORMATION

Connecting to circuit blocks







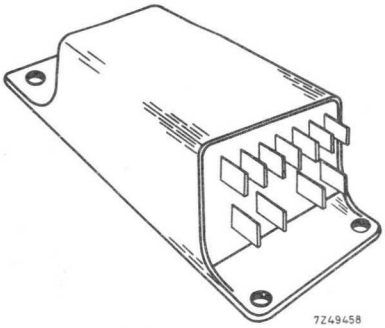
Application Suggestions

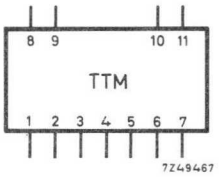
Revolution counting
Angular positioning
Digital Tachos
Analogue Tachos
Weighing

Angular programming

Linear programming

THYRISTOR TRIGGER MODULE





drawing symbol

Supply voltage	12 V_{dc}
Number of outputs	2, isolated (output voltages in phase)

GENERAL

The thyristor trigger module is intended for use as a supply of repetitive gate trigger pulses for one or two thyristors.
It can be applied in a variety of circuits.
The possibility of logic control (e.g. in conjunction with 60-series Norbits or with circuit blocks of the 10-series or 20-series) makes it well adapted for automation and control systems. In conjunction with a phase shift module PSM 40 (catalog number 2722 010 02001), linear conduction angle control over 10 to 170° is possible.
With three TTM's 3-phase operation of thyristors can be achieved.
For further applications, see section "APPLICATION SUGGESTIONS".

CONSTRUCTION

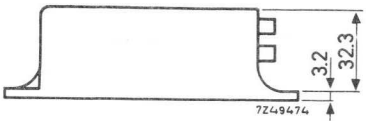
The TTM comprises a blocking oscillator circuit, which is potted in epoxy resin. The whole is contained in a high grade plastic housing.

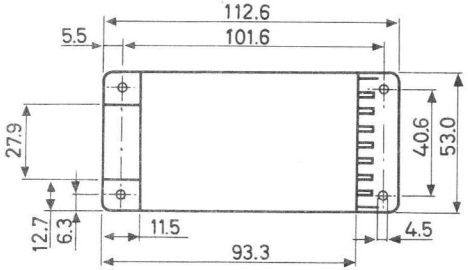
Four holes in the base allow the use of 4 mm bolts for mounting.
As the maximum operating temperature of the TTM is 85 °C, bolting the unit directly to the heatsink of the thyristor will in many cases be feasible.
If the gate and cathode connection leads have considerable length it is recommended to twist them as a pair for each thyristor.

Connection can be made by 0.250 Fastons supplied with the TTM.

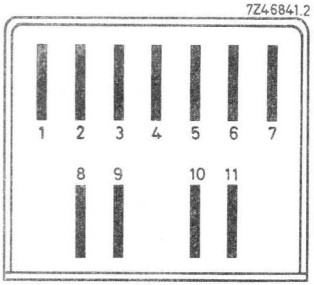
The weight is approximately 280 g.

Dimensions in mm





Terminal location

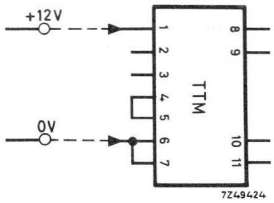


1 = supply +12V
2 = } interconnected, except for on-off control
3 = } and conduction angle control with a potentiometer or a control voltage
4 = } interconnected, except for control
5 = } with a switch which is normally open
6 = supply 0V
7 = safety-catch input
8 = gate thyristor 1
9 = cathode thyristor 1
10 = gate thyristor 2
11 = cathode thyristor 2

TECHNICAL DATA

Operating-temperature range	-25 to +85 °C
Storage-temperature range	-40 to +85 °C
Power supply	
Supply voltage	12 V_{dc} ± 5% Loss of supply voltage does not cause inadvertent trigger pulses.
Nominal consumed current	35 mA

12 V_{dc} ± 5%, filtered, obtained from e.g. power supply unit 2722 151 00021.



Input requirements

Current from control terminals (typical values)

4/5 to 6	1.5 mA
7 to 6	35 mA (I_{peak} = 57 mA)

See further section "INPUT CONTROL POSSIBILITIES".

Output data *

Number of outputs	2, isolated. Output voltages are in phase.
Isolation of outputs	rated at 500 V_{rms} operation
Voltage	≤ 10 V_{dc}
Current (one output loaded with 16Ω, the other output short-circuited)	250 mA. Short-circuiting of both outputs will not impair the reliability of the TTM and will not damage the power supply.
Impedance (both outputs or one output loaded with 16Ω)	25Ω
Nominal pulse frequency (both outputs loaded with 16Ω)	2.3 kHz
Pulse width at 3 V (both outputs loaded with 16Ω)	> 20 µs (see Fig. a)
Pulse rise time	< 0.5 µs (see Fig. a)

Shape of voltage pulse (both outputs loaded with 16Ω)

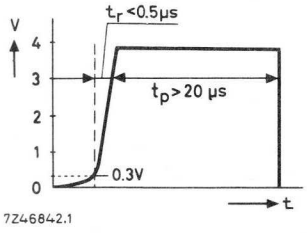


Fig. a

Shape of current pulse (both outputs loaded with 16Ω)

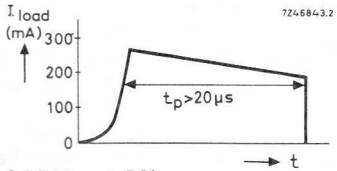
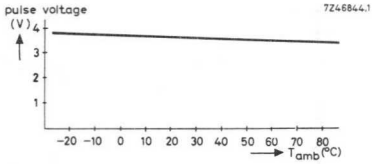


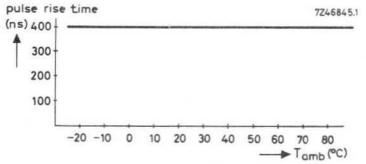
Fig. b

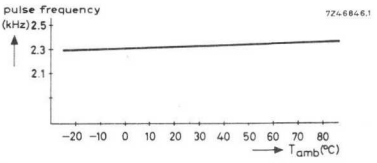
* The data given apply to a supply voltage of 12 V_{dc} ± 5%

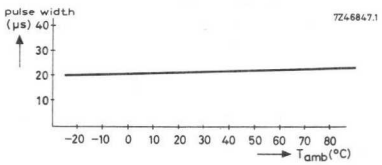
Temperature dependence of the pulse (both outputs loaded with 16 Ω)

see typical curves below



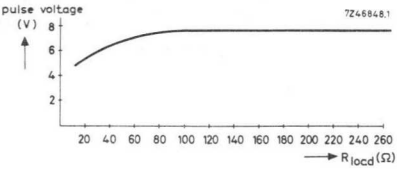


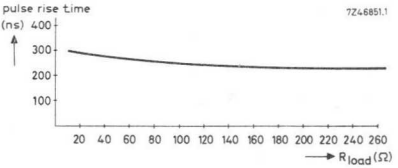


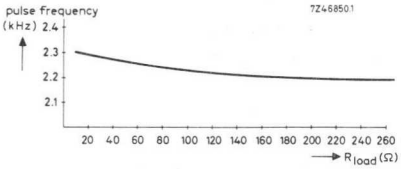


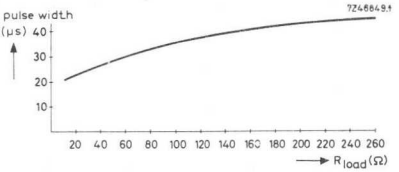
Load dependence of the pulse (one output loaded with 16 Ω, the other output with a variable load)

see typical curves below









The TTM can be used with thyristors of the following types (or other types having similar gate input requirements): BTX 12, BTX 13, BTY 79, BTY 80, BTY 81, BTY 87, BTY 91, BTY 95 and BTY 99.

Any two thyristors can be triggered simultaneously either in series, parallel or inverse parallel connection.

All precautions and restrictions to ensure operation within the limits of the thyristor e.g. voltage/current sharing as well as voltage and current derating for series/parallel circuits should be taken from the relevant thyristor data sheets.

Triggering into conduction of thyristors with highly inductive loads will only be possible if the current builds up well over the latching value within 20 µs.

Appropriate means of external circuitry (e.g. fly wheeling diode or resistive shunting of the load) can be adopted in situations that require these additions.

The low mark to space ratio of the pulse train (approximately 1 : 20) permits positive gate voltage during the negative half wave of the a.c. supply to the thyristor with a very slight derating of the permissible temperature of the thyristor stud.
Data sheets of the thyristors used, have to be consulted to evaluate the influence of additional reverse current losses in the actual circuit and the applicable derating.

Note: The output transformer has been designed to meet the recommendations according to B.S. 3188, viz. 3.1 kV_p for 1 min. This test voltage may only be applied to the transformer when the semiconductors are short-circuited or when they are removed from the circuit (e.g. prior to potting).

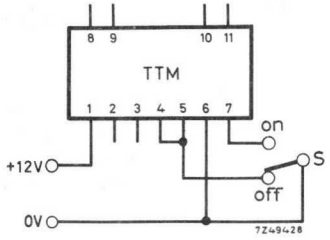
INPUT CONTROL POSSIBILITIES

Safety-catch operation

As the TTM has been supplied with a safety-catch input (terminal 7), for some applications use can be made of safety-catch operation, which gives a safeguarding against spurious trigger pulses.
If safety-catch operation is employed the TTM is controlled via two control terminals requiring phase opposition of the control voltages.
When an interference pulse will attack both control lines in phase, inadvertently triggering will be eliminated to a very large extent.
It should be noted that the employment of safety-catch operation gives a switching-time delay of the TTM of approximately 400 µs.

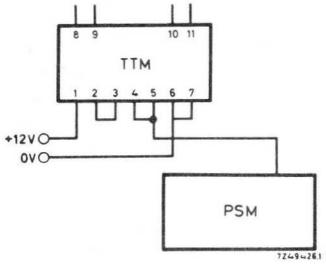
On-off control with safety-catch operation

Supply: 12 V_{dc} power supply unit
Maximum required switching capacity of the switch: 50 mA



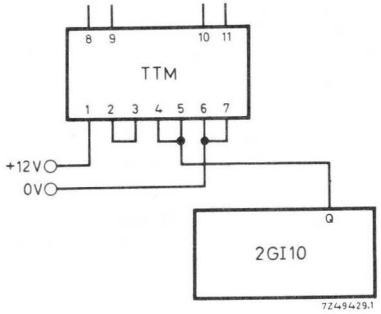
Conduction-angle control (10 - 170 °) with a phase shift module PSM, catalog number 2722 010 02001

Supply: 12 V_{dc} power supply unit



On-off control with a dual positive gate inverter 2GI 10 *

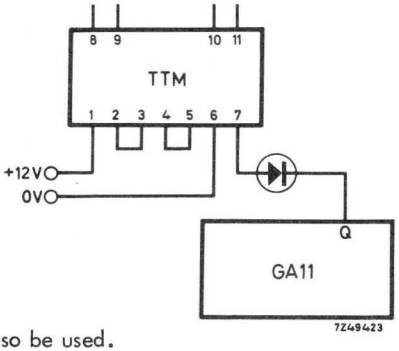
Supply: 12 V_{dc} power supply unit.
The TTM delivers trigger pulses only when the output level of the 2GI 10 is at "positive high".



Instead of the dual positive gate inverter 2GI 10, e.g. the flip-flops FF 10, FF 11, FF 12 or the pulse shaper PS 10 can be used.

On-off control with a gate amplifier GA 11

Supply: 12 V_{dc} power supply unit
Switching-time delay: 400 µs

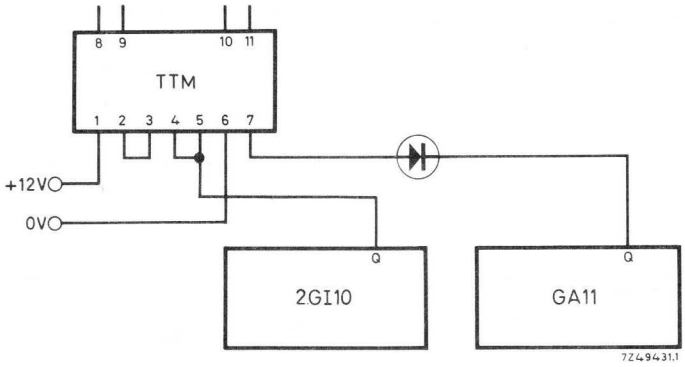


* Similar circuit block of the 20-series can also be used.

The TTM delivers trigger pulses only when the output level of the GA 11 is at "positive low".

On-off control with a dual positive gate inverter 2GI 10* and a gate amplifier GA 11, safety-catch operation

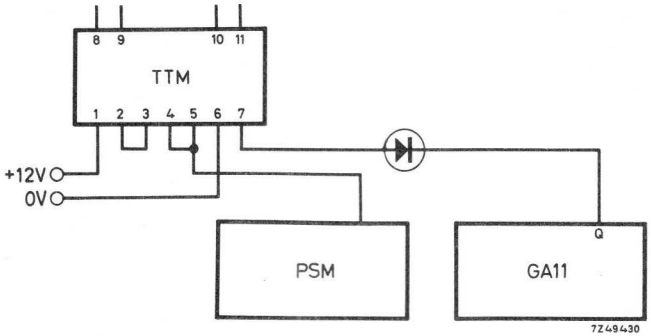
Supply: 12 V_{dc} power supply unit



The TTM delivers trigger pulses only when the output level of the 2GI 10 is at "positive high" and at the same time that of the GA 11 is at "positive low".

Conduction-angle control (10-170°) with a phase shift module PSM, and a gate amplifier GA 11, safety-catch operation

Supply: 12 V_{dc} power supply unit

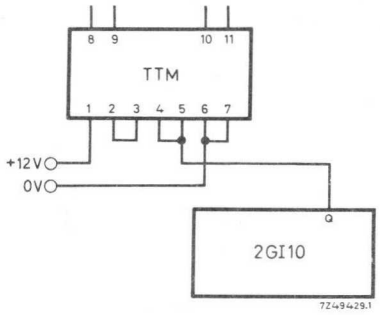


The TTM delivers trigger pulses only when the output of the GA 11 is at "positive low".

* Similar circuit block of the 20-series can also be used.

Electronic fusing facility with a dual positive gate inverter 2GI 10 *

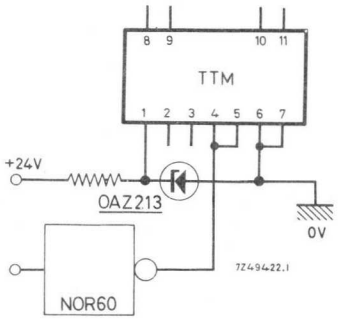
Supply: 12 V_{dc} power supply unit



As the TTM delivers trigger pulses only when the output level of the 2GI 10 (FF 10, etc.) is at "positive high", fusing is obtained by making excess thyristor current switch 2GI 10 output to zero.

On-off control with a 2.NOR 60

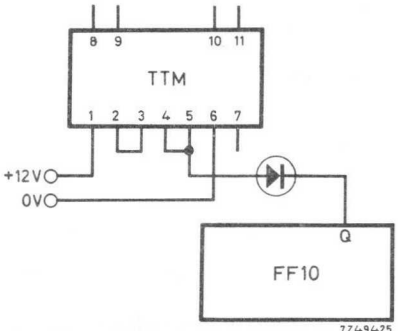
Supply: Norbit supply unit



The TTM delivers trigger pulses only when the output level of the 2.NOR 60 is high.

Single pulse output

For some applications single trigger pulse facility is of interest. This can be achieved when a suitable negative transient is available to reset a flip-flop e.g. FF 10 thereby stopping the TTM. The recovery time is approximately 500 µs.



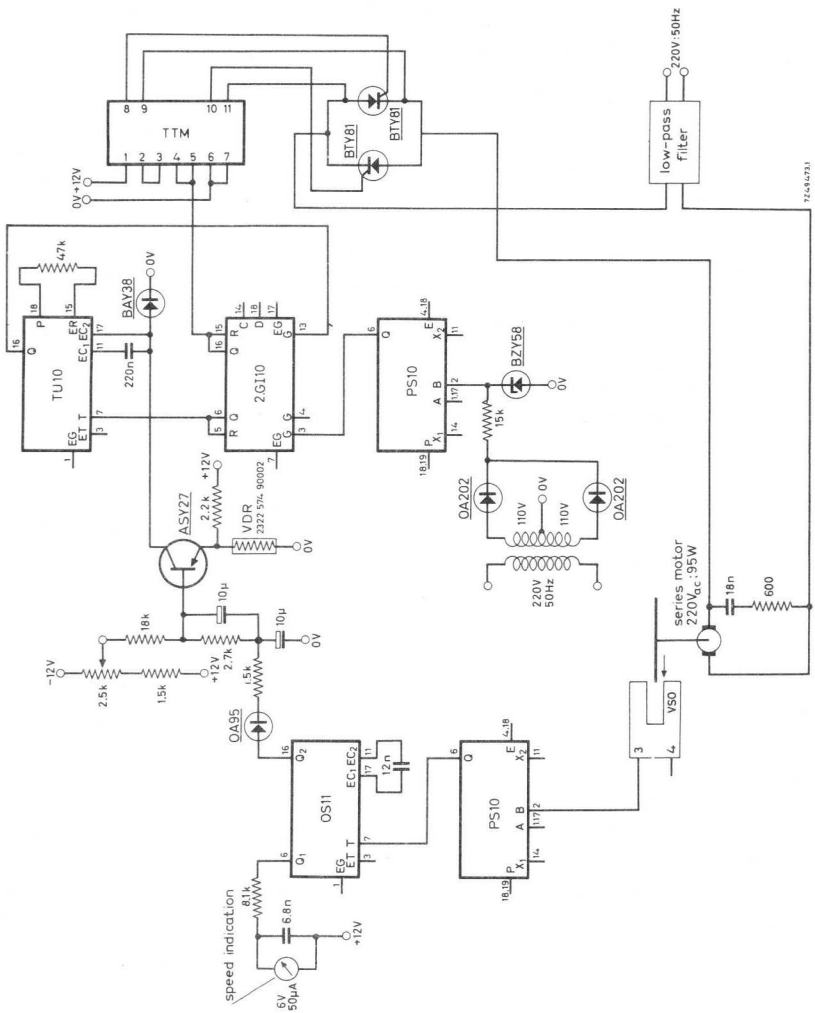
* Similar circuit block of the 20-series can also be used.

Control during a number of a.c. mains cycles

A feature in some power dosing applications can be obtained by having the output level of the 2GI 10, FF 10 etc. at "positive high" for a number of mains cycles only. This can be achieved by counting the mains "zero crossings" in a preset counter. Up on reaching the preset number, a negative going transient stops the TTM.

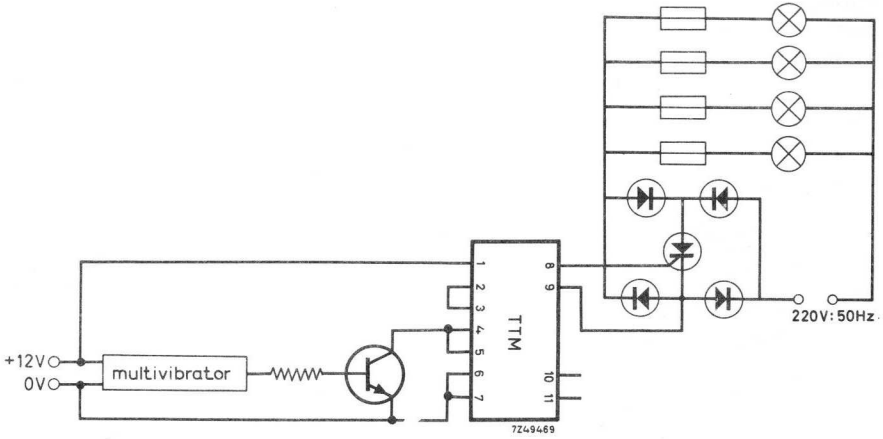
APPLICATION SUGGESTIONS

Automatic proportional speed control of an a.c. motor (see the figure on next page).
A metal disc, which has been attached to the motor shaft turns through the gap of a vane switched oscillator (VSO). In this way a pulse shaped voltage is obtained from the VSO of which the repetition frequency will be proportional to the motor speed. The output signal of the VSO drives a one-shot multivibrator (OS 11) via a pulse shaper (PS 10).
The outputs of the OS 11 give pulses with a duration of 150 μs and with a repetition frequency which is proportional to the motor speed. If this signal is integrated in the proper way the voltage level will be proportional to the frequency and so to the motor speed. The integrated signal of output Q_2 of the OS 11 gives a positive voltage level. If this voltage level is higher than a certain value preset with the potentiometer of 2.5 kΩ, the transistor ASY 27 will be cut off.
This transistor is capable to charge the external capacitor (220 nF) of the timer unit (TU 10) quickly.
The delay time of the TU 10 can vary between 1 and 11 ms, dependent on the value of the collector current of the ASY 27.
At the moment of the zero crossings of the mains voltage the TU 10 is triggered (so every 10 ms if the mains frequency is 50 Hz).
The thyristor trigger module (TTM) drives the two thyristors in the conducting state during the time the output level of the TU 10 is at "positive low" (0 V).
(Via the dual positive gate inverter 2GI 10 this gives a "positive high" signal, +12V, at the terminals 4 and 5 of the TTM).
In the case the motor speed is lower than the required value the base current of the ASY 27 increases and in turn the collector current increases too, so that the external capacitor of the TU 10 will be charged quickly. The delay time of the TU 10 decreases through which the thyristors are driven in the conducting state sooner and the motor will run faster.
Is the motor speed higher than the required value, the base current and the collector current of the ASY 27 decrease and the delay time of the TU 10 increases. Within the period of 10 ms the output level of the TU 10 will be at "positive low" during a shorter time, through which the thyristors will come in the conducting state later and the motor will run slower.


TTM
8 9 10 11
1 2 3 4 5 6 7
0V +12V
BTY81
BTY81
low-pass filter
220V 50Hz
4.7k
TU10
BAY38
0V
220n
2.G110
PS10
BZY58
15k
0V
OA202
110V
110V
220V 50Hz
OA202
ASY27
2.2k
+12V
VDR
2322 594 90002
0V
10µ
18k
10µ
0V
-12V
2.5k
1.5k
+12V
2.7k
1.5k
OA95
OS11
12n
PS10
VS0
series motor
220V$_{ac}$;95W
18n
600
speed indication
8.1k
6.8n
+12V
6V
50µA

On-off control of traffic light flasher

The multivibrator switches the TTM on and off. The switching frequency is determined by the circuit constants of the multivibrator.

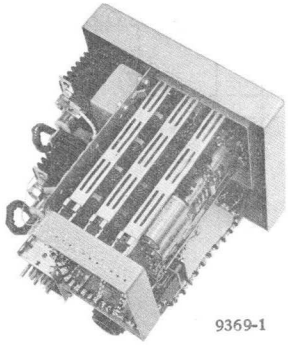


Cycle counting control for spotwelding

In the spotwelding technique it is necessary to dose accurately the energy put into the weld, especially when handling small pieces of work.

With this cycle counting control it is possible to set the welding time to 1, 2, 3 or 4 cycles of the mains.

The thyristors are controlled by a thyristor trigger module (TTM), moreover the conduction angle can be determined by connecting the output terminal of a phase shift module (PSM) to the TTM. The thyristors are conducting when the output level of the cycle counting control and the output level of the PSM are simultaneously at "positive high" (See next page).

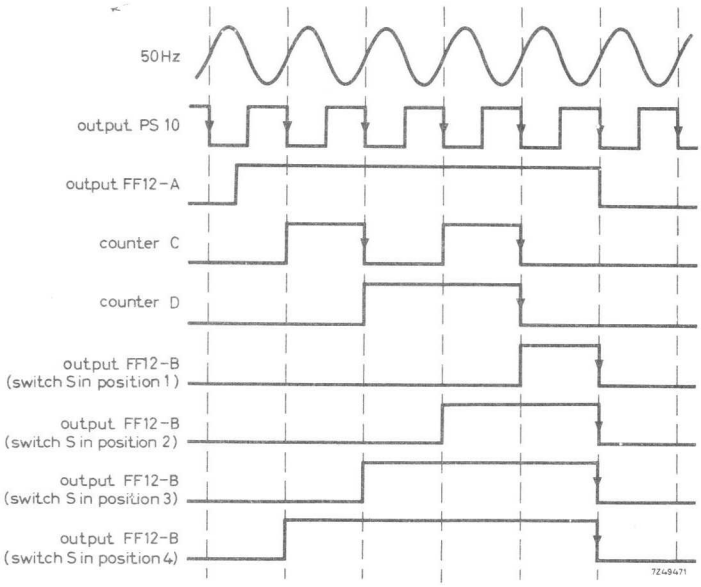


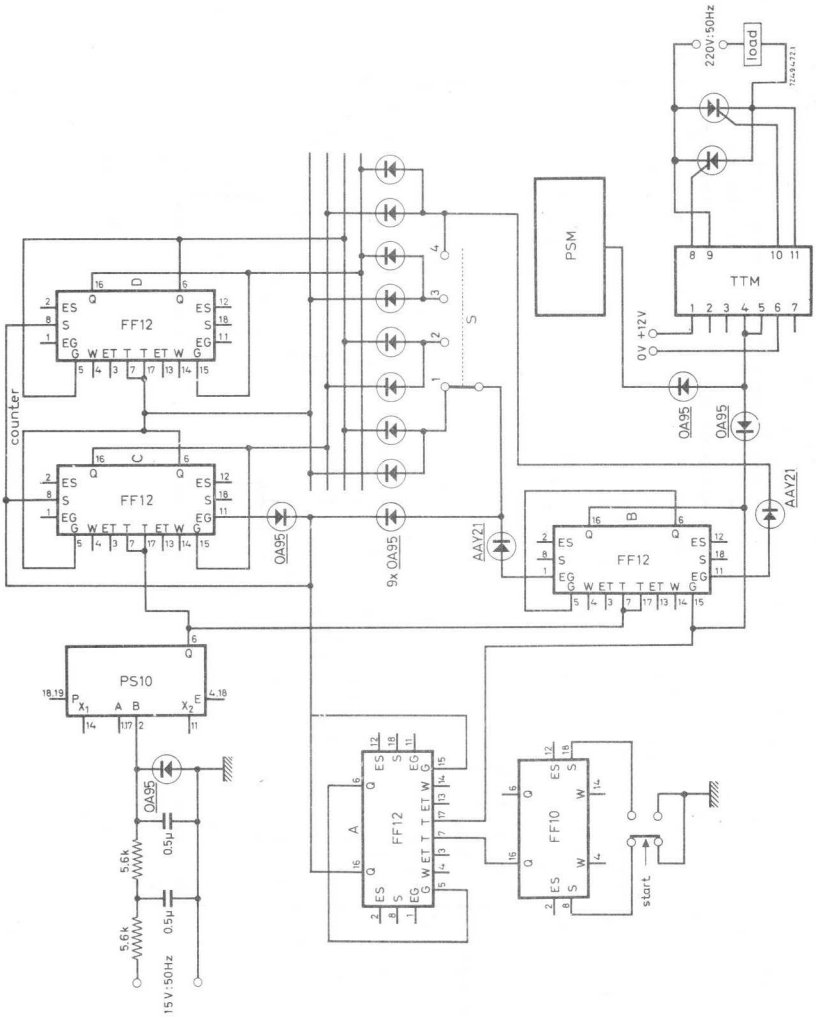
9369-1

The circuit can be started by pressing a push-botton. The flip-flop FF 10 is used to prevent the bouncing of the contacts influencing the circuit. The 50 Hz pulses are obtained from an a.c. voltage (15 V, 50 Hz), which is half-wave rectified and subsequently pulse shaped by the pulse shaper PS 10.

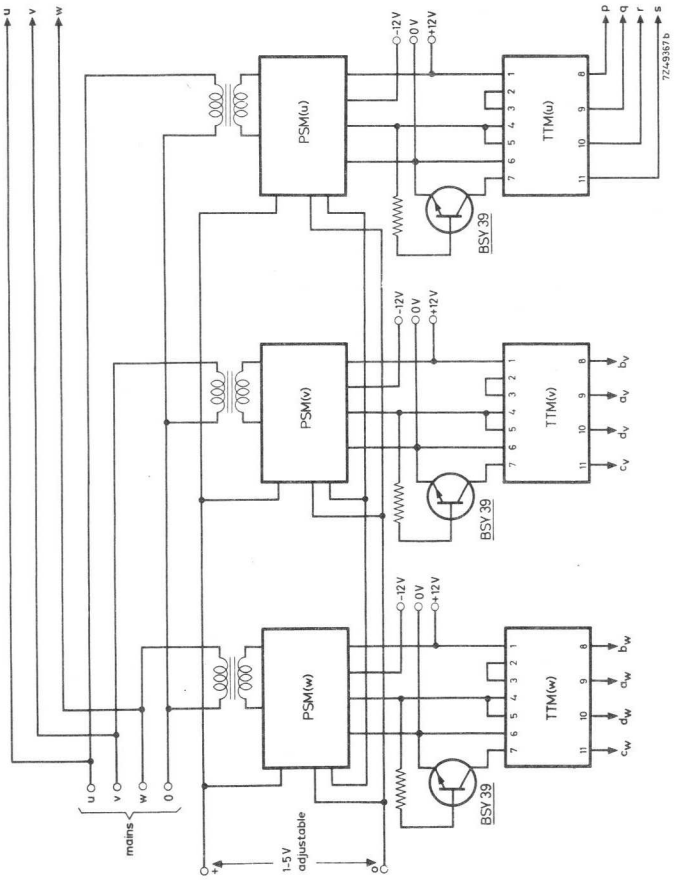
A low-pass filter is used to suppress interference signals of higher frequencies.

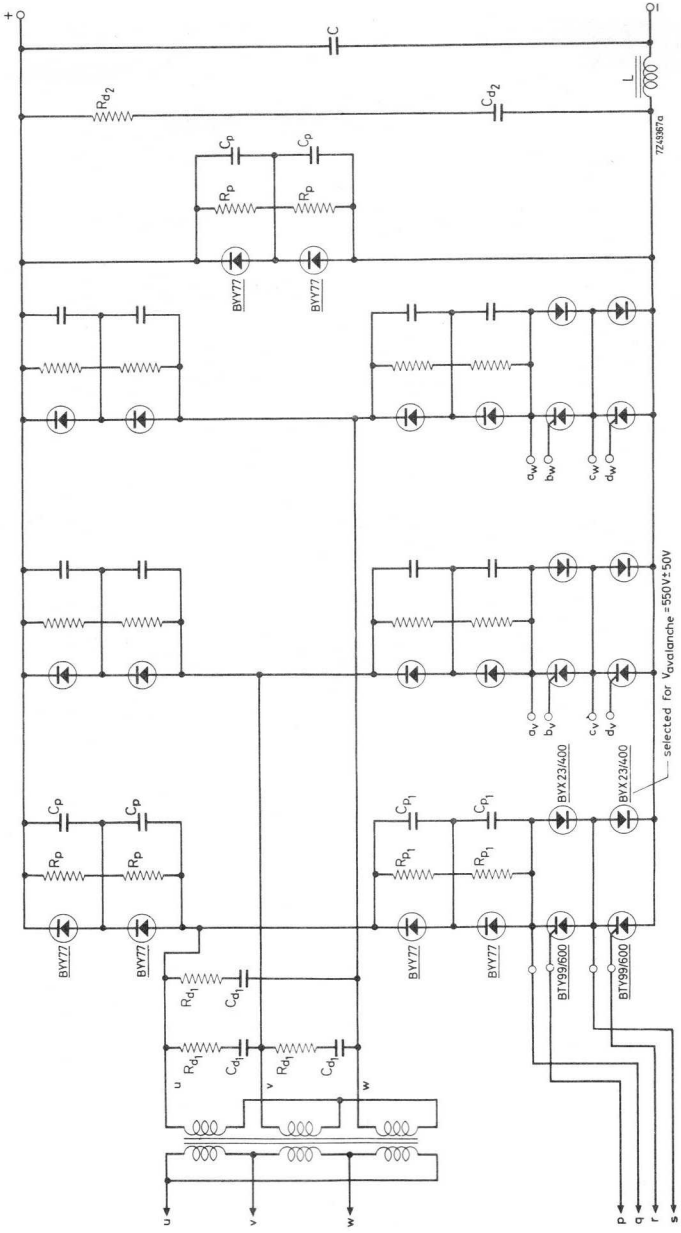
In the figure below the time sequence diagram is given. The output level of flip-flop FF 12-B is at "positive high" during 1, 2, 3 or 4 cycles when the switch is in the position 1, 2, 3 or 4 respectively.

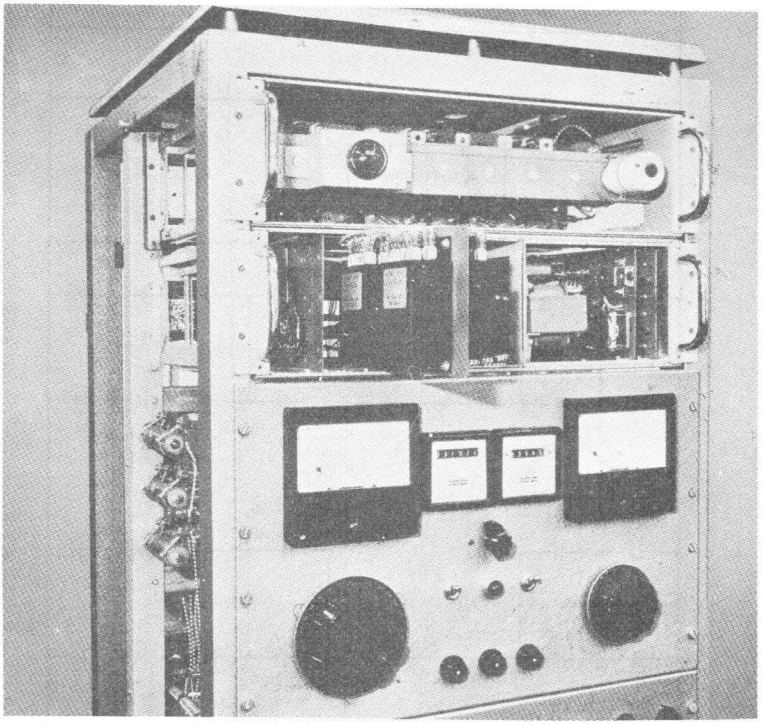



220V:50Hz
load
PSM
TTM
0V +12V
counter
FF12
FF10
PS10
OA95
AAY21
9x OA95
5.6k
0.5µ
15V:50Hz
start

Power supply for transmitter, 800 V_{dc}, 8.5 A



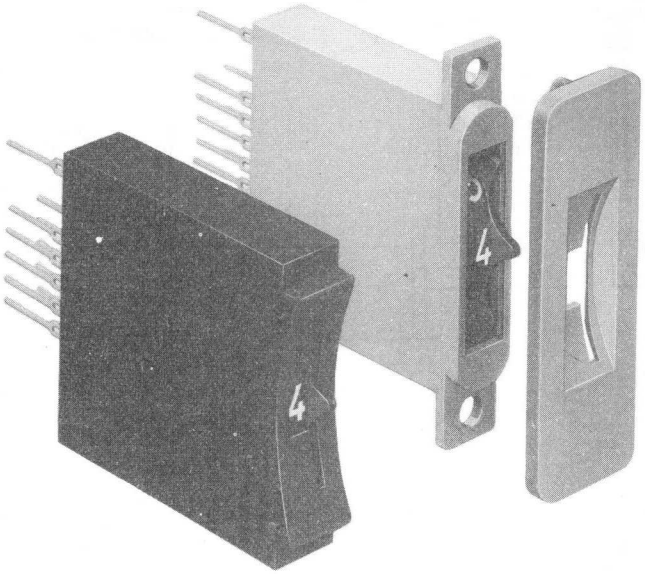

+
−
C
L
R_{d_2}
C_{d_2}
C_p
R_p
BYY77
BYX 23/400
BTY99/600
C_{p_1}
R_{p_1}
R_{d_1}
C_{d_1}
u
v
w
p
q
r
s
a_w
b_w
c_w
d_w
a_v
b_v
c_v
d_v
selected for $V_{avalanche}$ = 550V ± 50V
7249870a



A 48839-2

Power control unit.
Thyristors triggered by 4 TTM's are used for mains switching.

THUMBWHEEL SWITCHES



2428A

Contact resistance	≤ 50 mΩ
Operating temperature range	−25 to +85 °C.

APPLICATION

These thumbwheel switches have been developed to be used as pre-set devices in digital control systems in which numerical information is handled.

CONSTRUCTION

Housing	shock resistant polycarbonate colour: grey (facade mounting) black (block mounting)
Contact springs	heat-treated copper beryllium
Contact surface	721 rolled alloy (70% gold, 20% silver, 10% copper)
Terminals	tinplated brass suited for soldering or mini wire-wrap
Thumbwheel	high grade plastic, colour black; provided with white figures or signs
Thumbwheel detent	copper beryllium spring with low wear molybdenum bisulfide doped snap
Printed wiring boards	glass-epoxy; goldplated tracks
Type identification	catalog number is given on the closing strip at the rear, type abbreviation on housing

Dimensions in mm

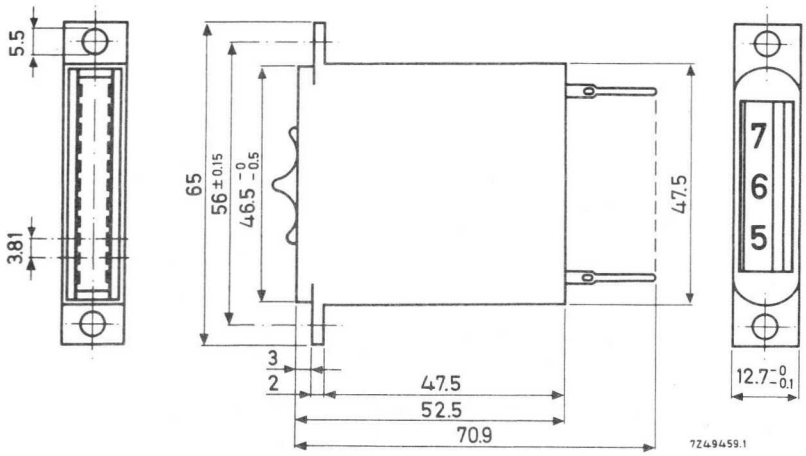


Fig.1. Switch for facade mounting.

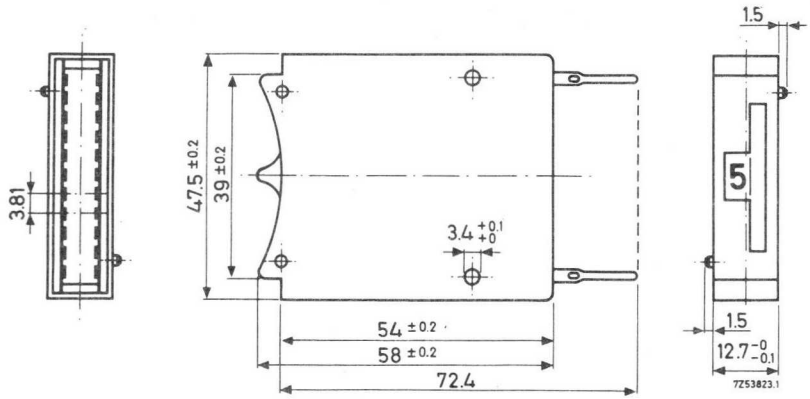


Fig.2. Switch for block mounting.

TECHNICAL PERFORMANCE

Working voltage	50 V_{dc}
Test voltage for 1 min *)	500 V_{dc}
Insulation resistance, measured at 100 V_{dc} *)	$\geq 10^8\ \Omega$
Current switching capacity in purely resistive circuits	0.1 A_{dc}

*) Between any pair of terminals and between any terminal and all others connected together.

Maximum current carrying capacity	0.5 A_{dc}
Contact resistance measured at 20 mV, 0.1 A, 1 kHz	$\leq$ 50 mΩ
Losses (tan δ), measured at 1 MHz between any terminal and all others connected together to earth	$\leq 25.10^{-4}$
Capacitance, measured at 1 MHz between any pair of terminals and between any terminal and all others connected together to earth	$\leq$ 15 pF
Operating temperature range	-25^{o} to 85 ^{o}C
Storage temperature range	-40^{o} to 85 ^{o}C
Humidity	in conformity with IEC 68, test C, 21 days
Life	in excess of 100 000 complete rotations, at a rate of 1 step/s
Operating torque	250 to 750 gcm
ater 20 000 rotations	150 to 650 gcm
Dimensions of the figures on the thumbwheel	6 x 4 mm, line thickness 0.8 mm
Weight	approximately 30 g

FACADE MOUNTING

The switches can be mounted in panels with a thickness up to 4 mm by means of mounting façades and the screws and washers supplied (see Fig.3.) When the panel thickness is less than 4 mm, additional washers must be used between the panel and the switch. The following mounting façades, giving facilities for mounting up to 10 switches, are available (Fig.4).

mounting façade	number of switches	catalog number
FMF 1	1	4311 027 80598
FMF 2	2	4311 027 80608
FMF 3	3	4311 027 80618
FMF 4	4	4311 027 80628
FMF 5	5	4311 027 80638
FMF 6	6	4311 027 80648
FMF 7	7	4311 027 81163
FMF 8	8	4311 027 81173
FMF 9	9	4311 027 81183
FMF10	10	4311 027 81193

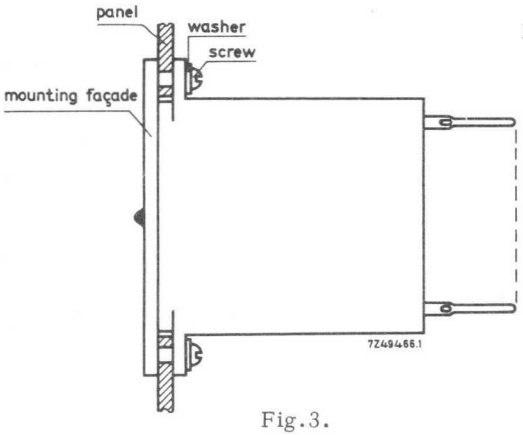
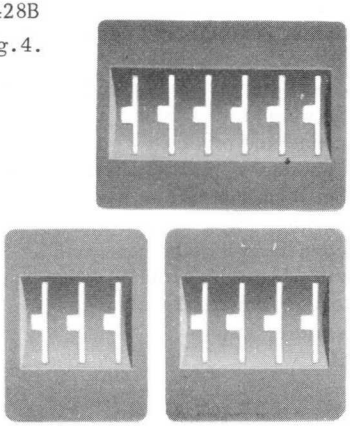


Fig.3.

2428B

Fig.4.



The dimensions of the necessary panel holes are indicated in Fig.5; the outline of the mounting façade is indicated by a dash line.

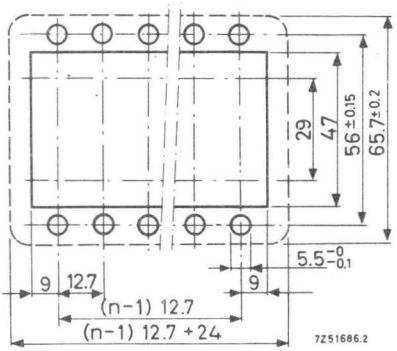


Fig.5. (n = number of switches)

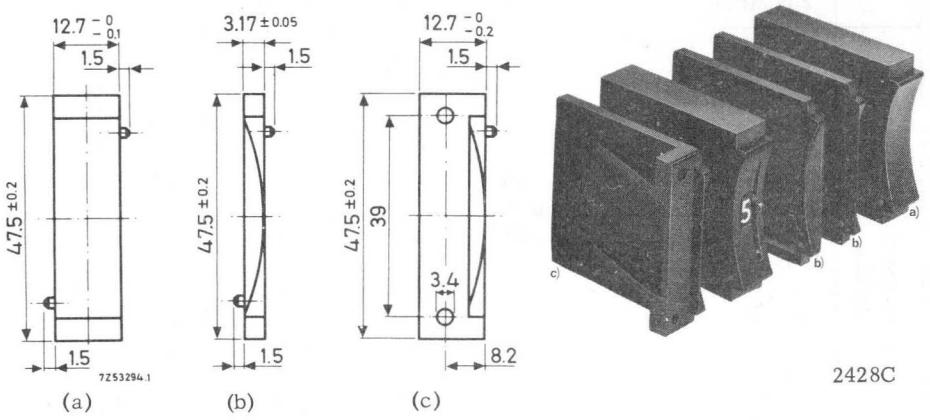
BLOCK MOUNTING

Type BM switches, which do not require a front façade, can be "block mounted" by means of mounting brackets and 3 mm tie rods, and can be supplied coupled in master-slave arrangements. Accessories include:

a) BM CLO, catalog number 4311 027 82141
(a blank housing suitable as distance piece for future extension, for housing slave switches or ancillary circuits, or for engraving)

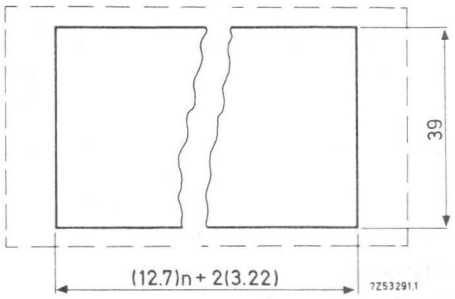
b) BM SEP, catalog number 4311 027 82161
(a spacer suitable for left and right hand mounting)

c) BM EXT, catalog number 4311 027 82151
(end piece suitable for left and right hand mounting)



(a) (b) (c)

Fig.6. Spacers and end piece



(n = number of switches)

Fig.7. Panel cut-out

SURVEY OF TYPES

	description	abbreviation	index	catalog no. 4311 027 ..... facade mounting	catalog no. 4311 027 ..... block mounting
decimal and 2 position switches	10 position 2 pole switch	10P2C	0 - 9	82201	82521
	10 position 1 pole switch	10P1C	0 - 9	82321	82401
	2 position 4 pole sign switch	2P4+ -	+, -	82231	82641
	2 position 2 pole sign switch	2P2+ -	+, -	82341	82601
	2 position 4 pole sign switch	2P4x ÷	x, ÷	82311	82651
	2 position 2 pole sign switch	2P2x ÷	x, ÷	82351	82611
	2 position 4 pole sign switch	2P401	0.1	82281	82661
	2 position 2 pole sign switch	2P201	0.1	82361	82501
	2 position 4 pole sign switch	2P4MA	M, A *)	82291	82671
	2 position 2 pole sign switch	2P2MA	M, A *)	82371	82621
	2 position 4 pole sign switch	2P4AvAr	Av, Ar **)	82301	82681
	2 position 2 pole sign switch	2P2AvAr	Av, Ar **)	82381	82631
binary decoding switches (including 4 diodes BAX13 and a resistor of 12 kΩ)	decoding switch 1248 negative logic	1248N	0 - 9	82221	82391
	decoding switch 1248 positive logic	1248P	0 - 9	82251	82411
	decoding switch 1242 (jump at 8) negative logic (Berkeley code)	1242N	0 - 9	82211	82711
	decoding switch 1242 (jump at 8) positive logic (Berkeley code)	1242P	0 - 9	82241	82721
	decoding switch 1248 negative logic ***)	1248N/C	0 - 9	82451	82541
	decoding switch 1248 positive logic ***)	1248P/C	0 - 9	82431	82551
	decoding switch 1242 (jump at 8) negative logic ***)	1242N/C	0 - 9	82441	82571
	decoding switch 1242 (jump at 8) positive logic ***)	1242P/C	0 - 9	82421	82581
	decoding switch 2 out of 5 + 2 out of 2	2522	0 - 9 plus blank		82771
binary coding switches	coding switch 1248	1248C	0 - 9	82271	82531
	coding switch 1242 (jump at 8)	1242C	0 - 9	82261	82701
	coding switch 1248 ****)	1248C/C	0 - 9	82471	82561
	coding switch 1242 (jump at 8)****)	1242C/C	0 - 9	82461	82591
	coding switch 1248	1248S	0 - 9		82511

Note: The contacts of all switches break before make.

*) "Start" and "Stop" for latin-based languages.

**) "Forward" and "Reverse" for latin-based languages.

***) Switch decodes 9-complement of decimal digit on thumbwheel.

****) Switch encodes 9-complement of decimal digit on thumbwheel.

DIAGRAMS AND TERMINAL LOCATION

10P2C

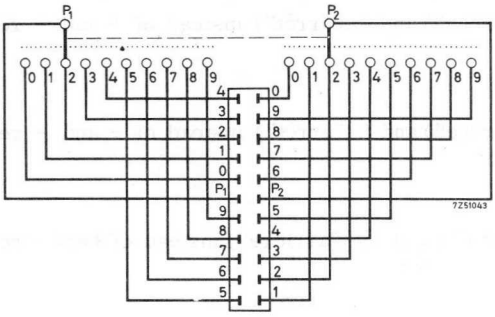


Fig. 9

10P1C

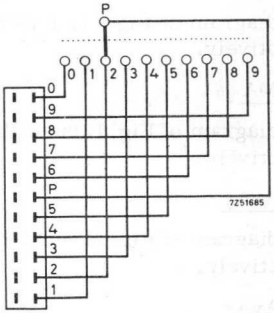


Fig. 10

2P4+−

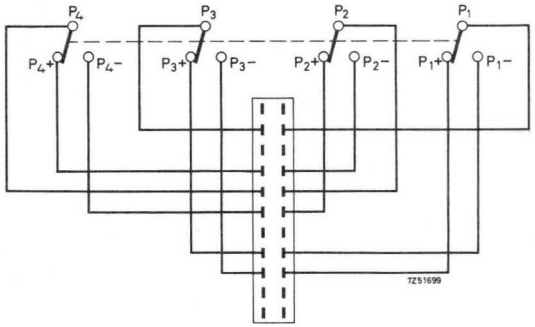


Fig. 11

2P2+−

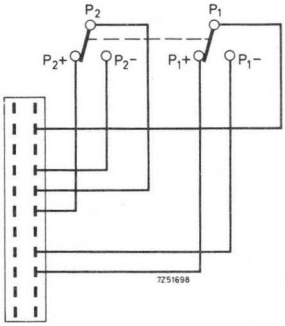


Fig. 12

2P4 x ÷

As diagram of Fig. 11 but with x and ÷ instead of + and − respectively.

2P2 x ÷

As diagram of Fig. 12 but with x and ÷ instead of + and − respectively.

2P401

As diagram of Fig. 11 but with 0 and 1 instead of + and − respectively.

2P201

As diagram of Fig. 12 but with 0 and 1 instead of + and − respectively.

2P4MA

As diagram of Fig. 11 but with M ("marche") and A ("arrêt") instead of + and − respectively.

2P2MA

As diagram of Fig. 12 but with M ("marche") and A ("arrêt") instead of + and − respectively.

2P4AvAr

As diagram of Fig. 11 but with Av ("avant") and Ar ("arrière") instead of + and − respectively.

2P2AvAr

As diagram of Fig. 12 but with Av ("avant") and Ar (arrière") instead of + and − respectively.

1248N

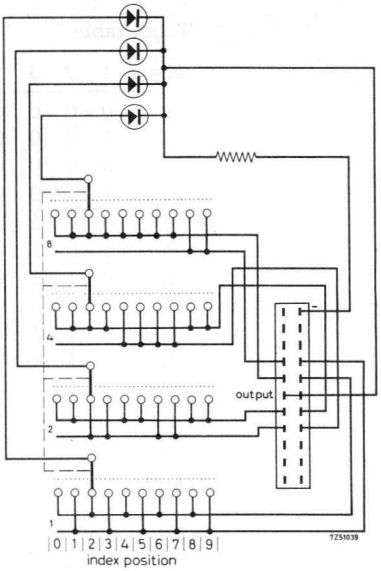


Fig.13

Truth table

Index	1	2	4	8
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

1248P

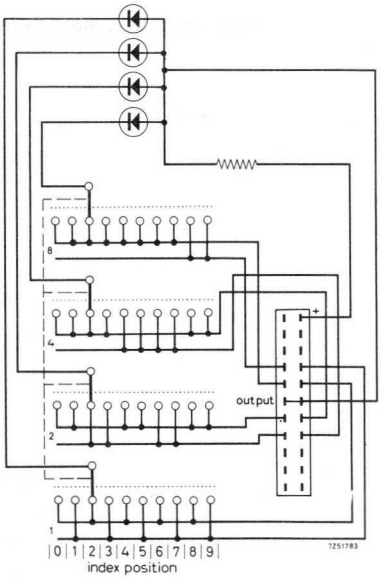


Fig.14

For truth table, see above

1242N

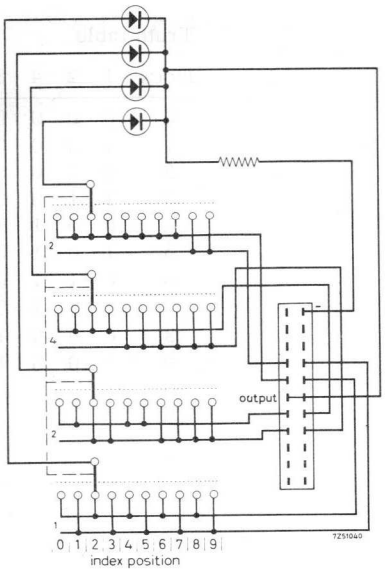


Fig.15

Truth table

Index	1	2	4	2
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	1	1	1
9	1	1	1	1

1242P

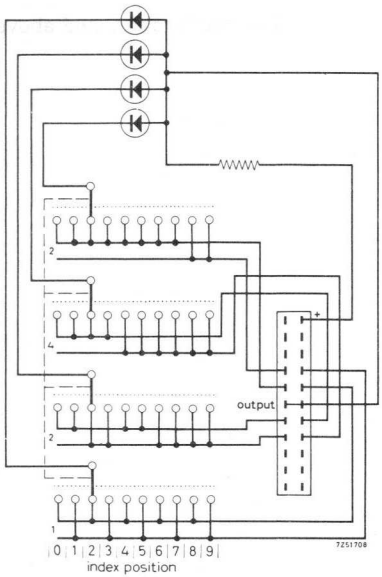


Fig.16

For truth table, see above

1248N/C

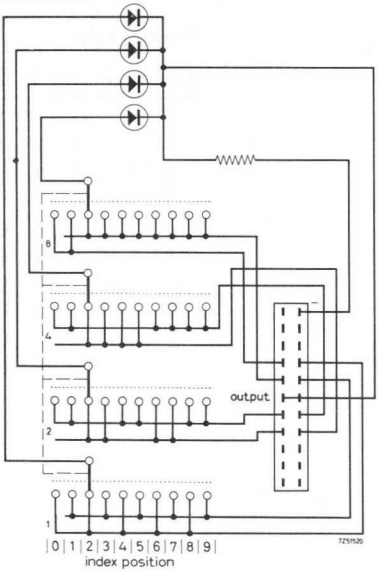


Fig.17

Truth table

Index	1	2	4	8
0	1	0	0	1
1	0	0	0	1
2	1	1	1	0
3	0	1	1	0
4	1	0	1	0
5	0	0	1	0
6	1	1	0	0
7	0	1	0	0
8	1	0	0	0
9	0	0	0	0

1248P/C

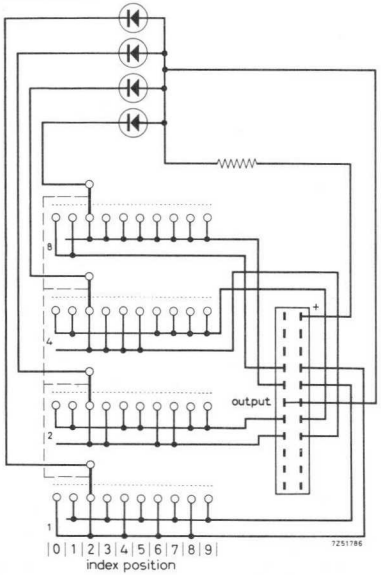


Fig.18

For truth table, see above

1242N/C

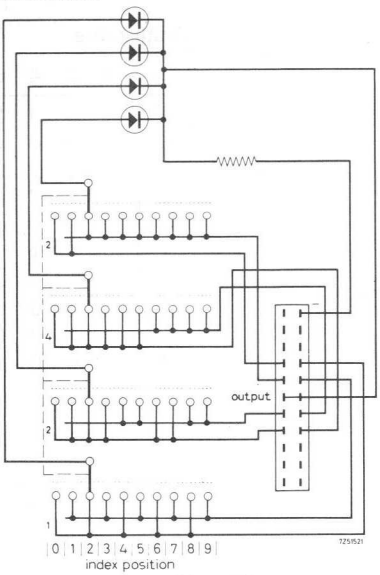


Fig.19

Truth table

Index	1	2	4	2
0	1	1	1	1
1	0	1	1	1
2	1	1	1	0
3	0	1	1	0
4	1	0	1	0
5	0	0	1	0
6	1	1	0	0
7	0	1	0	0
8	1	0	0	0
9	0	0	0	0

1242P/C

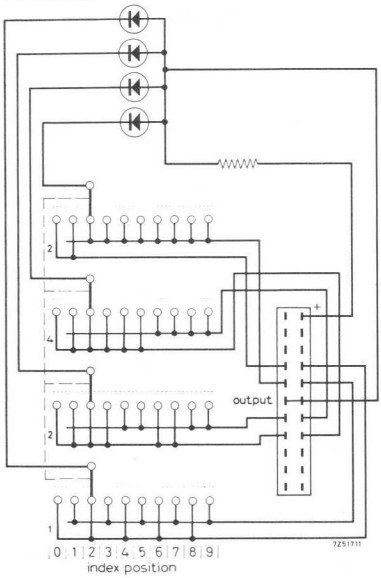


Fig.20

For truth table, see above

2522

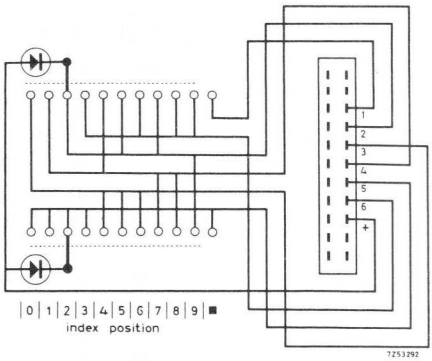


Fig.21

Truth table

Index	5	4	2	6	3	1	+
0	1	0	0	0	1	0	0
1	1	1	0	0	0	0	0
2	1	0	1	0	0	0	0
3	1	0	0	1	0	0	0
4	0	1	0	0	1	0	0
5	0	0	1	0	1	0	0
6	0	0	0	1	1	0	0
7	0	1	1	0	0	0	0
8	0	1	0	1	0	0	0
9	0	0	1	1	0	0	0
■	1	0	0	0	0	1	0

1248C

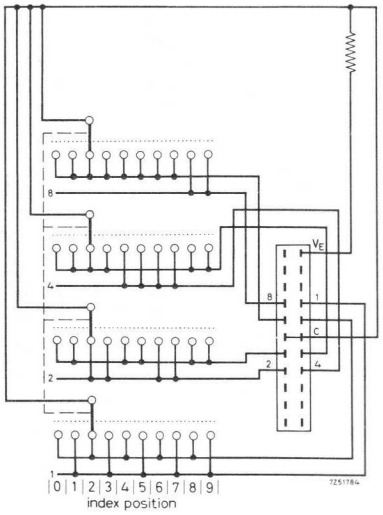


Fig.22

Truth table

Index	1	2	4	8
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

1242C

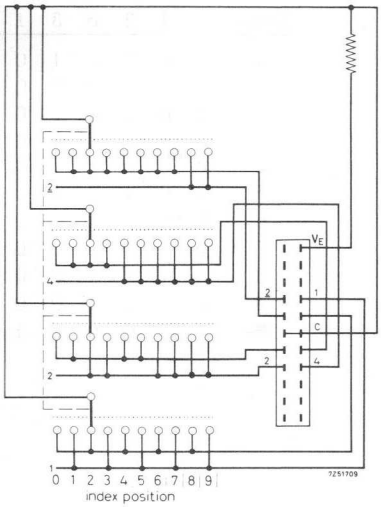


Fig.23

Truth table

Index	1	2	4	2
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	1	1	1
9	1	1	1	1

1248C/C

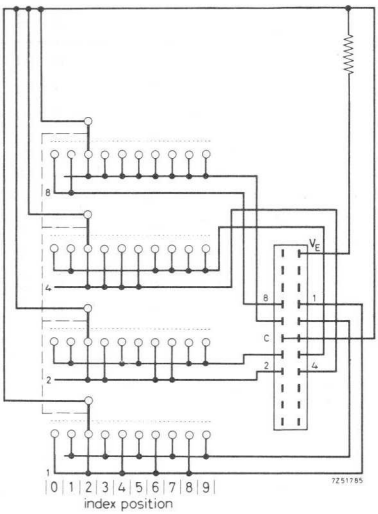


Fig.24

Truth table

Index	1	2	4	8
0	1	0	0	1
1	0	0	0	1
2	1	1	1	0
3	0	1	1	0
4	1	0	1	0
5	0	0	1	0
6	1	1	0	0
7	0	1	0	0
8	1	0	0	0
9	0	0	0	0

1242C/C

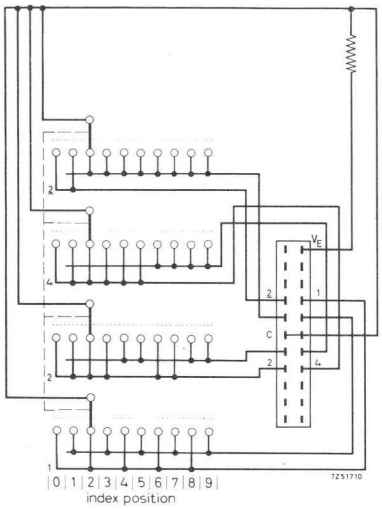


Fig.25

Truth table

Index	1	2	4	2
0	1	1	1	1
1	0	1	1	1
2	1	1	1	0
3	0	1	1	0
4	1	0	1	0
5	0	0	1	0
6	1	1	0	0
7	0	1	0	0
8	1	0	0	0
9	0	0	0	0

1248S

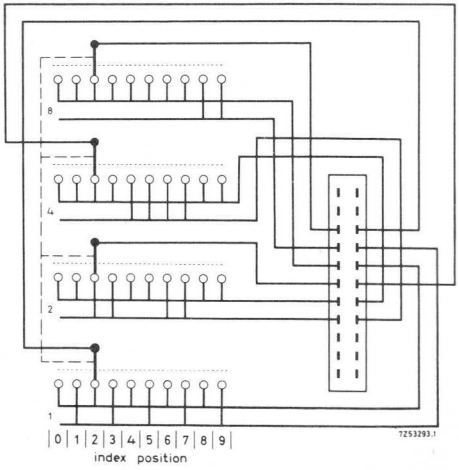
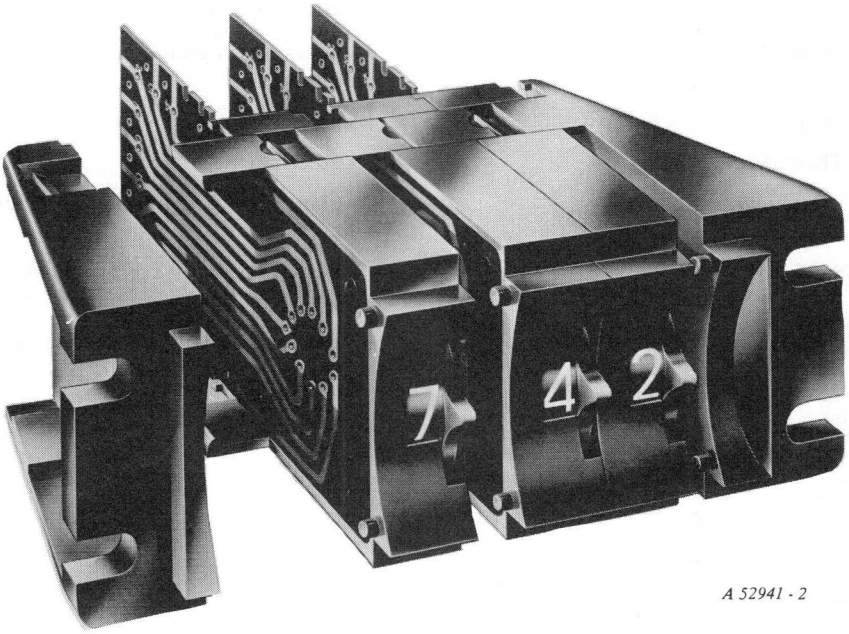


Fig.26

Truth table

Index	1	2	4	8
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

MINIATURE THUMBWHEEL SWITCHES



A 52941 - 2

Contact resistance	≤ 100 mΩ
Operating temperature range	−25 °C to +70 °C

APPLICATION

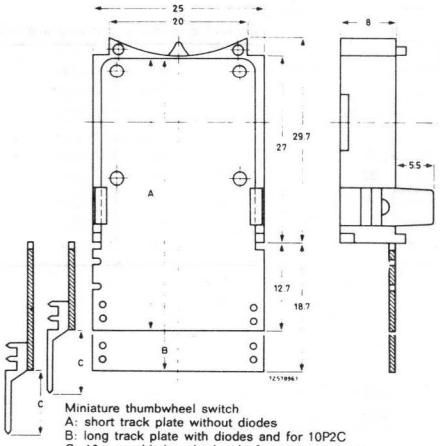
These miniature thumbwheel switches have been developed for use as preset devices in digital systems which have to handle numerical data.

The dimensions are considerably smaller than those of standard switches and allow for easy operation.

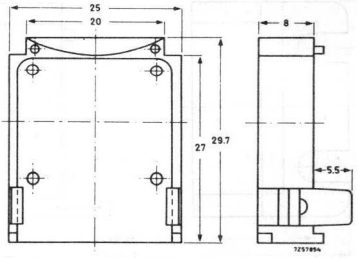
CONSTRUCTION

Housing	black shock-resistant polycarbonate
Contact springs	heat-treated copper beryllium
Contact surface	721 alloy balls (70% gold, 20% silver, 10% copper)
Terminals	holes or tin plated pins for wire wrapping
Thumbwheel	polycarbonate
Thumbwheel detent	steel spring
Printed-wiring board	glass epoxy, gold plated tracks on nickel
Stacking	switch housings are provided with "snap in" hooks to eliminate tie bolts
Type identification	catalogue number suffix is given on the rear of the switch, type abbreviation on top of the housing

Dimensions in mm



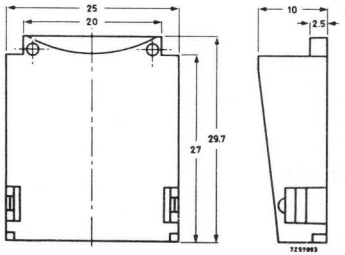
Miniature thumbwheel switch
A: short track plate without diodes
B: long track plate with diodes and for 10P2C
C: 10 mm added to the height for mini-wrap pins



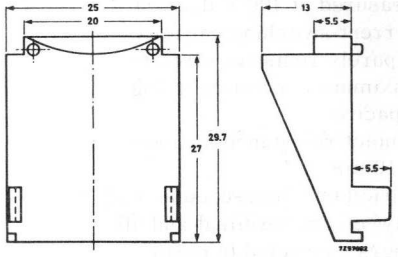
Spacer

Dimensions in the drawings are in mm

mm	inches	mm	inches
2.5	0.098	18.7	0.736
5.5	0.217	20	0.787
8	0.315	25	0.984
10	0.394	27	1.063
12.7	0.500	29.7	1.169
13	0.512		

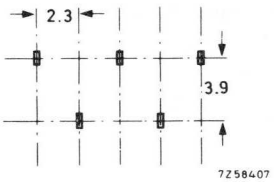


Female end piece (to left of operator)



Male end piece (to right of operator)

Terminal pitch (complementary types)

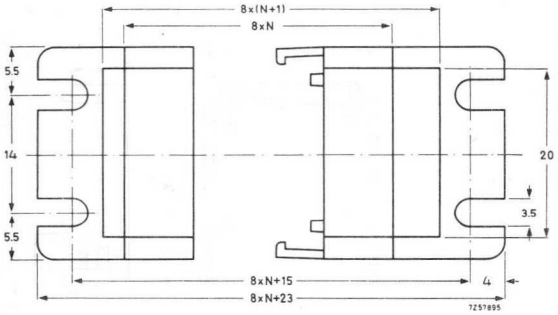


2.3 mm = 0.091 inch
3.9 mm = 0.154 inch

Weight approx. 7 g

Numerals size 5 x 3 mm
line thickness 0.6 mm

Mounting



N = number of switches + spacers

Dimensions in the drawing are in mm

mm	inches
3.5	0.138
4	0.158
5.5	0.217
8	0.315
14	0.551
15	0.591
20	0.787
23	0.906

TECHNICAL PERFORMANCE

Working voltage	60 V d.c.
Test voltage for 1 min. *)	500 V d.c.
Dielectric strength at air pressure of 20 mbar	400 V d.c.
Insulation resistance, measured at 100 V d.c. *)	$> 10^9\ \Omega$
Current switching capacity in purely resistive circuits	0.1 A d.c.
Maximum current carrying capacity	2 A d.c.
Contact resistance measured at 10 mA	< 100 mΩ
Capacitance measured at 1 MHz between one terminal and all others connected to earth	< 10 pF
Standard gate resistor	3900 Ω
Operating temperature range	−25 °C to +70 °C
Storage temperature range	−40 °C to +85 °C
Life	in excess of 100000 complete rotations at a rate of 1 step/s
Operating torque	100 to 200 gcm

Quality control tests:
IEC 68, test A (cold)
test B (dry heat)
test C (damp heat)
test F (vibration)

*) Between any pair of terminals and between any terminal and all others connected together.

SURVEY OF TYPES

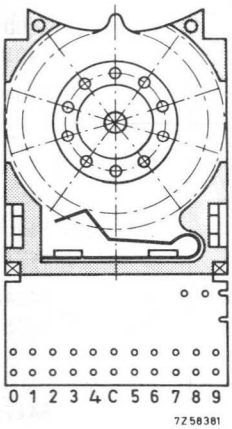
Description	Type *)	Catalogue number
Decimal switches		
10 position 1 pole switch	M 10P1C	4311 027 84001
	MW 10P1C	84011
10 position 2 pole switch	M 10P2C	84041
Binary switches		
Decoding types:		
decoding switch 1.2.4.8, negative logic, with complement	M 1248/NC	4311 027 84201
	MW 1248/NC	84211
decoding switch 1.2.4.8, positive logic, with complement	M 1248/PC	84241
	MW 1248/PC	84251
Encoding types:		
encoding switch 1.2.4.8	MW 1248	84171
encoding switch 1.2.4.8, with complement	M 1248/C	84161
	MW 1248/C	84291
encoding switch 1.2.4.8, with isolating diodes for negative logic	M 1248/N	84081
	MW 1248/N	84091
encoding switch 1.2.4.8, with isolating diodes for positive logic	M 1248/P	84121
	MW 1248/P	84131
Mounting accessories		
Male end piece (to right of operator)		4311 027 84321
Female end piece (to left of operator)		84331
Spacer		84591

Note: The contacts of all switches break before make.

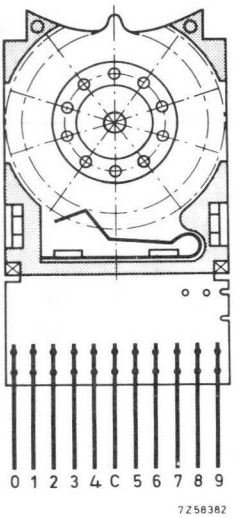
*) Terminal style: M = without pins (solder direct to track plate)
MW = with pins (for wire wrapping)

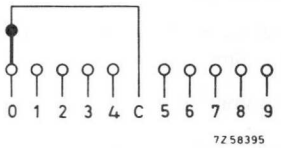
DIAGRAMS AND TERMINAL LOCATION

M10P1C

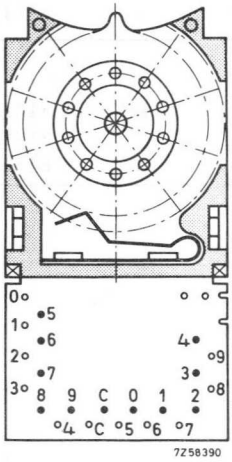


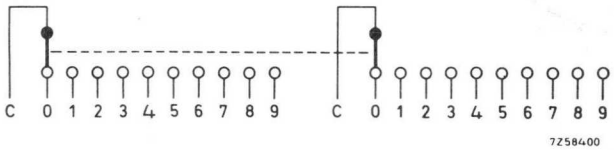
MW10P1C



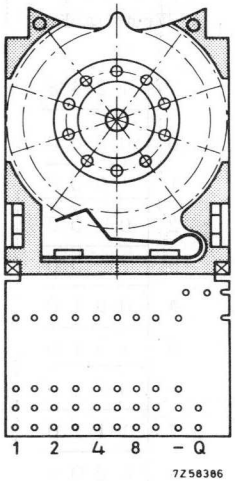


M10P2C

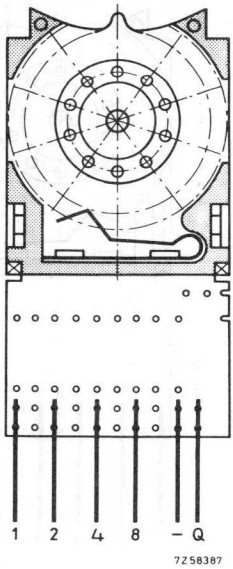




M1248/N

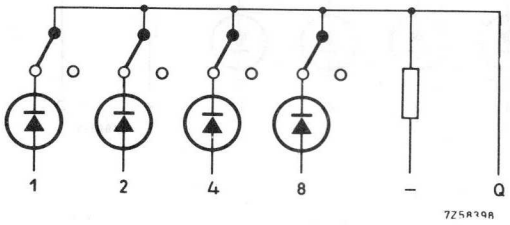


MW1248/N

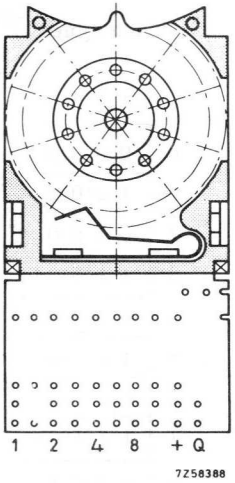


Truth table

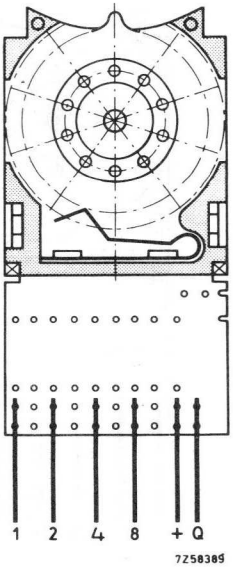
	1 2 4 8
0	0 0 0 0
1	1 0 0 0
2	0 1 0 0
3	1 1 0 0
4	0 0 1 0
5	1 0 1 0
6	0 1 1 0
7	1 1 1 0
8	0 0 0 1
9	1 0 0 1



M1248/P

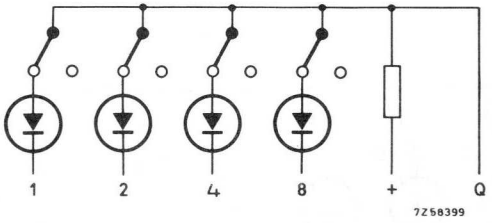


MW1248/P

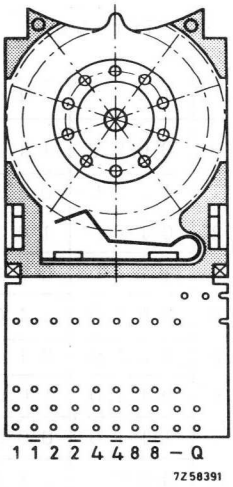


Truth table

	1 2 4 8
0	0 0 0 0
1	1 0 0 0
2	0 1 0 0
3	1 1 0 0
4	0 0 1 0
5	1 0 1 0
6	0 1 1 0
7	1 1 1 0
8	0 0 0 1
9	1 0 0 1



M1248/NC



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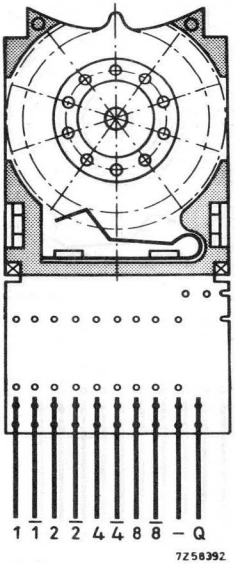

Truth table

	1 2 4 8	$\bar{1}$ $\bar{2}$ $\bar{4}$ $\bar{8}$
0	0 0 0 0	1 1 1 1
1	1 0 0 0	0 1 1 1
2	0 1 0 0	1 0 1 1
3	1 1 0 0	0 0 1 1
4	0 0 1 0	1 1 0 1
5	1 0 1 0	0 1 0 1
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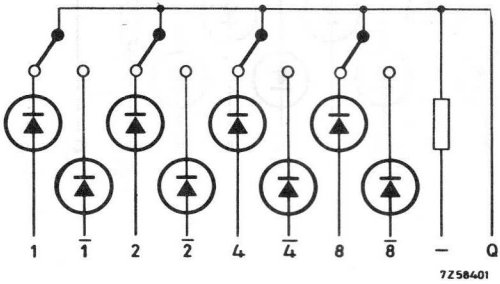
7	1 1 1 0	0 0 0 1
8	0 0 0 1	1 1 1 0
9	1 0 0 1	0 1 1 0



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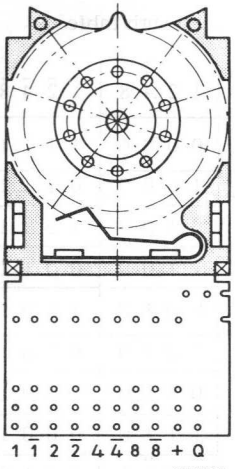

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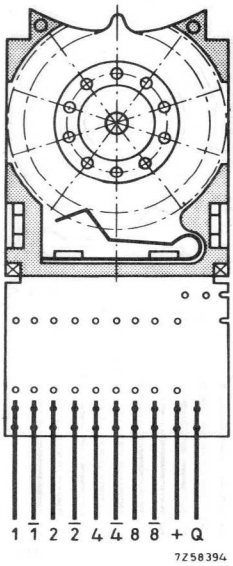

Truth table

	1 2 4 8	1̄ 2̄ 4̄ 8̄
0	0 0 0 0	1 1 1 1
1	1 0 0 0	0 1 1 1
2	0 1 0 0	1 0 1 1
3	1 1 0 0	0 0 1 1
4	0 0 1 0	1 1 0 1
5	1 0 1 0	0 1 0 1
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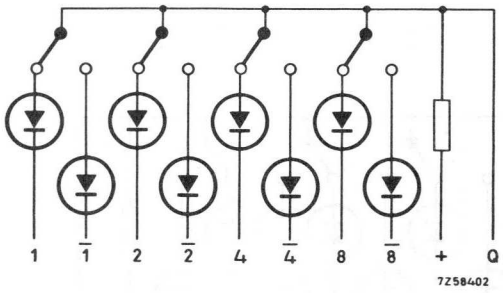

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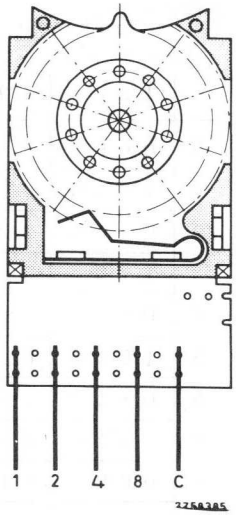

Truth table

	1	2	4	8
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
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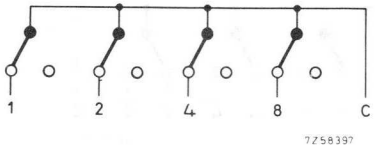

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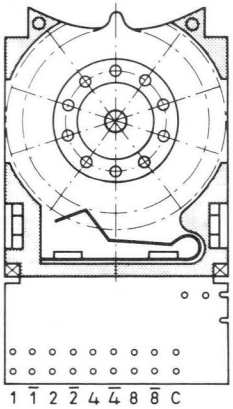

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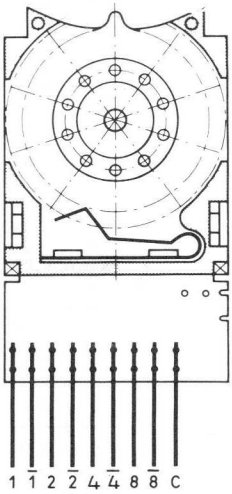

Truth table

	1 2 4 8	$\bar{1}$ $\bar{2}$ $\bar{4}$ $\bar{8}$
0	0 0 0 0	1 1 1 1
1	1 0 0 0	0 1 1 1
2	0 1 0 0	1 0 1 1
3	1 1 0 0	0 0 1 1
4	0 0 1 0	1 1 0 1
5	1 0 1 0	0 1 0 1
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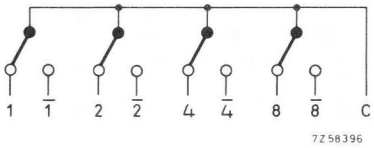

CONTENTS

INPUT/OUTPUT DEVICES

Printed in The Netherlands

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