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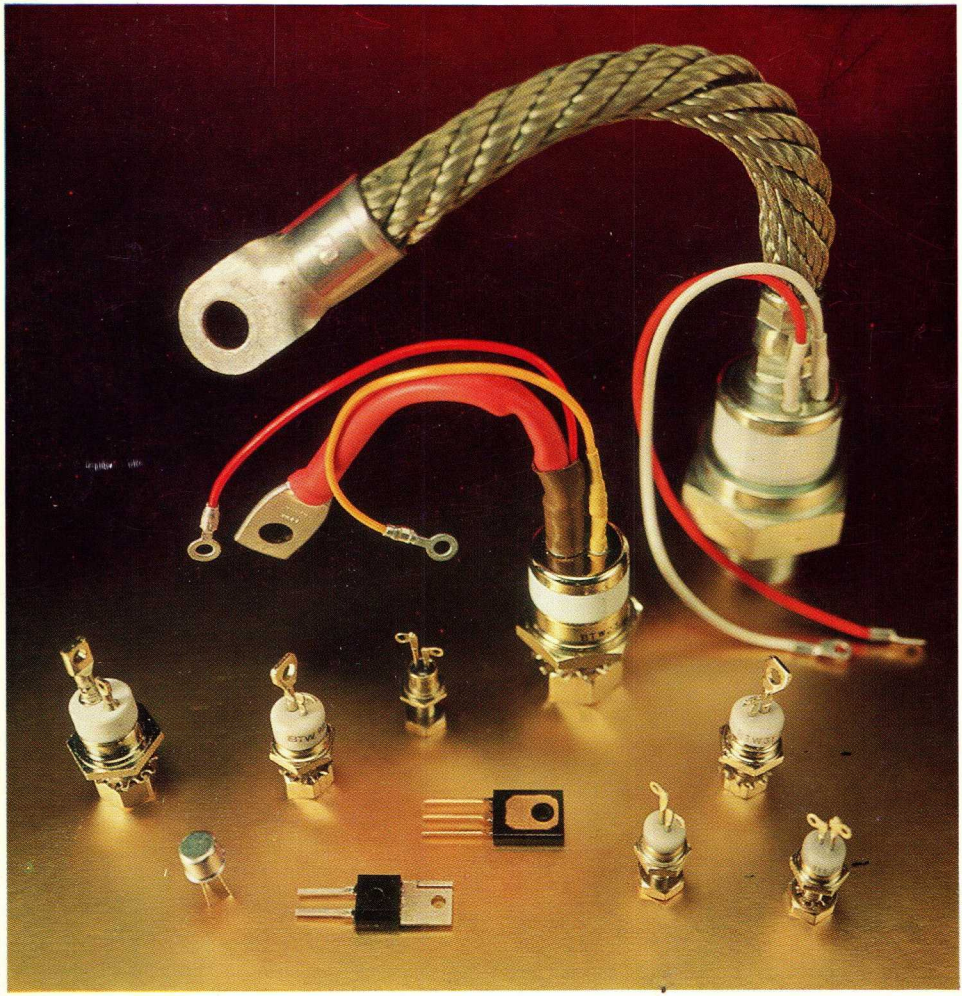
THYRISTORS



Thyristors

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Contents

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List of Main Symbols used in the Text

This list does not contain all symbols used in the book; it contains the majority, however, including the standard thyristor parameters (V_{RRM}, $V_{(BR)R}$ etc.) which are used but not always defined in the text.

a_t	total heat dissipation area
f_a	altitude correction factor (free convection)
f_p	position correction factor (free convection)
f_r	radiation form factor
h_c	heat transfer coefficient for free convection
h_f	heat transfer coefficient for forced convection
h_r	heat transfer coefficient for radiation
h_t	total heat transfer coefficient
$I_{fu(M)}$	max. possible instantaneous value to which fuse limits short-circuit current
I_g	gate current
$I_{sc(M)}$max	max. possible value of short-circuit current
I_{TSM}	non-repetitive peak on-state current
l_c	effective length of heatsink in metres
l_f	effective length of heatsink (forced convection)
M	multiplication factor (electron or hole)
P_{RRM}max	maximum repetitive peak reverse power dissipation
$R_{th\ d-a}$	thermal resistance from device direct to ambient
R_{fu}	resistance of fuse
$R_{th\ h-a}$	thermal resistance from hottest spot of heatsink to ambient
$R_{th\ j-mb}$	thermal resistance from junction to mounting base
$R_{th\ mb-h}$	thermal resistance from mounting base to heatsink
T_{amb}	absolute ambient temperature
T_h	absolute temperature of heatsink
ΔT_{h-a}	temperature difference (°C) between heatsink and ambient
T_j	junction temperature
t_d	delay time (turn-on)
t_r	current rise time
t_s	spreading time

V_{BB}	base-to-base voltage (U.J.T.)
V_{BO}	breakover voltage
$V_{(BR)R}$	reverse avalanche breakdown voltage
V_{DRM}	repetitive peak off-state voltage
V_{DWM}	crest working off-state voltage
V_p	peak point voltage (U.J.T.)
V_{RRM}	repetitive peak reverse voltage rating
V_{RWM}	crest working reverse voltage
V_{WM}	crest working voltage rating
α	base gain (only in ref. to turn-on mechanism)
γ_a	thermal conductivity of air
γ_s	thermal conductivity of heatsink
ε	emissivity coefficient
η	intrinsic stand-off ratio (only when used in ref. to U.J.T.)
η_h	heatsink efficiency
ρ	density
σ	Stefan-Boltzman constant (7.51×10^{-8} W/m^2 °K^4)

1 Thyristors and their characteristic properties

1.1 Terminology

The term "thyristor" is used in three ways. Firstly, it is a generic term and is used to denote

a bistable semiconductor device, comprising three or more junctions, which can be switched from the off-state to the on-state or vice versa

I.E.C. Definition

Secondly, it is commonly used for a particular type of thyristor – the reverse blocking triode thyristor or SCR (in which sense it will be used in this book, where it is clear from the context what is meant). I.E.C. recommendations allow this use and also (the third use) employment of the term to cover any single member of the thyristor family when such use does not result in ambiguity or misunderstanding.

This book is a general treatment of the whole family of thyristors and therefore special properties of specific members of the thyristor family will be treated separately only when it is absolutely necessary. In such cases the device name will normally be used, but if the term "thyristor" is used then the context will dispel any ambiguity.

1.2 Brief Survey of Thyristor Family

Thyristors form a large family and it will be helpful, at this stage, to consider the constituents which, according to their combination, determine the type of any given thyristor.

In essence, a thyristor is a *PNPN* sandwich. If an ohmic connection is made to the first *P* region and the last *N* region, and no other connection is made, the device is a diode thyristor. If an ohmic connection is made, in addition, to the intermediate *N* region (*N* gate type) or the intermediate *P* region (*P* gate type), the device is a triode thyristor. If an ohmic connection is made to both intermediate regions, the device is a tetrode thyristor. All such devices have a forward characteristic of the general form shown in Fig. 1.1.

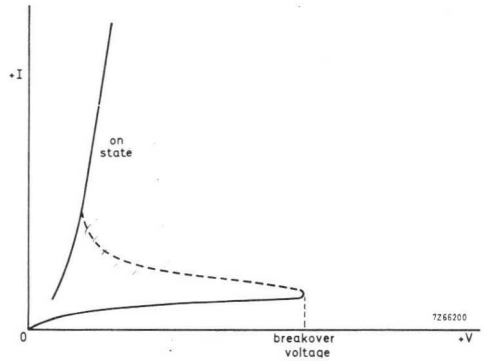
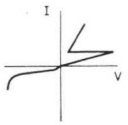
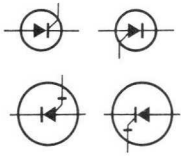
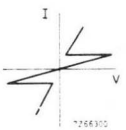


Fig. 1.1. General form of thyristor forward characteristic.

Table 1.1

number of terminals → / numbers of layers ↓	2 terminals	3 terminals	4 terminals
4 pnpn 	reverse blocking diode thyristor 	reverse blocking triode thyristor or SCR (silicon controlled rectifier) also GTO (gate turn off) which can be turned on or off by a gate signal 	reverse blocking tetrode thyristor or SCS (silicon controlled switch) which can be switched on by either gate 
5 pnpnp 	bi-directional switch 	triac 	

Reverse characteristics are of three types – blocking (as in normal diodes), conducting (large reverse currents at reverse voltages comparable in magnitude to the forward on-state voltage), and approximate mirror image of the forward characteristic (bi-directional thyristor). Reverse blocking devices usually have four layers or less whereas reverse conducting and mirror image devices usually have five layers.

Table 1.1 shows the general form of the thyristor family in terms of layers and terminals.

Normally, when a triode-thyristor has been turned on, it cannot be turned off by a gate signal. There is, however, a type which can be turned on and off by a gate signal of the appropriate polarity (gate turn-off thyristor).

At this point, it will be worthwhile to consider two devices which, although more strictly transistors than thyristors, have an important role in many thyristor triggering techniques. They are the diac and the unijunction transistor.

The diac is a switching device ideal for use with triacs but also effective in SCR circuits. It is often manufactured by diffusing an n-type impurity into both sides of a *P* type slice. The electrical characteristics are, of course, symmetrical. Important characteristics are breakover voltage, breakover current and breakback voltage as shown in Fig 1.2.

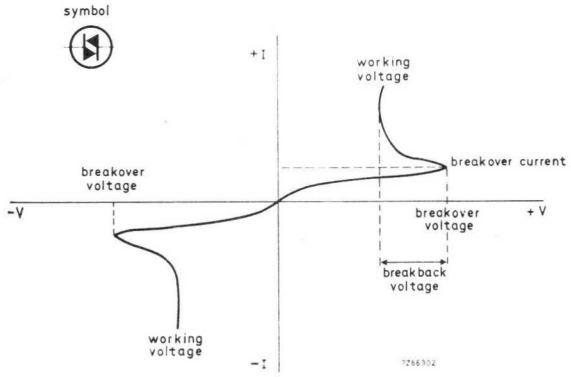


Fig. 1.2. Symbol and main characteristic of diac.

Device performance requirements can best be understood by reference to the most common triac triggering circuit (Fig. 1.3). In each half-cycle of the mains sinewave, the capacitor charges up on time constant RC. When the capacitor voltage exceeds the diac breakover voltage (typically 32 V) the diac turns on and the capacitor discharges through the triac gate – this turns the triac on. If the diac breakover voltages and currents in both directions are identical, the triac triggering points will occur at the same time after the start of positive half-cycles as they will after the start of negative half-cycles. Phase control is obtained by adjustment of the potentiometer R.

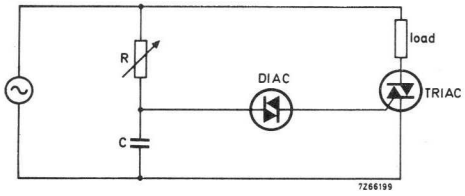


Fig. 1.3. Diac circuit for triggering triac.

If, in Fig. 1.4, terminal 1 is positive with respect to terminal 2, J_1 is reverse biased and J_2 forward biased. J_1 has reverse leakage current I_{R1} passing through it. Also, J_1 receives a component of injected forward current from J_2. In passing across J_1, this component is subject to multiplication so the current from $J_2 = M_2\alpha_2 I$ where I is the external current.

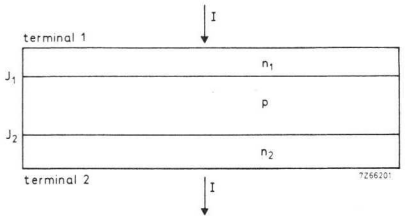


Fig. 1.4. Schematic of diac crystal.

The total current at J_1, which must equal the external current if continuity is to be observed, is

$$I = I_{R1} + IM_2\alpha_2$$

that is,

$$I = \frac{I_{R_1}}{1 - M_2\alpha_2}$$

$$= \frac{I_{R2}}{1 - M_1\alpha_1}$$

in the opposite half cycle.

When $M\alpha = 1$ the current appears to be infinite. In fact, this is the switching point and the voltage collapses to maintain reality. When the voltage drops below the breakover voltage, the multiplication coefficient M falls dramatically; however the current gain α rises with increasing current. Breakover occurs at the locus of points where $M\alpha = 1$.

The device gain is controlled by the injection efficiency of the junctions, the basewidth and the minority carrier lifetime. If the current gain is made too high, even a low value of M can be sufficient for triggering (attention to this is particularly necessary at high temperatures where leakage currents, minority carrier lifetimes and thus current gains rise dramatically). This is illustrated in Fig. 1.5 (*a*).

If this is overcompensated by reduction of the gain, timing becomes unreliable because very high breakover currents are necessary to achieve switching. Fig. 1.5 (*b*) shows two examples of breakover currents – one at 75 °C and the other at 25 °C.

Gain needs to be just right, which is difficult to achieve as the correct value is determined by three parameters. In addition

(a) capacitive current produced by dV/dt charging of the reverse-biased junction can cause premature triggering (this favours a less sensitive design)
(b) a high value of breakback voltage requires a very high current gain to force a large drop in M, and therefore voltage, in retaining the stable $M\alpha = 1$ condition.

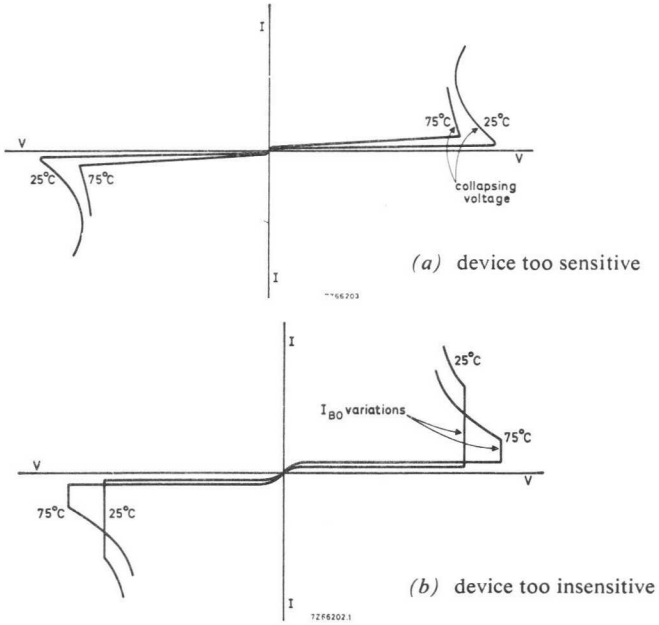


Fig. 1.5. Variation of breakover currents and voltages with temperature.

The unijunction transistor, Fig. 1.6, is used in a variety of thyristor triggering circuits. V_{BB}, the voltage between the two bases, sets the voltage at the junction of R_{B1} and R_{B2}. To a first approximation, when the voltage between the emitter and B_1 exceeds the voltage drop across R_{B1} plus the forward voltage drop of the emitter diode, the unijunction transistor turns on and a large current flows from emitter to base 1. Thus,more accurately,

$$V_P = \eta V_{BB} + V_D$$

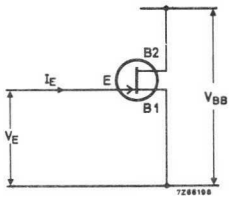
where V_P is the peak point voltage (i.e. the voltage between emitter and base 1 at which the device turns on),

η is the intrinsic stand-off ratio and lies between 0.51 and 0.82,

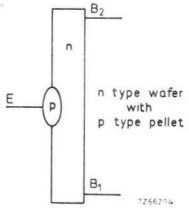
V_{BB} is the base-to-base voltage,

and V_D is the diode forward voltage drop (usually about 0.5 V at 25 °C).

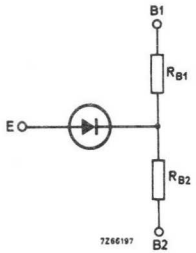
V_P decreases with temperature but this can be compensated by a resistor in series with base 2.



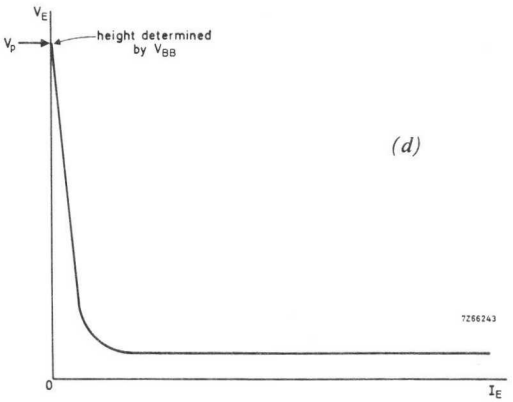
(a)



(b)



(c)



(d)

Fig. 1.6. Unijunction transistor; *(a) symbol (b) crystal structure (c) equivalent circuit (d) emitter characteristic.*

1.3 Physical Processes in the Thyristor

1.3.1 Junction Diode Action

It will be useful, before examining thyristor action, to consider the action of a junction diode (see Fig. 1.7). The base can be N type (forming a rectifying junction with a heavily doped P layer) or P type (forming a rectifying junction with a heavily doped N layer). Junction breakdown voltage is determined by the width and doping concentration of the base – high concentration produces the abrupt high-field junction and low breakdown voltage of a voltage regulator (zener) diode, while low concentration gives low-field junctions and an avalanche breakdown level at high voltage. Base resistivities in the range 10^{-2} to 10^{3} ohm·cm will produce breakdown voltages between 10 V and 5000 V.

Fig. 1.7. Junction diode schematic.

Notwithstanding the wide range of base resistivities, the forward voltage drop of all silicon rectifiers is approximately the same. This is because forward conductivity is not determined primarily by the doping level of the base. If the base is P type, the N region injects electrons into the base and these soon reach a concentration well in excess of the resident holes. Thus, when the device is forward biased, the resistivity is determined by the injected minority carriers (in this case electrons) and not by the majority carriers (in this case holes). The base, in this condition, is said to be conductivity modulated. The injected electrons reach an equilibrium concentration which is determined by the rate of injection and the rate at which they recombine with holes in the base; the total number of injected electrons is known as the minority carrier stored charge.

1.3.2 Simplified Charge-Controlled Concept of Thyristor Action

A thyristor turns on if the forward breakover voltage is exceeded or if an appropriate signal is applied to the gate. It will be convenient to consider the physical mechanism of forward breakover first, as it is simpler, and then progress to a consideration of what happens when a triggering signal is fed to the gate.

Forward Breakover

When the anode is more positive than the cathode (see Fig. 1.8), junctions J_1 and J_3 are forward biased. Region N_1 is much more highly doped than region P_1 so, if a high current flows through the thyristor, the junction current at J_1 is mainly electrons which are being injected into P_1. Region P_2 is much more highly doped than region N_2 so at high conduction levels the junction current at J_3 is mainly holes which are being injected into N_2.

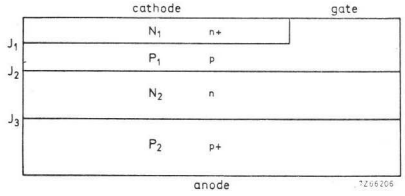


Fig. 1.8. Simplified thyristor crystal showing regions and junctions.

This tends to bring about a state of conductivity modulation, in which the level of conductivity is determined by the density of injected minority carriers rather than by the original majority carrier doping levels; in other words, P_1 may be considered to be modulated to an N region and N_2 to a P region.

However, as J_2 is initially reverse biased, conductivity modulation of P_1 and N_2 cannot occur until the reverse voltage across J_2 reaches the avalanche breakdown level. As soon as the avalanche breakdown voltage across J_2 is reached, conductivity modulation occurs in P_1 and N_1 and the device conducts like a single forward-biased junction. This junction (J_2) will then be the region in which injected holes and electrons combine.

Because avalanche breakdown is always initiated at a discrete point, conductivity modulation will be also. Thus there will be a transverse gradient of stored charge in the device. Carriers will diffuse down this gradient, spreading the conduction gradually over the whole cathode region provided the current is high enough.

Gate Turn-On

The electrons which flow as gate current, from the cathode N_1 to the gate lead, modulate P_1 in the vicinity of the gate. Electrons drift into the depletion layer of J_2 and are accelerated into N_2, lowering the potential there. This causes J_3 to become more forward biased and thus more holes are injected into N_2, so N_2 becomes locally modulated. An initial

"filament" of conduction is thus formed near the gate and spreads, if the forward current is high enough, over the remainder of the cathode.

Holding Current

When the entire cathode is in conduction and the forward current is gradually reduced, the stored charge decreases. At lower current levels it becomes more difficult to sustain conductivity modulation. When the holding current level is reached, conductivity modulation is no longer possible so the device turns off and the four layer structure re-establishes itself.

In fact, regions of the cathode will turn off, one by one, in reverse order of easiness to modulate. The last region may have:

(a) the highest injection efficiency, owing to fluctuations of cathode doping,

(b) the narrowest, or highest-lifetime, bases (P_1 and N_2 are known, respectively as the P and N bases) – which are the easiest to modulate.

It is possible to influence the holding current by the test method. For instance, if the device is turned on to a low test current there will be insufficient injected charge to establish conduction over the whole cathode; in this circumstance it is possible that the most sensitive point may be excluded.

Latching Current

If a thyristor is gate-triggered, the initial "filament" of conduction is near the gate. As determination of latching current consists of initiating conduction and then removing the gate signal, it really measures the holding current of the region near the gate. This may well not be the highest gain point of the whole cathode so the latching current can be no lower than, and is almost invariably higher than, the holding current.

The ratio of latching current to holding current gives some indication of device uniformity; a ratio of 2 : 1 is quite common.

Other Parameters

It is quite easy, by the above rationale, to explain dV/dt, di/dt, turn-on time and turn-off time. The stored charge concept demands a three-dimensional appreciation of the structure. Each thyristor can be regarded as thousands of thyristors in parallel.

1.3.3 Calculation of Turn-On Point

The current through the thyristor is I (see Fig. 1.9). J_2 is reverse biased and has a leakage current I_R; J_2 also receives electrons injected from the cathode N_1. These are subject to recombination en route and the total reaching J_2 is a fraction ,α_1 (injection efficiency multiplied by a transport factor). When these electrons cross the charge depletion layer of J_2 they may experience multiplication so the total contribution from J_1 is

$$\alpha_1 M_1 I,$$

where M_1 is the electron multiplication factor.

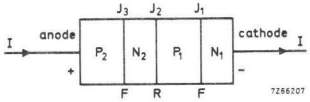


Fig. 1.9. Theoretical representation of thyristor.

A similar contribution of holes is made by J_3, that is,

$$\alpha_2 M_2 I,$$

where M_2 is the hole multiplication factor.

But the total current through J_2 is I, the external current.

We can therefore write

$$I = I_R + \alpha_1 M_1 I + \alpha_2 M_2 I,$$

which simplifies to

$$I = \frac{I_R}{1 - (\alpha_1 M_1 + \alpha_2 M_2)}. \tag{1}$$

Gate current makes an extra contribution of $\alpha_1 M_1 I_G$ to J_2. If this is taken into account

$$I = \frac{I_R + \alpha_1 M_1 I_G}{1 - (\alpha_1 M_1 + \alpha_2 M_2)}. \tag{2}$$

The device switches on when

$$\alpha_1 M_1 + \alpha_2 M_2 = 1.$$

Theoretically this suggests that I has risen to infinity but in practice it can simply be taken to imply that the off state is no longer valid.

The base gains (α's) are very current sensitive, α_1 in particular will rise rapidly at high gate currents.

Complex device geography and extreme non-homogeneity of transient (and even D.C.) conduction make it virtually impossible to put accurate values into these formulae. In addition, forward breakdown is usually initiated at the side of the crystal (and thus remotely from the cathode), so the P base is determined more by lateral geometry than by P basewidth (see Fig. 1.10). Finally, when gate current flows, many electrons pass wastefully out of the edge of the conduction path (see Fig. 1.10). However, the formulae do serve to give a qualitative understanding of thyristor action.

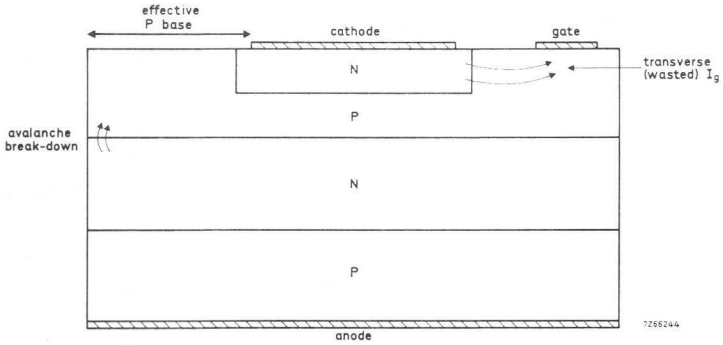


Fig. 1.10. Position of avalanche breakdown and wasted I_G.

1.4 Relation Between Manufacturing Technology and Device Properties

1.4.1 Alloyed Thyristors

Fig. 1.11 shows an alloyed thyristor and illustrates some of the refinements which improve performance. Both high-voltage junctions (J_2 for forward breakover voltage and J_3 for reverse avalanche voltage) are diffused, but the cathode is alloyed with gold antimony. The junctions are bevelled to reduce the surface field and thus ensure that avalanche breakdown occurs in the bulk of the crystal rather than at the edges; this improves the blocking voltage capability.

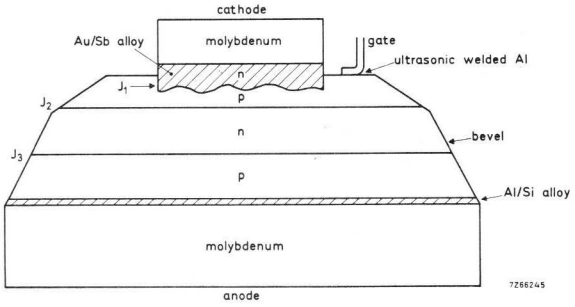


Fig. 1.11. Alloyed thyristor.

Such devices have given many years of good service and have particularly reliable contacts. However, they suffer from three main defects:

(a) non uniformity of the P base – this is shown in exaggerated form in Fig. 1.11 by variations in alloying depth – which gives a high ratio of I_L to I_H and a wide variation of I_H, I_L and I_G from device to device.
(b) the structural non-uniformity virtually ensures that gate turn-on occurs at a localised point and spreading is slow – leaving the device vulnerable to di/dt failure.
(c) when a rapid transient in the forward direction charges the junction capacitance of J_2, the charging current is supplied by injection from the alloyed cathode – this can lead to premature dV/dt triggering at levels as low as 10 V per microsecond.

1.4.2 Semi-Planar Thyristors

Thyristor design has evolved through the stage of coarse all-diffused processes, still retaining many of the alloyed device problems, and is now in the phase of complex semi-planar technology. The term "semi-planar" indicates that oxide masking is used to control junction geometries but not to give protection from surface effects. Thus junction bevelling is still desirable at high-voltage levels.

A semi-planar thyristor design is shown in Fig. 1.12. Uniformity of the diffused regions makes gate turn-on possible at more than one point; greatest advantage of this can be taken if an extended interface, between the cathode perimeter and the gate contact, is provided. However, as the interface is lengthened, the gate current, necessary to bring into being the required triggering current, is increased. A central gate is a typical compromise.

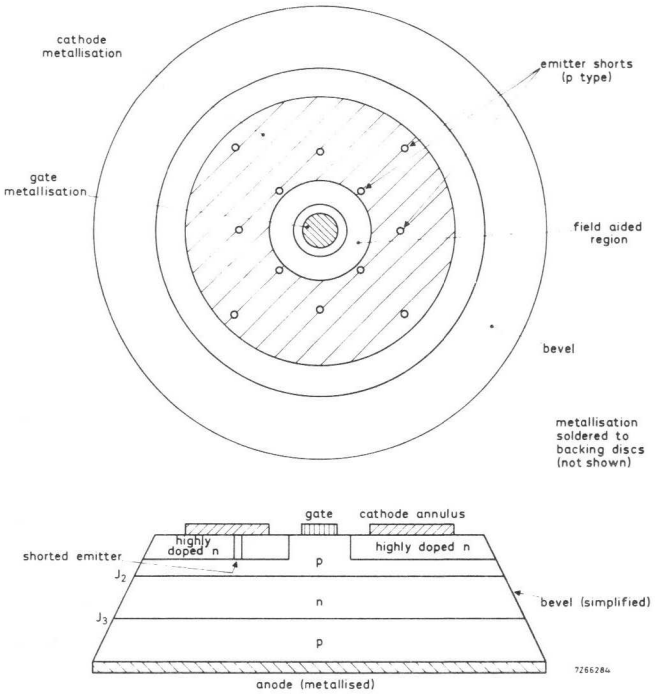


Fig. 1.12. Semi-planar thyristor.

The P type shorts in the diffused cathode constitute what is called "shorted emitter" and provide a means of charging the junction capacitance of J_2 without injection from the N type region of the cathode; this allows the device to withstand very high dV/dt transients. These shorts suppress cathode injection at low currents but not at high currents. dV/dt improvement is thus accomplished at the cost of a slight fall in gate sensitivity.

A further design feature is "field-aided turn-on", sometimes called forced

field conduction. This is illustrated in Fig. 1.13 by a magnified view of the gate-cathode region. The gate initiates conduction in the immediately adjacent cathode region; however, this region is not metallised, so the initial anode-cathode current has to traverse a relatively high impedance region – perhaps of the order of 1 Ω. The voltages marked on Fig. 1.13

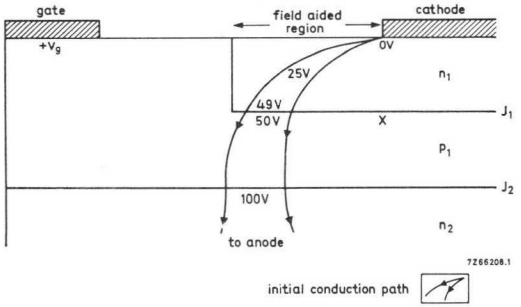


Fig. 1.13. Field-aided turn-on.

represent the very early stage of turn-on, when only a small region is conducting and its forward voltage is, say, 100 V. If there were no transverse current across P_1, point X would be at 50 V and J_1 would be forward biased to the 50 V level. However, this cannot be and, in fact, the voltage drop across the field-aided N region initiates transverse base current which forces conduction back to the metallisation. From there, spreading proceeds at the normal speed. Although the area of conduction may still be small, the benefit is crucial during the first few microseconds when di/dt dissipation can be most damaging. In addition to this, the higher the di/dt impressed on the device, the faster the conduction spreads.

An important problem arises, however, in such devices. The field-aided voltage raises the potential of P_1 near the gate contact and, at high di/dt levels, this potential can exceed the gate voltage (see Fig. 1.14). Gate current is therefore reversed through the external circuit and the negative gate effect is produced; this negative gate effect can turn off regions of the cathode where conduction has just been established and prevent the turn-on of other regions. Field-aided voltages may be 50 V at 200 A/μs turn-on rate to a steady-state current of 100 A and much higher (perhaps 200 V) at a turn-on di/dt of 1000 A/μs to a steady-state current of 1000 A. If very high di/dt is anticipated, the gate circuit must be protected against field-aided voltages by means of a fast diode; high-voltage triggering can often be the most effective means of protection.

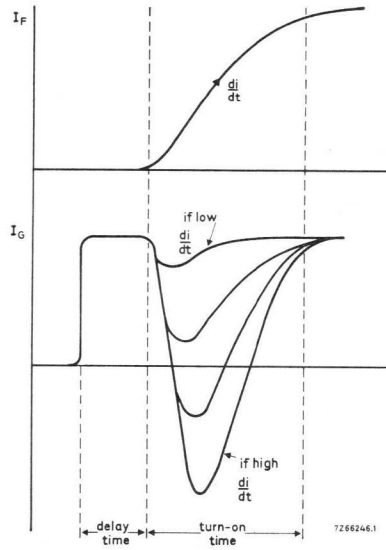


Fig. 1.14. Negative gate effect.

This negative gate anti-spreading effect has been eliminated by further developments; these include Regenerative Gate, Amplifying Gate and Accelerated Cathode Excitation. While each mechanism is slightly different, they all have in common the basic principle of diverting part of the anode-cathode current to trigger other areas and thus speed-up the spread of conduction. Fig. 1.15 shows the regenerative gate device. The external gate lead is placed near a very pronounced field-aided region and the gate-cathode interface is short, so the trigger sensitivity will be high. The auxiliary gate contact can pick up a voltage of, say, 25 or 50 volts and distribute it around the cathode perimeter. Auxiliary gate drive can be at a very high level (many amps) to ensure that the secondary conduction regious are driven hard on; it also makes the initial area of conduction greater – so reducing turn-on time. This method, like the field-aided mechanism, only operates at high di/dt, ceases when conduction reaches the cathode metallisation and produces high positive voltages at the gate connection (against which the external circuitry must be protected).

All of the anode-cathode current diversion techniques provide higher di/dt operation than field-aided turn-on, but they are all more expensive. However, a di/dt rating of 100 to 200 A/μs is adequate in most applica-

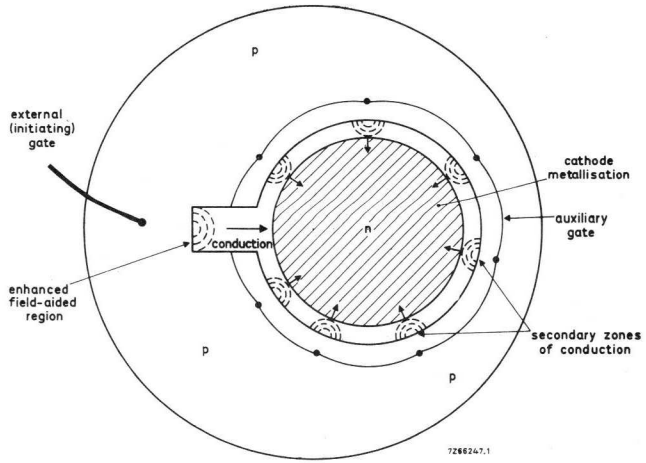


Fig. 1.15. Regenerative gate thyristor.

tions; the complicated technology required to provide ratings of 1000 A/μs will, almost certainly, be limited to specialised applications.
The above technology can also, of course, be adapted to improve di/dt performance with V_{BO} triggering. However, since the maximum possible breakover voltage is much higher than the minimum guaranteed crest working voltage, the V_{BO} turn-on dissipation is higher than the turn-on dissipation for gate triggering, and so the V_{BO} di/dt ratings will be lower than those for gate triggering. (As V_{BO} turn-on occurs by means of the avalanche mechanism, it is very fast. Such speed makes the task of spreading the area of conduction rapidly enough very difficult and makes it likely that V_{BO} di/dt ratings will always be lower.)

1.4.3 High Power Thyristors

As might be expected, the development of high-power thyristors has proceeded very rapidly in recent years; 500 A devices are now freely available and soon 1000 A types will be just as common. Nevertheless, the high-power field still has many basic problems. It is not easy to manufacture silicon ingots of the required quality and diameter. Moreover, these thyristors have such large cathodes that it may take 0.5 ms for conduction to become fully established – so there can be no question of anything but low-frequency operation unless the cathode structure is made very complex.

Silicon is very brittle and has an expansion coefficient much lower than the copper base; thus there is always risk of strain and fracture when the crystal is soldered to the base (even via expansion-matching intermediaries such as tungsten discs). So, although soldering gives a more intimate thermal contact, it has had to be abandoned on large thyristors in favour of pressure contacts. These give good thermal contact and allow for expansion as the surfaces can slide against each other to some extent. The internal structure of pressure contact thyristors is quite complex – threaded bushes, spring washers, soft discs (often made of silver) to act as pressure pads, nuts and insulating sleeves for the gate lead. All surfaces must be flat, and specially elongated top caps may be necessary to accomodate everything.

Recently there has been a significant advance, with the introduction of the "Press Pack" or "Hockey Puck" encapsulation. This is much simpler and cheaper and is supplied with little pressure on its contacts – pressure is applied externally when the device is clamped to the heatsink. The Hockey Puck device can be clamped with either anode or cathode to the heatsink; thus many stack arrangements can be simplified. It can also be mounted with a heatsink on both sides; this makes a great improvement in the thermal resistance and mean rating of the thyristor (but has little effect on the surge rating, unfortunately, which is largely determined by the crystal properties).

New bevelling techniques and improved processing have made possible the manufacture of high crest-working voltage thyristors. Minority carrier lifetime needs to be very great if the forward voltage is to be acceptable because the crystal may be more than 1 mm thick. Turn-off times are very great and transit times are long, as also are turn-on times. The di/dt and surge capabilities are much inferior to those of the lower voltage types.

1.4.4 Fast-Switching Thyristors

By contrast, the high-speed thyristors are devices in which voltage ratings have been sacrificed in favour of turn-off or turn-on speeds.

Short turn-off times are achieved by "gold killing". Gold in silicon reduces minority carrier lifetime but, unfortunately, also increases leakage currents. The faster the device, the higher the leakage current – so the lower the crest-working voltage. At present, at current ratings of about

50 A, 600 V types which turn off in less than 6 μs and 1200 V types which turn off in less than 20 μs are practicable.

Pulse modulator thyristors usually operate at only a few thousand pulses per second and their design is optimised for rapid turn-on. Both *N* and *P* bases are minimised to reduce transit time, and doping levels are low so that conductivity modulation can be achieved with the minimum of injected charge. Spreading velocity can be as high as 0.2 mm per microsecond (0.1 mm per microsecond is normal for thyristors) and 800 V devices can turn on completely in 0.25 μs; d*i*/d*t* ratings well in excess of 1000 A/μs are available. (If saturable reactors are used to delay the main current pulse until after the thyristor voltage has collapsed, thereby minimising the peak power loss, then a d*i*/d*t* performance of 3000 to 4000 A/μs is possible.)

1.4.5 Triacs

Unidirectional thyristors are basically d.c. controllers because they conduct in one direction only; if they are used for a.c., two are required connected in inverse parallel. The triac is equivalent to such an inverse-parallel arrangement – but in a single crystal and triggered by only one gate (which accepts both positive and negative trigger signals). This means that a single heatsink can be used and triggering circuits can be greatly simplified. Fig. 1.16 shows the main static characteristic.

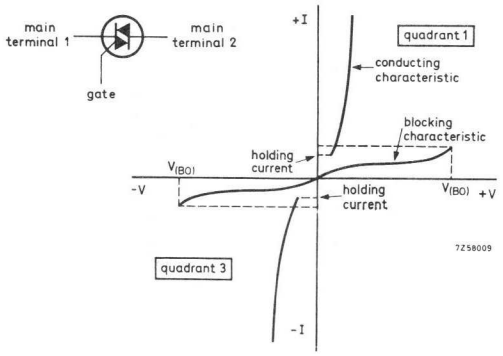


Fig. 1.16. Static characteristic of triac.

Triggering Modes

A triac can conduct in either direction. When Main Terminal 2 of the crystal is positive with respect to Main Terminal 1, the triac is said to be operating in the "first quadrant" (see Fig. 1.16); when the polarity is reversed, the operating mode is said to be "third quadrant".

In either quadrant, triggering may be positive or negative. To illustrate the four triggering modes, an appropriate cross-section of the triac crystal is shown (either through the *p* region or the *n* region of the gate) and reverse or forward bias at junctions is shown by the letters *R* and *F*. Polarity of gate triggering signals is shown by plus and minus signs. A triac crystal and a key to the cross-sections, is given in Fig. 1.17.

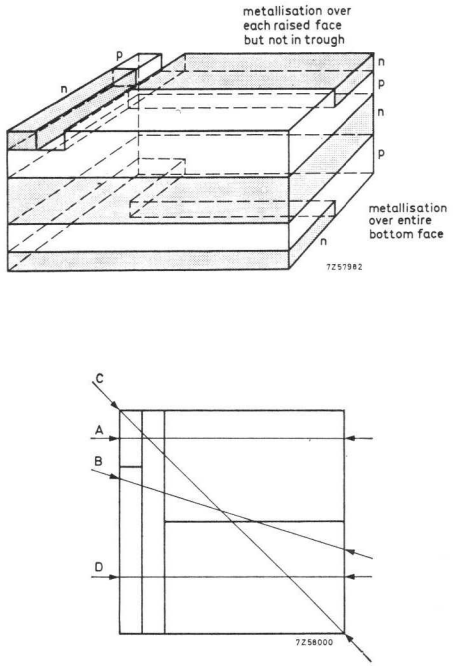
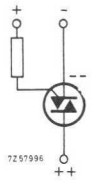
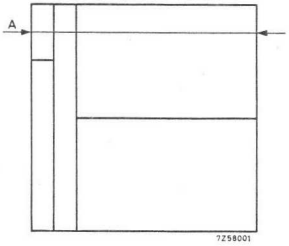


Fig. 1.17. Practical triac structure and key to cross-sections.

First quadrant positive triggering is shown in Fig. 1.18. The gate-cathode junction p_1n_3 is forward biased and electrons from n_3 are collected by the n_1 region. These lower the n_1 region potential, providing more forward bias for the p_2n_1 junction. Holes from p_2 reach the n_1 region and are collected by p_1 and the triac switches on (as a normal thyristor).





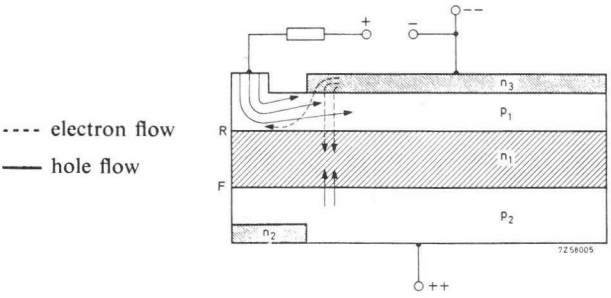
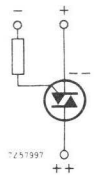
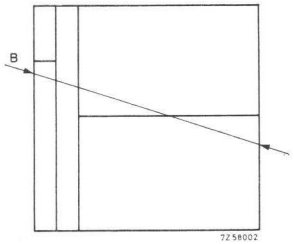


Fig. 1.18. First quadrant positive.

Negative triggering in the first quadrant is shown in Fig. 1.19. Forward bias is applied at the junction p_1n_4. Electrons from n_4 are collected by the n_1 region and lower the potential there. Thus the p_2n_1 junction becomes more forward biased. Holes from p_2 reach the n_1 region and are collected by p_1. The triac then switches on.





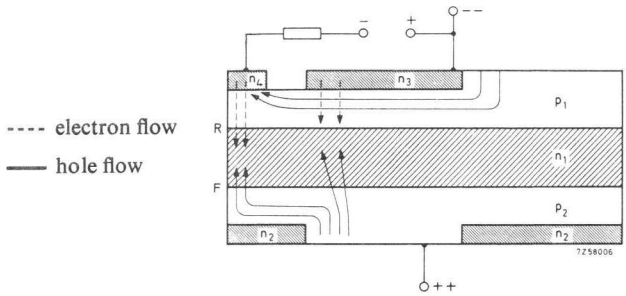


Fig. 1.19. First quadrant negative.

Fig. 1.20 shows third quadrant positive triggering. The gate-cathode junction p_1n_3 is forward biased. Electrons reach n_1, which becomes more negative. Hole current from p_1 to n_1 increases and the holes in n_1 are collected by p_2; this hole flow causes n_2 to emit electrons and these are collected by n_1. Current flows down the left-hand side of the crystal (as viewed in Fig. 1.20) which then switches on. Current then rapidly spreads from the gate region to the main anode and cathode regions on the right-hand side whose p_1 and n_2 regions are contiguous with those of the gate area.

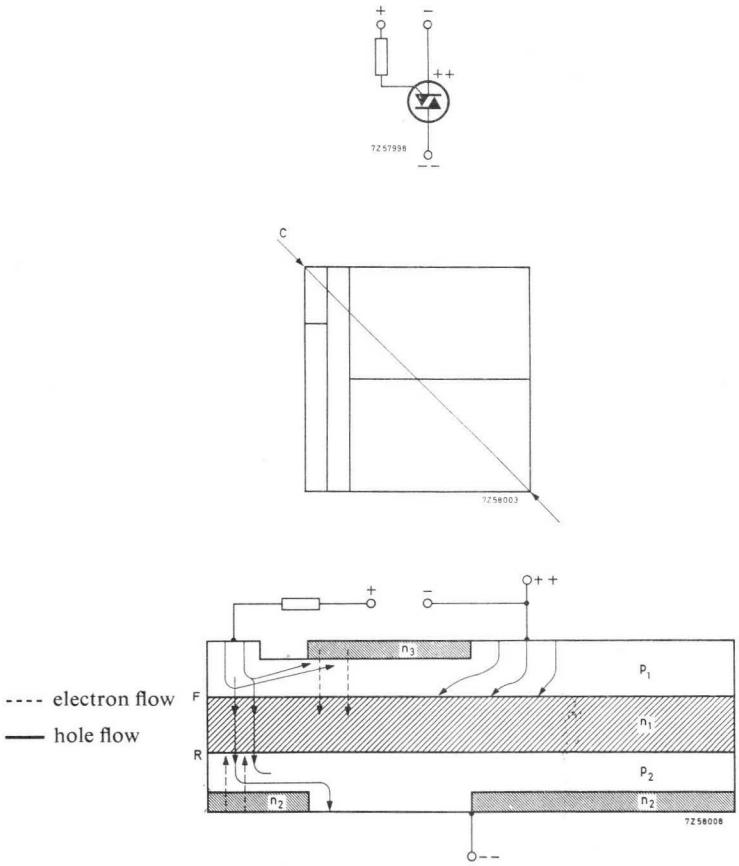


Fig. 1.20. Third quadrant positive.

Third quadrant negative triggering is shown in Fig. 1.21. The junction p_1n_4 is forward biased and electrons reach n_1, lowering the potential there. Hole flow from p_1 to n_1 increases and the holes in n_1 are collected by p_2. Electrons are emitted from n_2, as a result of hole flow, and are collected by n_1. Current flows down the left-hand side of the crystal and, if sufficient current can flow in the main circuit, the triac switches on fully (as a thyristor with a remote gate).

Triac triggering mechanisms are contrived by means of complex surface and bulk geometrical arrangements and sometimes depend on transverse current flow through regions of carefully optimised geometry and resistance. Especially careful optimisation is required for the third quadrant positive, and this is more feasible with large crystals such as the BTX94.

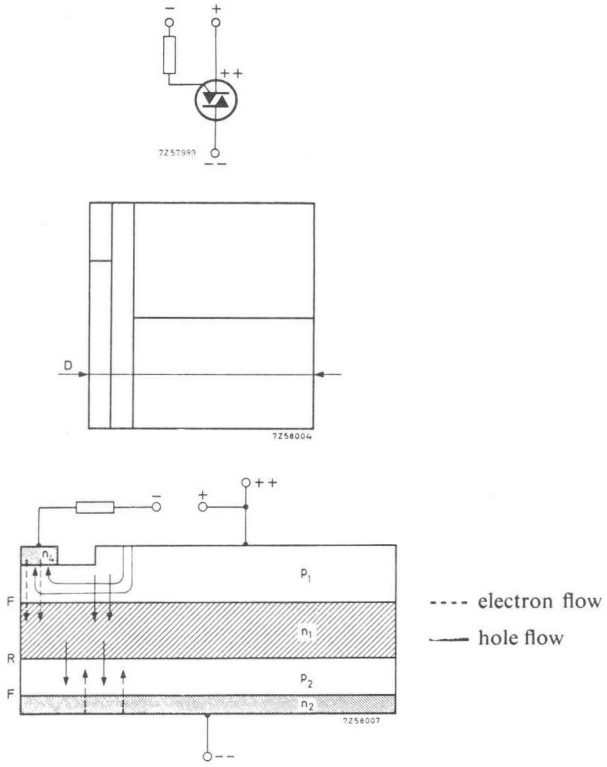


Fig. 1.21. Third quadrant negative.

Quadrant-to-quadrant commutation may suffer if triggering sensitivity is optimized; when one half of the triac is conducting, injected charge drifts into regions of the other half and is available to turn the other half on if commutation is too rapid. This effect becomes worse when the load is inductive. Prevention of this unwanted switching is difficult because overlapping of the two halves is essential to some triggering mechanisms. However, the problem can be overcome by careful design and has in the case of the BTX 94, which operates successfully with inductive loads.

1.4.6 The Gate-Controlled Switch (GCS)

This device, sometimes called the gate turn-off switch, is unique among thyristors in that it can be turned off as well as on by a gate signal; a positive gate signal turns it on and a negative gate signal turns it off.

Fig. 1.22 shows a thyristor in the on state. The *P* base has been modulated by electrons injected from the cathode (the excess of electrons over holes in the base is the minority carrier stored charge) and the *N* base is similarly modulated by a stored charge of holes. Gate and cathode form a diode and a reversal of bias at this junction, from forward to reverse, produces the familiar extraction of stored charge as shown in Fig. 1.23.

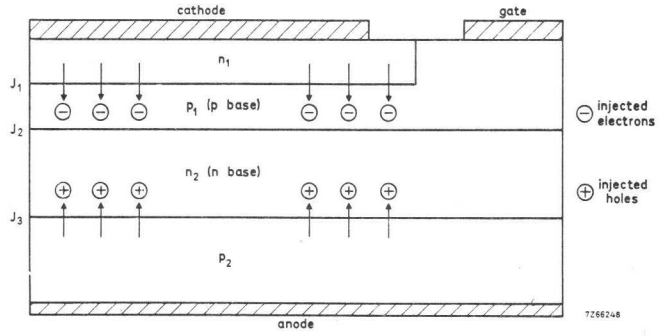


Fig. 1.22. Thyristor in forward conduction.

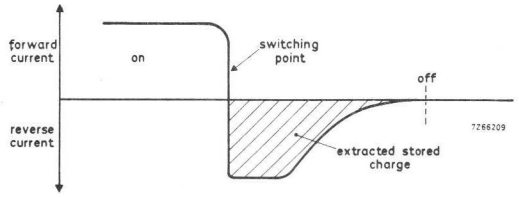


Fig. 1.23. Diode turn-off waveform.

Thus, a negative signal at the gate extracts the stored charge in the P base. Extraction takes place first in the region immediately adjacent to the gate so the thyristor turns off near the gate while being on in other regions. Charge in the N base cannot be extracted directly and gradually recombines with majority carriers; therefore the N base lags the P base as shown in Fig. 1.24.

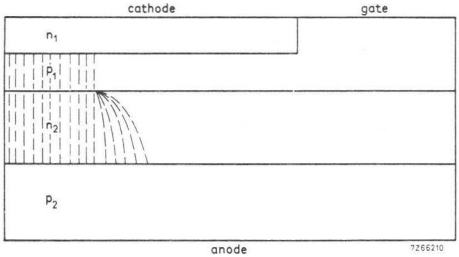


Fig. 1.24. Stored charge during turn-off period.

The area of conduction is gradually "pinched" by continued negative gate current. At first the effect is small, as the external anode-cathode circuit "fights" the gate signal by increasing the current density through the remaining "on" region. However, as the turn-off process continues, the increasing current density through the decreasing device area causes the anode-cathode impedance to rise and the main current to fall. Eventually conduction ceases.

This "pinch-off" effect is the opposite of turn-on behaviour, where a small region of conduction spreads gradually outwards over the cathode, and carries the same danger of high currents in very small areas (di/dt effects in turn-on); in fact, gate turn-off is more dangerous because it is slower and therefore generates more losses.

Turn-off speed is charge controlled – the quicker the P base charge is removed (i.e. the higher the turn-off gate current) the quicker the device turns off and the lower the losses. Owing to the tendency of the external circuit to fight the turn-off process (especially with inductive loads) high gate currents would appear to be particularly desirable. However, there is another effect to be taken into account. The demodulated cathode

junction, J_1 (see Fig. 1.25), is reverse biased near the gate to the extent of the applied gate voltage. This junction normally has a low voltage-breakdown (between 10 and 20 volts) and if it goes into breakdown the thyristor will not turn off, conduction being sustained as shown in Fig. 1.26.

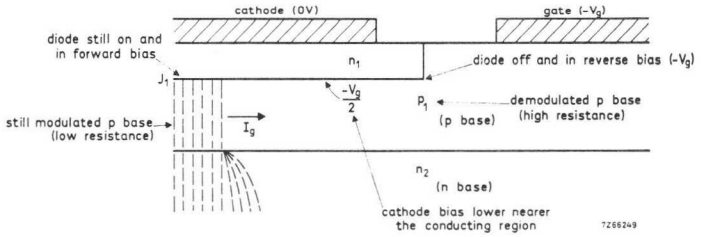


Fig. 1.25. Gate-cathode during turn-off.

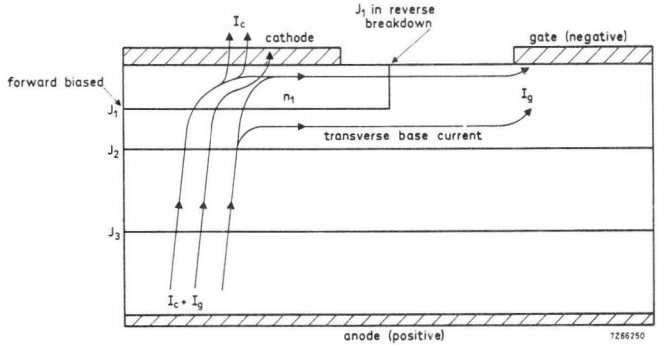


Fig. 1.26. Sustained conduction mode.

The bulk of gate-cathode current flows through the lower impedance cathode region. Junction J_1, remote from the gate, remains forward biased – sustaining conduction by injecting electrons into the *P* base. A small current flows across the high-impedance demodulated *P* base. The reverse cathode breakdown voltage must not, of course, be exceeded during turn-off – this limits the turn-off gate current and it must be remembered that, although the external impedance of the gate circuit may

be low, the internal (device) gate impedance is quite high. Fixing of the maximum turn-off gate current effectively limits the peak anode-cathode current; the maximum gate current turns off progressively higher anode currents progressively more slowly. When the turn-off time is long, e.g. 10 μs or more, the dissipation in the gradual pinch-off becomes unacceptably high.

The design of a practical device centres around the avoidance of reverse cathode breakdown and sustained conduction. Fig. 1.27 shows how turn-off time varies with negative gate current.

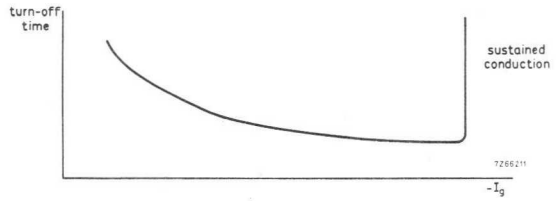


Fig. 1.27. Turn-off speed performance.

To ensure that a moderate gate voltage will produce a high turn-off gate current, it is essential that the *P* base impedance be fairly low. The cathode can be a long thin strip so that a long gate strip at its side has a low impedance path to collect the relatively small stored charge in its vicinity. Better still is a gate strip on each side of the cathode which leads to what is probably the best technique of all – interdigitated patterns of gate and cathode.

A wide, highly-doped *P* base ensures that the amount of stored charge is small and that this stored charge is extracted through an impedance which would otherwise be high.

A thyristor is only just in the "on" state when the sum of the *N* base and *P* base current gains is unity. So the gain of a practical gate controlled switch must remain as close to unity as possible. Ideally, as the stored charge in the *N* base is inaccessible and diffuses out when the device is almost off (and at high voltage), producing high losses, the *N* base gain and stored charge should be minimised. Preferential gold killing of the *N* base can be useful but the gain would normally be quite low since the base consists of the original lightly doped silicon into which all the other regions are diffused; it must be wide to support high blocking voltages

and this reduces the transport factor. The high doping of the *P* base also minimises *P* base gain and thus stored charge. Deliberately reduced injection efficiency of the cathode, or more commonly the anode, may also be employed.

In Fig. 1.28 a practical gate-controlled switch crystal is shown. It is not unduly surprising that, with optimising of turn-off performance, the turn-on performance has suffered somewhat. The gate-controlled switch (GCS) is, of course, insensitive and slow to turn on (when turn-on is initiated, spreading across the cathode is slow as there is no large gradient of stored charge). Forward voltage drop is much higher than that of a conventional thyristor and the forward surge capability is not good (though superior to that of a transistor). These characteristics must be taken into account when the decision whether to use a GCS or one of the alternatives (transistors or thyristors with commutation circuits – these commutation circuits may be thyristor circuits or commutation capacitors and inductors) is being made.

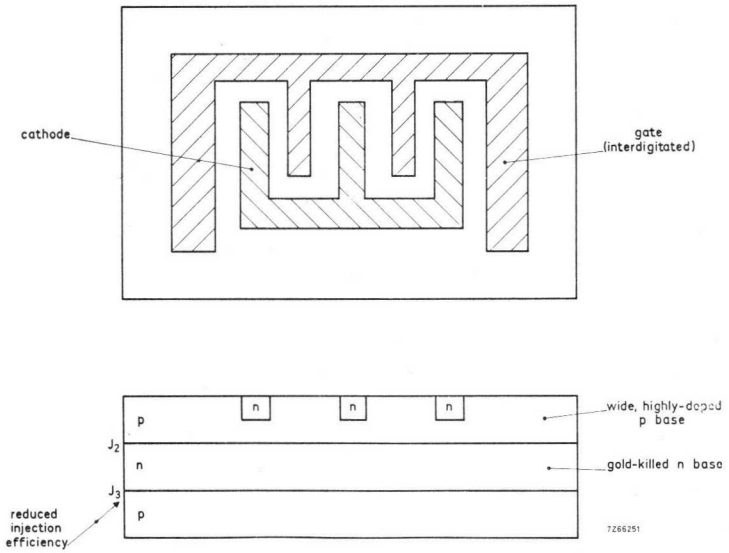


Fig. 1.28. GCS Crystal design.

The complex geometries of GCS are not conducive to large high-current contacts so there may be times when an arrangement in which one conventional thyristor switching another is dictated by high-current requirements. However, the GCS, with its rapid turn-off performance, will operate at higher switching frequencies than a two-thyristor arrangement and offers the advantage of circuit elegance.

A GCS provides a memory when in the "on" state; this may be useful in some circuits. Although slower to turn off than a transistor, it is much better at withstanding voltage and current transients.

1.4.7 SUMMARY

Finally, the compromises in device technology necessary for the achievement of specialised performance are summarised in Table 1.2.

Table 1.2 Summary of performance compromises

parameter required	penalty
low turn-off time	high V_F { lower di/dt rating higher turn-on losses high leakage { lower V_{RWM} lower V_{DWM} low gate sensitivity
low turn-on losses	thinner n-base { lower V_{RWM} lower V_{DWM} lower V_f high turn-off
accompanied by high di/dt	low dv/dt } for pulse-modulator types low T_j max. {
	(this is for extreme optimisation of di/dt only)
low turn-off plus low turn-on	lower V_{RWM} lower V_{DWM}

1.5 Encapsulation

Reliable performance of diodes and thyristors is achieved by protection of the crystal against chemical, thermal and mechanical causes of deterioration.

Ingress of dust and moisture must be prevented and chemical links with the device environment must not be permitted to exist. For this purpose the crystal is covered with silicon rubber or a laquer with chemical protective properties and capable of withstanding high electrical fields. Assembly during manufacture is carried out in an environment which is dust-free and moisture free and filled with an inert gas. A hermetically sealed envelope isolates the crystal assembly from the outside environment. Encapsulation parts are fixed together so that the hermetic seal survives varying electrical, mechanical and thermal loads and forces. Finally, a means of collecting anything left in the assembly (like a "getter" in a vacuum tube) is provided.

In order to limit the mechanical forces caused by differences in thermal expansion coefficients in adjacent materials, the crystal is placed between expansion matching discs – the forces (reduced in magnitude) then exist between the expansion matching discs and the contacts rather than the crystal and the contacts. Tungsten or molybdenum are chosen for these discs – not only for their coefficients of expansion but for their excellent mechanical, thermal and electrical properties.

An envelope protects the whole assembly and ensures that no mechanical forces are applied directly to the crystal. The envelope conducts both electrical and heat energy so the natural choice of material is copper. There must be no high resistances in the connections and the envelope shape must be conducive to good electrical and heat transfer (in some cases this means a flat base). Finally, the envelope isolates the anode from the cathode; it must do this successfully even in the most adverse circumstances.

Recently, plastic envelopes have been developed which do the above things quite well and considerably more cheaply.

Fig. 1.29 shows a number of the most common types of encapsulation.

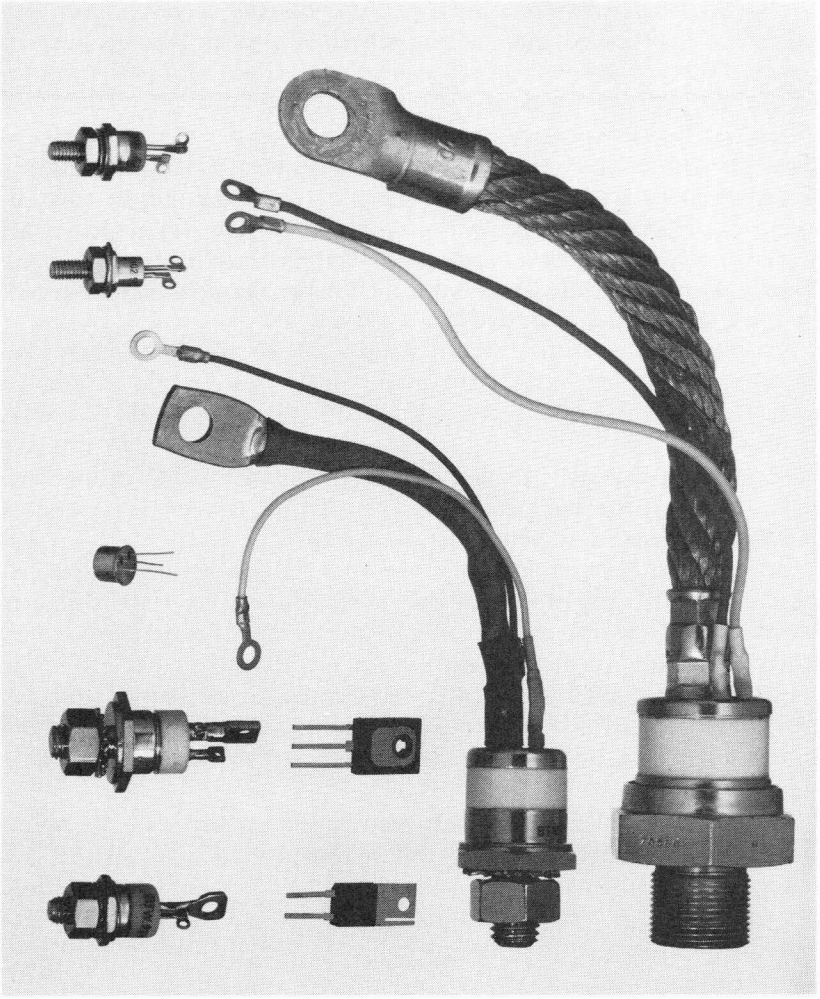


Fig. 1.29. Common encapsulations.

2 Thyristor Turn-on Methods

2.1 Introduction

As shown in Chapter 1, the turn-on point of a thyristor can be described by means of the relation

$$I = \frac{I_R + \alpha_1 M_1 I_G}{1 - (\alpha_1 M_1 + \alpha_2 M_2)}.$$

When I becomes infinite (which happens when $\alpha_1 M_1 + \alpha_2 M_2 = 1$), the thyristor turns on.

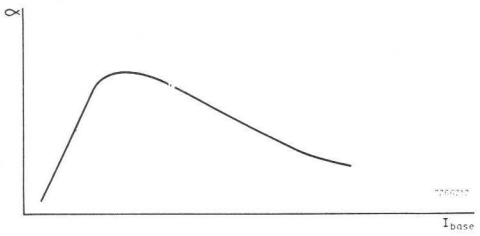


Fig. 2.1. Dependency of base gain (α) on base current.

Because the base gains (α_1 and α_2) are very current-dependent (see Fig. 2.1), an increase of the base current can bring about turn-on. Base-current increase can be caused by increase of leakage current resulting from a rise in junction temperature, a higher off-state voltage, a higher rate-of-rise of off-state voltage, or the connection of an external current-source to the gate. Of these methods, gate triggering is the one usually employed; V_{BO} triggering may sometimes occur and, in any case, it is made use of as a means of protection when avalanche thyristors are connected in series. Measures are taken to suppress the other two influences.

In this chapter we shall briefly survey the non-preferred triggering methods and then proceed to a detailed examination of gate triggering.

2.2 Turn-on by Leakage Current

As the junction temperature rises, so also does the leakage current. Eventually, if junction temperature continued to rise, leakage current would become great enough to initiate forward conduction (i.e. leakage current carrier energy becomes great enough to dislodge further carriers in the junctions until a type of avalanche breakdown occurs). At a certain critical temperature (above T_j max) the thyristor will not support a large voltage at all.

2.3 Turn-on by Excessive dV/dt

Any p-n junction has capacitance – the larger the junction area the larger the capacitance. If a voltage ramp is applied across the anode-to-cathode of a p-n-p-n device, a charging current i will flow in the device to charge the device capacitance according to the relation:

$$i = C\frac{dV}{dt}.$$

When i becomes great enough, the density of moving current carriers in the device induces switch-on.

2.4 Turn-on by Exceeding the Breakover Voltage

When the breakover voltage across a thyristor is exceeded, the thyristor turns on. This effect is not normally used as a triggering method (and most circuit designs attempt to avoid its occurrence) although there are circumstances in which it can become an advantage. For instance, when avalanche thyristors are connected in series it is inherent in the design that they should break over in this way and thus not be destroyed by voltage overload. In addition to this, the fall time of the forward voltage is considerably less (about 1/20th) when the thyristor is triggered by the exceeding of V_{BO} than it is when the device is gate-triggered; this is shown in Fig. 2.2 for thyristors type BTX92 and BTX95. It must be remembered, however, that although a thyristor switches faster with V_{BO} turn-on the permitted di/dt is lower.

In Fig. 2.3, the idealised main current and voltage waveforms are shown.

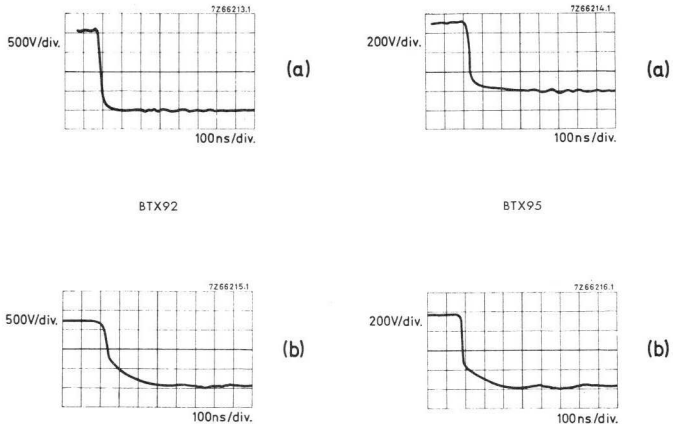


Fig. 2.2. Turn-on behaviour of two thyristors when triggering is effected by exceeding V_{BO} (a), and by gate-triggering (b).

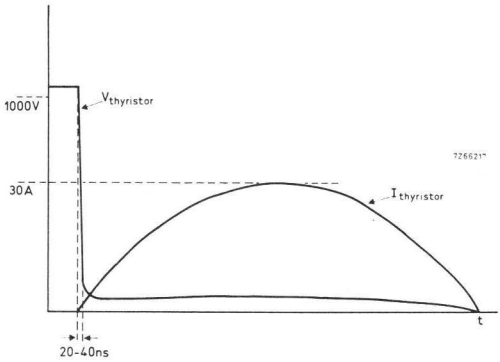


Fig. 2.3. Main current and voltage waveforms of thyristor under test.

2.5 Turn-on by Gate Triggering

Gate triggering is the usual method of turning a thyristor on. A variety of methods of gate triggering are in use and it is with these, and their relative merits, that a designer will be most intimately concerned.

2.5.1 The Gate Characteristic

This characteristic (Fig. 2.4) is often misinterpreted so the following explanation is put forward to show how the graph is built up.

To a first approximation, the gate-to-cathode junction of a thyristor acts as a p-n diode. Thus, when the current is plotted horizontally, the forward characteristic will be as shown in Fig. 2.5.

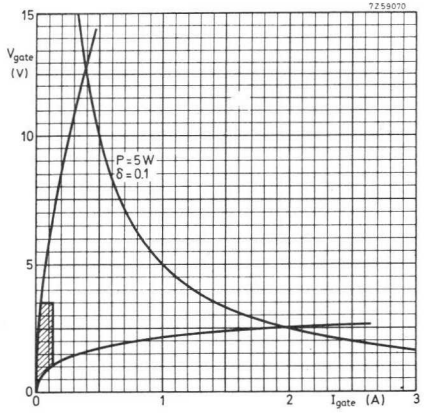


Fig. 2.4. The thyristor gate characteristic.

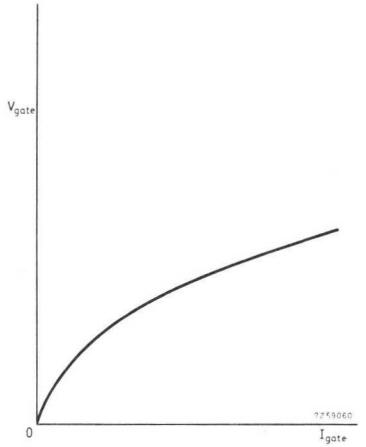


Fig. 2.5. Forward characteristic of gate.

Spread in Characteristics

As there is always a spread in forward characteristics of gate junctions (more than for normal diode junctions) one must, for a given thyristor type, draw a number of curves (Fig. 2.6) to cover all individual variations. For convenience, we draw only the two extreme curves (Fig. 2.7) – knowing that all of the others lie between them.

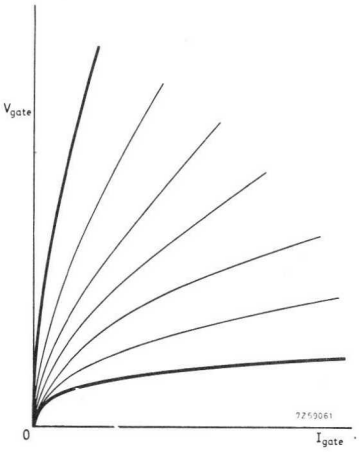


Fig. 2.6. Typical curves for a given type of thyristor.

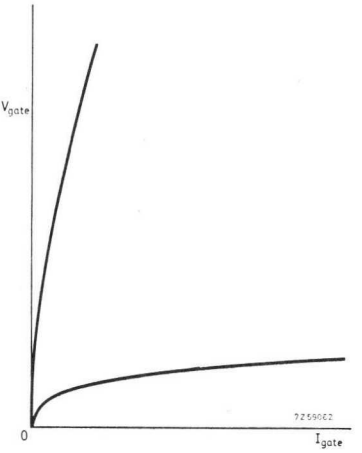


Fig. 2.7. The boundary curves.

Maximum Dissipation

Let us consider, for the moment, a typical thyristor with gate-to-cathode ratings and characteristics as follows:

Ratings		
Reverse peak voltage	(V_{RGM})	max. 5 V
Average power dissipation	(P_{GAV})	max. 0.5 W
Peak power dissipation	(P_{GM})	max. 5 W
Characteristics		
Voltage to trigger all devices	(V_{GT})	> 3.5 V
Voltage not to trigger any device	(V_{GD})	< 0.25 V
Current to trigger all devices	(I_{GT})	> 65 mA

(The voltages given are measured at the device terminals; they are *not* the open-circuit voltages of the gate trigger input circuits.)

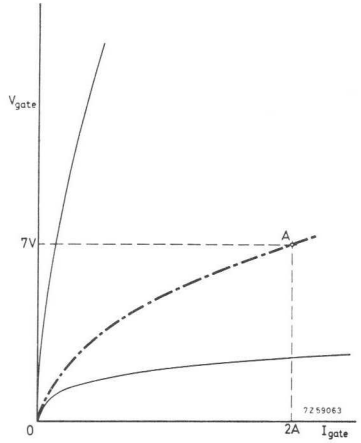


Fig. 2.8. Average gate forward characteristic.

Assuming that the gate forward characteristic is about average for the type, we will represent it by a chain dot line as shown in Fig. 2.8. If we take an arbitrary point (Point *A*) on this line, we can check its suitability as a triggering point by multiplying the corresponding current and voltage and comparing this product with the appropriate power rating. In the case of Point *A*, the voltage is 7 V and the current is 2 A so the power dissipated is 14 W. This is clearly in excess, not only of the continuous power rating (0.5 W), but of the peak power rating (5 W) as well. How-

ever, a point closer to the origin can be found at which the voltage/current product is 5 W. If this point were found for each curve in Fig. 2.6, the line joining these points would be a hyperbola (see Fig. 2.9). This line is obviously the ultimate power curve as 5 W is the peak power rating. If the 5 W curve is used, the duty cycle must not exceed

$$\frac{\text{average power rating}}{\text{peak power rating}} = \frac{0.5}{5} = 0.1.$$

Continuous steady operation would demand that the 0.5 W curve be used. In between these two curves is a region suitable for pulsed operation.

Thus, voltages and currents permitted for triggering lie within the area bounded by three curves (Fig. 2.10).

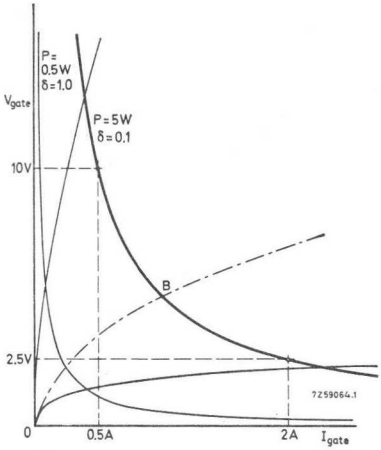


Fig. 2.9. The ultimate power curve.

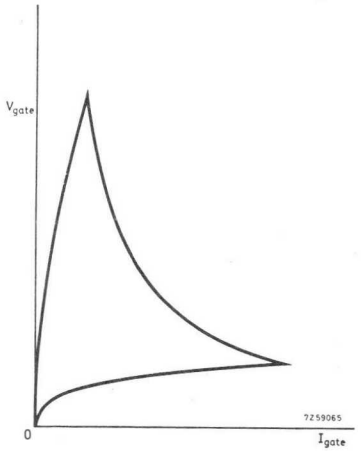


Fig. 2.10. Triggering area.

Triggering Circuit

Fig. 2.11 shows a typical triggering circuit. For maximum triggering certainty, the load line (for R) should touch the 5 W curve as shown in Fig. 2.12.

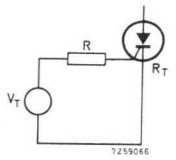


Fig. 2.11. Typical triggering circuit.

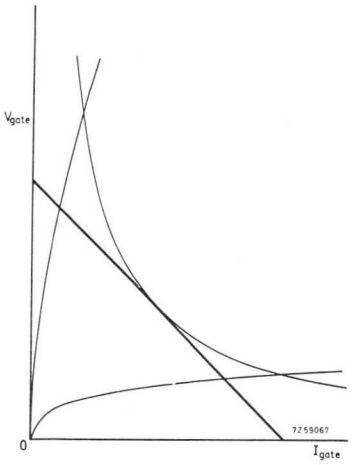


Fig. 2.12. Load line for maximum triggering certainty.

Minimum Triggering Level

At the other end of the scale, the level below which triggering becomes uncertain is determined by the minimum number of carriers needed in the gate-cathode junction to bring the thyristor into conduction by regenerative action. This minimum current decreases with increasing temperature. Fig. 2.13 shows this region. In Fig. 2.14 an expanded view of the region is given to illustrate the current-temperature dependency. Fig. 2.15 shows minimum gate voltage. Clearly, if triggering is to be guaranteed, the load line must not encroach into the region shown in Figs 2.14 and 2.15 (bearing in mind that the region varies with temperature).

We have now established the characteristic shown in Fig. 2.4.

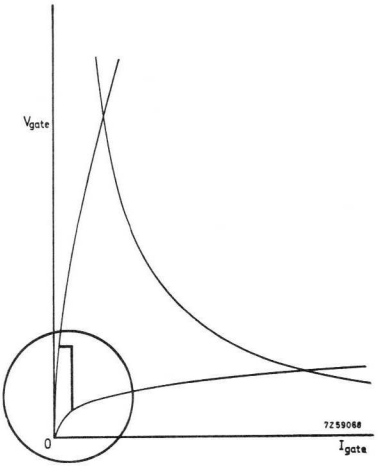


Fig. 2.13. Minimum triggering level.

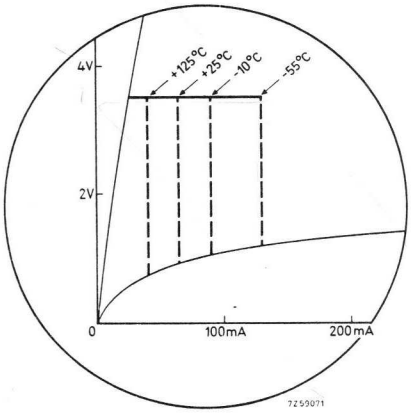


Fig. 2.14. Magnified view showing current-temperature dependency.

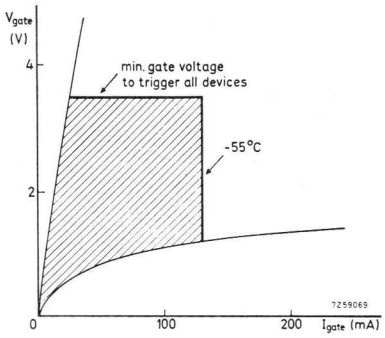


Fig. 2.15. Minimum gate voltage.

2.5.2 Gate-Cathode Impedance and Bias

Gate-cathode Resistance

An external resistance between gate and cathode bypasses some current round the gate junction; thus a higher anode current is required to initiate and maintain conduction. Low-current high-sensitivity thyristors can be triggered by such a low current through the gate junction that a specified external gate-cathode resistance is necessary to prevent triggering by thermally-generated leakage current. This resistance also bypasses some of the internal anode current caused by rapid rate-of-change of anode voltage (high dV/dt), and raises the breakover voltage. Latching and holding currents are also affected by the presence of this resistance and turn-off time is reduced because the external resistance assists in recovery of stored charge, raises holding current and raises the amount of anode current required to initiate re-triggering.

Gate-cathode Capacitance

A low shunt capacitive reactance can, at high frequencies, reduce the sensitivity of a thyristor to dV/dt of anode voltage just as a resistor can, but it maintains higher sensitivity to d.c. and low-frequency gate signals. This may be particularly useful if high-frequency noise is present in either the anode or the gate circuit.

At the triggering point, however, gate voltage must increase as anode current increases, so a capacitor between gate and cathode will tend to retard the triggering process and the di/dt of anode current. In addition, when the thyristor is on, the capacitor is charged to the gate-cathode voltage so, when the anode current is removed, the capacitor can still supply triggering current for a while and may prevent commutation. A compromise in the size of the capacitor will therefore be necessary to suit the prevailing circumstances and requirements. (Generally, we do not recommend a capacitor in this position.)

Gate-Cathode Inductance

Inductive reactance between gate and cathode reduces sensitivity to slowly changing anode current or gate source current whilst maintaining sensitivity to rapid changes. However, this effect is not often desired.

Positive Gate Bias

Positive gate current, if flowing when reverse voltage is applied to the anode, increases reverse blocking (leakage) current substantially; so the thyristor dissipates additional power. This situation should be avoided or, if it is impossible to do so, one must either make allowance for the additional power or limit it to a negligible value.

If derating curves are given for this effect, the temperature derating (ΔT) must be found and subtracted from the maximum allowable stud temperature (found from the device derating curve); if the device is lead-mounted, ΔT must be subtracted from the value found from the ambient temperature curve. Derating becomes negligible if the gate voltage is less than 0.25 volts or ΔT is 1 °C or less.

A diode clamping circuit can be connected to the gate, to attenuate positive gate signals when the anode is negative. A fast series diode in the gate lead may be necessary to protect the gate circuit when the thyristor turns on with high di/dt. This is explained in Chapter 1, Paragraph 1.4.2 and illustrated in Fig. 1.14.

Negative Gate Bias

The gate should never be allowed to become more negative with respect to cathode than the specification permits. This can be arranged by means of a diode clamping circuit which can simply be a diode connected between cathode and gate.

If the clamping between cathode and gate is removed while the thyristor is on, considerable negative gate current may flow. As this current would be limited only by the impedance of the gate circuit, it could be large enough for the allowable gate dissipation to be exceeded; this, in turn, could lead to failure of the thyristor.

Negative gate bias, when the anode is positive, tends to increase the forward breakover voltage and the dV/dt capability; this effect is greater in small junction-area devices than it is in those with a large junction area.

2.6 di/dt and Switching Losses

When a thyristor is turned on, power is switched and losses occur during the time taken for the forward voltage to drop from the blocking value

to the conducting value; thus turn-on time is a vital factor in the consideration of dissipation losses. A limiting factor, however, in any attempts to reduce turn-on time, is the maximum allowable di/dt in the forward direction; if this maximum value is exceeded, local heating of the crystal will occur, and may result in breakdown of the thyristor.

Where high di/dt is encountered, a fast diode in series with the gate may be necessary to protect the gate circuit (see Chapter 1).

Fig. 2.16 shows the three important stages of turn-on – t_d, t_r and t_s

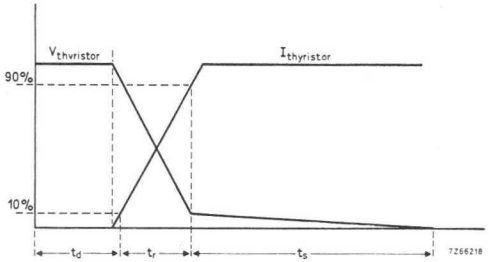


Fig. 2.16. The three stages of thyristor turn-on.

2.6.1 Current Rise Time, t_r

Most of the switching losses occur during the time (t_r) taken by the forward current to rise from 10% to 90% of its maximum value; this time is determined by the maximum rate at which plasma can spread in the crystal and is given by:

$$t_r \approx 2\sqrt{\left(\frac{t_1 t_2}{\alpha_1 + \alpha_2 - 1}\right)},$$

where

t_r is the forward current rise time from 10% to 90%,

t_1 and t_2 are the base transit times,

α_1 and α_2 are the current gain factors (base gains, see 2.1).

2.6.2 Spreading Time, t_s

The spreading time is the time, after t_r, taken for the entire crystal to

become conducting. It, of course, depends on the spreading velocity, V, which is given by

$$V = k\sqrt{\frac{D}{t_r}},$$

where D is the diffusion constant, and t_r has the same meaning as in the previous paragraph; the constant k is about 1.5.

Fig. 2.17 shows t_d and t_r plotted against gate current for a BTW23 thyristor.

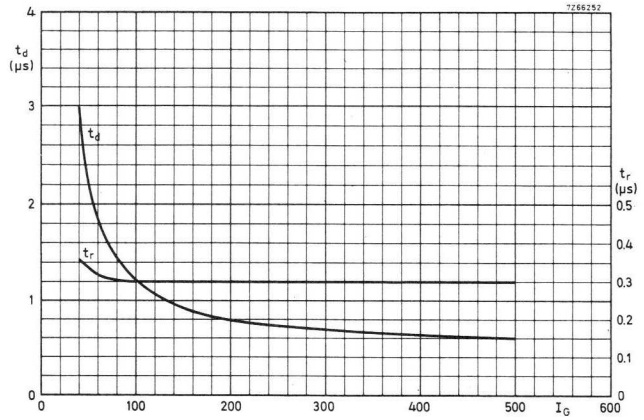


Fig. 2.17. t_r and t_d plotted against I_g for the BTW23.

2.6.3 Calculation of Switching Losses

Fig. 2.18 shows a theoretical approximation of the turn-on phenomenon. In time t_1, the forward voltage drops from V_3 to V_2 and the forward current rises from zero to I. Thus the energy dissipated in the t_1 interval is:

$$E_{t_1} = \frac{1}{T}\int_0^{t_1} V f(t)\, I_g(t)\, \mathrm{d}t,$$

where $T = t_1$.

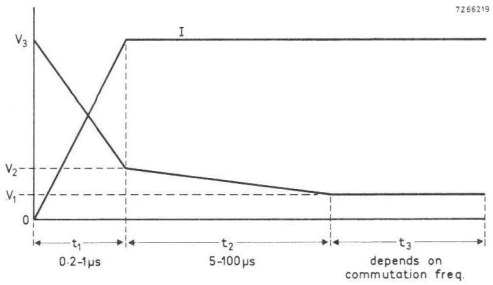


Fig. 2.18. Theoretical approximation of turn-on.

Insertion of a numerical value for t_1 (assuming a linear time function) gives

$$E_{t_1} = {}^1/_6 \, V_3 \, I t_1 \text{ (Ws)},$$

if V_2 is neglected because $V_3 \gg V_2$. (The final t_1 is retained for use in the overall expression.)

During the t_2 interval, the energy dissipated is

$$E_{t_2} = \frac{1}{T} \int_{t_1}^{t2} Vh(t) \, Ik(t) \, \mathrm{d}t,$$

where $T = t_2$.

By a similar method to that used for the t_1 interval

$$E_{t_2} = \tfrac{1}{2} (V_2 - V_1) \, I t_2 \text{ (Ws)}.$$

During the t_3 interval, the energy (steady state) dissipated is

$$E_{t_3} = V_1 I t_3 \text{ Ws}.$$

So the total switching power losses, including steady-state losses, are:

$$P_{total} = \frac{I \{ {}^1/_6 \, V_3 t_1 + \tfrac{1}{2} (V_2 - V_1) \, t_2 + V_1 t_3 \}}{T} \text{ (W)},$$

where T is the total "on" period $(t_1 + t_2 + t_3)$.

In Fig. 2.19, switching power dissipation is given as a function of frequency, with

$I = 10$ A steady state,
$V_3 = 400$ V.
$V_2 = 2$ V,
$V_1 = 1.2$ V
$t_1 = 2$ μs
$t_2 = 50$ μs
$t_3 = 1/(2f) - (t_1 + t_2)$,

where f is the switching frequency.

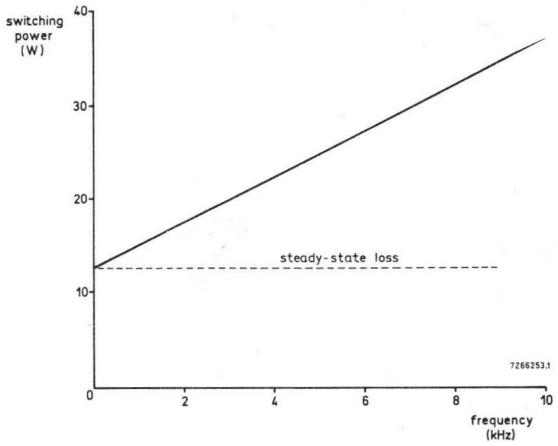
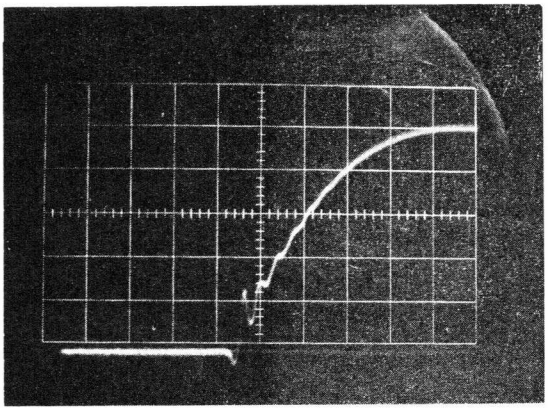


Fig. 2.19. Switching loss as a function of frequency.

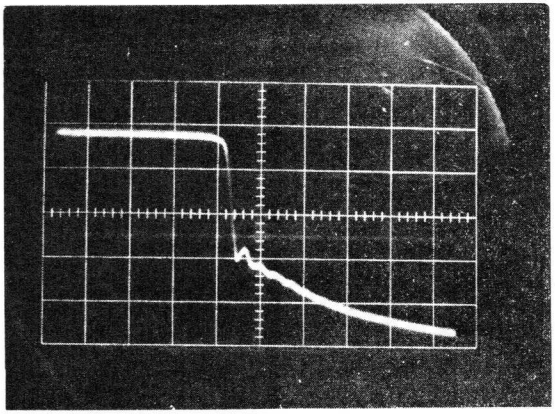
Clearly, switching losses become more important as switching frequency increases. When $1/(2f) < t_1 + t_2$ it is better to use two smaller thyristors in parallel or to choose a thyristor with a greater spreading velocity.

Fig. 2.20 shows examples of thyristor turn-on and in Fig. 2.21 a diagram for calculation of turn-on losses in the thyristor Type BTW23 is given.



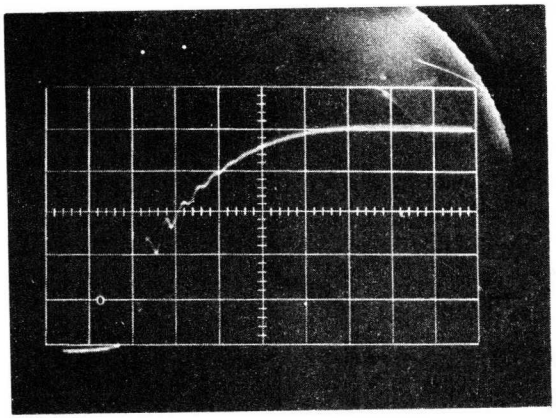
Current Waveform
$t = 0.5$ μs/div.

$I_{TM} = 200$ A
$V_{TM} = 1000$ V



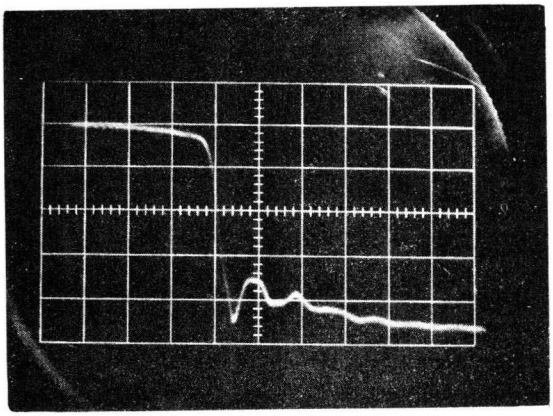
Voltage Waveform
$t = 0.2$ μs/div.

Fig. 2.20 (a). Turn-on waveforms (at 25 °C) for type BTW24 thyristor.



Current Waveform
$t = 0.5\ \mu s$/div.

$I_{TM} = 100\,A$
$V_{TM} = 1000\,V$



Voltage Waveform
$t = 0.2\ \mu s$/div.

Fig. 2.20 (b). Turn-on waveforms (at 25 °C) for type BTW92 thyristor.

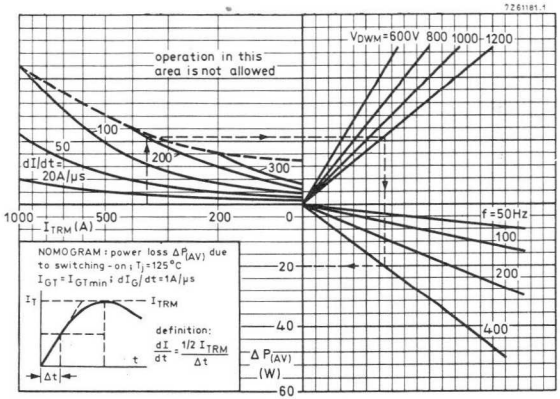


Fig. 2.21. Turn-on losses caused by $\mathrm{d}i/\mathrm{d}t$ *(at* $I_g = 1.0$ *A and* $\mathrm{d}I_g/\mathrm{d}t = 1$ *A/μs) for BTW23 thyristor.*

3 Thyristor Turn-off Methods

3.1 Introduction

A thyristor will turn off in either of two general circumstances – if the main current drops below the holding value (sometimes known as "natural turn off") or if the anode-cathode voltage is reversed. It is important to remember, however, that the thyristor will turn on again if the reapplied forward voltage occurs before a minimum time period has elapsed; this is because the charge carriers in the thyristor at the time of turn-off take a finite time to recombine.

Anode-cathode voltage reversal, or commutation, is contrived by two main methods – natural commutation and forced commutation (which can be effected by the mains or by means of special circuits).

3.2 Turn-off Time and Reverse Recovery

Turn-off time is that period between the point at which forward current reverses and the earliest point at which the thyristor can block reapplied

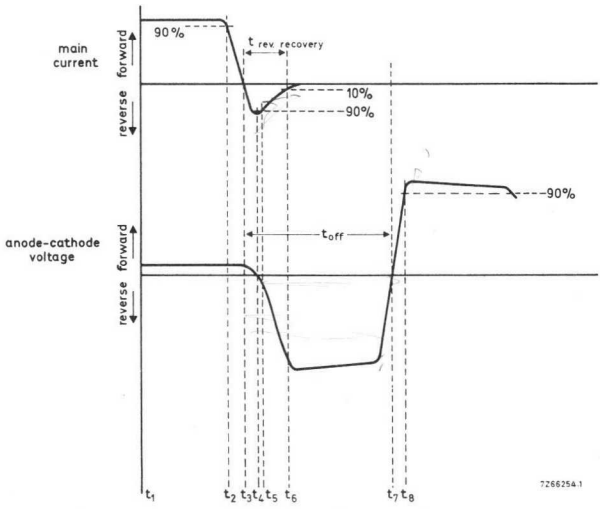


Fig. 3.1. Turn-off waveforms and times.

forward voltage (t_3 to t_7 in Fig. 3.1). Reverse recovery time is the period during which reverse recovery current flows (t_3 to t_6 in Fig. 3.1); it is the period between the point at which forward current ceases and the earliest point at which the reverse recovery current has dropped to 10% of its peak value.

3.2.1 Turn-off Time

As we have seen, if forward voltage is applied to a thyristor too soon after the main current has ceased to flow, the thyristor will turn on. The reason for this can be understood in terms of the physical mechanism of thyristor action as outlined in Chapter 1.

The turn-off time (t_3 to t_7 in Fig. 3.1) is not constant and increases with:

(a) increase in junction temperature
(b) increase in forward current amplitude (t_1 to t_2)
(c) increase in rate of reduction of forward current (t_2 to t_4)
(d) decrease in peak reverse current (t_4)
(e) decrease in reverse voltage (after t_6)
(f) increase in the rate of rise of forward blocking voltage (t_7 to t_8)
(g) increase in forward blocking voltage
(h) increase in external gate impedance
(j) increase in positive gate bias.

Thus the turn-off time is specified for defined operating conditions. Circuit turn-off time is the turn-off time that the circuit presents to the thyristor; it must, of course, be greater than the thyristor turn-off time.

3.2.2 Reverse Recovery

Reverse recovery time, in typical thyristors, is of the order of a few microseconds. This time increases with increase of forward current and also increases as the forward current decay rate decreases.

Reverse recovery current can cause high values of turn-on current in full-wave rectifier circuits (where thyristors are used as rectifying elements) and in certain inverter circuits. When reverse recovery current ceases (which it can do suddenly), large voltage transients and radio frequency interference can occur. It should be remembered, too, that if thyristors are connected in series, the reverse voltage distribution can be seriously affected by mismatch of reverse recovery times.

3.3 Natural Commutation

The thyristor main current can be interrupted by means of a switch (either in series or parallel with the thyristor). The switch must be operated for at least the device turn-off time and it must be remembered that opening of a parallel switch and closing of a series switch imposes high dV/dt on the thyristor. Natural commutation is the name given to this type of turn-off.

It is rare, in practice, for a mechanical switch to be suitable for this type of commutation; thus a variety of suitable static switching circuits have been devised.

3.4 Forced Commutation

If, as is usually the case, natural commutation is unsuitable for the application in hand, forced commutation must be used. In forced commutation, current is forced through the thyristor in the reverse direction. The advantage of forced commutation, which makes it generally preferable to natural commutation, is that it reduces turn-off time.

Forced commutation can be subdivided into two main categories – self commutation and commutation by external means.

3.4.1 Forced Commutation by Self Commutation

In self-commutation circuits the thyristor will automatically turn off at a predetermined time after application of the trigger pulse. The thyristor conduction period is determined by a property of the commutation circuit, such as the resonant cycle of an *LC*-circuit, or the volt.second capability of a saturable core reactor. The energy needed for commutation is delivered by a capacitor included in the commutation circuit.

LC circuit in Series with the Thyristor

When the thyristor is triggered, the resulting main current excites the resonant circuit. After half a resonant cycle, the *LC* circuit starts to reverse the anode current and turns the thyristor off. Thus the thyristor conduction interval is half a resonant cycle. It is essential, for proper commutation, that the resonant circuit be less than critically damped.

Fig. 3.2 shows the circuit diagram and Fig. 3.3 gives the relevant waveforms.

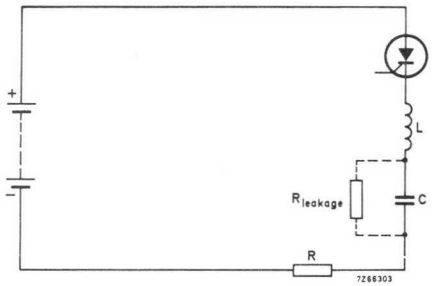


Fig. 3.2. Self commutation with LC circuit in series with thyristor.

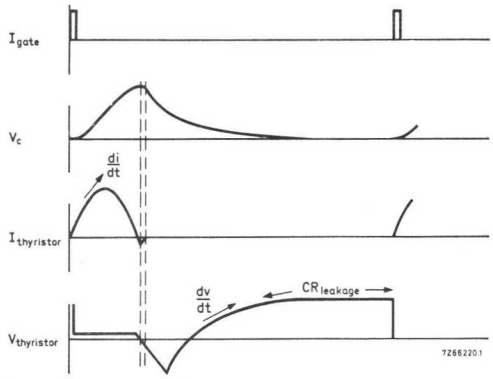


Fig. 3.3. Waveforms for LC series self commutation (Fig. 3.2).

LC Circuit in Parallel with the Thyristor

Initially C charges to the supply voltage E. When the thyristor is triggered, the load current I_R flows through R but at the same time C discharges through the thyristor in the forward direction. When it has discharged (i.e. after one resonant half-cycle of the LC circuit), it begins to charge in the opposite direction and, when this charging current is greater than the thyristor forward current, the thyristor turns off.

See Fig. 3.4 for the circuit diagram and Fig. 3.5 for the waveforms.

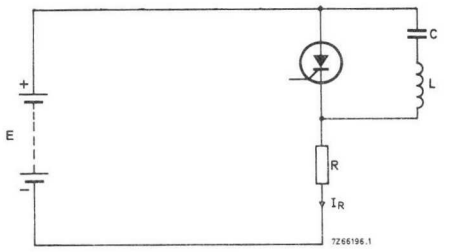


Fig. 3.4. Self commutation circuit with parallel LC network.

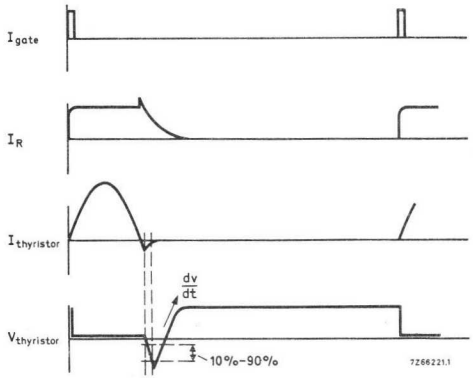


Fig. 3.5. Waveforms for LC parallel self commutation (Fig. 3.4).

Capacitor and Saturable Core Reactor in Parallel with the Thyristor

The circuit chosen (Fig. 3.6) to demonstrate this type of self commutation is that known as the Morgan chopper; it is not the only possible arrangement but it serves well to illustrate the method.

Initially, C is charged to the battery voltage and the reactor is saturated positively. When the thyristor is triggered, the voltage across the capacitor is applied to L_2 – pulling the core out of positive saturation. Between t_1 and t_2 (Fig. 3.7), the load current flows through R_L and, of course, the capacitor is discharging. When t_2 is reached, the core goes into negative saturation and the inductance of L_2 changes from a high (unsaturated) value to a low saturated value. Because of the low value of L_2, C proceeds to discharge and then to charge very rapidly in the opposite polarity

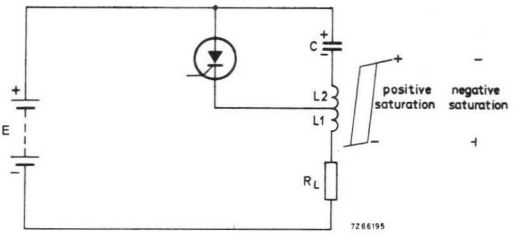


Fig. 3.6. Self commutation circuit using capacitor and saturable reactor.

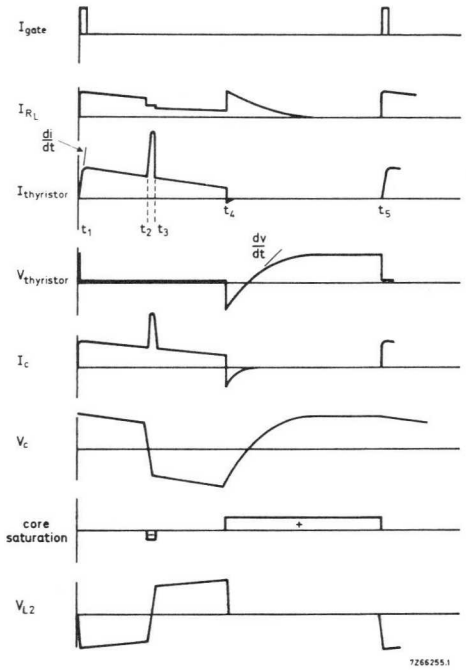


Fig. 3.7. Waveforms for the capacitor and saturable reactor circuit (Fig. 3.6).

(between t_2 and t_3); this charging current reaches maximum then, as it decreases, the voltage across L_2 reverses and the core comes out of saturation. The inductance rises again to a high value and C continues to discharge slowly (t_3 to t_4). At t_4 the core goes into positive saturation and the capacitor forces current through the thyristor, in the reverse

direction, via the low inductance of L_2; this reverse current turns off the thyristor. Capacitor C then charges to the battery voltage and the circuit waits for the next trigger pulse.

3.4.2 Forced Commutation by External Means

A.C. Line Commutation

If the supply is an alternating voltage, the thyristor can conduct only during the positive half cycle.
Fig. 3.8 shows a circuit arrangement and Fig. 3.9 shows the waveforms.

It is important to ensure that the duration of a half cycle is greater than the thyristor turn-off time.

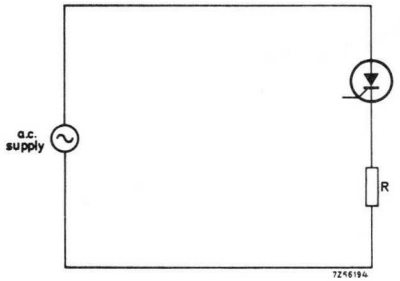


Fig. 3.8. A.C. line commutation.

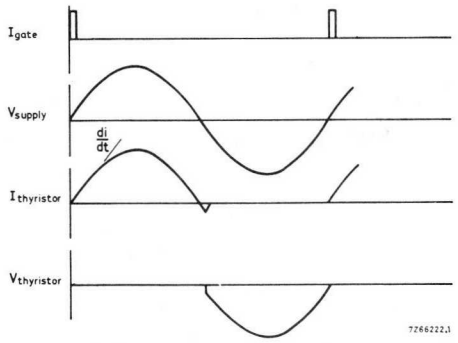


Fig. 3.9. A.C. line commutation waveforms (Fig. 3.8).

Commutation by a Second Load Carrying Thyristor

If TH_2 is conducting, C will be charged with the polarity shown in Fig. 3.10. When TH_1 is triggered, C is switched across TH_2 via TH_1. The discharge current of C opposes the main current in TH_2 and turns TH_2 off Fig. 3.11 shows the waveforms.

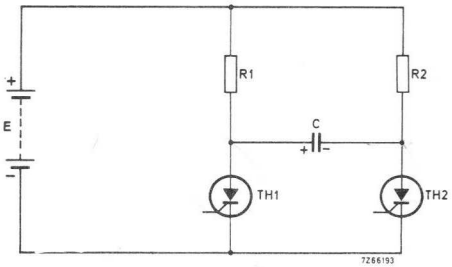


Fig. 3.10. Commutation by a second load-carrying thyristor.

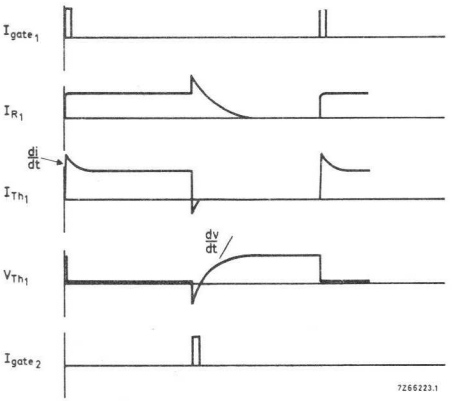


Fig. 3.11. Waveforms for commutation by a second load-carrying thyristor (Fig. 3.10).

Commutation by an Auxiliary Thyristor

The circuit in Fig. 3.10 could be used for this purpose if only one of the thyristors carried the load current and the other simply acted as an auxiliary turn-off thyristor; the auxiliary thyristor would have an anode resistor of, say, ten times the value of the load resistor

Another circuit is that shown in Fig. 3.12. TH_2 must be triggered first to charge C to the polarity shown; when C is charged, the current through TH_2 drops below the holding value and TH_2 turns off. When TH_1 is triggered, current flows in two paths – load current through R and commutation current through L and D to C. The charge on C becomes rever-

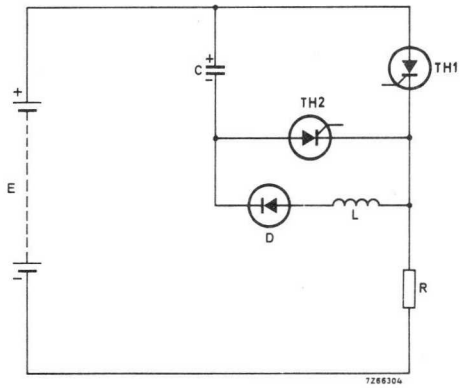


Fig. 3.12. Commutation by an auxiliary thyristor.

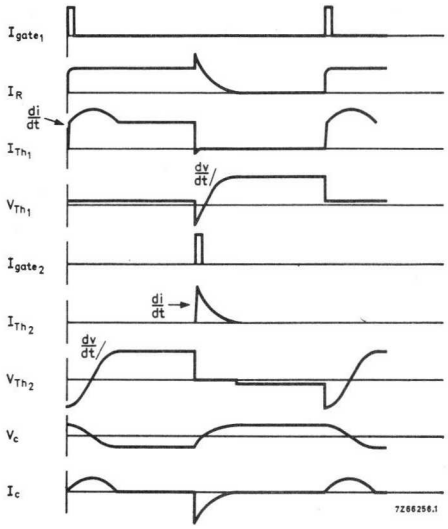


Fig. 3.13. Waveforms for commutation by an auxiliary thyristor (Fig. 3.12).

sed and C remains isolated by D until TH_2 is triggered and C is thus connected across TH_1 – turning it off. Waveforms are given in Fig. 3.13.

A circuit which has an outstanding ability to commutate reliably is the Jones chopper (Fig. 3.14). Initially C is discharged. When TH_1 is triggered, current is induced in L_2 by the close coupling with L_1 and C becomes charged in the polarity shown. When TH_2 is triggered, TH_1 becomes reverse biased and turns off; C then becomes charged in the opposite polarity. The next time TH_1 is triggered, C discharges through L_2 and TH_1 - thus its polarity is reversed and ready for the next trigger pulse.

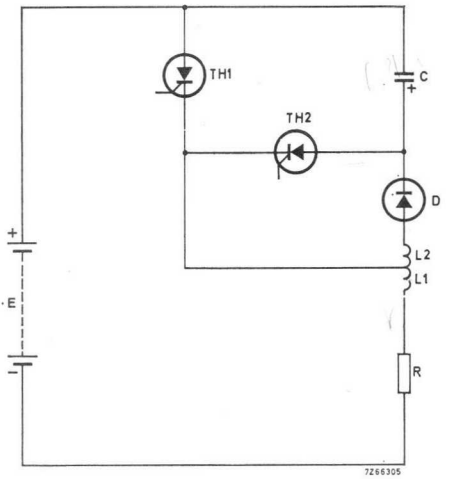


Fig. 3.14. The Jones Chopper.

Better turn-off times can be obtained with this circuit than with the previous one; however, higher voltages appear across the thyristors Waveforms are shown in Fig. 3.15.

Commutation by an External Pulse Source

Fig. 3.16 shows a suitable circuit for this type of commutation. It is important that the transformer is so designed that it will not saturate in the conditions it will meet in this circuit; at the same time, as the secondary is in series with the load, it must be capable of carrying the load current with a small voltage drop compared with the supply voltage.

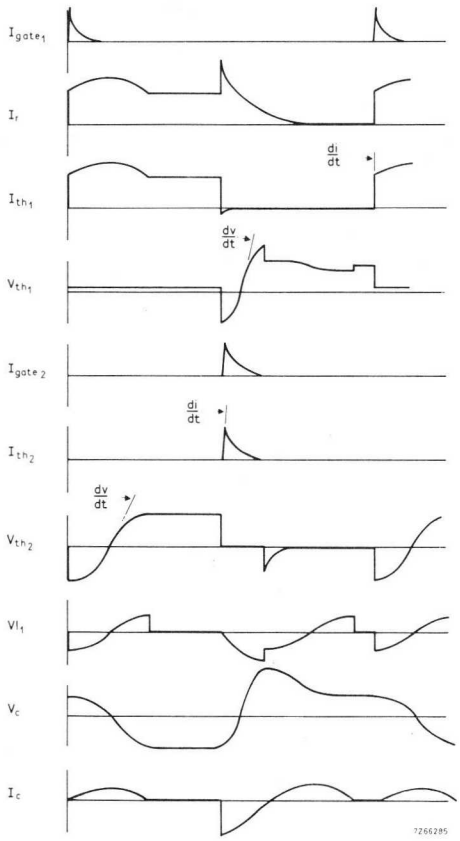


Fig. 3.15. Waveforms for the Jones Chopper circuit (Fig. 3.14)

When TH_1 is triggered, the main current flows through the pulse transformer and the load. A positive pulse is now needed at the thyristor cathode to turn it off; this is supplied by the external pulse generator via the pulse transformer. C is charged to only about one volt when the thyristor is on and, for the duration of the turn-off pulse, it can be assumed to present zero impedance. Thus the pulse at the cathode reverses the thyristor voltage for the required turn-off time and supplies the reverse recovery current. Waveforms are shown in Fig. 3.17.

It is possible to dispense with C if a saturable-core transformer is used.

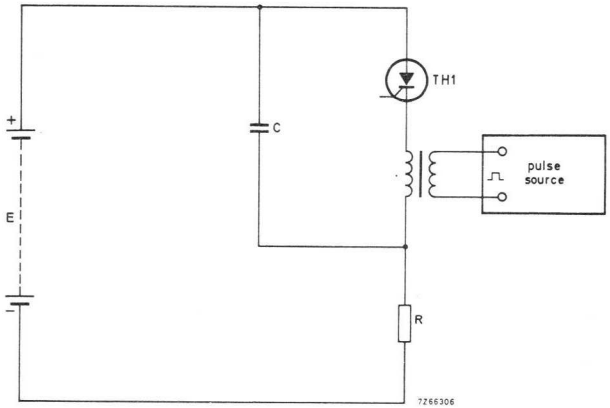


Fig. 3.16. Commutation by an external pulse source.

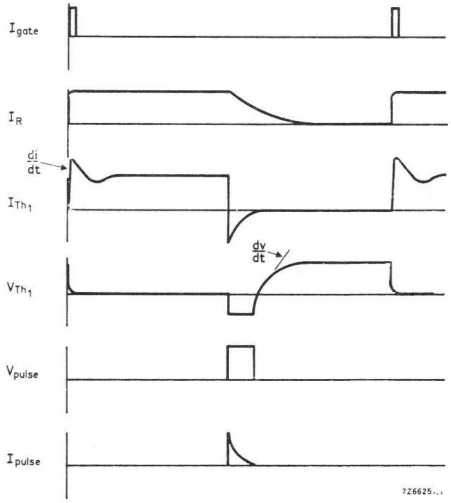


Fig. 3.17. Waveforms for external pulse commutation circuit (Fig. 3.16).

3.5 Application of Turn-off Methods

Table 3.1 outlines the areas in which the various methods of thyristor turn-off are most suitable.

Table 3.1 Turn-Off Methods

method			sect.	field of applications	commutation energy delivered by	commutation period determined by	inherent turn-off time
natural commutation			3.3	alarm and crowbar circuits; certain low-current information read-out circuits; pulse modulator circuits	—	—	approx. 50-1000 μs
forced commutation	self-commutation	*LC*-circuit in series with thyr. *LC*-circuit in parallel with thyristor cap. and sat. core reactor in parallel with thyristor.	3.4.1	series inverters choppers static d.c. switches	commutating capacitor	properties of commutation circuit	see specification sheet
	commutation by external means	a.c. line commutation	3.4.2	controllable rectifiers controllable a.c. converters frequency converters static a.c. switches	a.c. supply source	supply frequency	
		commutation by a second load-carrying thyristor	3.4.2	parallel inverters power flip flop resonant impulse commutated inverters	commutating capacitor	trigger frequency	
		commutation by an auxiliary thyristor	3.4.2	choppers static d.c. switches			
		commutation by an external pulse source	3.4.2	choppers static d.c. switches some inverter types	pulse source		

It should be mentioned that triacs, because of their relatively low dV/dt capability, are generally not very suitable for use with forced commutation methods. Mains commutation, in which reversal of the mains supply voltage turns the triac off, is the usual method used. Triacs have been used with this type of commutation in a variety of applications including control of inductive loads, temperature control, closed-loop single and three-phase power control and static a.c. switches.

Very inductive loads, however, especially d.c. inductive loads, do give severe post-conduction dV/dt problems with triacs; with such loads it is necessary to provide a safeguard to ensure reliable commutation. Fig. 3.18 gives a good illustration of the problem. When the d.c. output voltage drops to zero, the load inductance forces current through the rectifier

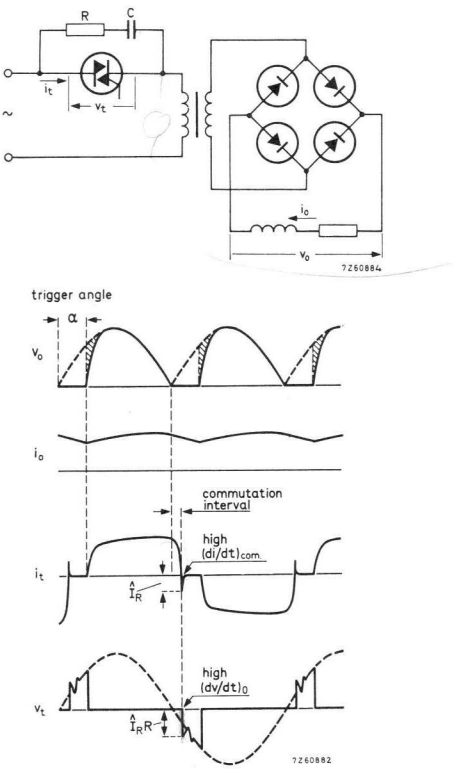


Fig. 3.18. Triac control of transformer supplying rectifier with inductive load.

diodes – this effectively shorts the transformer secondary for some time after the zero transitions of the mains voltage and applies a reverse voltage to the triac (turning it off). Because of transformer leakage inductance, the triac does not turn off immediately but continues to conduct over the commutation interval. During this interval, a high current decay-rate $((\mathrm{d}i/\mathrm{d}t)_{\mathrm{com}})$ results because the leakage inductance is small and the secondary effective short makes fairly heavy demands on the primary. The high $(\mathrm{d}i/\mathrm{d}t)_{\mathrm{com}}$ gives a high rate of voltage rise $((\mathrm{d}V/\mathrm{d}t)_0)$. As the current decays rapidly, the peak reverse recovery current, $\hat{I}_R$, is fairly large; at turn-off, $\hat{I}_R$ is abruptly transferred to the transient suppression elements C and R so the voltage across the triac rises stepwise to $\hat{I}_R R$ (C uncharged initially). Owing to the high value of both $(\mathrm{d}i/\mathrm{d}t)_{\mathrm{com}}$ and $(\mathrm{d}V/\mathrm{d}t)_0$, loss of control follows unless measures are taken to prevent it.

A saturable choke in series with the transformer primary provides a satisfactory solution (Fig. 3.19). Saturation should occur at a fraction of

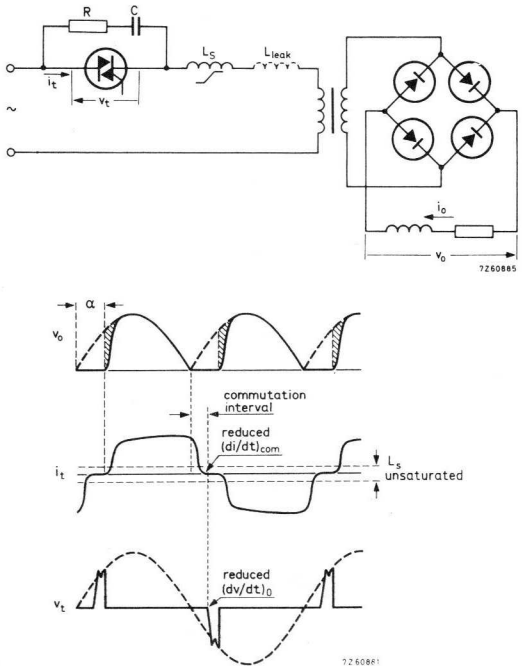


Fig. 3.19. Insertion of saturable choke to ensure commutation.

the rated load current so that the loss in rectifier output voltage (hatched V_0 areas) is minimised. At low currents, the high inductance "softens" commutation and thus eliminates transients. The choke delays voltage rise and thus provides a quiescent period of a few tens of microseconds, during the commutation interval, during which the triac can recover. There is no difficulty in designing the choke so that $(di/dt)_{com}$ and $(dV/dt)_0$ are sufficiently reduced for control to be reliable.

3.6 Calculation of Switching Losses

Turn-off switching losses can be obtained directly from switching loss diagrams; Figs 3.20 and 3.21 show, respectively, switching loss diagrams for a slow and a fast thyristor.

An example is given on each diagram to make the method clear.

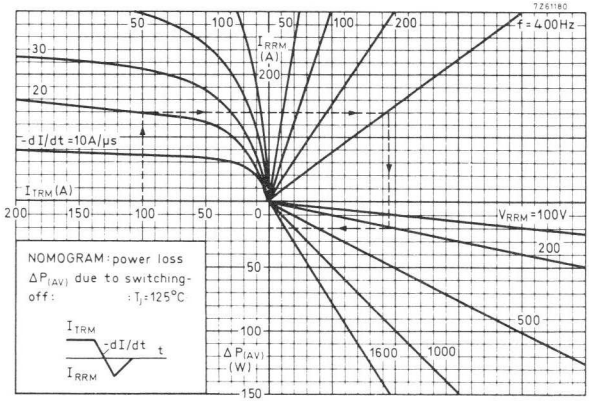


Fig. 3.20. Turn-off losses diagram (BTW23).

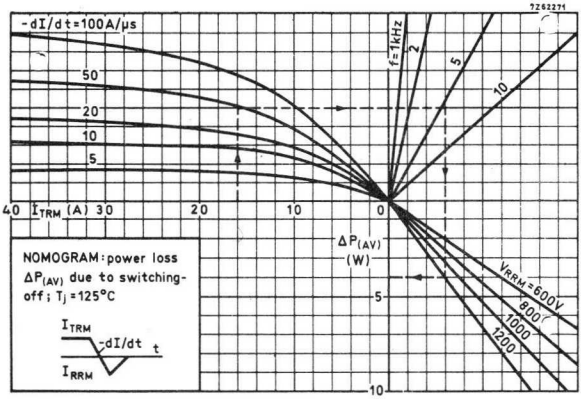


Fig. 3.21. Turn-off losses diagram (BTW30 series).

4 Protective Measures

4.1 Cooling

4.1.1 Introduction

Power devices are mounted on heatsinks to remove internally generated heat. Use of a suitable heatsink enables the power device to be operated at heavy loads without the maximum permissible junction temperature being exceeded. When large power dissipation levels are involved, forced air or water circulation may become necessary to provide sufficient cooling.

The heatsink has a relatively large thermal time constant, so it will be effective in limiting the junction temperature to the rated level only during long load cycles (several minutes duration). For short load cycles (from about 1 s to subcycle surge conditions) the rise in temperature of the heatsink will be negligible. Under such conditions, the peak junction temperature will be determined by the thermal time constant of the device itself (a few seconds), or even by the heat storage capacity of the junction area alone (thermal time constant a few milliseconds), depending on how long the load is applied.

For effective heatsink design it is necessary to have the following data: maximum rated junction temperature, thermal resistance of the device, thermal resistance from the device to the heatsink (obtained from the data sheets *), power dissipation, and ambient temperature (dictated by the application).

Heat transfer direct from the case of the device to ambient can constiture an important factor in heatsink design, since it materially reduces the power flow via the heatsink path. The graphs given in this section allow for the effect of the envelope thermal resistance, thus ensuring optimum heatsink design.

4.1.2 Heat Transfer Theory

At temperature equilibrium, the total energy supplied per second is equal

* Where data sheets are mentioned, the reader is referred to our Data Handbook System.

to the total energy removed per second. The equation for heat transmission is, therefore:

$$P = \eta_h h_t a_t \Delta T \tag{4.1}$$

where P = power dissipation of the device
η_h = heatsink efficiency
h_t = total heat transfer coefficient,
a_t = total heat dissipation area,
ΔT = temperature difference.

Total Heat Transfer Coefficient

Heat transfer can take place by free or forced convection, and by radiation. The following heat transfer coefficients may be distinguished:

h_c, the transfer coefficient for free (natural) convection;
h_f, the transfer coefficient for forced convection;
h_r, the transfer coefficient for radiation.

The total heat transfer coefficient, h_t equals $h_c + h_r$ for free convection and $h_f + h_r$ for forced convection.

Heat Transfer by Free Convection

The term free convection applies when the movement of air is due exclusively to local temperature differences in the vicinity of the heatsink. The heat transfer coefficient h_c, expressed in terms of W/m^2 deg C, can be found from the following expression:

$$h_c = 1.4\,(\Delta T_{h-a}/l_c)^{1/4} f_p f_a = A f_p f_a, \tag{4.2}*$$

where ΔT_{h-a} = temperature difference in degC between heatsink and ambient,
l_c = effective length of heatsink in m, see Table 4.1,
f_p = position correction factor, see Table 4.2,
f_a = altitude correction factor, see Fig. 4.1.

The factor $A = 1.4\,(\Delta T_{h-a}/l_c)^{1/4}$ can be found graphically from Fig. 4.2.

* See Ref. 1

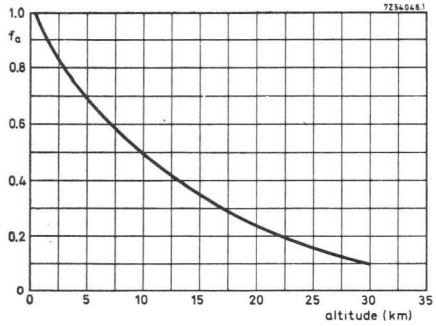


Fig. 4.1. Altitude correction factor f_a vs altitude.

Table 4.1 Effective length l_c of heatsink (free convection)

shape	position	effective length l_c
rectangular	vertical	height (max. 0.6 m)
	horizontal	$\frac{\text{length times width}}{\text{length plus width}}$
circular	vertical	$\pi/4$ times diameter
	horizontal	half diameter

Table 4.2 Position correction factor f_p (free convection)

position	side	correction factor f_p
horizontal	top	1.29
	bottom	0.63
	combined effect	0.96
vertical	either	1
	combined effect	1

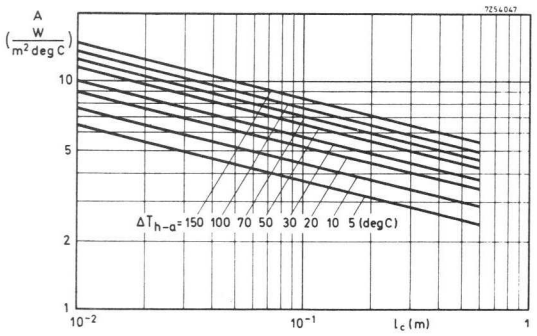


Fig. 4.2. Factor A vs heatsink effective length L_c.

Heat Transfer by Forced Convection

In the case of forced convection, circulation of the ambient air is caused by blowers or fans. The transfer coefficient h_f, expressed in W/m² degC, can be found from the equation:

$$h_f = \{0.055\, \gamma_a/(\mu^3/\varrho^3)^{1/4}\} \cdot (v^3/l_f)^{1/4} \cdot f_a, \tag{4.3a}$$

which, if

$$0.055\, \gamma_a/(\mu^3/\varrho^3)^{1/4} = B \quad \text{and} \quad (v^3/l_f)^{1/4} = C,$$

may be written:

$$h_f = BCf_a. \tag{4.3b}$$

In these expressions:

γ_a = thermal conductivity of air (W/m³deg C),
μ = kinematic viscosity of air (kg/ms),
ϱ = specific density of air (kg/m³),
v = air velocity in the vicinity of the heat sink (m/s),
l_f = effective length of heatsink at forced convection (m).

The value of l_f depends only on the shape of the heatsink. For a rectangular sink, l_f is the length in the direction of the air flow. For a circular heatsink l_f equals $\pi/4$ times the diameter. The factors B and C have been plotted in Figs 4.3 and 4.4 respectively.

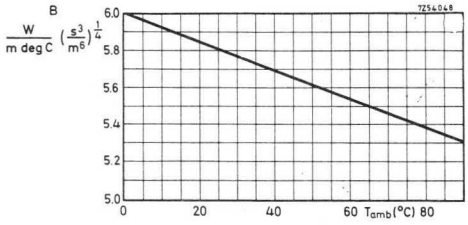


Fig. 4.3. Factor B vs ambient temperature, T_{amb}.

The effectiveness of the heatsink can be increased by painting its surface a dull colour. At air velocities exceeding 3 m/s heat removal by forced convection will, however, be predominant, and the effect of surface coating can then be ignored.

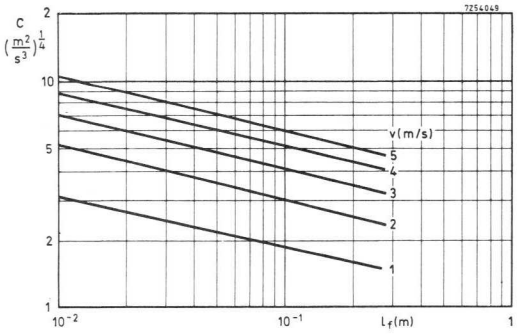


Fig. 4.4. Factor C vs heatsink effective length, L_f.

Heat Transfer by Radiation

Apart from being transferred by conduction and convection, heat can be radiated. The transmission coefficient for this type of heat transfer, h_r, expressed in terms of W/m²deg C, can be found from the equation:

$$h_r = \frac{\sigma\,(T_h^4 - T_{amb}^4)}{\Delta T_{h-a}} \cdot \varepsilon f_r = D \cdot \varepsilon f, \tag{4.4}$$

where σ = Stefan-Boltzmann constant (7.51×10^{-8} W/m² · °K⁴),
T_h = absolute temperature of the heatsink (°K),
T_{amb} = absolute ambient temperature (°K),
ε = emissivity coefficient, see Table 4.3,
f_r = radiation form factor, see Fig. 4.5.

The factor D can be found from the graph plotted in Fig. 4.6.

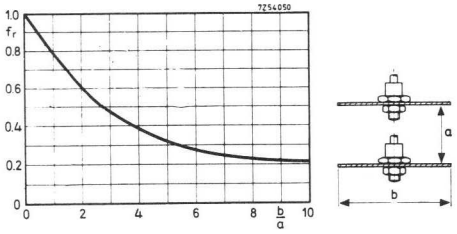


Fig. 4.5. Radiation form factor f_r vs ratio b/a for each of the facing sides of the heatsinks; the other sides radiate in free space.

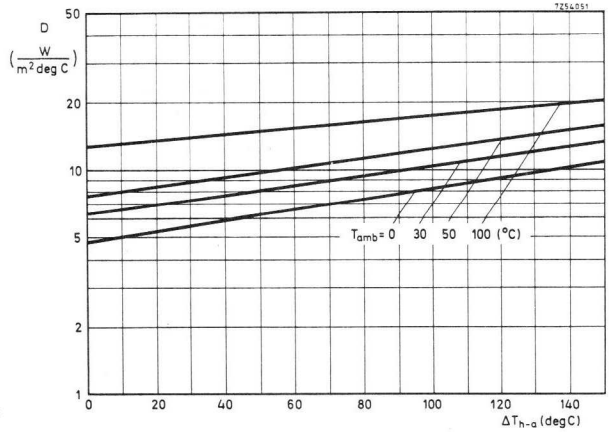


Fig. 4.6. Factor D vs temperature difference from heatsink to ambient, ΔT_{h-a}.

Table 4.3 Emissivity coefficient ε *

surface	emissivity coefficient ε
aluminium, polished	0.05
aluminium, oxidized	0.20
aluminium, anodised	0.90
copper, polished	0.03
copper, oxidized	0.60
brass, polished	0.10
brass, oxidized	0.60
aluminium paint	0.25 to 0.70
oil paint (all colours)	0.92 to 0.96
lacquer (all colours)	0.80 to 0.95
varnish	0.90

* The emissivity coefficient ε is unity for an ideal black surface. All painted surfaces, even white, have approximately the same emissivity, regardless of colour. Glossy paint has a slightly lower emissivity than a matt painted surface. Emissivity is lowest for polished surfaces but will substantially increase as the surface oxidizes. In cases where the heatsink carries a protective coating, emissivity will be determined by the coating and not by the metal.
Note that about 20% of the heat is lost by radiation (convection accounting for the remaining 80%).

Heatsink Efficiency

Calculations of heat transfer such as those above, which are based on the assumption that the entire surface of the heatsink has the same temperature as the hottest spot, are optimistic and should be corrected for the lower rate of heat transfer occurring at the cooler extremities.

Since the heatsink material has a finite thermal conductivity, the surface temperature will decrease as the distance to the heat source (i.e. the power device) increases, owing to surface cooling effects. Consequently, a practical heatsink will have an efficiency η_h, defined as the ratio of the heat actually transferred by the heatsink to the heat that would be transferred if its entire surface were at the temperature of the hottest spot.

A hypothetical circular heatsink, exhibiting no temperature difference over the surface, would have by definition 100% efficiency. The radius in m of such a hypothetical circular heatsink is given by:

$$r_h = (\gamma_s t/2h_t)^{1/2}, \tag{4.5}$$

where γ_s = thermal conductivity of the heatsink (W/m^{3}deg C),
t = thickness of the heatsink (m),
h_t = total heat transfer coefficient (W/m^{2}deg C).

Fig. 4.7 is a plot of r_h versus h_t for aluminium and copper heatsinks of 0.002 m and 0.003 m thickness. The thermal conductivity γ of various materials is given in Table 4.4.

Table 4.4 Thermal conductivity γ of several metals

material	copper	aluminium	brass	iron	unit
γ	380	210	110	44	W/m^3 degC

To find the efficiency of a practical heatsink, we introduce dimensions r_i and r_s in Fig. 4.8 and find the heat input radius to be:

$$r_i = (d_1 + d_2)/4. \tag{4.6}$$

The heatsink surface is defined by r_s, which equals the external radius for a circular sink. For a rectangular heatsink of length l and width w (provided $l/w \simeq 1$):

$$r_s = (lw/\pi)^{1/2}. \tag{4.7}$$

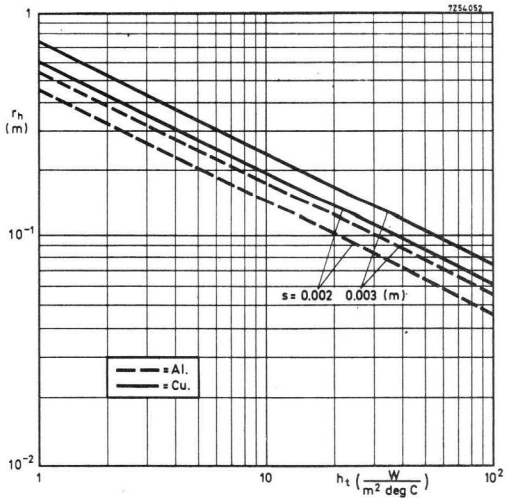


Fig. 4.7. Radius of hypothetical heatsink r_h vs total heat transfer coefficient h_t.

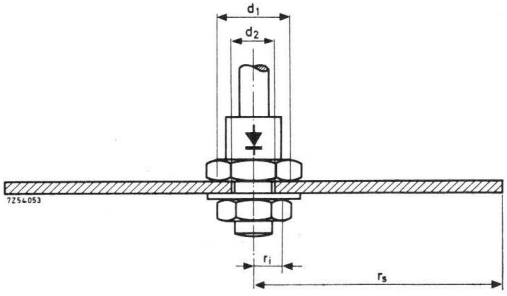


Fig. 4.8. Practical heatsink dimensions.

Knowing the ratios $p = r_h/r_i$ and $q = r_s/r_i$ one can find η_h, the efficiency of a practical heatsink, by reference to Fig. 4.9. Optimum design should yield a figure of about 0.5. An efficiency appreciably lower than 0.5 indicates that the material used is too thin. One as high as 0.9 suggests that the material is too thick, so the sink will be unnecessarily expensive.

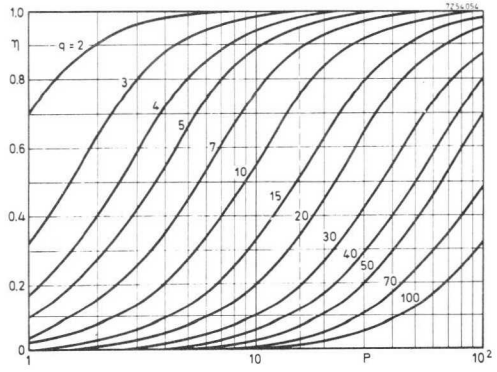


Fig. 4.9. Heatsink efficiency η_h vs ratios p and q.

Thermal Resistance of the Heatsink

Eq. (4.1) can be rewritten:

$$R_{th\ h-a} = \Delta T/P = 1/\eta_h h_t a_t, \tag{4.8}$$

where $R_{th\ h-a}$ is the thermal resistance that exists between ambient and the hottest spot of the heatsink.

For free convection:

$$R_{th\ h-a} = 1/\eta_h\,(h_c + h_r)\,a_t, \tag{4.9}$$

and for forced convection:

$$R_{th\ h-a} = 1/\eta_h\,(h_f + h_r)\,a_t. \tag{4.10}$$

Since there is some loss of heat direct to ambient from the envelope and connecting leads to the device, only part of the power dissipation will be removed by the heatsink. This implies that $R_{th\ h-a}$ can safely be increased to some extent, i.e. that a smaller heatsink will provide adequate cooling (cf. Sub-Section 4.1.3).

4.1.3 Effect of Heat Removal from the Device Envelope

In heatsink design, then, an economy can be made by taking into account the heat lost by the device via its leads and envelope. This more direct path to ambient lies in parallel with that through the heatsink, and its

effect is thus to help the crystal get rid of its generated heat. Accordingly, in Fig. 4.10, the simple heat flow diagram *a* has been developed into a more accurate version *b* by shunting an additional thermal resistance $R_{th\ d-a}$, representing the more direct path from device to ambient, across the thermal resistance $R_{th\ h-a}$ from heatsink to ambient and the thermal resistance $R_{th\ mb-h}$ from mounting base to heat sink.

Actual values of $R_{th\ d-a}$ can be found on reference to curves of the type shown in Fig. 4.11, both for free and forced cooling.

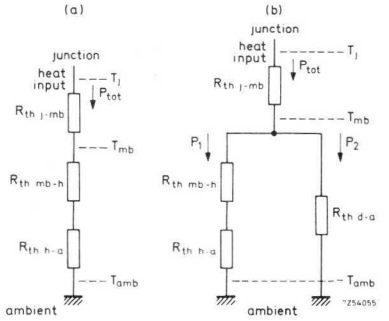


Fig. 4.10. Diagrammatic representation of heat flow (a) neglecting heat removal by device envelope (b) heat removal by device envelope accounted for.

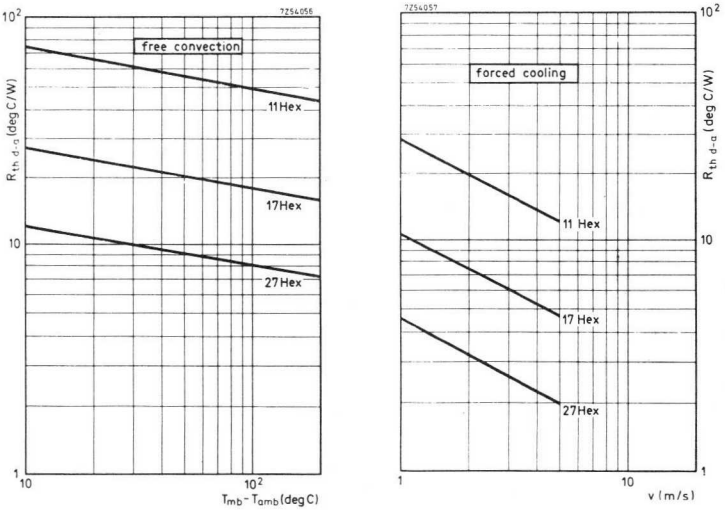


Fig. 4.11. Actual values of direct-to-ambient thermal resistance.

The values quoted by the manufacturer for the thermal resistance from heatsink to ambient always take into account the heat removal from the envelope direct to ambient.

4.1.4 Heatsink Nomograms

In heatsink nomograms (Fig. 4.13) $R_{th\ h-a}$ values are plotted along the ordinate which accounts for the loss of heat from the envelope and leads direct to ambient, so enabling the designer to dimension heatsinks with the utmost economy. Individually, the nomograms relate to particular types of heatsinks, distinction being made between free and forced convection. In the case of free convection, the air flow along the heatsink is caused by the temperature difference between heatsink and ambient. The higher the power dissipation, the higher will be the temperature difference and hence the heat transfer coefficient. When, on the other hand, the air movement is forced by blowers, the power dissipation rate does not greatly affect the heat transfer coefficient and a fixed point on the power scale may be used as a reference.

Flat Heatsinks

The use of the nomogram for flat heatsinks shown in Fig. 4.12 may be explained as follows, distinction being made between free convection and forced cooling.

Free Convection. Assume that the type of thyristor and its envelope, the power dissipation and the calculated maximum value of the thermal resistance from heatsink to ambient are known. Draw a straight line from the point on line 2 that corresponds to the free convection point of the thyristor used, through the thermal resistance value on scale 3, to the vertical line 4. Then move horizontally to the free convection line. The intersection of the vertical through this point with the horizontal through the power dissipation value on scale 1 gives the required heat sink area (interpolate between the values of the lines 6).

Example. An example has been plotted in Fig. 4.12 for a thyristor of encapsulation 14 to 17HEX, dissipating 17.5 W at $T_{amb} = 73$ °C. Accord-

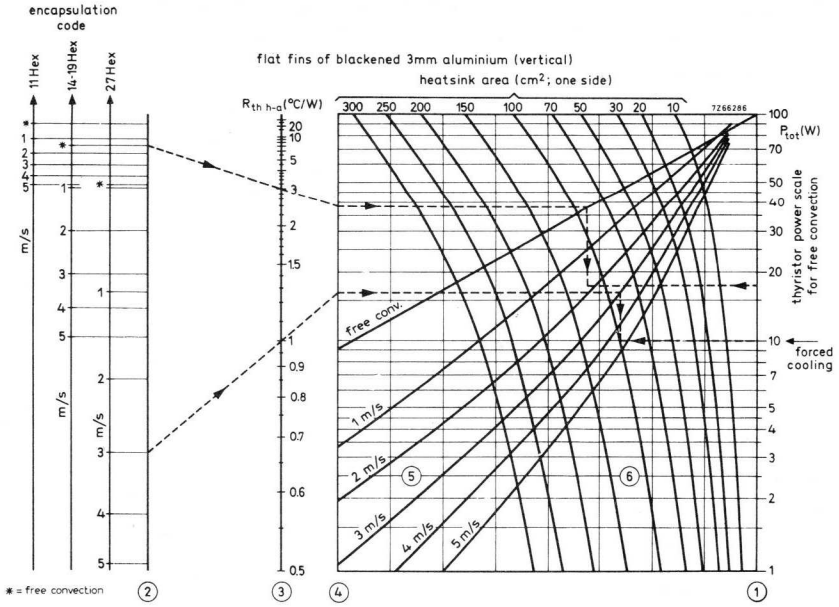


Fig. 4.12. Nomogram for finding data on flat heatsinks of blackened 3 mm thick aluminium (vertical).

ing to the data sheets, a thermal resistance from heatsink to ambient of 3 deg C/W is required. The nomogram shows that the heatsink area should be 125 cm^2.

Forced Cooling. Assume that the type of thyristor and its envelope, the calculated maximum value of the thermal resistance from heatsink to ambient and the velocity of the cooling air stream are known. Draw a straight line from the point on line 2 that corresponds to both the air velocity and the type of thyristor through the thermal resistance value on scale 3, to the vertical line 4. Then move horizontally through the appropriate line for the air velocity (lines 5) and from there vertically to the intersection with the horizontal line through the arrow "forced cooling" at scale 1. This intersection gives the required heatsink area (interpolate between the values of the lines 6).

Example. In the nomogram an example has been plotted for a BTW23 (27HEX envelope) thyristor, for which a required thermal resistance from mounting base to ambient of 1.1 deg C/W has been calculated and which will be cooled with a forced velocity of 3 m/s. Since the thermal resistance from mounting base to heatsink is 0.1 deg C/W, the thermal resistance from heatsink to ambient should be 1 deg C/W. The nomogram shows that in this case the required heatsink area is 100 cm^2.

Unless the heatsink is mounted vertically, the position correction factor f_p, given in Table 4.2, should be taken into account.

Influence of ambient temperature. It should be kept in mind that the nomograms are for an ambient temperature of 30 °C, but for other ambient temperatures no correction need be made except where the removal of heat takes place mainly by radiation. This is the case with, for example, painted heatsinks (high emissivity) at free convection. For these heatsinks, therefore, at an ambient temperature of, say, 10 °C the values found in the nomogram are too high; the correct $R_{th\ h-a}$ value is 5% lower. Similarly, at an ambient temperature of, for example, 60 °C the nomogram values are too low and should be increased by 10%. (Interpolate for intermediate temperatures).

Conversely, when the nomograms are used to ascertain the surface area of the heatsink for a given required value of $R_{th\ h-a}$, the latter should be decreased accordingly for ambient temperatures in excess of 30 °C or increased for ambient temperatures below this value if removal of heat takes place mainly by radiation.

Die-Cast and Extruded Heatsinks

When, instead of flat heatsinks, die-cast or extruded types are to be used, the designer is referred to other graphs, as for example those given in Fig. 4.13 for die-cast heatsinks and those given in Fig. 4.14 for an extruded one. These curves are not to be considered as nomograms since they depend on the type of thyristor used.

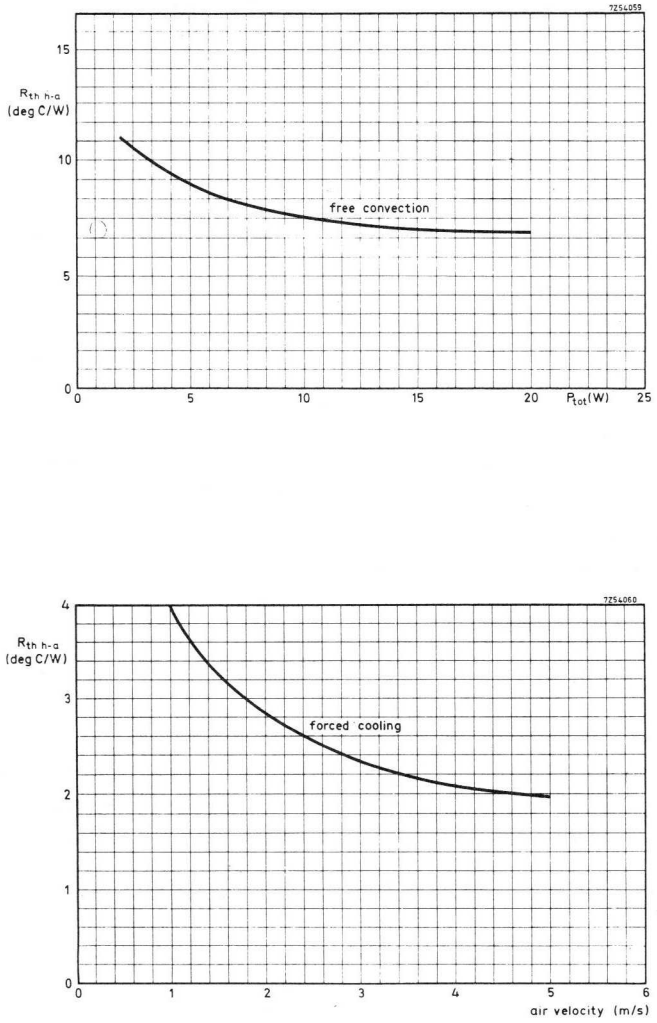


Fig. 4.13. Graph of $R_{th\ h-a}$ for die-cast heatsink type 56256 (top) free convection; (bottom) forced cooling.

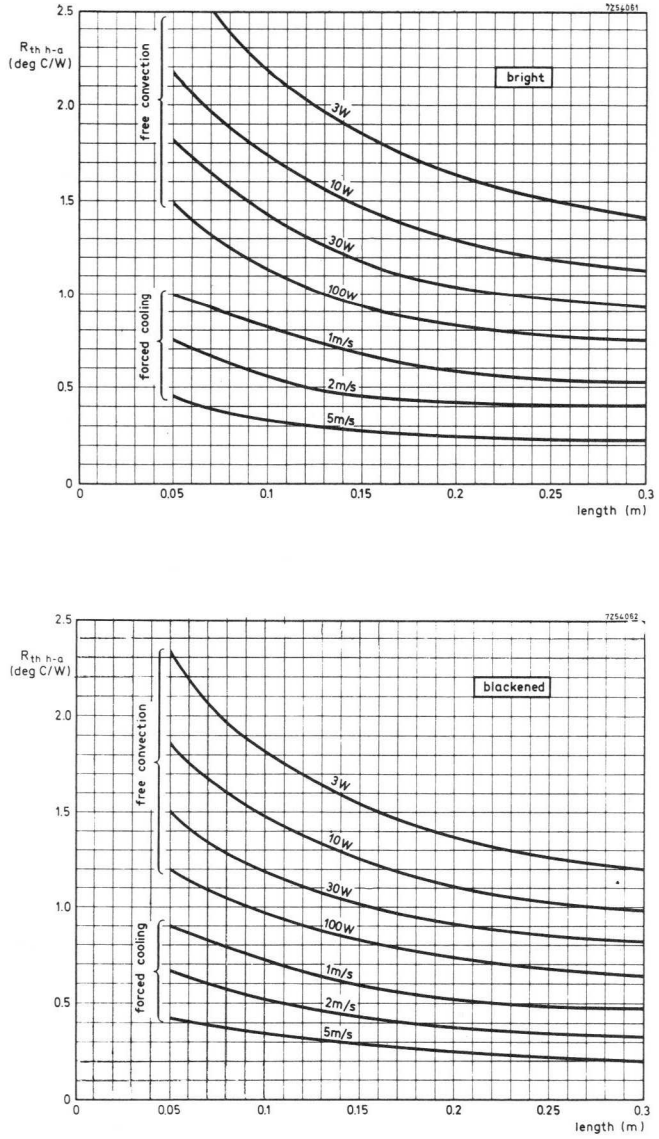


Fig. 4.14. Graph of $R_{th\ h-a}$ for extruded-aluminium heatsink type 56230 (top) bright; (bottom) blackened.

4.1.5 Use of Heatsink Compounds

Heatsink compound or vacuum grease is often inserted between the mounting base of the power device and its heatsink, to reduce the thermal resistance from mounting base to heatsink. Measurements show that this thermal resistance decreases by a factor of about 3 when, for example, a thin film of heatsink compound Dow Corning 340 is used and by a factor of about 1.5 when Dow Corning 280-300 vacuum grease is applied. However, the temperature difference between the mounting base and heatsink will not decrease by the same factor owing to the parallel path to ambient via the device envelope. When the thermal resistance drops, the mounting base temperature will also drop. As a result, the thermal radiation from the envelope decreases, causing an increased power flow via the heatsink. The heatsink temperature will therefore be higher and the temperature drop from mounting base to heatsink will be larger than would be the case in the absence of a thermal resistance directly from the envelope to ambient.

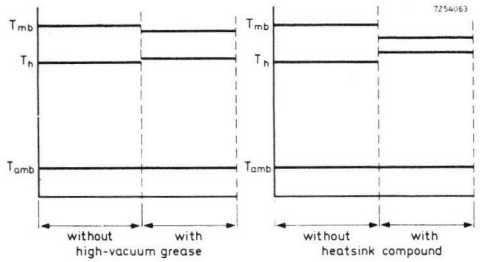


Fig. 4.15. Effect of high-vacuum grease or heatsink compound on mounting base and heatsink temperatures.

Fig. 4.15 illustrates the effect of compound or grease on the temperature levels of mounting base and heatsink, at a given ambient temperature. The use of compound or grease has additional value in preventing corrosion of the surfaces in contact.

4.1.6 Choice of Practical Heatsink

Let us assume that we require a heatsink for a BTW92 avalanche thyristor which is to be used in a single-phase full-wave rectifier circuit.

We have the following information (assuming no switching losses):

conduction angle	$\alpha = 180°$
average forward current	$I_{TAV} = 9$ A (per thyristor)
ambient temperature	$T_{amb} = 65$ °C

From the left hand part of the graph in Fig. 4.16 it follows that at $I_{TAV} = 9$ A and $\alpha = 180°$ the average forward power + average leakage power = 15.5 W per thyristor.

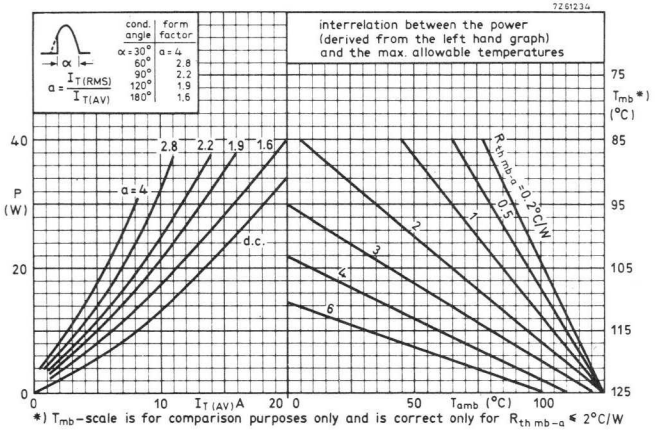


Fig. 4.16. BTW92 curves for heatsink calculation.

From the right hand part of the graph we can find the thermal resistance required for $P_{tot} = 15.5$ W at $T_{amb} = 65$ °C

$R_{th\ mb-a} \approx 3$ °C/W.

The contact thermal resistance $R_{th\ mb-h} = 0.2$ °C/W Hence the heatsink thermal resistance should be:

$$R_{th\ h-a} = R_{th\ mb-a} - R_{th\ mb-h} = 3 - 0.2\ °C/W = 2.8\ °C/W.$$

The applicable heatsink(s) may then be found in the section HEATSINKS in our Data Handbook - SEMICONDUCTORS AND INTEGRATED CIRCUITS.

4.1.7 Water Cooling

A water-cooled heatsink must allow heat to be carried away by cooling water at the same rate as it is generated in the thyristor crystal. Between the crystal and the cooling water, there exists a heat conduction path which has a certain thermal resistance. The crystal junction temperature must not rise above a certain specified maximum value (usually 125 °C).

However, the heatsink-to-water thermal drop depends on inlet water temperature and heat transfer rate. In turn, the heat transfer rate depends on the heatsink configuration, the flow rate and the water passage size. In addition to this, while too large a water passage merely results in a waste of cooling water, too small a passage can cause a pressure drop across the heatsink which may well exceed the capability of the water supply system.

This being so, the usual design procedure is to fix some of the variables and proceed by a series of trial-and-error steps.

The first, and most useful, variable to fix is the heatsink configuration. An efficient and easily constructed type is shown in Fig. 4.17. Three holes are drilled into the edges of the block to form a roughly "*U*" shaped water passage round the thyristor mounting base.

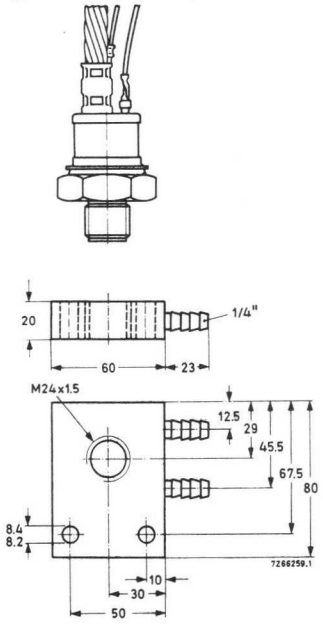


Fig. 4.17. Water-cooled heatsink (Type 56311).

Another variable that we can fix at the outset is the cooling water inlet temperature. It is common to assume a value of 30 °C for this.

Now it remains only to determine water-passage size and water-flow rate. This can be done by means of the following steps.

1. Find the thyristor power dissipation P and the maximum allowable mounting-base temperature $T_{mb\ max}$ from the device specification sheet. If $T_{mb\ max}$ is not given but maximum power dissipation, junction-to-mounting base thermal resistance and maximum junction temperature (usually 125 °C) are, $T_{mb\ max}$ can be found from

$$T_{mb\ max} = T_{j\ max} - P.R_{th\,j-mb} \qquad (°C)$$

In general, other power losses are negligible (those due to forward and reverse leakage currents, gate current and switching) but at high frequencies the switching losses become important.

2. Find the water film temperature T_f from:

$$T_f = T_{mb\ max} - P\,(R_{th\ mb-h} + R_{th\ h-f}) \quad (°C).$$

Obtain the mounting base-to-heatsink thermal resistance $R_{th\ mb-h}$ from the thyristor data and the heatsink thermal resistance $R_{th\ h-f}$ from:

$$R_{th\ h-f} = \frac{s}{\gamma d\, L_w} \quad (\text{deg C/W}),$$

where s = mean thickness of heatsink material between mounting base and cooling water (m),

γ = thermal conductivity of heatsink material (W/(m degC)),

d = water passage diameter (m) (choose a value for this),

L_w = water passage length (m).

If the value chosen for d is very small, the flow-rate needed may be too high for the water system and the passage may be susceptible to clogging; if d is too large, the heatsink can become too thick for the thyristor to engage enough threads in the nut.

3. Find the film drop θ from:

$$\theta = T_f - T_w - \Delta T_w/2 \quad (°C),$$

where T_f = water film temperature calculated in Step 2,
T_w = water temperature at heatsink inlet,
$\Delta T_w/2$ = average rise in water temperature (assume 5 °C to start with).

4. Determine the heat transfer rate H. This is the ratio of the power dissipation P and the heat transfer area F:

$$H = P/F \quad (\mathrm{W/m^2}).$$

The heat transfer area is:

$$F = \pi\, d\, L_w \quad (\mathrm{m^2}),$$

where d is the water passage diameter.

5. Determine the required water velocity V_w, from the graph in Fig. 4.18, using d, θ and H. As the water viscosity changes with temperature, a correction is needed for water inlet temperatures other than 30 °C.

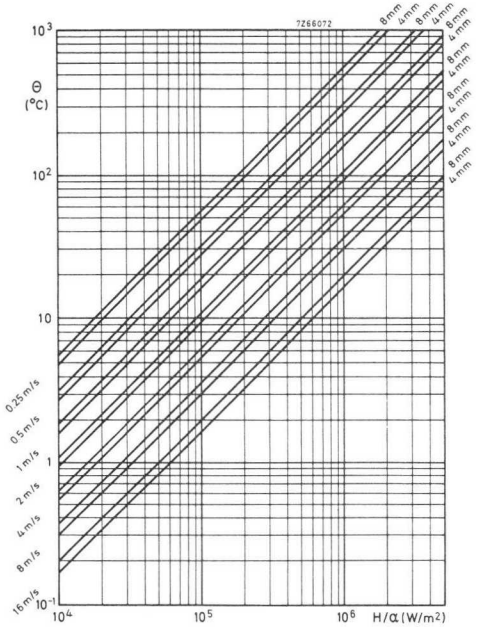


Fig. 4.18. Film drop θ vs. heat transfer rate H for various values of water velocity and water passage diameter. For correction factor α see Fig. 4.19.

Thus H/α, rather than H, is plotted horizontally in Fig. 4.18 – α being the correction factor (see Fig. 4.19).

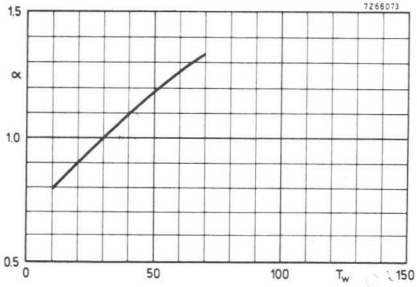


Fig. 4.19. Correction factor α vs. water inlet temperature T_w (compare Fig. 4.18).

6. Determine the water flow rate Q and the pressure drop. The water flow rate is given by:

$$Q = 4.71 \times 10^4 \, v_w \, d^2 \quad \text{(litres/min)},$$

where v_w and d are expressed in m/s and m respectively.

The water pressure drop depends on the total effective length L_t of the cooling system, which is given by:

$$L_t = L_w + 2\,L_e + L_h \quad \text{(m)},$$

where L_w = water passage length,
L_e = equivalent length of each square elbow in the water passage (Fig. 4.20),
L_h = connecting hose length.

If we neglect the pressure loss across the fittings, we can now find the pressure drop from Fig. 4.21 using the value of Q and L_t just obtained. Should this pressure drop exceed the capability of the water supply, restart

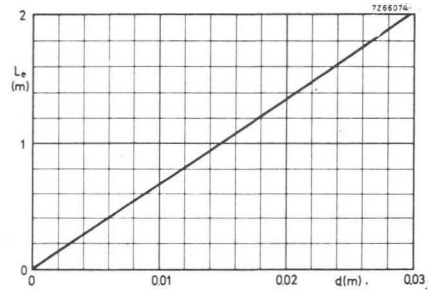


Fig. 4.20. Equivalent length L_e of square elbow vs. diameter d of water passage.

the design at Step 2-taking a larger water passage diameter. Industrial water supplies can deliver a few hundreds of m^3/hour at pressures up to about 100 m water column; a city water system should be able to supply 0.5 m^3/hour to 1 m^3/hour at pressures ranging between about 20 m water column and 30 m water column. If the required pressure drop is smaller than the capability of the water supply, a hand-operated valve should be installed to reduce the water flow rate.

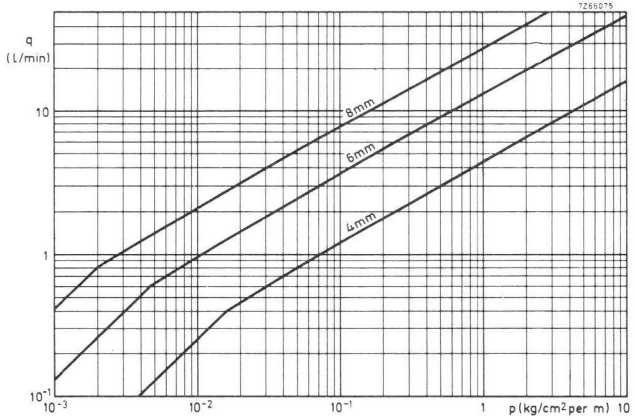


Fig. 4.21. Water flow rate Q vs. pressure drop p for 8 mm, 6 mm and 4 mm inner tube diameter (note $p = P_t/L_t$; $L_t = 1$ m).

7. Check the rise ΔT_w in water temperature. The rise in water temperature at the heatsink outlet is:

$$\Delta T_w = 8.64 \times 10^{-4} P/Q \quad (°C),$$

where P is expressed in watts and Q in m^3/hour.

Check that $\Delta T_w/2$ is smaller than the value assumed in Step 3. If it is not, re-start the design at that step, taking a larger value for $\Delta T_w/2$.

Practical Example

If we already have a heatsink and its data sheet and we have the published data on the thyristor, the problem is simply to discover the necessary water flow-rate and pressure.

Suppose, for instance, we wish to cool a thyristor Type BTX41 which is delivering an average current of 250 A. We have, for this purpose, our heatsink Type 56311.

BTX41 data sheets give us the following information:

dissipation at 250 A	400 W
thermal resistance ($R_{th(j-mb)}$)	0.12 °C/W
max. allowable junction temperature	110 °C.

From this we can obtain the maximum allowable mounting base temperature as follows:

$$T_{mb} = T_j - P \cdot R_{th(j-mb)} = 110 - (400 \times 0.12) \approx 60\ ^\circ\text{C}.$$

Maximum thermal resistance between mounting base and water ($R_{th(mb-w)}$) assuming, in this case, a maximum water inlet temperature of 40 °C, is

$$R_{th(mb-w)} = \frac{T_{mb} - T_w}{P} = \frac{60 - 40}{400} = 0.05\ ^\circ\text{C/W}.$$

With this figure, we find from the first graph given in the heatsink 56311 data ($R_{th(mb-w)}$ against water flow rate) that a water flow rate of about 3.75 litres per minute is required. Using this figure in the second graph (pressure drop against water flow rate), we find that a pressure of about 0.26 atmospheres is required.

4.1.8 Allowance for Switching Losses

When a heatsink is being calculated, it can be important that switching losses are not neglected; at high operating frequencies, switching losses form a significant part of the total dissipation.

In Chapters 2 and 3, a method of calculating the turn-on and turn-off switching losses is given. When these have been calculated, it is only necessary to add them to the forward conduction dissipation in order to obtain the correct value of device dissipation for heatsink calculations.

4.2 Voltage Transient Suppression

4.2.1 Voltage Transients and Thyristor Ratings

Semiconductors, in their early years of development, carried a reputation for great sensitivity to overvoltage conditions; their limited voltage ratings, in those days, served only to accentuate this shortcoming when comparisons were made with vacuum or gas-filled tubes. However, this problem has now virtually disappeared and semiconductor devices can

be produced with voltage capabilities of several thousand volts peak. Nevertheless, there is still a need to protect thyristors against voltage transients because the transient may have a high enough dV/dt to turn on the thyristor.

Some thyristors are easily damaged by low-energy voltage transients above their peak voltage ratings, others (avalanche types) can dissipate quite large amounts of transient energy in the blocking condition without sustaining damage and yet others (some bidirectional types) may switch non self-destructively into conduction under the influence of excess voltage. All of these may require some form of transient suppression – the type and extent of this will be determined by the individual case.

4.2.2. Voltage Transient Sources

There are three major sources of the type of transients which afflict thyristor circuits:

(a) the mains supply (lightning and other major disturbances),
(b) the mains and load contactor (opening and closing),
(c) the rectifying and load circuit (commutation).

The transients must be suppressed (they can also be allowed for in component ratings to some extent) by additional components or removed at source in order to ensure reliable circuit operation.

4.2.3. Voltage Transient Suppression Methods

Three types of circuit are commonly employed to suppress voltage transients – an RC series network across the thyristor stack, an RC series network across individual thyristors and a series choke between the stack and the mains contactor.

In some cases only one type of suppression circuit will be required but in others two or even all three will be necessary.

4.2.4. Input Filter

Most of the mains-borne and contactor transients can be removed or reduced to a safe level by a suitable shunt capacitance across the input terminals of the thyristor array. Although in some applications individual suppression circuits for the thyristors may be required, these circuits have

little effect on the input filter, and the two types of circuit can be considered separately.

The complete input filter circuit for a single-phase system with a solid neutral connection is shown in Fig. 4.22 where L_1 and R_1 represent the line source impedance plus any additional series choke and its associated loss component. Capacitor C_1 is the shunt suppression component, resistor R_2 is a series damping resistor, and R_3 provides a discharge path for C_1.

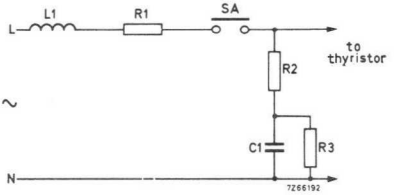


Fig. 4.22. Input filter for single-phase system.

The line impedance is largely inductive, so at frequencies above a few kilohertz:

$$\omega L_1 R_1 > 1.$$

When the thyristors are in their non-conducting state and the mains contactor S_A is closed, a series resonant circuit is formed of L_1 and C_1 with series damping $(R_1 + R_2)$. If the loss components of this circuit are small, the circuit will ring and the voltage appearing across capacitor C_1 will exceed the supply voltage, as shown in Fig. 4.23.

If resistor R_2 is zero or very small, most of this ring voltage will appear across the bridge input and may result in the forward breakover of a thyristor, although the presence of capacitor C_1 may have effectively slowed down the rate of rise of voltage to a safe value of dV/dt for the

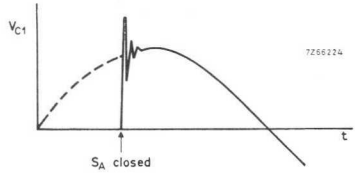


Fig. 4.23. Voltage across capacitor C in input filter.

thyristor. It is therefore most important to ensure that the combined value of R_1 and R_2 is large enough to provide sufficient circuit damping.

Unfortunately, too large a value of resistor R_2 reduces the effectiveness of capacitor C_1, and it is not easy to make R_1 large. It is clearly not possible to make R_1 a physical resistance as the power losses would be too large, but it is sometimes possible to make this the series loss component of a choke which has negligible loss at 50 Hz but a useful loss at higher frequencies. Because of these difficulties, a compromise has to be made between acceptable damping and filtering efficiency.

In many cases, the supply impedance will only be known to lie between broad limits so that no accurate design will be possible. Alternatively, a series choke may be used to swamp the supply inductance and provide a better defined input circuit. The final choice will probably be dictated by economic considerations, and in low-power systems the choke is quite often omitted.

The design procedure is summarised in sub-section 4.2.9. Two design abacs are given, for single-phase and three-phase systems, for values of inductance and shunt capacitance that have been proved practicable. It has also been proved in practice that for reliable operation of thyristors at least 600 V types should be used for single-phase (220-240 V) supplies, and 1200 V types for single-phase line-to-line or three-phase (380-440V) supplies.

4.2.5 Individual Device Suppression

The input circuits which have been described so far for transient and dV/dt suppression rely for their operation upon the neutral side of the supply being connected when the line contact is made. In many practical circuits this will not necessarily be the case, as the mains will be connected through a two-pole contactor whose contacts will never close at exactly the same instant, and in any case contact bounce is likely to give rise to random transients following the initial make.

In these cases, a large voltage transient can be applied to a particular thyristor through the circuit stray capacitance to earth of the load. Although the capacitance current that would follow thyristor turn-on would not sustain thyristor conduction, this initial charging current may be immediately followed by the closing of the neutral contact so that full conduction into the load can follow.

Spurious turn-on by this process requires a certain sequence of events

in the contactor to occur near the supply-voltage crest. Such a sequence of events may occur, say, once every 100 operations; but if it can happen and the consequences of this are the destruction or premature ageing of thyristors, or perhaps some undesirable rotation of a motor, preventive measures must be taken.

It has been found that a series combination of capacitance and resistance connected across each thyristor effects a complete cure and reduces initial dV/dt in all known cases to a safe level. This arrangement alone will not be sufficient to attenuate input voltage transients, so that both suppression circuits will normally be required except where the neutral is not switched.

Circuit Condition with Open-circuit Neutral

The circuit diagram of a half-controlled bridge fitted with an input filter and individual device suppression is shown in Fig. 4.24. If the contactor contact S_B closes before S_A and remains closed, then the input suppression circuit L_1, R_1 and C_1 operates to protect the thyristors from large values of dV/dt or mains-borne voltage transients.

On the other hand, if S_A closes first, a circuit exists from line to earth, through the load and its stray capacitance, which may result in a high value of dV/dt across the thyristors. The following conditions exist.

If the line terminal is positive to earth, diode D_1 conducts and current flows to charge the stray capacitance C_S. Capacitor C_1 will normally be much greater than C_S, so that both a.c. bridge terminals will remain at about the same potential, and the voltage across diode D_2 will therefore also be small. As no load current can flow and the load impedance is low,

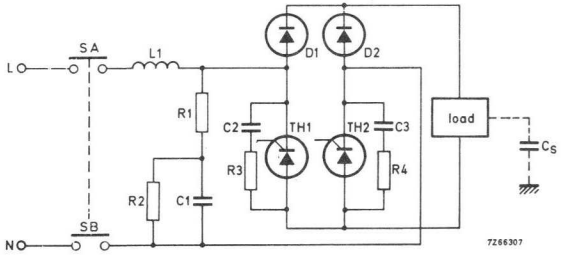


Fig. 4.24. Single-phase half-controlled bridge with input filter and individual device suppression circuits.

the voltage drop across the load will only be that due to the charging current for C_S. There will therefore only be a small voltage drop across the two thyristors.

If the line terminal is negative to earth when S_A is closed, the diodes D_1 and D_2 are reverse-biased, and nearly all the mains voltage appears across the two thyristors in the forward direction. The rate of change of forward applied voltage can be as high as 1000 V/μs if the switch is closed when the mains supply is near to its crest voltage. If capacitors C_2 and C_3 are connected across the two thyristors, the rate of rise of voltage across either thyristor can be reduced to an acceptable level. Some series resistance, R_3 and R_4, must also be included to limit the peak capacitor discharge current when the thyristors are triggered into conduction. High peak currents could damage the thyristors by exceeding the rated value of di/dt during the switch-on period. A practical upper limit of capacitance is about 1.0 μF, and a 10-47 Ω resistor will, in most cases, limit the peak discharge current to a safe level. A lower limit is difficult to define on the basis of dV/dt protection alone, but a minimum value of 0.1 μF is probably a good compromise.

dV/dt *with Individual Device Suppression*

Before proceeding further, we will consider the effects of these components on the normal operation of the circuit with the neutral contact making first, or with a solid neutral connection.

If the line is positive when S_A (Fig. 4.24) is closed, diode D_1 will conduct and, as the load has a very low impedance compared with the forward leakage of the other components of the thyristor bridge, nearly all the mains voltage appears across thyristor TH_2. Because of the low voltage drop across the load, the voltage difference between the d.c. terminals of the bridge will be small so that very little voltage appears in reverse across the other thyristor TH_1. If the line terminal is negative when S_A is closed, exactly the same conditions exist except that the roles of the diode and thyristor pairs are reversed.

The input suppression circuit L_1, R_1 and C_1 will reduce the rate of rise of voltage across the a.c. terminals of the bridge as already described. Now the rate of rise of voltage applied to the thyristors will be further reduced by the combined effects of the series impedance of the bridge diode and load as a series element, and C_2 and R_3 or C_2 and R_4 as a shunt element.

The non-linear characteristic of the bridge diodes as a part of this second filter modifies the voltage rise characteristic across the thyristors, making the rate of rise of voltage more nearly linear as shown in Fig. 4.25. The upper line shows the almost exponential voltage waveform across the bridge a.c. terminals, while the lower line shows the rate of rise of voltage across the thyristor itself to be very nearly linear. In this case the component values were as follows:

$$L_1 = 160\ \mu\text{H};\ C_1 = 4\ \mu\text{F};\ R_1 = 5.6\ \Omega$$

$$C_2 = C_3 = 0.22\ \mu\text{F};\ R_3 = R_4 = 10\ \Omega.$$

It will be seen that the initial rate of rise of voltage with input suppression only is about 7.5 V/μs, while with additional device suppression it is about 4.0 V/μs – an improvement of nearly 2 : 1. Apart from the additional protection provided by individual device suppression when double-pole switching is used, a significant improvement is obtained in normal operation which would otherwise require a fourfold increase in either the input choke inductance or capacitance value.

With the neutral open-circuit but with the circuit otherwise unchanged, the maximum rate of rise of voltage across a thyristor is shown in Fig. 4.26, where the vertical scale is 200 V/division and the horizontal scale

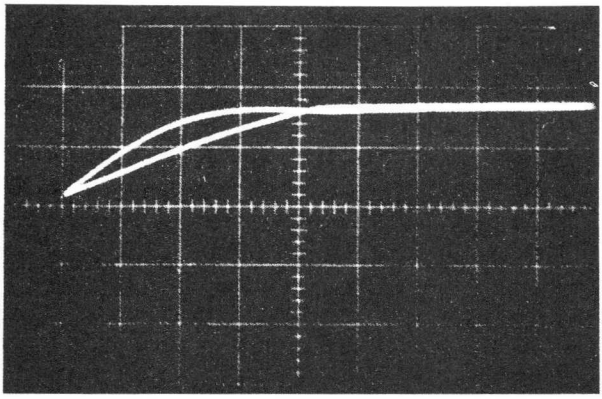


Fig. 4.25. Observed $\mathrm{d}V/\mathrm{d}t$ *waveform in single-phase thyristor bridge.*
Upper trace – voltage across a.c. terminals of bridge.
Lower trace – voltage rise across thyristor.
(Vertical scale 200 V/div.: horizontal scale 20 μs/div.)

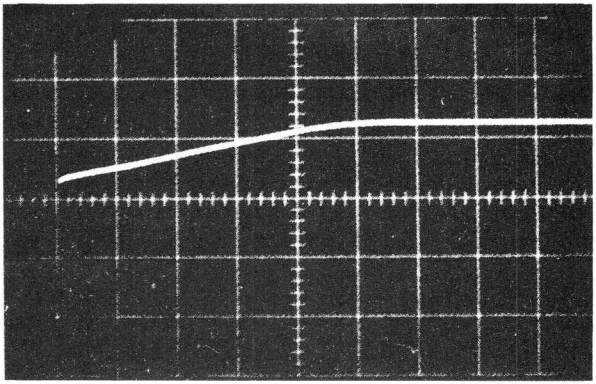


Fig. 4.26. Observed dV/dt *waveform in single-phase thyristor bridge with open-circuit neutral. (Vertical scale 200 V/div.: horizontal scale 10 μs/div.)*

10 μs/division, giving a dV/dt value of 4.5 V/μs. It is interesting to note that the maximum voltage reached with the neutral open-circuit is only about 250 V, compared with the 340 V shown in Fig. 4.25, because of the additional voltage drop across the impedance to earth.

The rate of rise of voltage across the thyristors with individual suppression and an open-circuit neutral is very little affected by the series line choke. Removing the choke altogether and leaving about 50 μH of series line inductance only increases the dV/dt value only to about 5 V/μs. This is to be expected as the additional series impedance provided by diodes and load is considerably greater than that of the series choke.

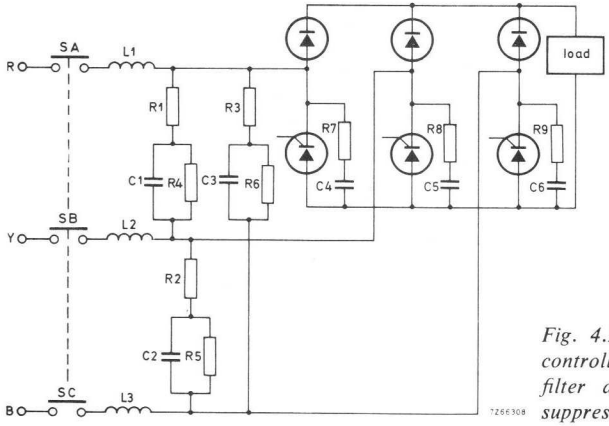


Fig. 4.27. Three-phase half-controlled bridge with input filter and individual device suppression.

Individual thyristor suppression is shown applied to a three-phase half-controlled bridge in Fig. 4.27. The circuit functions in the same way as the single-phase system.

Peak Current in Suppression Capacitor Circuit

When the mains contactor S_A and S_B is closed, the suppression capacitors C_2 and C_3 in Fig. 4.23 will charge through the series line choke L_1, their individual damping resistors R_3 and R_4, and the load circuit. The peak charging current will be limited by all these series circuit elements to a moderate value, even when the mains circuit is made near the crest voltage of the supply.

When a thyristor is triggered, however, the only impedance in the capacitor discharge circuit is that of the series resistor and the thyristor itself. To avoid damage to the thyristor during its turn-on interval, the rate of rise of current must stay within the rated maximum value. The worst case will exist when the thyristor is triggered at the mid-point of the cycle, at which time the suppression capacitor will be charged to its maximum voltage. Under these conditions, measurements show that the peak discharge current is about 18 A (which is less than expected because the thyristor is not a perfect switch and does not turn on immediately) for a circuit where C_2 and C_3 are 0.22 μF, R_3 and R_4 are 10 Ω and the supply voltage is 240 V. The mean power dissipation in the series resistor R_3 and R_4 under these conditions is about 0.4 W. A 0.5 W carbon resistor was used for these measurements.

In the three-phase case (Fig. 4.27) where the peak voltage across each thyristor is increased by a factor of $\sqrt{3}$, the peak current will be increased in the same ratio to about 30 A. The resistor mean power dissipation will be increased by a factor of 3 to about 1.2 W. In both cases, the pulse of current is roughly triangular in shape with a duration of less than 10 μs, and will be within the permitted rating of most thyristors.

4.2.6 Suppression of Contactor Transients

Magnetically-operated mechanical mains contactors all suffer from contact surface imperfections and contact bounce effects to some extent, although some types will obviously be superior to others. It is not the intention here to discuss the characteristics of particular contactors, but rather to indicate the nature of the problem and the electrical effects

which may be produced by some contactors. It should be remembered that it is not the near-ideal operation of a new contactor which is being considered. but the operation of an old contactor in need of service though still functioning well enough to have escaped the attention of the works maintenance electrician.

To obtain some qualitative measure of the effects of contactor operation, we made transient voltage waveform measurements across a thyristor in a half-controlled bridge circuit. The individual device suppression components were omitted but the input transient suppression components were retained. So as not to confuse the results by double contact operation, the neutral was left open-circuit.

Fig. 4.28 shows typical contact bounce effects with higher-frequency transients before and after each major bounce period. The vertical scale is 200 V/division, the horizontal scale 1 ms/division.

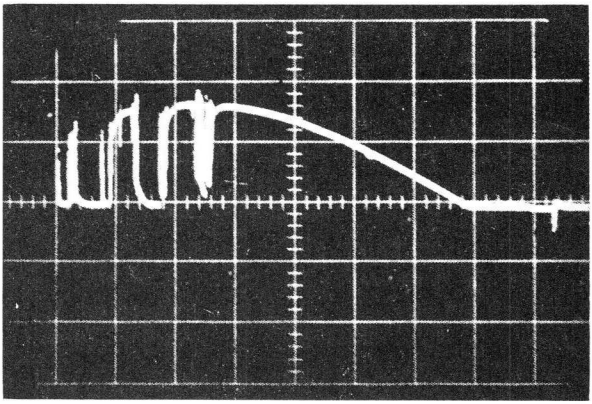


Fig. 4.28. Contact bounce effects with higher-frequency transients before and after each major bounce period.
(Vertical scale 200 V/div.: horizontal scale 1 ms/div.)

If one of the major bounce periods is expanded a picture like that of Fig. 4.29 is obtained, where the time scale is 50 μs/division. The early part of this waveform may be expanded still further, when it appears as shown in Fig. 4.30 with a time scale of 20 μs/division.

Examination of the leading edge of a single transient reveals that the rate of rise of voltage is of the order of 1000 V/μs, as shown in the

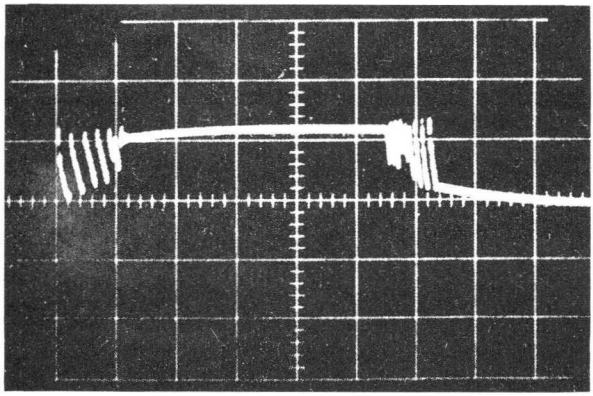


Fig 4.29. Expansion of major bounce period.
(Vertical scale 200 V/div.: horizontal scale 50 μs/div.)

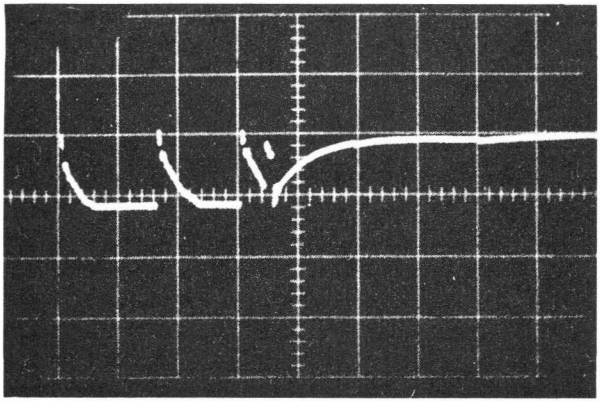


Fig. 4.30. Early part of waveform in Fig. 4.29.
(Vertical scale 200 V/div.: horizontal scale 20 μs/div.)

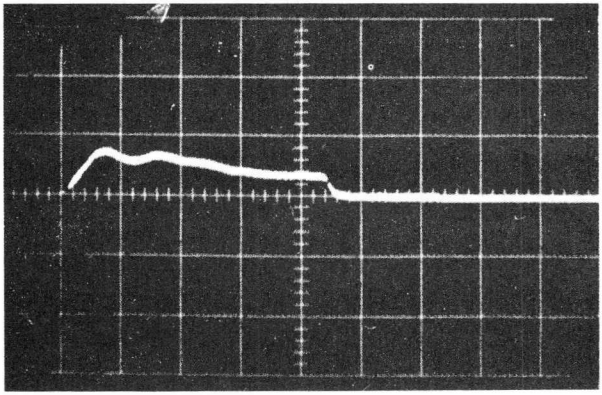


Fig. 4.31. Leading edge of single transient from Fig. 4.30.
(Vertical scale 400 V/div.: horizontal scale 0.5 μs/div.)

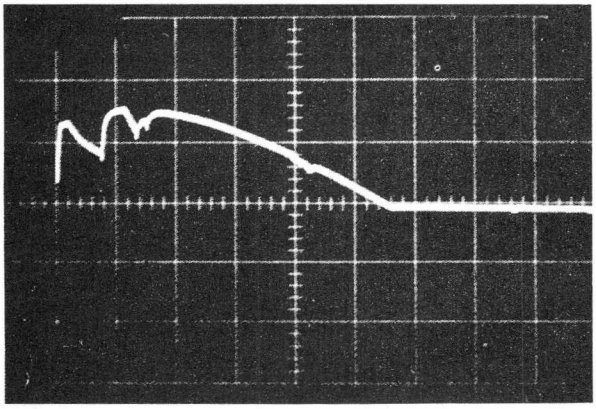


Fig. 4.32. Contact bounce effects with RC filter across each thyristor. Compare with Fig. 4.28 which has same scale.
(Vertical scale 200 V/div.: horizontal scale 1 ms/div.)

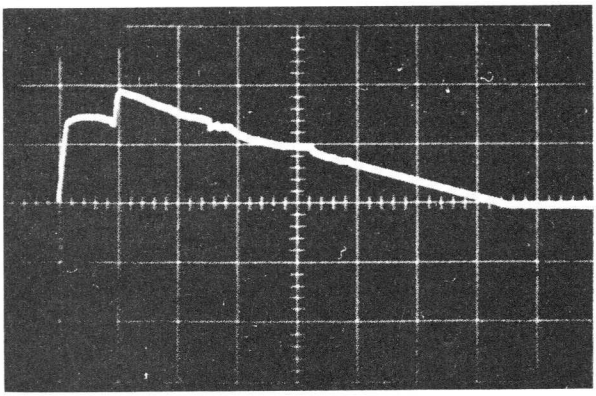


Fig. 4.33. Contact bounce effects as in Fig. 4.32 but with improved suppression filter. (Vertical scale 200 V/div.: horizontal scale 500 μs/div.)

greatly expanded waveform of Fig. 4.31. Here the vertical scale has been reduced in sensitivity to 400 V/division, and the horizontal scale is 0.5 μs/division (representing the limit of writing speed of the storage oscilloscope which was used).

Repetitive transients of this type represent a serious hazard to the correct operation of thyristor equipment, and should be reduced to more reasonable proportions by suitable filters.

Fortunately, the addition of a simple RC filter across each thyristor provides an adequate solution. The waveform of Fig. 4.32 (1 ms/division) should be compared with Fig. 4.28. It shows the effect of the additional filter components. A rather larger value of capacitance or a larger discharge resistance value gives even better results, as shown in Fig. 4.33 (500 μs/div). The main discharge path for the capacitors C_2 or C_3 in Fig. 4.24 is resistor R_2, the discharge resistor for the mains transient suppression capacitor.

If R_2 is 33 kΩ, and C_2 and C_3 are 0.22 μF, the discharge time-constant is 7 ms. This corresponds approximately with the constants of the circuit used to obtain the waveform of Fig. 4.33. The maximum rate of rise of voltage in this case was about 5 V/μs as described in the section on individual device suppression.

It should be noted that our all-diffused thyristor types have greatly improved dV/dt capabilities (> 200 V/μs).

4.2.7 Series Line Chokes

The use of series chokes has already been referred to in connection with the reduction of voltage transients and dV/dt, and some indications of the effects of the choke Q-factor are given in Sub-Sect. 4.2.9. A series choke may also be used to limit peak prospective fault currents to assist in the fuse protection of thyristors and rectifier diodes. The design of chokes will depend very much upon whether the choke is required to perform all or only some of these functions.

If the choke is required in conjunction with fuse protection, it must retain its design inductance to very large values of current. For this reason, it is usually an air-cored component of quite large physical dimensions. On the other hand, if the choke is only required to reduce the dV/dt across non-conducting thyristors, the current up to which the design inductance must be maintained may be quite small, and ferrite-cored chokes may be adequate provided that the windings are capable of carrying the full-load current. Between these two extremes, there is a place for moderate-sized iron-cored a.c. chokes designed to retain their inductance at normal load currents, and so provide full transient and dV/dt protection but only partial fault current limitation.

The final choice of choke construction and inductance will depend upon a number of factors such as the degree of transient and fuse protection required, and the size and cost of the equipment, which will in turn have a bearing upon the space available for suppression chokes, and the proportion of the overall cost which can be allocated for protection equipment. All these factors and others have to be weighed up by the designer of the equipment, who will know the seriousness of an occasional device forward breakover, or in the worst case an occasional device failure.

4.2.8 General Recommendations

Because of the very wide range of applications to which thyristor control circuits can be put, it is difficult to give any definite recommendations about the amount of suppression required for a particular circuit. It is much easier to design suppression circuits to give complete protection regardless of cost than it is to design to an adequate level of protection at minimum cost. It is necessary, therefore, to assess each application individually, and when in doubt about the protection required, use the full suppression circuits.

The commonly used thyristor control circuits are listed in Table 4.5 together with the type of protection that will generally be required. If information is available about the types of transients likely to be encountered, then it may be possible to dispense with some of the suppression components shown in the circuit diagrams related to the table, Figs 4.34 to 41. As can be seen from Table 4.5 the amount of suppression required depends on the type of load. If the load is mainly resistive and of constant impedance (such as some types of furnace), and if avalanche thyristors are used, it is possible in almost all cases to use the thyristor circuit without any suppression components at all. The factors that should be considered when the degree of protection necessary is being decided are listed below.

1. In the event of spurious thyristor triggering, will the current that flows be limited by the load to a safe value for the load, thyristors, and rectifier diodes?
2. Will this current cause any other damage by, for instance, rotation or movement of machinery (which may even constitute a hazard to personnel)?
3. Will the voltage or current transients damage the thyristors and rectifier diodes, or shorten their lives?

On the basis of these factors, the knowledge of the type of transients likely to be encountered, and the degree of risk of a device failure that is acceptable, a compromise between the number of suppression components and the cost can be reached.

Table 4.5 Suppression Recommendations for Different Types of Loads

	configuration	type of load					
		resistive	inductive	tungsten lamp	induction motor	trans-former coupled	d.c. shunt motor
Single Phase	A.C. controller, line-to-neutral	A	C	B	C	C	—
	A.C. controller, line-to-line	B	C	B	C	C	—
	half-controlled bridge, line-to-neutral	B	C	B	—	—	C
	half-controlled bridge, line-to-line	B	C	B	—	—	C
	fully controlled bridge, line-to-neutral	—	C	—	—	—	C
	fully controlled bridge, line-to-line	—	C	—	—	—	C
Three Phase	half-controlled a.c. controller	B	C	B	C	C	—
	fully controlled a.c. controller	C	C	C	C	C	—
	half-controlled bridge	B	C	B	—	—	C
	fully controlled bridge	—	C	—	—	—	C

A No suppression
B Some suppression (input filter or device filter)
C Full suppression
(For details of full suppression see separate circuits, Figs 4.34 to 4.41)

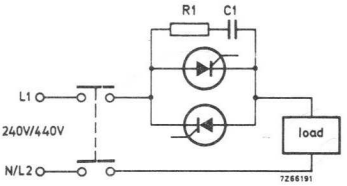


Fig. 4.34. Single-phase a.c. controller with transient suppression.

Line-to-neutral (240 V)
R_1 = 10 Ω, 2 W. C_1 = 0.22 μF, 250 V a.c. working.

Line-to-line (440 V)
R_1 = 10 Ω, 6 W. C_1 = 0.22 μF, 440 V a.c. working.

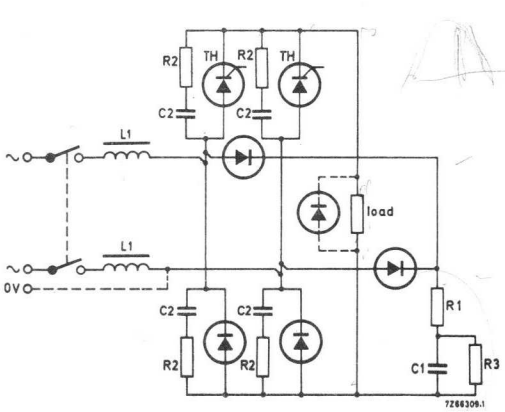


Fig. 4.35. Single-phase half-controlled bridge (ohmic or moderately inductive load).

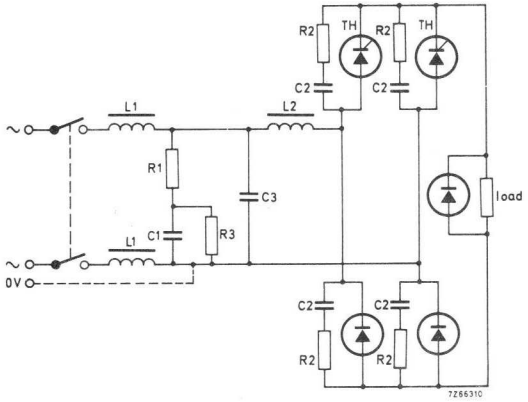


Fig. 4.36. Single-phase half-controlled bridge (highly inductive loads).

Components list to Fig. *4.35* **and** *4.36* (All components 10% tolerance)*

Nominal suply voltge 240 V r.m.s.

$R_1 = 8.2\ \Omega$, 2 W $\quad C_1 = 5\ \mu$F, 280 V a.c. $\quad L_1 = 250\ \mu$H
$R_3 = 33\ k\Omega$, 2 W $\quad C_3 = 1.5\ \mu$F, 280 V a.c. $\quad L_2 = 50\ \mu$H

Thyristors (alloy-diffused types):

10-20 A range	20-30 A range	30 to 70 A range
$R_2 = 33\ \Omega$, 1 W	33 Ω, 2 W	33 Ω, 2 W
$C_2 = 0.1\ \mu$F, 1000 V d.c.	0.15 μF, 1000 V d.c.	0.22 μF, 1000 V d.c.

Nominal suply voltge 415 V r.m.s.

$R_1 = 12\ \Omega$, 10 W $\quad C_1 = 2\times 10\ \mu$F, 280 V a.c. in series $\quad L_1 = 500\ \mu$H
$R_3 = 47\ k\Omega$, 5.5 W $\quad C_3 = 2\times 5\ \mu$F, 280 V a.c. in series $\quad L_2 = 100\ \mu$H

Thyristors (alloy-diffused types):

10-20 A range	30-70 A range
$R_2 = 47\ \Omega$, 2 W	47 Ω, 5.5 W
$C_2 = 0.1\ \mu$F, 1500 V d.c.	0.22 μF, 1500 V d.c.

* For information on filter designs using all-diffused thyristors, reference is made to our publication AN146 (ordering code 9399 250 64601).

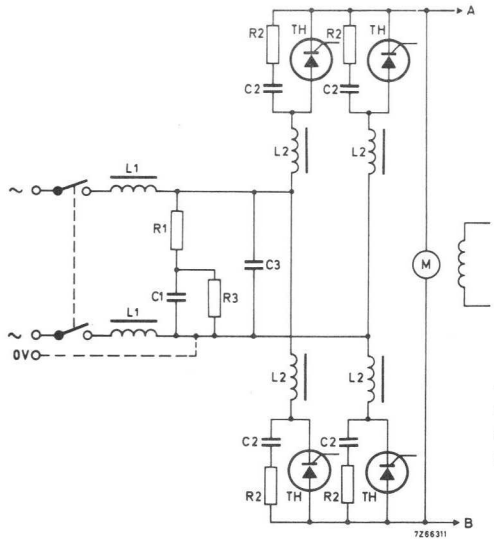


Fig. 4.37. Single-phase fully-controlled bridge (A-B is parallel connection to bridge working in opposition).

Components list to Fig. *4.37* (All components 10% tolerance)*

Nominal supply voltage 240 V r.m.s.

$R_1 = 8.2\ \Omega$, 2 W $\quad C_1 = 5\ \mu$F, 280 V a.c. $\quad L_2 = 250\ \mu$H
$R_3 = 33\ k\Omega$, 2 W $\quad C_3 = 1.5\ \mu$F, 280 V a.c. $\quad L_1 = 250\ \mu$H (d.c. choke)

Thyristors (alloy-diffused types):

10-20 A range	20-30 A range	30 to 70 A range
$R_2 = 82\ \Omega$, 1 W	68 Ω, 2 W	56 Ω, 2 W
$C_2 = 0.1\ \mu$F, 1000 V d.c.	0.15 μF, 1000 V d.c.	0.22 μF, 1000 V d.c.

Nominal supply voltage 415 V r.m.s.

$R_1 = 12\ \Omega$, 10 W; $C_1 = 1 \times 10\ \mu$F, 280 V a.c. in series; $L_1 = 500\ \mu$H
$R_3 = 47\ k\Omega$, 5.5 W; $C_3 = 2 \times 5\ \mu$F, 280 V a.c. in series; $L_2 = 500\ \mu$H (d.c. choke)

Thyristors (alloy-diffused types):

10-20 A range	30-70 A range
$R_2 = 100\ \Omega$, 2 W	100 Ω, 2 W
$C_2 = 0.1\ \mu$F, 1500 V d.c.	0.1 μF, 1500 V d.c.

* See footnote page 107.

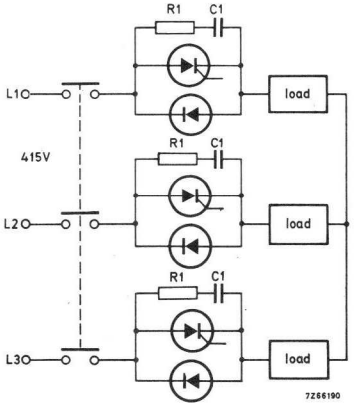


Fig. 4.38. Three-phase half-controlled controller with transient suppression.
$R_1 = 100\,\Omega$, 6 W; $C_1 = 0.22\ \mu$F, 440 V a.c. working.

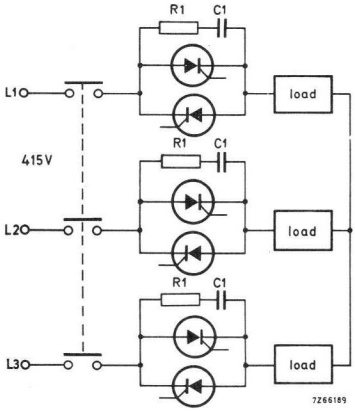


Fig. 4.39. Three-phase fully-controlled controller with transient suppression.
$R_1 = 100\,\Omega$, 6 W; $C_1 = 0.22\ \mu$F, 440 V a.c. working.

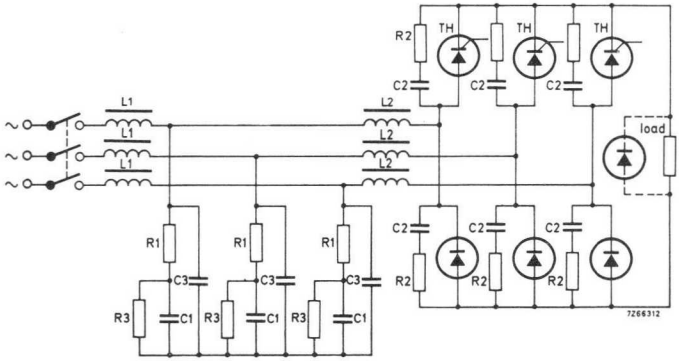


Fig. 4.40. Three-phase half-controlled bridge.

Components list to Fig. *4.40* (All components 10% tolerance)*

Nominal supply voltage 415 V r.m.s.

R_1 = 8.2 Ω, 10 W
R_3 = 33 kΩ, 2 W

L_1 = 250 μH
L_2 = 50 μH

Thyristors (alloy-diffused types):

10-20 A range	30-70 A range	100-250 A range
R_2 = 47 Ω, 2 W	33 Ω, 5.5 W	22 Ω, 10 W
C_1 = 5 μF, 280 V a.c.	10 μF, 280 V a.c.	10 μF, 280 V a.c.
C_2 = 0.1 μF, 1500 V d.c.	0.22 μF, 1500 V d.c.	0.47 μF, 1500 V d.c.
C_3 = 1.5 μF, 280 V a.c.	5 μF, 280 V a.c.	5 μF, 280 V a.c.

* See footnote page 107

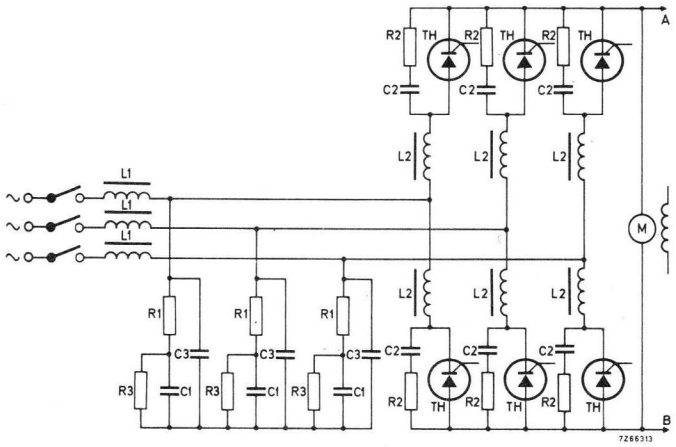


Fig. 4.41. Three-phase fully-controlled bridge (A-B is parallel connection to bridge working in opposition).

Components list to Fig. *4.41* (All components 10% tolerance)*

Nominal supply voltage 415 V r.m.s.

R_1 = 8.2 Ω, 10 W
R_3 = 33 kΩ, 2 W

L_1 = 250 μH
L_2 = 250 μH (d.c. choke)

Thyristors (alloy-diffused types):

10-20 A range	30-70 A range	100-250 A range
R_2 = 82 Ω, 2 W	82 Ω, 2 W	56 Ω, 5.5 W
C_1 = 5 μF, 280 V a.c.	10 μF, 280 V a.c.	10 μF, 280 V a.c.
C_2 = 0.1 μF, 1500 V d.c.	0.1 μF, 1500 V d.c.	0.22 μF, 1500 V d.c.
C_3 = 1.5 μF, 280 V a.c.	5 μF, 280 V a.c.	5 μF, 280 V a.c.

* See footnote page 107

4.2.9 Circuit Analysis and Design Procedure

Single-Phase Circuits

The input suppression circuit has to be designed to limit dV/dt at switch-on, and to have an acceptable voltage overshoot and a known ability to absorb random supply voltage transients.

The circuit analysis will be described under the following subsections:

1. dV/dt as a function of damping factor,
2. voltage overshoot as a function of damping factor,
3. filter output voltage as a function of choke quality factor,
4. dV/dt as a function of choke quality factor,
5. transient suppression as a function of transient amplitude and duration.

From the results of this analysis, it is possible to formulate certain broad conclusions. Design abacs are given from which suitable component values can be selected.

dV/dt *as a Function of Damping Factor.* In the equivalent circuit of Fig. 4.42, the a.c. supply has been replaced by a battery of voltage V, where in practice V is the crest supply voltage V_{WM}.

If the output voltage immediately after closing of switch S is V_o, it can be shown that:

$$\frac{dV_o}{dt} = V\left[\frac{\omega_n}{\sqrt{(1-\eta^2)}} \cdot \sin\left\{\omega_n t \cdot \sqrt{(1-\eta^2)} + 2\phi\right\} \exp\left(-\eta\omega_n t\right)\right], \tag{4.11}$$

where $\omega_n = 1/\sqrt{(LC)}$, the damping factor $\eta = R/(2\omega_n L)$, and $\phi = \arcsin \eta$. The time t_c at which this expression has a maximum value is given by:

$$t_c = \frac{\pi/2 - 3 \arcsin \eta}{\omega_n \sqrt{(1-\eta^2)}}. \tag{4.12}$$

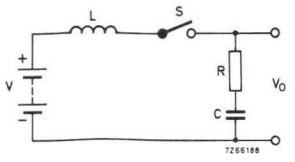


Fig. 4.42. Equivalent circuit of input transient suppression filter.

It can be shown that t_c takes negative values for $\eta \geqslant 0.5$, so only the interval $0 \leqslant \eta \leqslant 0.5$ need be considered. The solutions of Eq. 4.12 for times t_c between 0 and $\pi/(2\omega_n)$ are shown graphically in Fig. 4.43.

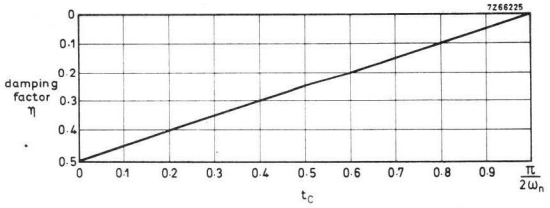


Fig. 4.43. Solutions of Eq. 4.12 for range $0 \leqslant \eta \leqslant 0.5$.

To find the maximum value of dV_o/dt, the value of $t = t_c$ from Eq. 4.12 is substituted into Eq. 4.11 which gives:

$$\left(\frac{dV_o}{dt}\right)_{max} = V\left[\omega_n \,.\, \exp\left\{\left(\frac{\pi}{2} - 3 \arcsin \eta\right)\left(-\frac{\eta}{\sqrt{(1-\eta^2)}}\right)\right\}\right], \tag{4.13}$$

for $0 \leqslant \eta \leqslant 0.5$.

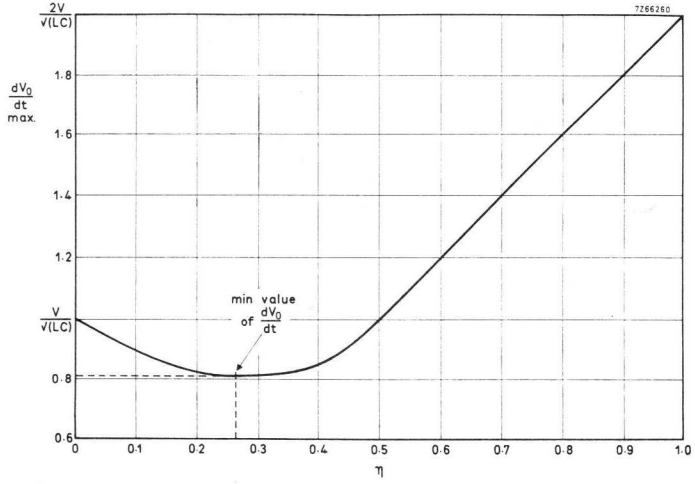


Fig. 4.44. Solutions of Eq. 4.13 for range $0 \leqslant \eta \leqslant 1.0$.

For the special case $\eta = 0.5$:

$$\left(\frac{dV_o}{dt}\right)_{max} = 2\,\eta\omega_n V = V\frac{R}{L} = V\left\{\frac{1}{\sqrt{(LC)}}\right\}.$$

The solutions of Eq. 4.13 for a range of values of η are shown graphically in Fig. 4.44, from which it may be seen that the minimum value of (dV_o/dt) max. occurs when $\eta \simeq 0.265$. Under these conditions:

$$\left(\frac{dV_o}{dt}\right)_{max} = 0.81\,V\left(\frac{R}{L}\right) = 0.81\,V\left\{\frac{1}{\sqrt{(LC)}}\right\}.$$

Voltage Overshoot as a Function of Damping Factor. It can be shown that the instantaneous output voltage from the equivalent circuit of Fig. 4.42 is given by:

$$v_o = V\left[1 - \frac{\cos\{\omega_n t\,.\,\sqrt{(1-\eta^2)} + \phi\}}{\sqrt{(1-\eta^2)}}\,.\exp(-\eta\omega_n t)\right]. \tag{4.14}$$

The value of v_o has a maximum value when:

$$t = \frac{(\pi - \phi)}{\omega_n\,.\,\sqrt{(1-\eta^2)}}\,. \tag{4.15}$$

Substituting Eq. 4.15 in Eq. 4.14 gives:

$$V_{o(max)} = V\left[1 + \frac{1}{\sqrt{(1-\eta^2)}}\,.\exp\left\{(\pi - \arcsin\eta)\left(-\frac{\eta}{\sqrt{(1-\eta^2)}}\right)\right\}\right]$$

This peak voltage V_p may be expressed as a percentage overshoot of the applied voltage V:

$$V_p = \frac{1}{\sqrt{(1-\eta^2)}}\,.\exp\left\{(\pi - \arcsin\eta)\left(-\frac{\eta}{\sqrt{(1-\eta^2)}}\right)\right\} \times 100\,\%$$

The values of V_p for a range of values of η are shown graphically in Fig. 4.45.

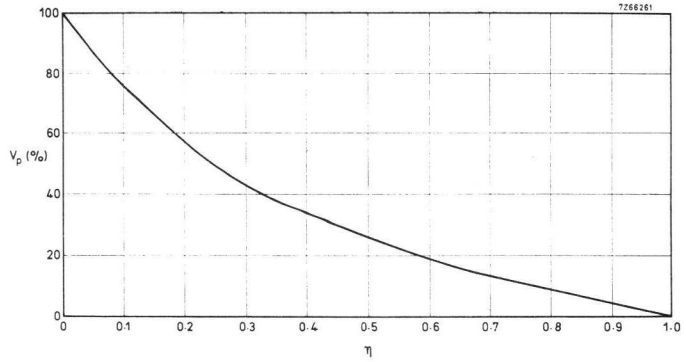


Fig. 4.45. Percentage overshoot V_p for range $0 \leqslant \eta \leqslant 1.0$.

It should be remembered that the total input series inductance must be used when the value of damping resistance is being calculated. This will include the leakage inductance of any input transformer as well as line and series choke inductance.

Filter Output Voltage as a Function of Choke Quality Factor. If the series choke or supply impedance shown in Fig. 4.22 as a series loss component R_1 is not negligible compared with R_2, further calculations are necessary. To simplify the result, we shall consider only the case when the circuit is critically damped, that is, when $\eta = 0.5$. In this case:

$$\eta = \frac{(R_1 + R_2)}{2\omega L_1}.$$

It can be shown by normal circuit analysis methods that the instantaneous output voltage is given by:

$$v_o = V\left(\frac{\omega t}{Q} + 1\right)\left\{1 - \exp(-\omega t)\right\}, \tag{4.16}$$

where:

$$\omega = \frac{1}{\sqrt{(L_1 C_1)}}, \quad \text{and} \quad Q = \frac{\omega L_1}{R_1}:$$

that is, Q is the quality factor of the series choke. Eq. 4.16 has been evaluated for a range of values of Q from $Q = 1$ to $Q = \infty$. The results are shown graphically in Fig. 4.46.

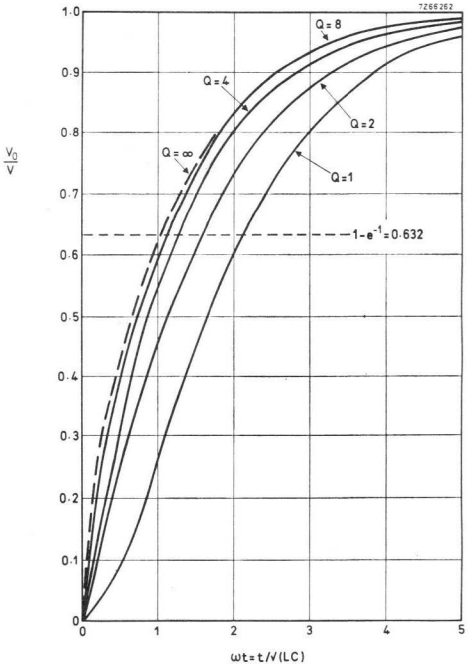


Fig. 4.46. Solutions of Eq. 4.16 for Q = 1, 2, 4, 8 and ∞.

It will be seen that for chokes with a Q-factor of more than 8, there is very little change in voltage rise or maximum dV/dt, but if the Q-factor of the choke is less than 2 the shape of the curve is modified considerably.

This graph also indicates the need for a clear definition of dV/dt, as the maximum value does not always occur at $t = 0$; it is internationally agreed to take the 63.2% point. This level is indicated on Fig. 4.46 and shows a factor of 2 improvement between similar circuits where the Q-factor of the choke is either high or unity. It may therefore be possible to introduce useful circuit economies by intentionally introducing high-frequency loss into the series choke, and thereby reducing the size of the shunt capacitor or inductance of the choke that is required to achieve a given value of mean dV/dt.

dV/dt *as a Function of Choke Quality Factor.* Differentiating Eq. 4.16 gives:

$$\frac{dV_o}{dt} = \omega V\left(\frac{\omega t - 1}{Q} + 1\right)\exp(-\omega t).$$

For values of $Q \geqslant 2$, the maximum real value of this expression occurs at time $\omega t = 0$. When $Q = 1$, the maximum dV_o/dt is at $\omega t = 1$.

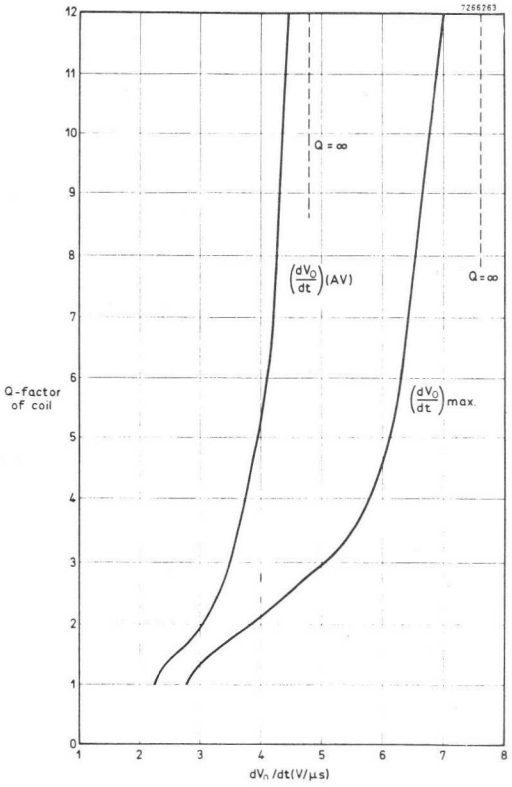


Fig. 4.47. Values of dV_0/dt *for a critically-damped circuit with a crest supply voltage of 340 V, inductance of 500 μH and a 4 μF capacitor.*

In the general case for $Q \geqslant 2$:

$$\left(\frac{\mathrm{d}V_o}{\mathrm{d}t}\right)_{\max} = \omega V\left(1 - \frac{1}{Q}\right),$$

and for the particular case $Q = 1$:

$$\left(\frac{\mathrm{d}V_o}{\mathrm{d}t}\right)_{\max} = 0.368\ \omega V.$$

Values of $(\mathrm{d}V_o/\mathrm{d}t)$max. for a crest supply voltage of 340 V, an inductance of 500 μH, and a capacitor of 4 μF, all with the circuit critically damped, are shown graphically in Fig. 4.47. There are no values for $Q < 1$ as in such cases the circuit would become overdamped, and the boundary condition would not be valid. This graph clearly shows the advantage to be gained from the use of a choke with high losses, and also that for $Q > 5$, say, the losses may to a first approximation be neglected and the analysis will be valid, at least for circuits with component values of this order of magnitude.

So far the maximum value of $\mathrm{d}V/\mathrm{d}t$ has been considered. Alternatively the rate of rise of voltage in terms of the apparent time-constant of the circuit may be specified; that is, from the time taken for the output voltage to reach 63.2% of its final value. The same circuit constants yield a second set of values for $(\mathrm{d}V_o/\mathrm{d}t)_{AV}$ as shown in Fig. 4.47. Here the difference between the two methods of defining $\mathrm{d}V/\mathrm{d}t$ shows up most when the coil Q-factor is high. The choice of definition will depend upon the method used to specify the maximum permissible $\mathrm{d}V/\mathrm{d}t$ value for the thyristor.

Some measured results are shown in Fig. 4.48 all for iron-cored chokes rated at the full line current. Curve *A* may be compared with theoretical curves *X* and *Y*. From an examination of these curves, the difficulties associated with a theoretical approach to this problem will become apparent. For example, it appears that the 780 μH choke (*A*) has a Q-factor of about 2 at a frequency determined by a 1.0 μF capacitor, and a Q-factor of about 5 when the capacitor is increased to 6.0 μF. Since the chokes were designed for use at 50 Hz this performance is to be expected, and in fact can be put to good use as relatively smaller capacitors can be used for a given value of $\mathrm{d}V/\mathrm{d}t$. On the other hand, unless a considerable amount of information is available about choke loss at high frequency,

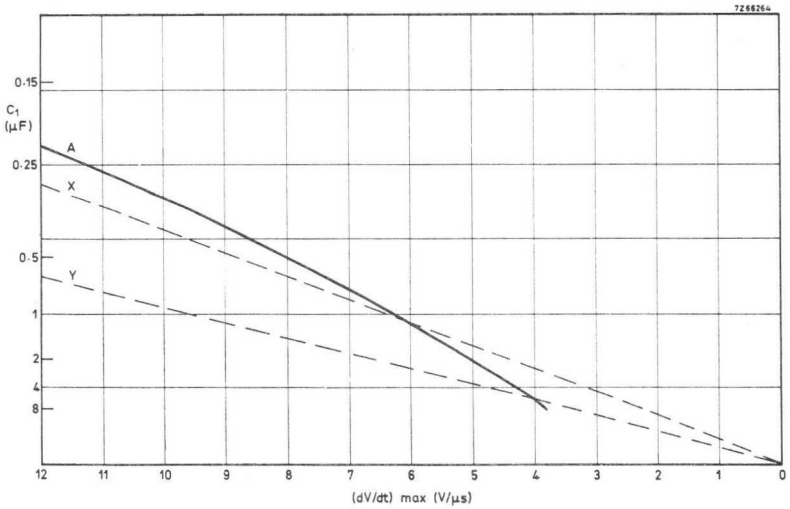


Fig. 4.48. Measured values of $(dV/dt)max$ *for iron cored chokes rated at full line current (unbroken line) with theoretical values (broken lines) for comparison.*

Curve	*Inductance (μH)*	*Resistance (Ω)*	*Rating (A)*	*Q-factor*
A*	780	22	36	—
X	780	22	—	2
Y	780	22	—	5

* circuit approximately critically damped

it is difficult to predict the performance of a particular circuit with any accuracy.

It is possible, and in some cases desirable, to use air-cored chokes, the performance of which can be obtained more accurately; but the high-frequency losses will be lower, requiring a larger capacitor. Thus both the capacitor and choke will almost certainly be more expensive.

Transient Suppression as a Function of Transient Amplitude and Duration. The bridge input inductance-capacitance filter serves two purposes. It reduces dV/dt on switch-on, and reduces the amplitude of random voltage transients which may occur on the mains.

If the maximum rate of rise of output voltage from the filter is known in terms of crest applied voltage, the time taken to reach a certain voltage level may be calculated. The relationship between peak transient voltage, transient duration, and output voltage may therefore be established.

For a given critically-damped filter circuit:

$$\left(\frac{dV_o}{dt}\right)_{max} = \omega V\left(1 - \frac{1}{Q}\right),$$

where $\omega = \dfrac{1}{\sqrt{(L_1 C_1)}}$,

Q is the Q-factor of the series choke, and V is the crest voltage V_{WM}. For most input circuits, $Q \gg 1$, therefore:

$$\left(\frac{dV_o}{dt}\right)_{max} \simeq \omega V.$$

If a transient of amplitude V and duration τ is applied, the maximum output voltage is given by:

$$\left(\frac{dV_o}{dt}\right)_{max} = \omega V \quad \text{or} \quad V_o = \omega V \tau.$$

In practice, it will be necessary to keep the value of V_o below a certain maximum value such that the crest supply voltage plus V_o is always less than the forward breakover voltage of the thyristors. For a 240 V single-phase supply, it is normally satisfactory to use 600 V thyristors (which have a forward blocking capability of 700 V). With a 10% rise in supply voltage, the crest supply becomes 375 V, so that the maximum possible transient is 225 V. For safety, the maximum permissible transient voltage

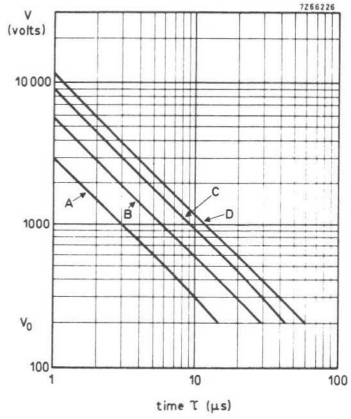


Fig. 4.49. Maximum possible transient peak voltage-time product for single-phase circuits using 600 V thyristors.

Curve	*Inductance* (μH)	*Capacitance* (μF)	*Q-factor*
A	50	4	∞
B	200	4	∞
C	500	4	∞
D	500	4	5

input to the bridge is taken as 200 V; that is, $V_{o(\max)} \leqslant 200$ V. Thus:

$\omega V\tau \leqslant 200$, or if ω is known: $V\tau \leqslant 200/\omega$.

It is therefore possible to calculate, for any particular single-phase circuit, the maximum permissible peak voltage-time product. Some typical results are shown in Fig. 4.49.

Three-Phase Circuits

All that has been said in the preceding part of this section concerning single-phase systems applies equally to three-phase systems, particularly when the suppression network is connected between each line and a common neutral. Usually, in a three-phase system, a higher voltage excursion is permissible. The crest voltage of 440 V supply +10% is 685 V,

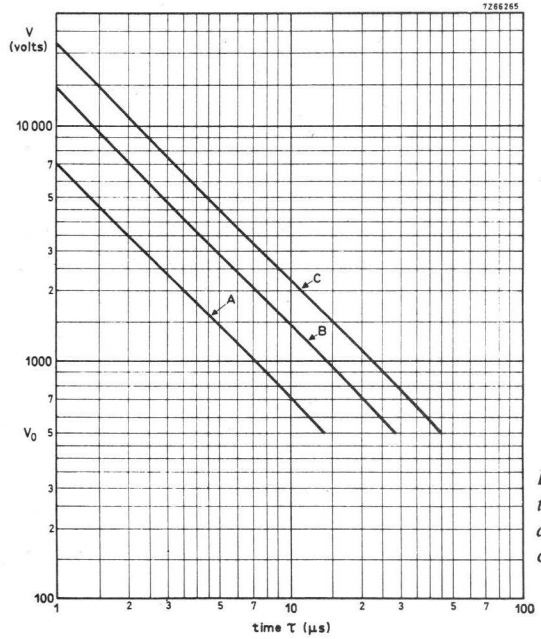


Fig. 4.50. Maximum permissible transient peak voltage-time product for three-phase 440 V circuits using 1200 V thyristors.

Curve	*Inductance* (μH)	*Capacitance* (μF)	*Q-factor*
A	50	4	∞
B	200	4	∞
C	500	4	∞

so that if 1200 V thyristors are used a transient of up to 500 V may be permitted. Thus:

$$V\tau \leqslant 500/\omega.$$

Some typical solutions are shown in Fig. 4.50.

When a neutral is not available, the input suppression circuits may be connected from line-to-line, and to some extent are equivalent to the single-phase line-to-line circuit. A complete analysis of this system has not been carried out, but measured results correspond very closely with those obtained from the single-phase line-to-line analysis. It is recommended, however, that the suppression circuits should be connected line-to-neutral whenever possible.

4.3 Fusing

4.3.1 Introduction

Because of their low heat capacity, semiconductor devices are sensitive to overloads containing sufficient energy to damage the junction. Power circuits using semiconductor devices therefore require careful fusing to achieve the most economical design consistent with adequate protection.

A distinction should be drawn between fuses for short-term overloads and those for long-term overloads. In a short-term overload, a rapid surge of current occurs of such a high value that (with no fuse) the semiconductor device breaks down within one half-cycle, that is, within 10 ms. With a long-term overload, the current exceeds the permitted continuous limiting value but does not cause a breakdown of the device until after 10 ms, and in some cases not until after seconds or even minutes. Protection against short-term overloads is generally provided by special fuses having an ultra-fast fusing characteristic. For protection against long-term excess current, there are suitable fuses available although the usual method is to use a fast-operating overload contactor. Protection can also be provided by electronic means to prevent triggering of thyristors after an overload has occurred.

When a circuit has been fused for both short-term and long-term overloads, it is described as having complete protection. In some cases, this protection can be provided by a single fuse. This is particularly so when the semiconductor devices are used with currents below the nominal rating, and correspondingly weaker fuses can be used.

4.3.2 General Considerations of Fusing

Construction

The body of a fuse generally consists of a glazed, metal-capped ceramic tube. Large contact blades or helical lugs provide good electrical contact, while at the same time serving to dissipate heat. The fusing elements, preferably made of pure silver, are embedded in a quenching material – for example, specially treated quartz sand – which provides good heat transfer and rapid quenching of the partial arc that occurs on fusing.

The fusing elements, according to the rated voltage of the fuse, have one or more constrictions arranged one after the other, the number and form of which greatly affect the fusing characteristic and interrupting capacity of the fuse. This applies particularly to ultra-fast fuses where the constrictions attain relatively high temperatures even at the rated current.

Characteristics of Short-circuit Current

For calculation of the current characteristic when a short-circuit occurs, the equivalent circuit shown in Fig. 4.51 is used. In the figure, R represents the total resistance in the short-circuited line, and L represents the total inductance. The current characteristic can be calculated from the expression:

$$i_{sc} = I_{sc(M)} \{\sin(\omega t + \psi - \phi) - \sin(\psi - \phi) \exp(-\omega t/\tan\phi)\} \quad (4.17)$$

where i_{sc} is the instantaneous value of short-circuit current surge, $I_{sc(M)}$ is the peak value of the transient short-circuit current, and ψ is the angle between zero voltage and the occurrence of the short-circuit which is taken to be at time $t = 0$.

Normally a short-circuited line is highly inductive, and the phase angle can be taken as 90° without any great error. Therefore the maximum

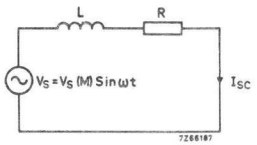


Fig. 4.51. Equivalent circuit for short-circuited line.

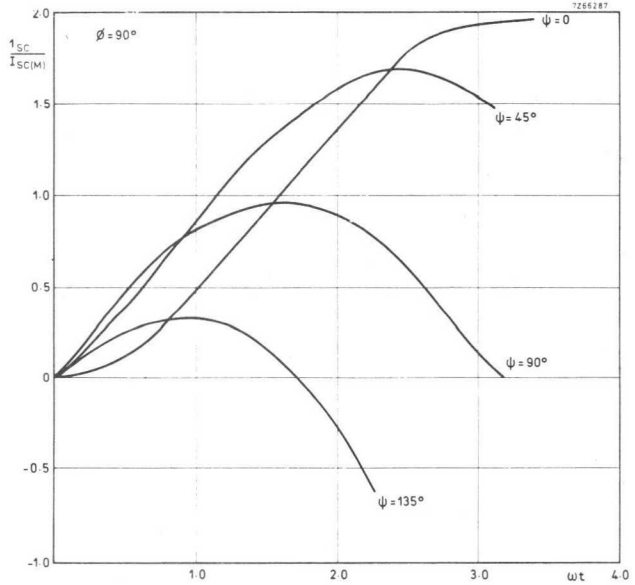


Fig. 4.52. Characteristics of short-circuit current for various values of Ψ.

possible value of short-circuit current is obtained if the short-circuit occurs when the supply voltage passes zero. This can be shown by substituting $\phi = 90°$ in Eq. 4.17, and if values of 0, 45, 90 and 135° are taken for ψ, the characteristics for $i_{sc}/I_{sc(M)}$ shown in Fig. 4.52 are obtained.

These curves show that the maximum possible peak value of $i_{sc}/I_{sc(M)}$ occurs for $\psi = 0$, the corresponding value of $I_{sc(M)}$ being denoted by $I_{sc(M)}\text{max}$. By differentiating Eq. 4.17 with respect to ωt and ψ, we can show that for any value of ϕ the value $I_{sc(M)}$ max is obtained when the short-circuit occurs at zero voltage, that is, when $\psi = 0$. For $\phi = 90°$:

$$\frac{I_{sc(M)}\text{max}}{I_{sc(M)}} = 2.$$

When the angle ϕ decreases, the value of the ratio decreases to 1 at $\phi = 0$.

The ratio $I_{sc(M)}\text{max}/I_{sc(M)}$ is plotted against angle ϕ in Fig. 4.53. In practice, values of about 1.6 are obtained for this ratio, corresponding to a phase angle of approximately 80°.

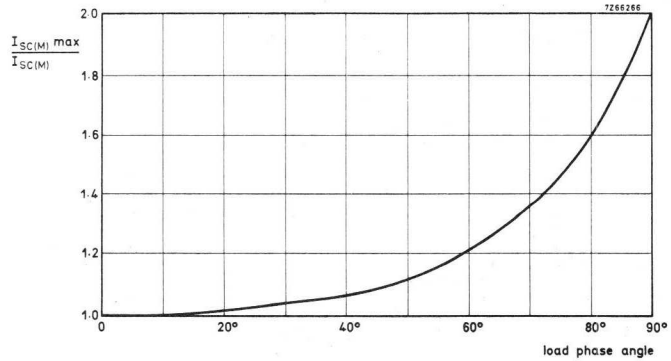


Fig. 4.53. Ratio of maximum possible peak-value to nominal peak value of short-circuit current, plotted against load phase angle.

It can be seen from Fig. 4.52 that the peak value of the ratio is not determined by the initial slope of the curve. If Eq. 4.17 is differentiated with respect to ωt, the initial slope of the curve is given by:

$$\text{initial slope} = I_{sc(M)} \cdot \frac{\sin \psi}{\sin \phi}$$

This shows that independently of the value of ϕ, the maximum initial slope occurs for $\psi = 90°$; that is, at the supply voltage crest.

In short, the maximum possible peak value of short-circuit current $I_{sc(M)}$max is obtained when the short-circuit occurs as the supply voltage passes zero. The maximum initial rate of rise of the short-circuit current occurs when the short-circuit occurs at the supply voltage crest.

Short-circuited Line with Fuse

If a fuse is incorporated in the circuit of Fig. 4.51 and a short-circuit is applied, the fusing element will melt as soon as a given energy – the melting energy – is attained. Two processes occur within the fuse. Initially the fusing element melts, and the time taken for this part of the process is called the melting time. Then an arc is established across the fuse gap, and the duration of this is called the arcing time. The sum of the melting and arcing times is called the clearing time of the fuse.

Melting Time. With a short-circuit, the energy is applied to the fuse so quickly that the heat dissipation can be neglected, and it can be assumed that all the energy is used to melt the fusing element. The value of the current at the instant the required melting energy is reached (bringing about the end of the melting time and introducing the arcing time) is of particular interest. This current value $I_{fu(M)}$ represents the maximum possible instantaneous value to which the fuse limits the short-circuit current. It is assumed that the short-circuit occurs at the "most unfavourable" time, that is, when $\psi = 90°$, so that the initial rise in the short-circuit current is the steepest, the time to attain the required melting energy is a minimum, and so the corresponding peak value of the current must be the maximum. Under these conditions, and assuming the line to be purely inductive ($\phi = 90°$), Eq. 4.17 simplifies to:

$$i_{sc} = I_{sc(M)} \sin \omega t. \tag{4.18}$$

This equation represents a special case when $\psi = \phi$, and shows that in this case there is no transient – so no excessive increase in current occurs.

Often the value to which the fuse limits the short-circuit current in the most favourable case is small compared with the peak value $I_{sc(M)}$. This means that up to the fusing value, the rise of the short-circuit current can be considered linear. The initial slope is obtained by differentiating Eq. 4.18 at $t = 0$, giving:

$$\text{initial slope} = \omega I_{sc(M)}. \tag{4.19}$$

The time taken for the current to reach the fusing value is obtained by integrating Eq. 4.19

$$i_{sc} = \omega I_{sc(M)} t \tag{4.20}$$

and solving for t.

The melting energy of a fuse E_{melt} is assumed to be constant and is given by:

$$E_{melt} = \int_{t_0}^{t_1} R_{fu} i_{sc}^{\,2} \mathrm{d}t = \bar{R}_{fu} \int_{t_0}^{t_1} i_{sc}^{\,2}\, \mathrm{d}t, \tag{4.21}$$

where R_{fu} is the resistance of the fusing element and $\bar{R}_{fu}$ the mean value, t_0 is the time at which the short-circuit occurs (usually taken as zero), and t_1 the time at which the fusing element melts.

If the melting energy and $\bar{R}_{fu}$ are combined to form one constant K. Eq. 4.21 becomes:

$$K = \int_{t_0}^{t_1} i_{sc}^2 \, dt. \tag{4.22}$$

This integral is known as the melting I^2t value of the fuse.

If the expression for i_{sc} from Eq. 4.20 is substituted in Eq. 4.22 and the integral evaluated, then:

$$K = \frac{\omega^2 I_{sc(M)}^2 \, t_1^3}{3},$$

(since $t_0 = 0$) from which the melting time t_1 can be obtained as:

$$t_1 = \left[\frac{3K}{\omega^2 I_{sc(M)}^2} \right]^{\frac{1}{3}}$$

and the fusing peak current value as:

$$I_{fu(M)} = [3K\omega I_{sc(M)}]^{\frac{1}{3}}. \tag{4.23}$$

The relationship between a given fuse (characterised by the fuse constant K) and the value to which the short-circuit current is limited by the fuse $I_{fu(M)}$ is shown by Eq. 4.23. To enable suitable fuses to be selected, manufacturers issue data from which the fusing current, as a function of the r.m.s. value of the short-circuit current, can be read off directly for each type of fuse.

The preceding calculations were based on the assumption that the fusing current was small compared with the peak value of the short-circuit current. This is usually so, although cases can occur where the difference between the two current values is small. It can then no longer be assumed that the current rises linearly to the fusing value. The fact that the maximum initial rate of rise occurs for $\psi = 90°$ is no longer significant, and the maximum *mean* rate of rise of the short-circuit current surge determines the value of the fusing current. The "most unfavourable" condition for a short-circuit is shifted from $\psi = 90°$ to a somewhat lower value.

Arcing Time. As soon as sufficient energy is applied to the fusing element, it melts. The melting process begins at the constrictions, and the arc generated causes the quenching material to sinter. The resistance of the sintered spiral which is formed increases very rapidly, and after a few milliseconds has already reached such a high value that the current becomes practically zero, and the circuit is interrupted.

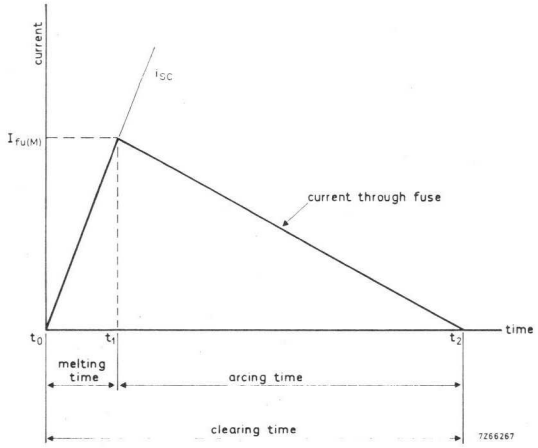


Fig. 4.54. Idealised flow of short-circuit current through a fuse when the fuse blows.

Fig. 4.54 is an idealised representation of the flow of current through a fuse. The clearing time of the fuse ($t_2 - t_0$) can only be determined experimentally, as it depends on the construction of the fuse and the rating of the circuit (particularly the applied voltage). The same is true of the area under the curve which represents the quenching integral over the time t_1 to t_2.

During the melting time t_0 to t_1, magnetic energy is stored in the inductance of the mains transformer or generator and the leads. The total magnetic energy E_{mag} at time t_1 is:

$$E_{mag} = \tfrac{1}{2} L I_{fu(M)}{}^2,$$

where L, the total inductance in the circuit, is taken to be independent of the current and therefore constant. The arc can only be quenched when

the magnetic energy has been dissipated, either as heat and light in the arc itself, or returned to the mains. The magnitude of the magnetic energy depends on the inductance and the square of the fusing current, whereas the time for the dissipation of the energy depends on the resistance of the inductive elements and the supply voltage, as well as on the inductance and fusing current.

During the dissipation process, a voltage arises from the inductance because of the change of current. The voltage across the fuse is therefore the difference between the supply voltage and the voltage from the inductance. Even if the supply voltage is zero or negative, the arc can be maintained by the voltage from the inductance.

By analogy with Eq. 4.22, an integral of the arcing current can be evaluated over the arcing time of the fuse to give the quenching I^2t value of the fuse. Unlike the melting I^2t value, the quenching I^2t value has no constant but depends on a number of factors.

The addition of the melting and quenching I^2t values gives the total I^2t value of the fuse. This value is an important characteristic of the fuse. It depends on the maximum possible short-circuit current and the voltage of the circuit in which the fuse is placed, and can be obtained from the data for the fuse.

4.3.3 Characteristics of a Fuse

Rated Current

There are two methods of determining, for a particular installation, the current value on which the choice of fuse is based. These methods are – selecting the fuse to suit the thyristors and selecting the fuse to suit the operating current.

When the fuse is selected to suit the operating current, the value used is the r.m.s. value of the current flowing through the fuse during normal working.

When the fuse is selected to suit the thyristor, the value used is the r.m.s. current rating of the thyristor which may be obtained from the data. This method of selection is considered in more detail in the next sub. section.

Rated Voltage

Every fuse is given a voltage rating by the manufacturer. This always refers to a.c. voltage (sometimes the peak value but usually the r.m.s. value). When selecting a fuse, always ensure that the rated voltage of the fuse is the same as, or greater than, the operating voltage.

When fuses are used in d.c. circuits, the operating voltage should be lower by a specified amount than the voltage rating of the fuse. Manufacturers provide data on this derating, and typical values, as recommended by English Electric, are shown in Table 4.6.

Table 4.6 Derating of Fuses for DC Applications

rated voltage (for a.c. operation) (V)	maximum voltage for d.c. operation (V)
150	115
300	200
450	200
1000	400
2000	1250
3000	1500

Fusing Peak Current

The fusing peak current value $I_{fu(M)}$ is the maximum possible value to which the fuse limits the short-circuit current. No definite value for $I_{fu(M)}$ can be given for a particular type of fuse, as it depends to a large extent on the maximum possible short-circuit current in the installation. Once this value for a particular installation has been determined, the corresponding $I_{fu(M)}$ value can be found from the manufacturer's data.

The $I_{fu(M)}$ value should be compared with the surge current rating of the thyristors. Since the fusing current characteristic is approximately a triangle of height $I_{fu(M)}$ (as shown in Fig. 4.54), while the surge current rating is the peak of a half-sinewave, no direct comparison is possible. However, it has been found in practice that the surge current rating of the thyristors is maintained when the $I_{fu(M)}$ value of the fuse is equal to or less than 1.4 times the I_{TSM} rating of the thyristors.

When the thyristors in a particular installation are supplied from the

secondary winding of a transformer, the rated secondary current and percentage impedance of the transformer are required before the short-circuit current can be calculated. If these values are not known or cannot be calculated from the transformer characteristics, they must be determined experimentally.

When the rated secondary current and percentage impedance of the transformer are known, the r.m.s. value of the short-circuit current can be calculated from:

$$I_{sc(r.m.s.)} = I_{sec(r.m.s.)} \cdot \frac{100}{Z_{pc}},$$

where $I_{sec(r.m.s.)}$ is the r.m.s. value of the transformer rated secondary current, and Z_{pc} is the percentage impedance of the transformer.

The peak value of the short-circuit current is:

$$I_{sc(M)} = \sqrt{2} \cdot I_{sc(r.m.s.)},$$

and the most unfavourable value occurring in practice is:

$$I_{sc(M)}\text{max} = 1.6 \times \sqrt{2} \cdot I_{sc(r.m.s.)},$$

as mentioned in Sub-Section 4.3.2.

I^2t Value

For a particular type of fuse, the I^2t value can only be found for a particular installation from the manufacturer's data. The I^2t value of the fuse must be lower than the I^2t rating of the thyristor to be protected.

Fusing-time (current/time) Characteristic

The fusing-time characteristic applies only to the overload range that is, for times equal to or greater than 10 ms. From this characteristic, the time between the occurrence of the overload and the blowing of the fuse can be found. The fusing-time characteristic is based on the assumption that the fuse carries the nominal current before an overload occurs. If the calculations are made on the basis that the fuse does not carry current initially, a different characteristic is obtained.

Protection against overload is given when the fusing-time characteristic

for the total overload range is lower than the corresponding limiting-current characteristic of the thyristor.

Rated Interrupting Capacity

The rated interrupting capacity of a fuse is specified either as a current value or as an output value. Nominal interrupting current is usually the r.m.s. value of the maximum permissible short-circuit current $I_{sc(r.m.s.)}$, but in exceptional cases the peak value $I_{sc(M)}$max is used instead.

The fuse will operate satisfactorily when the rated interrupting capacity is higher than the corresponding value of the installation.

Arc Voltage

An arc voltage can occur when the fuse blows, and care must be taken to ensure that the maximum possible arc voltage does not lead to a switching voltage which exceeds the permissible blocking voltage of the thyristor. The maximum possible arc voltage depends on the operating voltage, an example being given in Fig. 4.55, and can be found, for a particular type of fuse, from the manufacturer's data.

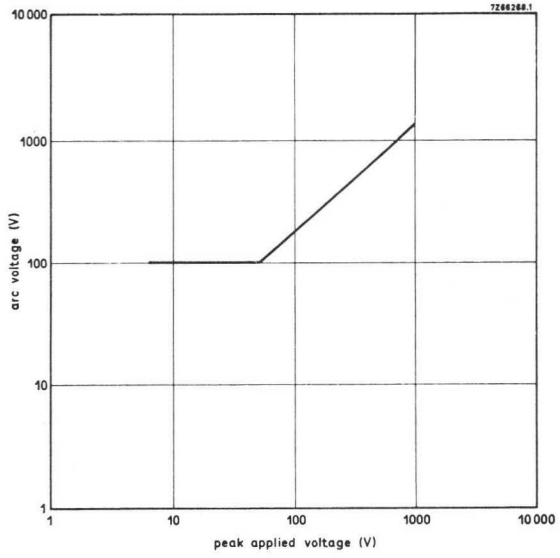


Fig. 4.55. Dependence of arc voltage in a short circuit on peak applied voltage, for a fuse with 1000 V rating.

4.3.4 Thyristor Characteristics that determine Fuse Selection

Rated Current

For the selection of a fuse (as stated in the previous section) the r.m.s. current of the installation, or of the thyristors, must be known. Most thyristors have a maximum r.m.s. current specified in the data, which usually applies over a wide range of form factors, or the r.m.s. value can be calculated from the given mean value. When a fuse is selected on the maximum r.m.s. current of an installation, it is necessary to know the form factor. The form factors for the commonly used configurations are listed in Table 4.7.

Table 4.7 Form Factors

configuration	form factor *)
half-wave	1.57
bridge	1.57
two-phase halfwave	1.57
three-phase bridge	1.73
three-phase halfwave	1.76
double star with interphase transformer	1.76
six-phase half-wave	2.45

* The form factor is for conversion of mean current value to the r.m.s. value; that is, $I_{o(r.m.s.)}$ = form factor $\times I_{o(AV)}$.

I^2t Value

The I^2t value is a measure of the heat capacity of the semiconductor element, and is usually specified. As the influence of heat dissipation for times less than 10 ms is slight, it is sufficient to give one I^2t value, generally referred to a time of 10 ms. This is a minimum value, and for increasing time the I^2t value increases.

To provide adequate protection against short-circuits, the I^2t value of the fuse should be lower than that of the thyristor.

Surge Current Characteristic Curve

The surge current characteristic is usually given for a range from 1 ms to 1 s. In the 1 to 10 ms range, it is normal to use the I^2t value for calculation. Even after the thyristor has been protected against short-circuits, it may still be that the surge current characteristic curve is below

that of the fuse in the range, say, 30 ms to 1 s. It may be more convenient in this range to limit the current by other methods. However, if a fuse is required to protect in all circumstances, the fuse current/time characteristic must be below that of the thyristor.

Maximum Surge Current

One of the absolute maximum ratings given for thyristors is the maximum surge current I_{TSM}. This is the peak value of a single 50 Hz half-sinewave when the device is in specified conditions. It has been found in practice that protection against short-circuits will be provided if the $I_{fu(M)}$ value is equal to or less than 1.4 times the I_{TSM} rating of the thyristor. However, this may give a conservative value, and calculations based on the I^2t value have proved satisfactory.

Transient Reverse Voltage

The maximum non-repetitive peak reverse voltage, V_{RSM}, given for most thyristors must only be maintained for very short times. In semiconductor devices with controlled breakdown, the breakdown voltage may be exceeded. Calculations on this problem involve complicated power considerations that go beyond the scope of this book. It is sufficient to say that the arc voltage should not exceed the non-repetitive peak reverse voltage of the thyristor or diode.

4.3.5 A Method of Fuse Selection

It was stated earlier that the I^2t value of a fuse varies with the applied voltage and the peak value of the short-circuit current. The thyristor data usually specify the value of I^2t at 10 ms. It is possible to draw a curve, using the fuse manufacturer's data at a given I^2t value, of applied voltage plotted against short-circuit current for various types of fuse.

As an example of the use of such curves, consider a rectifier bridge operating on a single-phase 220 V mains supply taking a supply current of 12 A. The r.m.s. current $I_{F(r.m.s.)}$ for each rectifier is 9 A. The peak applied voltage is taken as 350 V to allow a safety factor. From the curves in Fig. 4.56, if the 15 A fuse is selected for use in the supply line, the peak current must be limited to 400 A for protection against short-circuits. If this regulation is unacceptable, the 10 A fuse can be used in

series with each rectifier. The short-circuit current now must be limited to 2000 A, with improved regulation.

It is still necessary to ensure that the arc voltage of the fuse is less than the non-repetitive peak reverse voltage of the rectifiers, but the curves of Fig. 4.56 simplify the calculations for short-circuit protection.

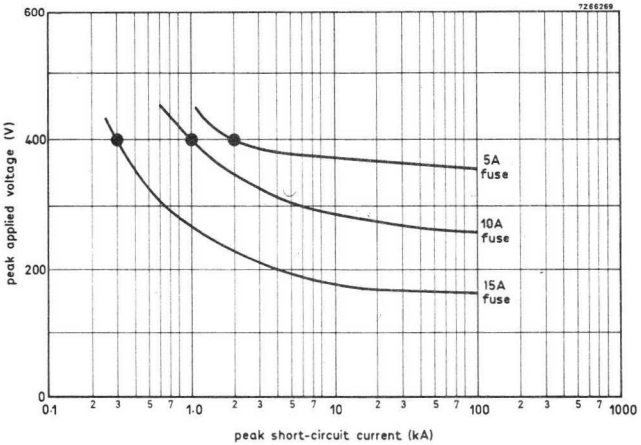


Fig. 4.56. Relationship between peak short-circuit current and peak applied voltage for fuses of different ratings.

References

1. See
   (a) "Introduction To Heat Transfer" by Brown and Marco, published by McGraw-Hill Book Company Inc., London.
   (b) "Heat Transfer" Volume I-II by M. Jakob, published by Chapman-Hall Limited, London.
   (c) "Heat Transmission" by William H. McAdams, published by McGraw-Hill Book Company Inc., London.

5 Thyristor Control Techniques

5.1 General

Since their introduction, thyristors have been steadily replacing earlier devices in all conventional areas of power control. At first, the high cost of the early thyristors restricted them to applications where conventional techniques were unsuitable; however, now that prices have fallen so much, there is rarely any good reason not to use thyristors in power control applications – the advantages they offer over earlier devices, but at a comparable price, make their choice almost inevitable.

There are two main techniques of controlling thyristors – on-off triggering and phase control. In on-off triggering, the thyristor is allowed to conduct for a certain number of positive half-cycles and then it is kept off for a series of positive half-cycles. Thus, by varying the ratio of "on time" to "off time", we vary the average power supplied to the load. In phase control, the thyristor is triggered into conduction at a point after the start of each positive half-cycle. Control is achieved by variation of the point, in the positive half-cycle, at which the thyristor is triggered.

5.2 Basic Thyristor Triggering

As we saw in Chapter 2, a thyristor can be triggered into conduction when a voltage of the appropriate polarity is applied across the main terminals and a suitable current is supplied to the gate. If the voltage across the main terminals is sinusoidal and the trigger pulse is supplied a little after the start of the positive half cycle, the voltage across the thyristor is as shown in Fig. 5.1(a). We can bring about this action by means of the circuit shown in Fig. 5.1(b). Greater stability of triggering point is achieved by the connection of a diode as shown in Fig. 5.1(c).

Even greater triggering stability can be attained if certain other devices are used in place of the diode. For instance, a diac can be used (see Fig. 5.2(a), which shows a trigger circuit suitable for both thyristors and triacs). Also, an SCS can be used (see Fig. 5.2(b)) but this is more suitable for triggering thyristors than triacs. If it is required to use an SCS for triac triggering, transformer coupling can be employed as shown in Fig. 5.2(c).

When there is a back e.m.f. across the load (for example, if the load is a motor), a wide trigger pulse is necessary to ensure triggering. It may be expensive to provide a transformer capable of passing a wide enough pulse so, for such cases, a good solution is to use a series of narrow pulses instead of a single wide one.

Nevertheless, an inductive load still imposes minimum limits on trigger-pulse width.

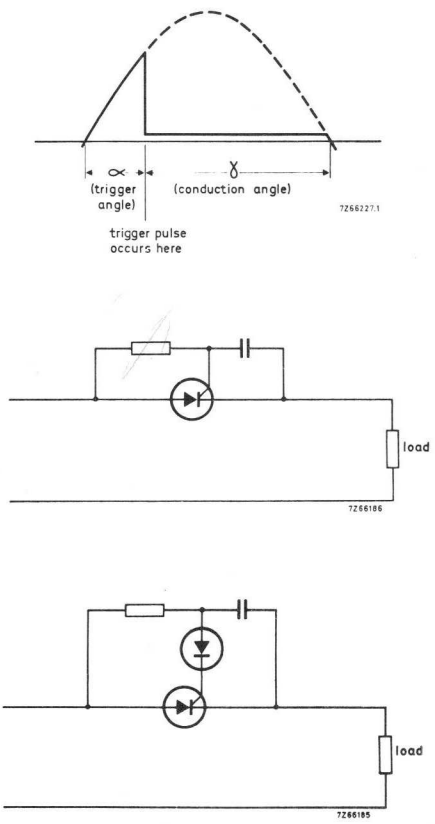
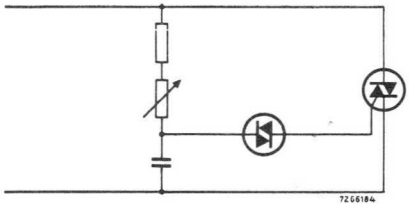
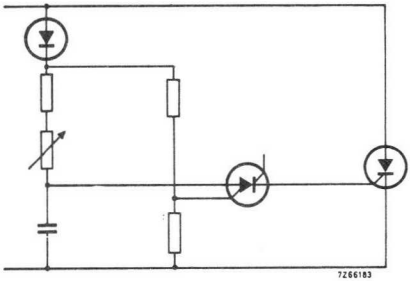


Fig. 5.1. (a) Voltage across thyristor,
(b) Basic trigger circuit,
(c) More stable trigger circuit.





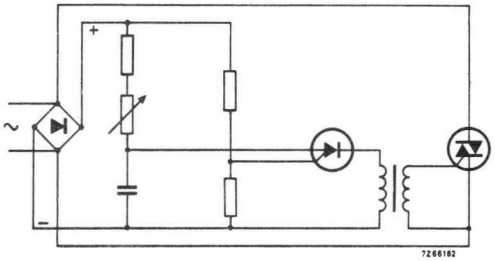
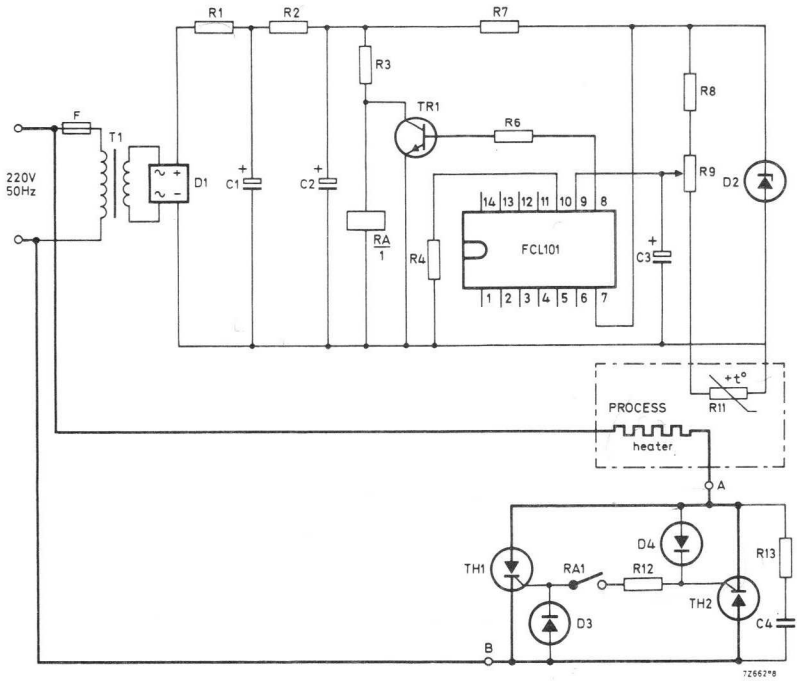
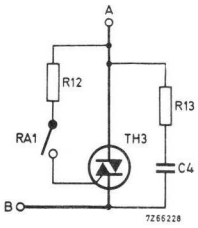


Fig. 5.2. (a) Diac trigger circuit,
(b) SCS trigger circuit,
(c) Triac trigger circuit with SCS.

5.3 On-Off Control

5.3.1 Simple On-Off Control





TR_1 = BC107

TH_1 = BTX68-600R
TH_2 = BTX68-600R
TH_3 = BTX94-600

T_1 = 220 V; secondary current 100 mA a.c.

RA = Reed relay 12 V, 15 mA, type 310/A1, catalogue no. 3522 247 68870

F = Fuse 220 V a.c., 50 mA

R_{12} = 220 Ω, 1/2 W
R_{13} = 56 Ω, 1/2 W
C_4 = 82 nF, 400 V d.c.
D_1 = BY123
D_2 = BZX79-C6V2
D_3 = BA148
D_4 = BA148

Fig. 5.3. On-off temperature control system (power circuit shown by heavy lines). Alternative power circuit using BTX94 triac (between points A and B) is shown below.

Often, a circuit is required to respond in a straightforward on/off way to maintain a physical variable at a constant value by regulating the flow of power to some form of energy converter. A typical example occurs in temperature control.

Fig. 5.3 shows an on/off temperature control circuit which uses an FCL101 level detector. The PTC thermistor R_{11} senses the temperature and establishes the voltage at the level detector input terminal (Terminal 9). A rise in temperature raises this voltage until the triggering level of the FCL101 is reached; the FCL101 then switches its output (Terminal 8) to high level – causing TR_1 to conduct. Reed relay RA cuts out and switches off gate current to TH_1 and TH_2 – so no more power is fed to the heater until the temperature drops sufficiently to reverse the process. Fig. 5.4 shows the heater waveforms.

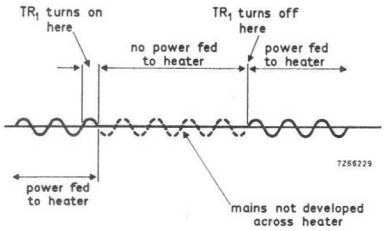


Fig. 5.4. Voltage across heater (heavy line).

5.3.2 Asynchronous Control

In asynchronous control, the thyristor(s) may be triggered at a point in the mains voltage other than the zero voltage crossover point. Asynchronous control circuits are usually relatively cheap but liable to produce radio frequency interference. The circuit of Fig. 5.3 is typical.

5.3.3 Synchronous Control

A step change in current, caused by the closing of any switch (mechanical or semiconductor), can give rise to radio frequency interference. However, if the switch is closed at the moment the supply voltage passes through zero there is no step rise in current and thus no radio frequency interference. Control systems where the switching is synchronised with zero passages of the supply voltage are known as synchronous control systems. They have the further advantage that, as the thyristors conduct over complete half cycles, the power factor is very good.

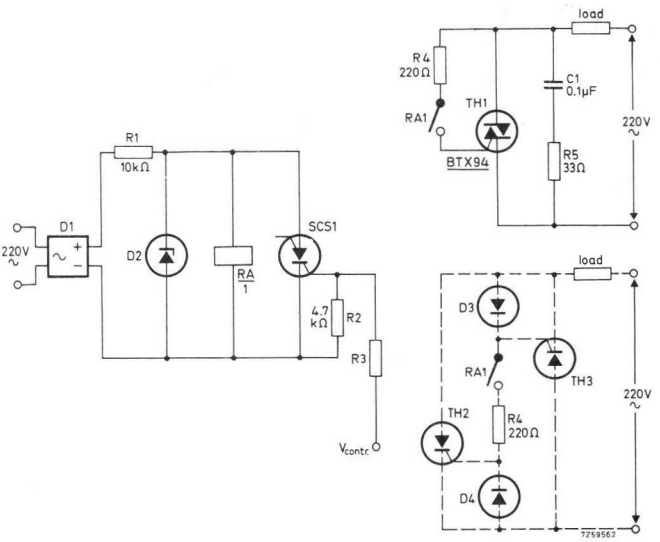


Fig. 5.5. Trigger circuit for triac switching using a reed relay. Alternative load control section employing thyristors in anti-parallel is shown dotted. All resistors 5%, 0.25 W.

The circuit shown in Fig. 5.5 is typical and can be used with inductive loads. When V_{contr} rises to a certain level, SCS_1 turns on and effectively shorts $RA/1$ – thus de-energising it. Contact RA_1 is opened and gate drive removed from the thyristors (or triac). While V_{contr} is below the level required for triggering of SCS_1, $RA/1$ is energised, RA_1 is made and gate drive is supplied to the thyristors (or triac) which supply power to the load.

Fig. 5.6 shows another typical synchronous control circuit (waveforms see Fig. 5.7). When SCS_1 is off the PA 60 oscillates, feeding pulses via the transformer to trigger the thyristors. If V_{contr} is increased sufficiently to turn SCS_1 on, the voltage across the PA 60 is reduced to about one volt and oscillation ceases – thus no trigger pulses are fed to the thyristors. Synchronised switching occurs because, although V_{contr} may be removed during a half-cycle, the SCS does not cease conduction until the end of the half-cycle; so trigger pulses are not applied to the

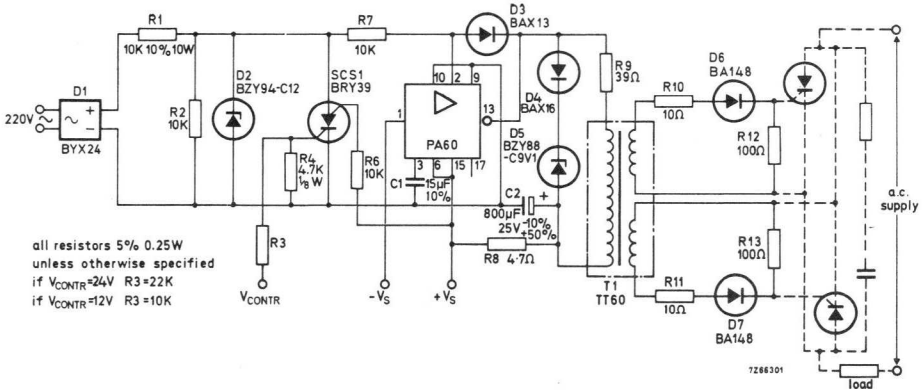


Fig. 5.6. Thyristor pulse triggering circuit with PA60 power amplifier. All resistors 5%, 0.25 W unless otherwise specified.

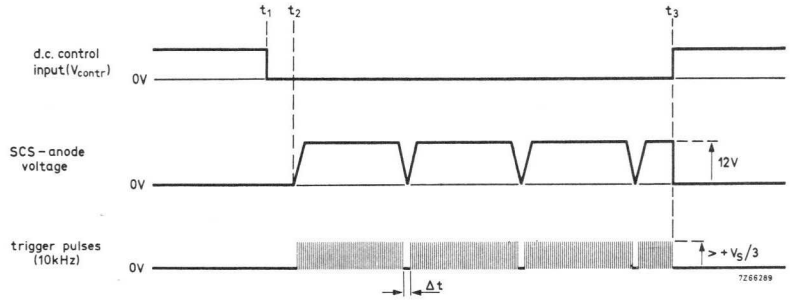
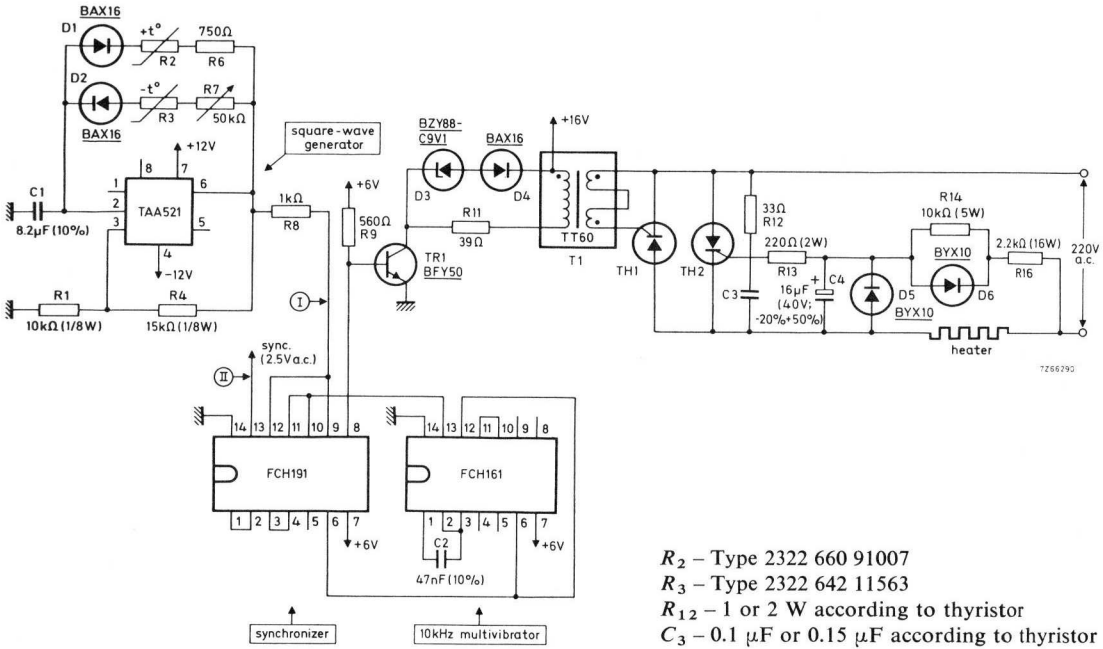


Fig. 5.7. Voltage waveforms of the circuit of Fig. 5.6 (forward on-state voltage of SCS assumed zero).

thyristors until the supply voltage passes zero. Similarly, although the SCS may be turned on during a half-cycle, the thyristors will continue to conduct until the supply voltage passes zero at the end of the half-cycle.

5.3.4 Time Ratio Control

More demanding applications often require the use of a continuously variable duty cycle of energy delivery – thus any change in the controlled variable is counteracted immediately. Such systems are known as time ratio control systems. A typical circuit is shown in Fig. 5.8.



R_2 – Type 2322 660 91007
R_3 – Type 2322 642 11563
R_{12} – 1 or 2 W according to thyristor
C_3 – 0.1 μF or 0.15 μF according to thyristor

Fig. 5.8. Time ratio control circuit using TAA 521 operational amplifier as square-wave generator. Temperature is set with R_7. All resistors 10%, 0.25 W unless otherwise specified.

Operational amplifier TAA521 and the immediately associated circuitry form a square-wave generator, the duty-cycle of which is varied by changes in the resistance of the sensors (the thermistors R_2 and R_3). The synchroniser (using an input synchronised with the mains supply–input II on terminal 13) ensures that the 10 kHz trigger pulses start to be fed to TH_1, whilst TH_1 is in anode reverse bias conditions, so that TH_1 can start to conduct as soon as its anode voltage goes positive. TH_2 is slave-triggered, i.e. the associated circuitry ensures that TH_2 will only trigger in half-cycles immediately following half-cycles in which TH_1 has conducted. The synchroniser will only pass trigger pulses while the output from the TAA 521 is positive – so the thyristors only conduct during this period. Waveforms showing the overall operation of the circuit are given in Fig. 5.9.

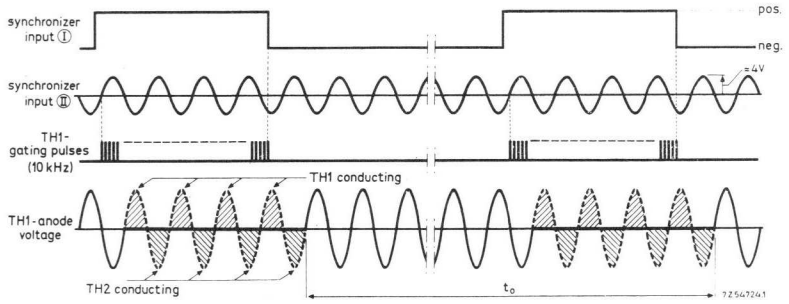


Fig. 5.9. Time ratio control waveforms.

5.4 Phase Control

5.4.1 Controlled Rectification

The a.c./d.c. converter using thyristors, which is often referred to as a controlled rectifier, can take a number of different forms. One of the most widely used configurations is the half-controlled bridge which can be used on both single-phase and three-phase supplies. In a half-controlled bridge, the thyristors can be connected in either arm of the bridge and, in practice, the construction of the stack (thyristors, diodes and associated heat-sinks) influences the thyristor connections.

It is often convenient to supply direct current to highly-inductive loads, such as motor field supplies or magnetic clutches, from the a.c. mains. It is essential that the thyristor current is commutated at the end of each half-cycle; this is usually ensured by use of a separate flywheel diode, or by flywheel-diode action within the bridge.

For certain applications, it is necessary to regenerate power from the load back into the supply. This power is usually in the form of inductive or mechanical energy, and in both these cases fully-controlled bridges are used. A further advantage of the three-phase fully-controlled bridge is that the output ripple frequency is six times the supply frequency.

Single-phase Half-controlled Bridge

The circuit of a single-phase half-controlled bridge is shown in Fig. 5.10.

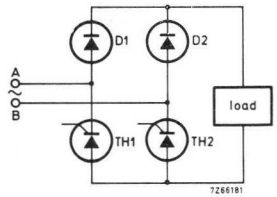


Fig. 5.10. Single-phase half-controlled bridge.

This configuration is the most commonly used arrangement for the control of d.c. power, and the mode of operation with a resistive load is the simplest for all the a.c./d.c. converters. The wave-forms of the load voltage and current in relation to the supply voltage with a resistive load are shown in Fig. 5.11.

When the voltage at A is positive with respect to B (that is, V_{AB} is positive), and when thyristor TH_2 is triggered, the load current flows through TH_2 and diode D_1. Thyristor TH_2 is turned off when the voltage V_{AB} is negative. During the next half-cycle when B is positive with respect to A, thyristor TH_1 and diode D_2 conduct the load current.

In practice, the controlled arms of the bridge can be connected in two configurations, as shown in Fig. 5.12. For resistive loads, both these configurations operate in the same manner. For complex loads, however, a parallel path is available for the current generated by the load inductance during the off periods of the thyristors (but see following material on

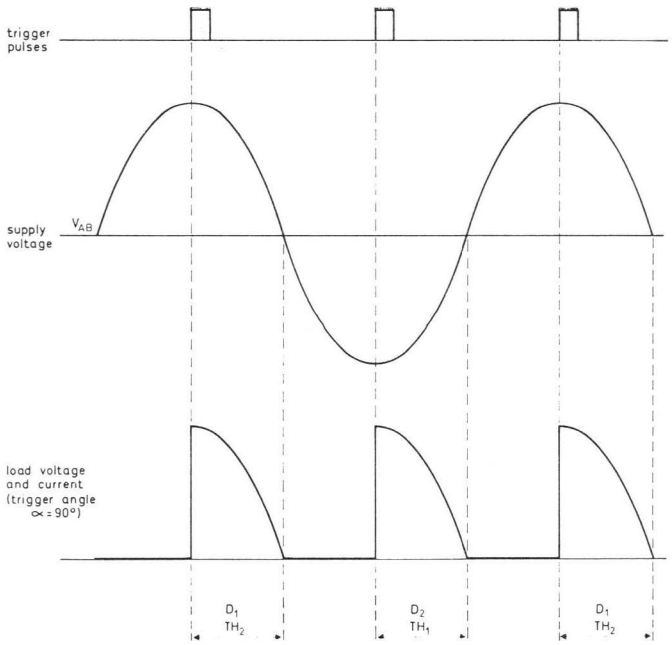


Fig. 5.11. Waveforms for single-phase half-controlled bridge with resistive load.

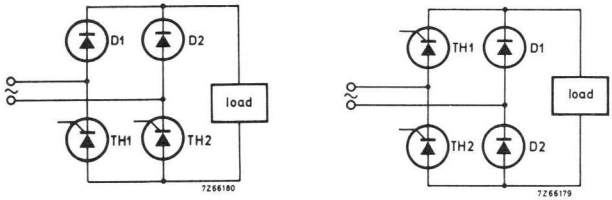


Fig. 5.12. Possible configurations of single-phase half-controlled bridge.
(a) thyristors in parallel arms,
(b) thyristors in series arms.

flywheel diodes). The operation of the bridge with a complex load will be considered for the configuration where the thyristors are in parallel arms of the bridge (Fig. 5.12a).

The waveforms of load voltage and current in relation to the supply voltage with a complex load are shown in Fig. 5.13. At the end of each half-cycle of the supply voltage, current flow is maintained in the load circuit by the inductance of the load. The thyristor which has been conducting, say TH_2, continues to conduct, but current transfers from diode

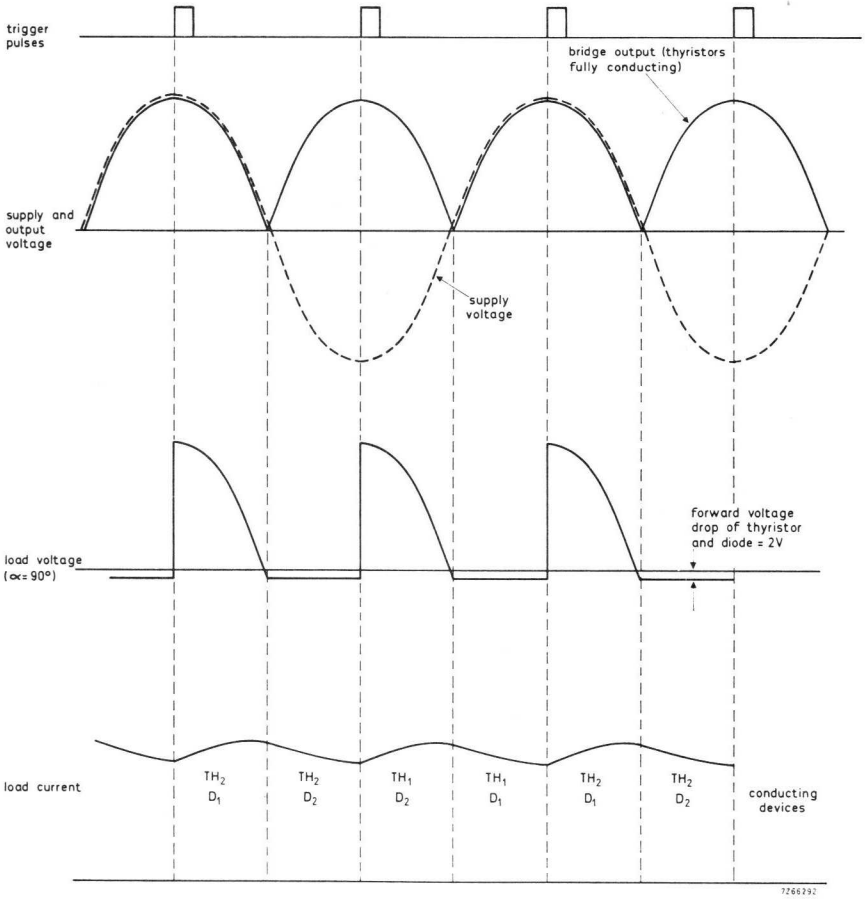


Fig. 5.13. Waveforms for single-phase half-controlled bridge with complex load.

D_1 to D_2 so that the load inductive back e.m.f. drives current through the bridge without including the reverse supply voltage. During this part of the cycle, the load current decays exponentially, and is unaffected by the supply voltage. When the other thyristor TH_1 is triggered, thyristor TH_2 is reverse biased by the supply voltage and turns off. Current now flows from the supply through diode D_2 and thyristor TH_1 into the load. Thyristor TH_2 is triggered in the next half-cycle, and the sequence repeated.

The load current can be controlled by alteration of the trigger angles of the thyristors, and in most respects the circuit operates satisfactorily. There is, however, one limitation with this circuit; it may not be possible to turn off the load current simply by not triggering the thyristors.

If the trigger pulses are removed immediately after one thyristor has been triggered, this thyristor will continue to conduct as usual for the rest of the half-cycle of the supply. The other thyristor will not receive trigger pulses, and so will not turn on. However, if the load is highly inductive, with a time-constant much greater than one half-cycle of the supply, the first thyristor will still be conducting at the end of this period, and will remain turned on for the following forward half-cycle. The circuit will continue to operate in this way indefinitely, with one thyristor conducting on complete alternate half-cycles and acting as a flywheel diode during the other half-cycles, until the mains supply is interrupted. In other words, the trigger circuit will have lost control of the load current.

This limitation can be overcome by arranging never to remove the trigger pulses completely, but to leave an "end stop" pulse at about 170° in each half-cycle to ensure that each thyristor is always commutated at the end of the half-cycle.

An expression for the mean output voltage of the bridge with resistive, complex, and purely inductive loads can be derived in terms of the supply voltage, in a way similar to that for the a.c./d.c. converters, and is

$$V_{o(AV)}(\alpha) = \frac{\sqrt{2} \cdot V_s}{\pi}(1 + \cos \alpha).$$

Single-phase Half-controlled Bridge with Flywheel Diode

If a flywheel diode is added to the half-controlled bridge, as shown in Fig. 5.14, the load current is transferred to the flywheel diode at the end

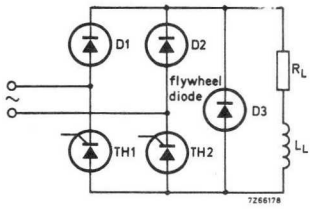


Fig. 5.14. Single-phase half-controlled bridge with flywheel diode.

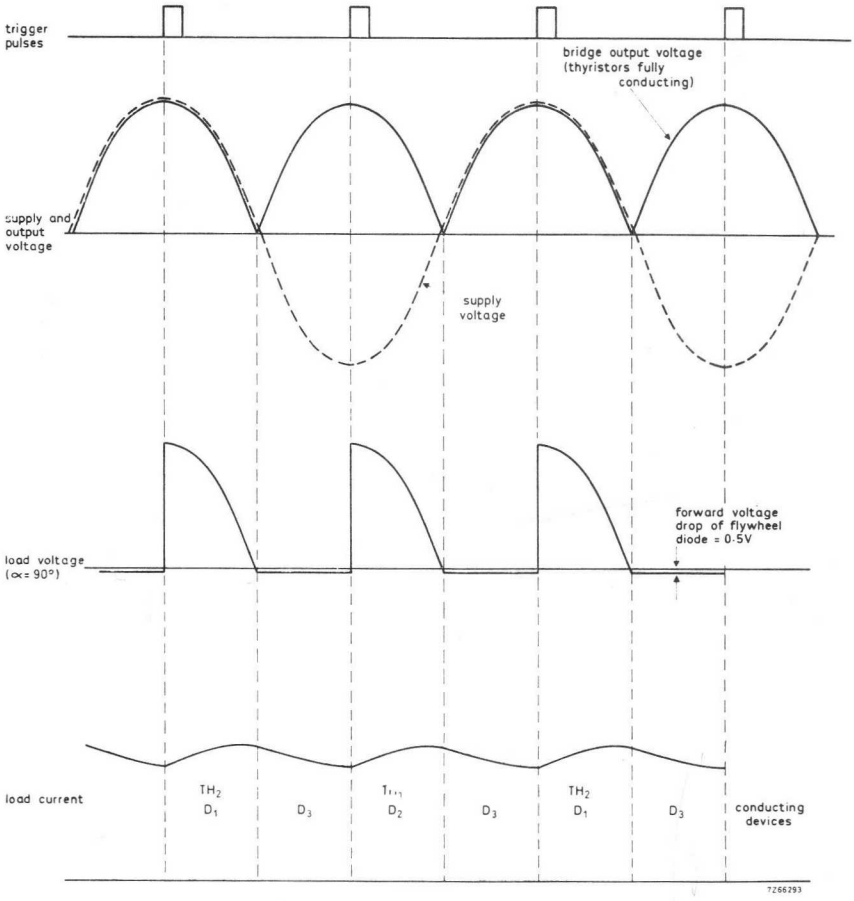


Fig. 5.15. Waveforms for single-phase half-controlled bridge with flywheel diode for complex load.

of each half-cycle of the supply. The load current waveforms for a complex load, shown in Fig. 5.15, are similar to those of the half-controlled bridge without a flywheel diode, but the exponential decay part of the load current is carried by the flywheel diode in this case. The addition of the flywheel diode ensures that each thyristor turns off at the end of each half-cycle, so that there is no risk of conduction carrying over into the next half-cycle. Load current, therefore, is always under the control of the trigger circuit, and there is no need to provide "end stop" pulses.

Circuit efficiency and component utilisation are improved, as only the current drawn from the supply flows through the bridge thyristors and diodes. The load recirculating current is returned through the flywheel diode only, which has a much lower forward voltage drop than the series combination of the thyristors and diodes in the bridge. Total circuit losses during the part of the cycle when the load current recirculates are therefore reduced to less than a third.

If the thyristors are triggered at the start of each half-cycle, no flywheel diode current flows, and the bridge must be rated to deliver the full load current. However, if the bridge is never to be run at maximum current except, perhaps, to establish the current initially, some reduction in the current ratings of the bridge thyristors and diodes is possible. For example, the maximum output voltage required may be only 100 V from a 230 V (205 V mean) supply. In this case, the load current will be almost half that possible with the bridge fully conducting, and only half this load current will flow through the bridge, the remainder being recirculated through the flywheel diode. By designing the bridge and flywheel diode stack for a particular application, a designer can often reduce component costs considerably by taking these current distribution factors into account. Generally, however, the forward current rating of the flywheel diode can be assumed to be 75% of the nominal output current of the bridge.

The expression for the mean output voltage of the half-controlled bridge with flywheel diode is:

$$V_{o(AV)}(\alpha) = \frac{\sqrt{2}\, V_s}{\pi}(1 + \cos \alpha)$$

as in the previous case where no flywheel diode was used.

Single-phase Fully Controlled Bridge

Fig. 5.16 shows a single-phase fully controlled bridge; no flywheel diode is used. The expression for $V_{o(AV)}(\alpha)$ for the various types of load is:

resistive . . . . . $\frac{\sqrt{2} \cdot V_s}{\pi}(1 + \cos \alpha)$

complex ($\alpha > \phi$) . . . . . $\frac{2\sqrt{2} \cdot V_s}{\pi} \sin \frac{\theta}{2} \cdot \sin\left(\alpha + \frac{\theta}{2}\right)$

(discontinuous load current)

complex ($\alpha < \phi$) . . . . . $\frac{2\sqrt{2} \cdot V_s}{\pi} \cos \alpha$

(continuous load current)

purely inductive . . . . . $\frac{2\sqrt{2} \cdot V_s}{\pi} \cos \alpha.$

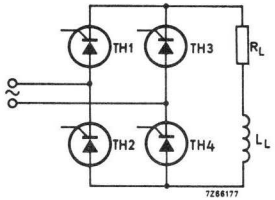


Fig. 5.16. Single-phase fully-controlled bridge.

Waveforms for the complex load case are given in Fig. 5.17. During forward conduction, voltage and current waveforms are similar to those of the half-controlled bridge. However, during the reverse half-cycle, the load current cannot recirculate through a flywheel diode or bridge diode but must continue to flow through the same thyristors and the supply impedance. Load current is therefore forced by the reverse supply voltage to decay more rapidly between forward conduction periods than would be the case in a half-controlled bridge.

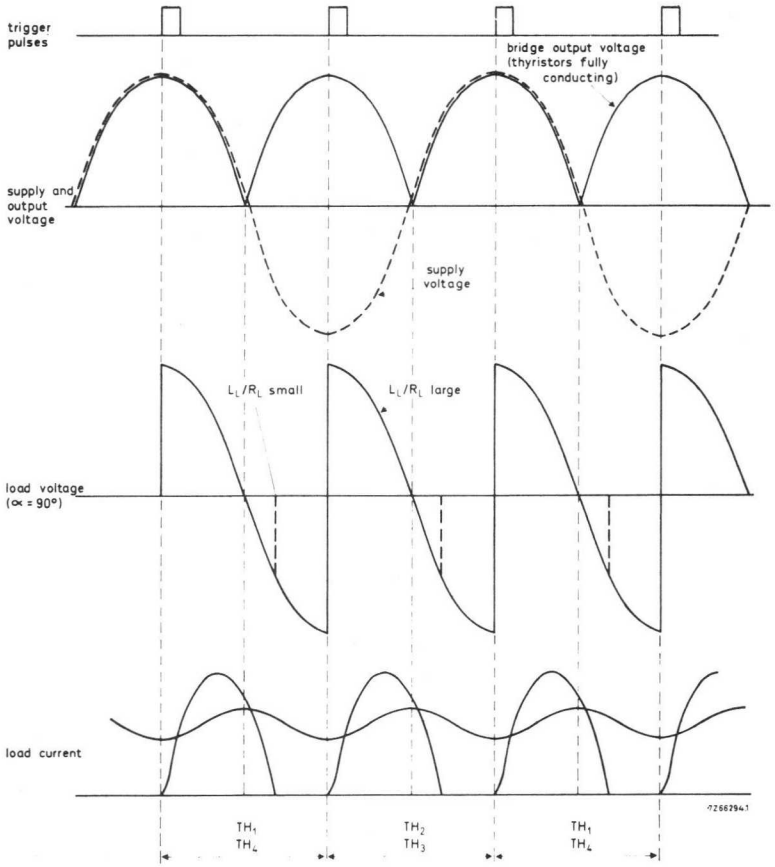


Fig. 5.17. Waveforms for single-phase fully-controlled bridge with complex load of short time-constant (broken lines) and long time-constant (full lines).

Three-phase Half-controlled Bridge

Fig. 5.18 shows a typical three-phase half-controlled bridge with a resistive load; the waveforms are given in Fig. 5.19. We shall assume a control range of 180° for the trigger pulses; thus, for convenience, the waveforms in Fig. 5.19 are divided into two groups – high trigger angle (therefore low conduction angle and low power) on the left and low trigger angle on the right.

For simplicity, we shall consider only the waveforms associated with the red-phase thyristor TH_R and the red-phase diode D_R. At high trigger angles, if TH_R is triggered at α_1, TH_R can only conduct into the blue phase because the yellow phase is more positive than TH_R anode. The

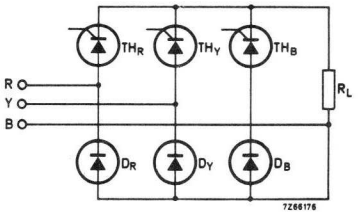


Fig. 5.18. Three-phase half-controlled bridge.

thyristor will conduct until the blue phase voltage becomes more positive than the red phase voltage. At low trigger angles TH_R is triggered at α_2 and conducts into the yellow phase. At point x in Fig. 5.19 (b), the blue phase voltage becomes more negative than the yellow and the current in TH_R then commutates from the yellow-phase diode D_Y to the blue-phase diode D_B. At point y, TH_Y is triggered and conducts into the blue-phase – thus commutating the current in TH_R.

At full power output, each thyristor conducts for 120°; however, a trigger-angle range of 180° is needed to achieve this. The total length of each block represents the required range of trigger pulse – the unshaded part is the trigger angle and the shaded part is the conduction angle.

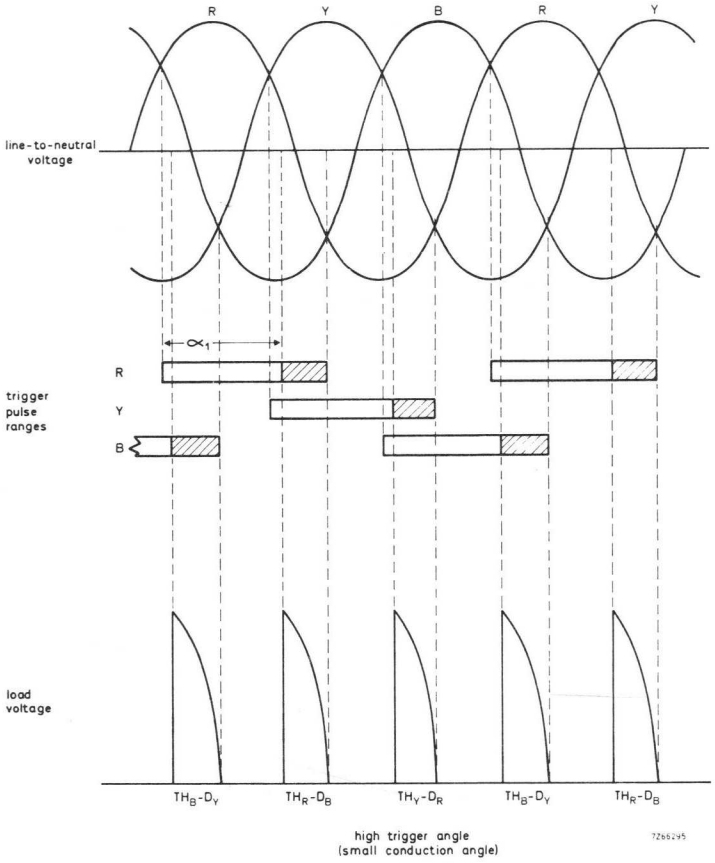


Fig. 5.19. Waveforms for three-phase half-controlled bridge with resistive load (the total length of a trigger pulse block represents the required trigger angle pulse range – the unshaded portion is the trigger angle and the shaded portion is the conduction angle).
(a) Small conduction angle

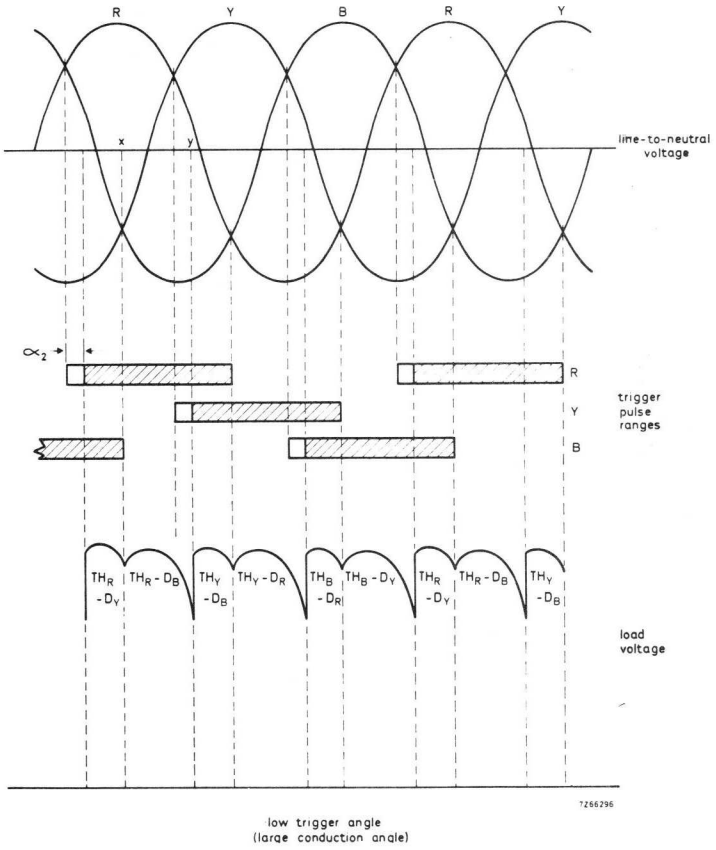


Fig. 5.19 (b). As Fig. 5.19 (a), for a large conduction angle.

5.4.2 AC Control

Two typical single-phase a.c./a.c. converters are shown in Fig. 5.20. That shown in Fig. 5.20(a) is simpler and needs individual gate signals.

The circuit in Fig. 5.20(b) uses one thyristor for both the positive and negative half-cycles of the supply waveform, and so ensures the optimum utilisation of the thyristor current capacity (reduced form factor). However, the reduction in efficiency caused by the sum of the voltage drops across the diodes and thyristor may be a drawback in certain low-voltage applications. Thyristor turn-off is sometimes a problem because the anode voltage never drops below zero, and for this reason the circuit is used only where circuit values and thyristor turn-off times are accurately known. Also, since the thyristor must carry all the current, the manageable power level will be lower for a given thyristor type in this circuit than in the other circuit.

In both these circuits, it is desirable that the thyristor working-voltage rating should be at least equal to the crest value of the supply voltage. In practice, values of twice this figure are used to prevent transients causing the thyristor to conduct by means of forward breakover.

Single-phase Thyristor AC/AC Converter with Resistive Load

The behaviour of the a.c./a.c. converter with a resistive load is the simplest to analyse. Waveforms for an inverse-parallel thyristor configuration with a resistive load are shown in Fig. 5.21. Thyristor TH_1 is triggered at angle α, and applies the instantaneous supply voltage to the load. It will conduct for the remainder of the positive half-cycle, turning off when the anode voltage becomes zero at 180°. Thyristor TH_2 is triggered at angle $(180 + \alpha)°$, and conducts for a time equal to that of TH_1, turning off when its anode voltage becomes zero at 360°. Thyristor TH_1 is triggered again at $(360 + \alpha)°$, and the sequence repeated. Current pulses, alternating in polarity and forming part of a sinewave, are fed to the load. The duration of each pulse is the conduction angle γ, that is $(180 - \alpha)°$, and the output power can therefore be controlled by variation of the trigger angle α.

As the thyristors are connected in the inverse-parallel configuration the forward voltage across one thyristor forms the reverse voltage for the other, as can be seen from the voltage waveforms in Fig. 5.21.

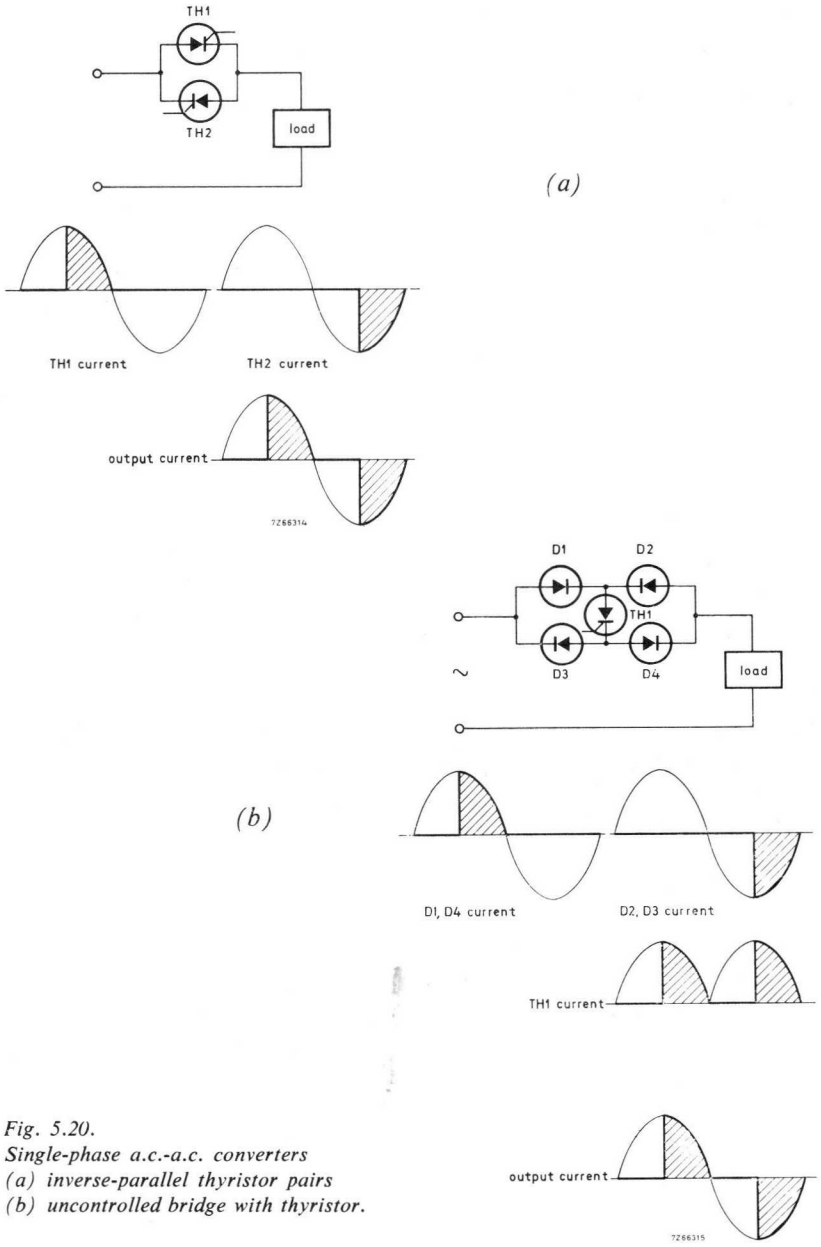


Fig. 5.20.
Single-phase a.c.-a.c. converters
(a) inverse-parallel thyristor pairs
(b) uncontrolled bridge with thyristor.

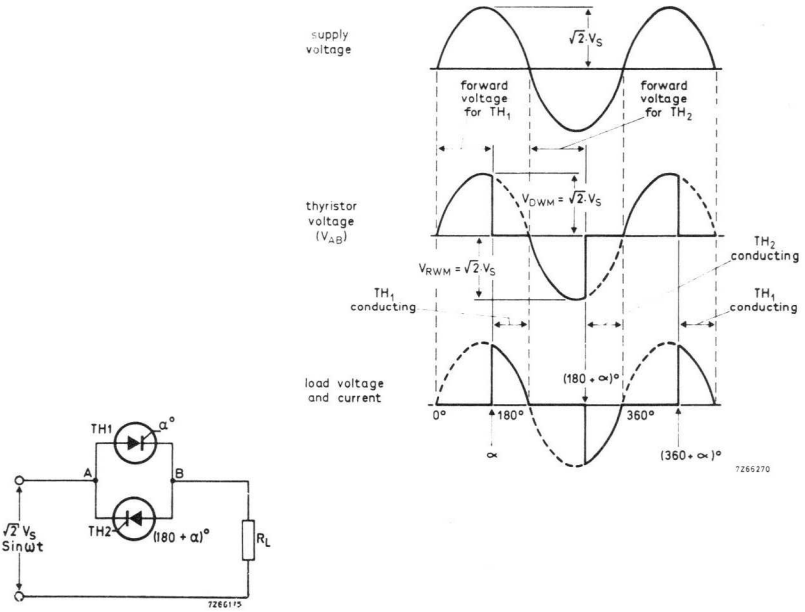


Fig. 5.21. Waveforms for inverse-parallel configuration with resistive load.

The various values of thyristor current and their relationships can be calculated in terms of the supply voltage. These expressions are listed in Table 5.1, together with the output voltage and power as a function of trigger angle. Curves of these expressions are plotted in the universal analysis charts of Fig. 5.22.

Because of the generation of harmonics in the a.c. load, the power factor presented to the a.c. supply will be lower than unity except when the trigger angle is zero, when ideally a purely sinusoidal current flows. The power factor presented to the supply $F_{p(in)}(\alpha)$ is the ratio of active input power (assumed equal to the active output power) to the apparent input power. Active output power (no reactive components) is the r.m.s. output power, which is listed in Table 5.1.

Apparent input power is:

$$P_{in(app)}(\alpha) = V_s I_s,$$

and I_s is obtained by dividing $V_{o(r.m.s.)}(\alpha)$, listed in Table 5.1, by R_L.

Table 5.1. Thyristor Currents, Form Factors and Output for Inverse-parallel and Back-to-Back Configurations with Resistive Load

quantity	symbol	expression
thyristor mean current at trigger angle α	$I_{T(AV)}(\alpha)$	$\dfrac{V_s}{\sqrt{2}\,.\,\pi R_L}(1+\cos\alpha)$
max. value of mean current (at $\alpha = 0$)	$I_{T(AV)}\text{max}$	$\dfrac{\sqrt{2}\,.\,V_s}{\pi R_L}$
mean current referred to maximum value	$\dfrac{I_{T(AV)}(\alpha)}{I_{T(AV)}\text{max}}$	$\dfrac{1+\cos\alpha}{2}$
thyristor r.m.s. current at trigger angle α	$I_{T(r.m.s.)}(\alpha)$	$\dfrac{V_s}{\sqrt{2}\,.\,R_L}\left[\dfrac{(\pi-\alpha+\frac{1}{2}\sin 2\alpha)}{\pi}\right]^{1/2}$
r.m.s. current referred to maximum value	$\dfrac{I_{T(r.m.s.)}(\alpha)}{I_{T(r.m.s.)}\text{max}}$	$\left[\dfrac{(\pi-\alpha+\frac{1}{2}\sin 2\alpha)}{\pi}\right]^{1/2}$
thyristor current form factor (r.m.s. to mean)	$F_{T(f)}(\alpha)$	$\dfrac{1}{1+\cos\alpha}\left[\pi(\pi-\alpha+\frac{1}{2}\sin 2\alpha)\right]^{1/2}$
thyristor current peak-to-mean factor	$F_{T(M/AV)}(\alpha)$	$\dfrac{2\pi}{1+\cos\alpha}$ $\quad 0\leqslant\alpha\leqslant\dfrac{\pi}{2}$ $\dfrac{2\pi\sin\alpha}{1+\cos\alpha}$ $\quad \dfrac{\pi}{2}\leqslant\alpha\leqslant\pi$
thyristor current peak-to-r.m.s. factor	$F_{T(M/r.s.m.)}(\alpha)$	$\left[\dfrac{4\pi}{\pi-\alpha+\frac{1}{2}\sin 2\alpha}\right]^{1/2}$ $\quad 0\leqslant\alpha\leqslant\dfrac{\pi}{2}$ $\sin\alpha\left[\dfrac{4\pi}{\pi-\alpha+\frac{1}{2}\sin 2\alpha}\right]^{1/2}$ $\quad \dfrac{\pi}{2}\leqslant\alpha\leqslant\pi$
r.m.s. output voltage	$V_{o(r.m.s.)}(\alpha)$	$V_s\left[\dfrac{\pi-\alpha+\frac{1}{2}\sin 2\alpha}{\pi}\right]^{1/2}$
r.m.s. output current	$I_{o(r.m.s.)}(\alpha)$	$\dfrac{V_s}{R_L}\left[\dfrac{\pi-\alpha+\frac{1}{2}\sin 2\alpha}{\pi}\right]^{1/2}$
r.m.s. output power	$P_{o(r.m.s.)}(\alpha)$	$\dfrac{V_s^2}{\pi R_L}(\pi-\alpha+\frac{1}{2}\sin 2\alpha)$

These expressions are plotted as the curves in Fig. 5.22.

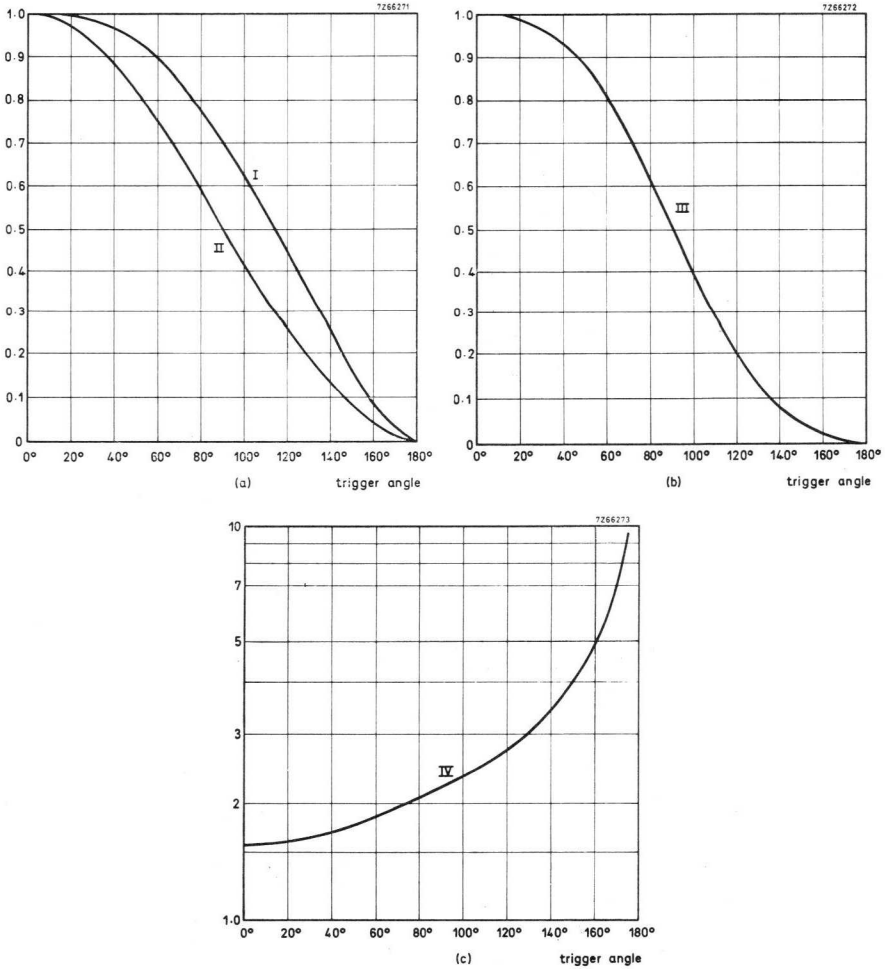
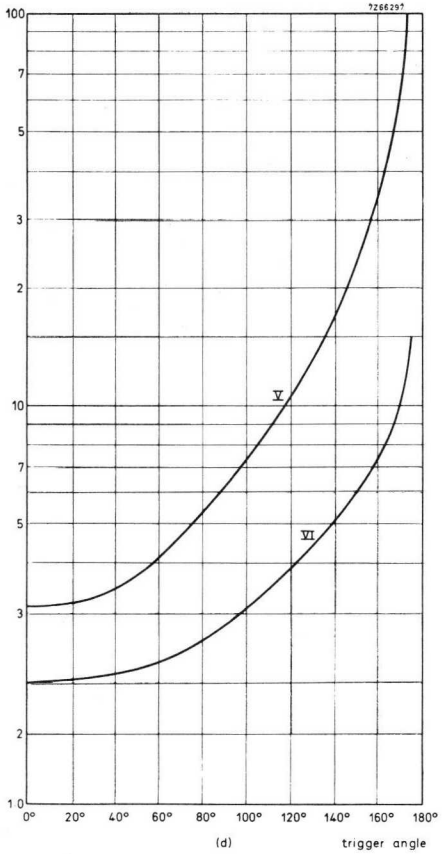


Fig. 5.22. Universal analysis charts for inverse-parallel and back-to-back configurations with resistive load (see also opposite page).

$$\text{Curve I} = \left[\frac{\pi - \alpha + \tfrac{1}{2}\sin 2\alpha}{\pi}\right]^{\frac{1}{2}} \qquad \text{Curve II} = \frac{1 + \cos\alpha}{2}$$

$$\text{Curve III} = \frac{\pi - \alpha + \tfrac{1}{2}\sin 2\alpha}{\pi} \qquad \text{Curve IV} = \frac{1}{1 + \cos\alpha}\left[\pi(\pi - \alpha + \tfrac{1}{2}\sin 2\alpha)\right]^{\frac{1}{2}}$$



$$\text{Curve V} = \frac{2\pi}{1 + \cos \alpha} \quad 0 \leqslant \alpha \leqslant \pi/2$$

$$= \frac{2\pi \sin \alpha}{1 + \cos \alpha} \quad \pi/2 \leqslant \alpha \leqslant \pi$$

$$\text{Curve VI} = \left[\frac{4\pi}{\pi - \alpha + \frac{1}{2} \sin 2\alpha}\right]^{\frac{1}{2}} \quad 0 \leqslant \alpha \leqslant \pi/2,$$

$$= \sin \alpha \left[\frac{4\pi}{\pi - \alpha + \frac{1}{2} \sin 2\alpha}\right]^{\frac{1}{2}} \quad \pi/2 \leqslant \alpha \leqslant \pi$$

Thus:

$$F_{p(in)}(\alpha) = \frac{P_{o(r.m.s.)}(\alpha)}{P_{in(app)}(\alpha)} = \left[\frac{\pi - \alpha + \frac{1}{2}\sin 2\alpha}{\pi}\right]^{1/2}.$$

This expression is also plotted in Fig. 5.22.

The expressions do not apply to the uncontrolled bridge configuration of Fig. 5.20(b), but new expressions will not be given as this configuration is not generally used in practice.

Single-phase Triac A.C./A.C. Converter with Motor Load

For the control of power to low-inductance loads (heating elements, lamps and squirrel-cage fan motors), a triac can be used; Fig. 5.23 shows a triac used in conjunction with a silicon controlled switch.

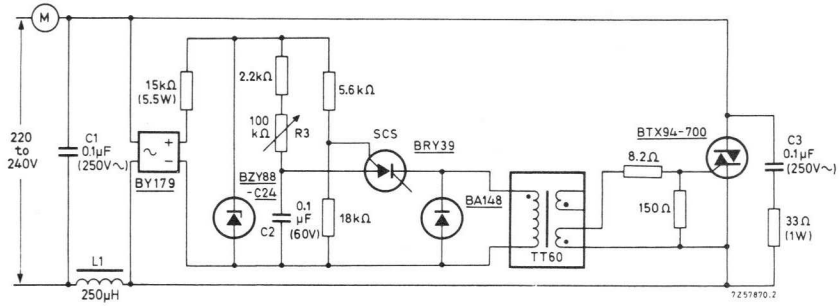


Fig. 5.23. AC fan motor control circuit. (All resistors 1/4 W unless otherwise shown. C_1 and C_3 are Cat.No. 2222 276 00009 capacitors.)

The mains is rectified, clipped by a zener diode, and fed to a resistive voltage divider which provides a reference and synchronising voltage for the anode gate of the SCS. Additionally, the zener stabilised voltage is fed to the RC timing circuit – giving further stability. At the end of a half-cycle, C_2 discharges – ensuring that initial charge on C_2 is always zero at the start of a half-cycle and thus eliminating hysteresis.

When the voltage across C_2 exceeds the anode gate voltage, the SCS conducts and feeds a current pulse via the transformer to the triac gate.

The triac then conducts for the remainder of the half-cycle. Rate of rise of capacitor voltage, and thus the point of turn-on of the triac, may be varied by means of the variable resistor.

Choke L_1 and Capacitor C_1 limit the steepness of current transients and help to suppress RFI. The RC network across the triac protects it against voltage transients.

5.5 Choppers and Inverters

5.5.1 Choppers

A chopper is a switch between a d.c. source and a load. Average load voltage is controlled by variation of the duty cycle of the chopper.

We shall consider the thyristor chopper in its most basic form first – a single thyristor chopper. Fig. 5.24 shows the circuit and waveforms.

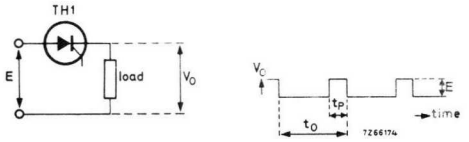


Fig. 5.24. (a) Basic chopper (b) output waveform.

Clearly, while the thyristor is conducting, the output voltage is equal to the supply voltage and during the intervening periods the output voltage is zero. Thus

$$V_{o(AV)} = t_p/t_o\, E,$$

where t_p is the conduction period
t_o is the repetition period
E is the supply voltage
and $V_{o(AV)}$ is the average output voltage.

Switching of the thyristor can be effected by three methods – oscillating the load, providing an auxiliary thyristor, and varying the frequency of the trigger pulses.

A two-thyristor chopper and the relevant waveforms are shown in Fig. 5.25. This circuit uses forced commutation – TH_1 is the load-current carrying thyristor and TH_2 is the auxiliary thyristor which turns TH_1 off by current reversal. Output is varied by variation of the instant t_4 at which TH_1 is made to conduct.

Before t_1, TH_1 is conducting and C_1 is charged to the supply voltage (lower plate positive). Period t_1 to t_3 is a commutation period; at t_1, TH_2 is triggered and allows C_1 to force reverse current through TH_1 – turning it off. Also at t_1, because TH_2 is triggered, the voltage on the lower plate of the capacitor is fed straight to the output – effectively doubling the output voltage for an instant, but C_1 immediately starts to discharge and recharge in the opposite direction (over t_1 to t_3).

At t_3, TH_2 turns off and the voltage across C_1 remains constant at a value equal to the supply voltage. Chopper output is zero so load inductance L_2 forces free-wheeling diode D_2 into conduction to maintain the load current.

At t_4 the voltage across C_1 is resonantly reversed by turn-on of TH_1; diode D_1 prevents discharge of C_1. The circuit then waits for retriggering of TH_2 which starts the next cycle.

Fig. 5.26 shows a forced-commutation three-thyristor chopper and the associated waveforms. Commutation is provided by the additional thyristor and thus is not influenced by load conditions. TH_1 passes current to the load, TH_2 commutates the voltage on C_1 and TH_3 turns TH_1 off. As any thyristor can be triggered first, the circuit starts reliably.

Before t_1, TH_1 is conducting. At t_1, TH_2 is triggered and the voltage on C_1 reverses resonantly (t_1 to t_2 is half a resonant period). At t_2 TH_2 turns off by self commutation; because TH_3 is not yet triggered, C_1 starts to discharge through R_1 so v_p decreases exponentially.

At t_3, TH_3 is triggered and TH_1 is turned off by the voltage on C_1. Load current, I_o, is transferred from TH_1 to TH_3 so C_1 discharges linearly.

Between t_4 and t_5, a steady-state condition exists because C_1 cannot discharge further. At t_4, TH_3 turns off for lack of forward current; it is not subjected to reverse voltage until TH_1 is again triggered at t_5. TH_1 continues to conduct, feeding the supply voltage to the load, until TH_3 is again triggered.

As conduction of TH_1 is not necessary for commutation, the chopper will continue to function even if this thyristor is not triggered. While the load is connected, the commutation capacitor loses part of its charge

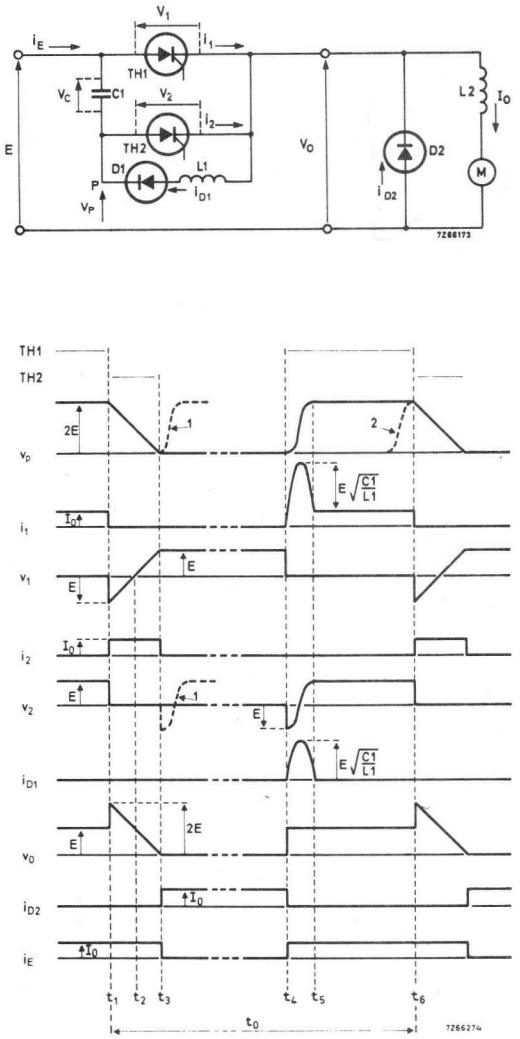


Fig. 5.25. (a) Forced-commutation two-thyristor chopper (b) waveforms.
I_o assumed pure d.c.: $v_c = E - v_p$: Thyristor conduction periods shown by solid horizontal lines above waveforms.
1 = waveform for earliest TH_1 triggering,
2 = waveform for latest TH_1 triggering,
t_o = chopper repetition period.

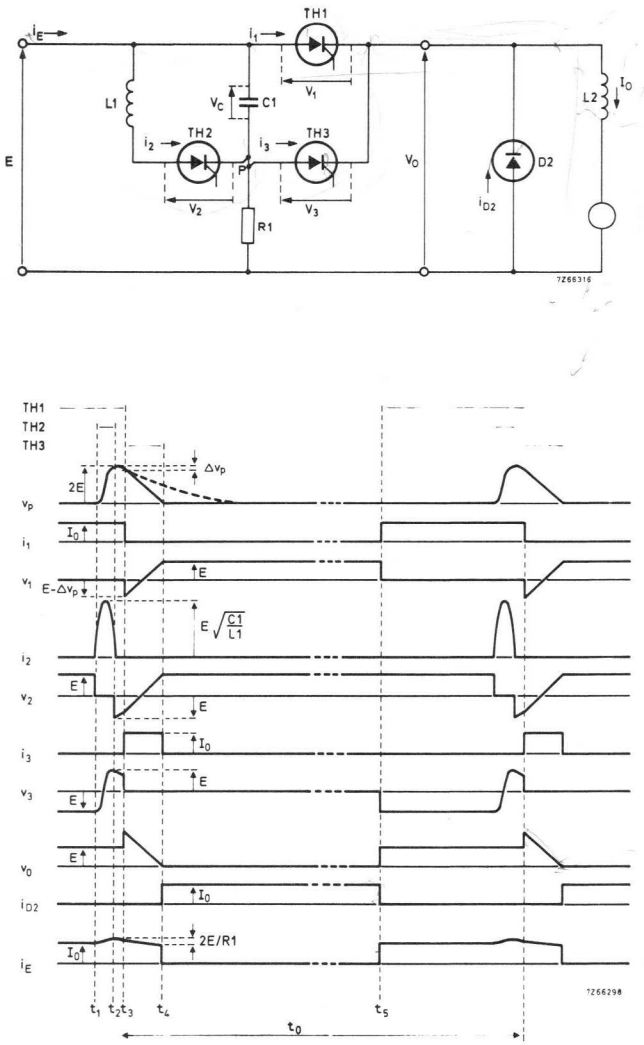


Fig. 5.26. (a) Forced-commutation three-thyristor chopper (b) waveforms.
$v_c = E - v_p$,
t_o = *chopper repetition period.*

through TH_3 so a residual output voltage exists. Apart from transients, thyristor voltages do not exceed the supply voltage.

In Chapter 3, descriptions are given of the Morgan (saturated core) and Jones choppers; also described there is a simple series-commutated chopper.

5.5.2 Inverter (DC-AC)

Fig. 5.27 shows a basic parallel inverter and the trigger pulses. When thyristor A is triggered, current flows from the positive supply through the left-hand half of the transformer primary. By auto-transformation, the right-hand half of the transformer primary develops a similar voltage

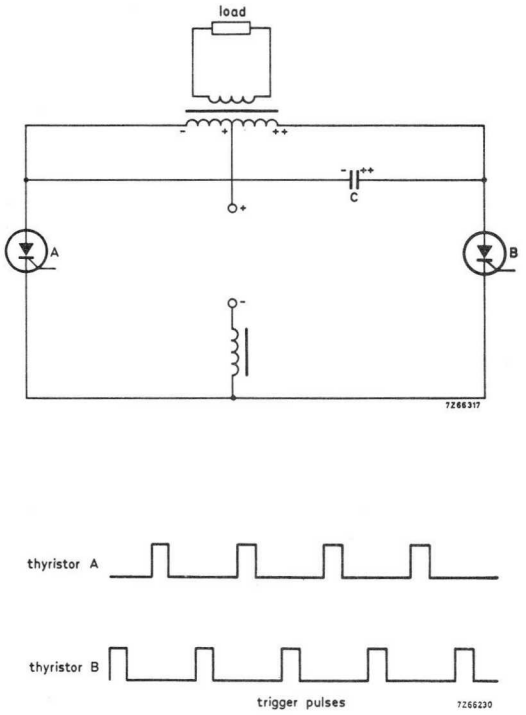


Fig. 5.27. Basic parallel inverter.

to the left-hand half (in series as shown in Fig. 5.27) so the capacitor becomes charged to twice the supply voltage. When thyristor *B* is triggered, the voltage across the capacitor opposes current flow through thyristor *A* – turning it off; also the polarities on the transformer primary are reversed. When thyristor *A* is triggered again the cycle repeats. If each trigger pulse to *A* is arranged to occur halfway between two trigger pulses to *B*, as shown in Fig. 5.27, a good symmetrical output is obtained.

In this basic circuit, load changes can effect commutation. Considerable improvement with inductive loads is gained if freewheeling diodes are connected as shown in Fig. 5.28 (this also improves voltage regulation); further improvement is gained if diodes are connected in series with the primary to prevent ringing by disconnecting the load from the commutating energy (again, in the manner shown in Fig. 5.28).

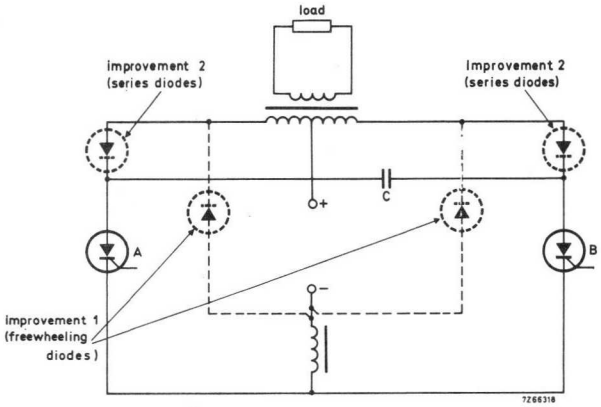


Fig. 5.28. Improvements to parallel inverter.

A series inverter and waveforms are shown in Fig. 5.29. When thyristor *A* is triggered, an oscillation current flows through *L* and the load transformer to charge *C*; this continues until the voltage across *C* is great enough to turn thyristor *A* off. Shortly after this, thyristor *B* is triggered and *C* discharges oscillatory through the load transformer, *L* and thyristor *B*, until this oscillation current reserves, turning off thyristor *B*. Then the cycle repeats.

Commutation is load-dependent because the load impedance is reflected into the path of the charge and discharge current of *C*; however this is usual with series inverters.

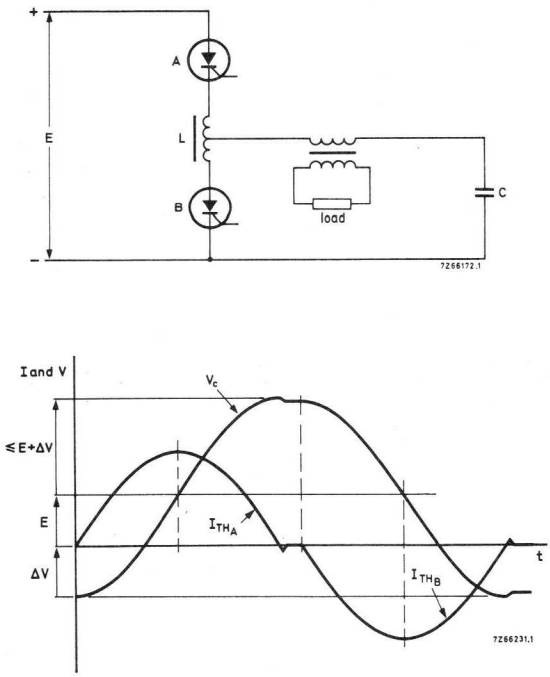


Fig. 5.29. Series inverter and waveforms.
ΔV = overswing.

Fig. 5.30 shows a bridge inverter. When thyristors A and B' are triggered, C charges to the supply voltage and applies its terminal voltage to the primary of the load transformer. When thyristors B and A' are triggered, the voltage across C is switched across thyristors A and B' to turn them off. Then thyristors B and A' charge C in the reverse direction (applying the other half-cycle to the load transformer).

As with the parallel inverter, freewheeling diodes and voltage limiting improve commutation.

This circuit can easily be adapted to three-phase applications.

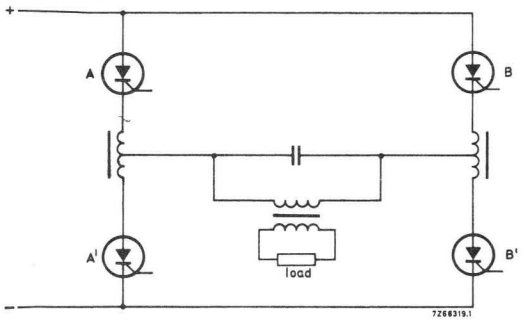


Fig. 5.30. Bridge inverter.

6 Series and Parallel Operation

6.1 Introduction

There are still some applications for which no single existing thyristor has adequate voltage or current ratings; if the voltage demands are too great a series-connected arrangement of thyristors is necessary, while if the current demands are excessive a parallel-connected arrangement is required.

Inevitably, thyristor characteristics vary slightly from one device to another and the resulting "spreads" in characteristics make it necessary for measures to be taken to ensure correct voltage and current sharing. It is with the nature of such measures that this chapter is mainly concerned.

6.2 Series Operation

6.2.1 General

With series-connected thyristors, the design precautions are primarily aimed at equalising the voltages (both forward and reverse) across individual thyristors.

If, for instance, we have three thyristors in series (as in Fig. 6.1) and

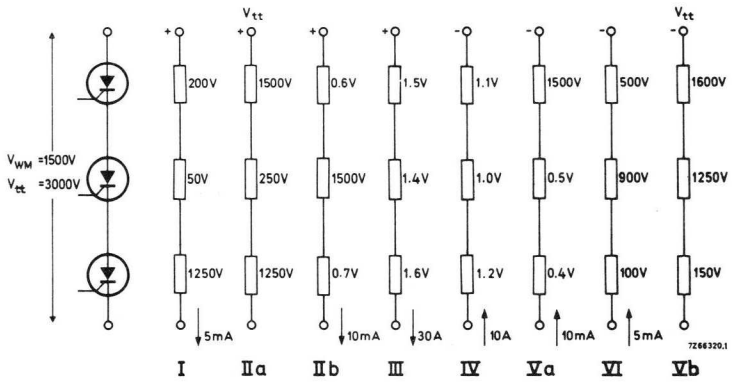


Fig. 6.1. Possible operating states of a series chain consisting of three thyristors without equalization networks.

apply a high voltage across the network thus formed, we find that in the eight possible operating states individual devices can have widely differing voltages across them. Indeed, a single device can at times experience virtually the entire applied network voltage. Thus precautions are needed to prevent this occurring and these can conveniently take the form of equalising resistors and capacitors connected across the thyristors.

States III and IV (Fig. 6.1), of course, provide no problems as the voltages across individual devices are small. In all of the other states (dynamic states II and V and static states I and VI) a high voltage can occur across an individual device and may exceed its maximum rating.

As well as providing a means of voltage equalisation, it is wise to incorporate measures for limiting di/dt and dV/dt to safe levels. We shall consider these too in this chapter. Because of the need for device selection for Q_S, t_d and V_T and the need for large suppression elements when non-avalanche thyristors are used, avalanche thyristors are usually preferable to non-avalanche thyristors. For completeness, however, we shall consider calculations for both types.

6.2.2 Static Voltage Sharing

As we have seen in Fig. 6.1, static voltage sharing must be achieved in both the off-state and the reverse blocking state (states I and VI respectively). Fig. 6.2 shows two thyristors in series – if a d.c. voltage is applied across the combination, either in the forward or the reverse direction, the voltage distribution will not be equal because of the unavoidable spreads in off-state, and reverse-blocking, characteristics. We shall now consider the remedy for both normal and controlled-avalanche thyristors.

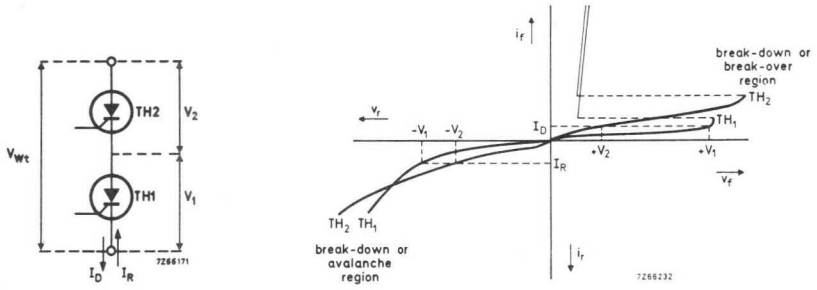


Fig. 6.2. Unequal off-state and reverse-voltage sharing across two thyristors connected in series owing to their spread in reverse and off-state characteristics.

If a resistor is connected in parallel with each thyristor it is possible to obtain such a voltage distribution that the highest voltage across a thyristor does not exceed the maximum allowable value.

Before starting the calculation, check that the off-state and reverse blocking characteristics are similar. (They usually are, as also are the respective leakage currents.) If they are not, calculate R_p separately for off-state and reverse blocking and use the lower of the two values. The most unfavourable case occurs when one ideal thyristor (no leakage current) is connected in series with $n-1$ thyristors which have the maximum leakage current (see Fig. 6.3). Furthermore, owing to the tolerances in R_p, the ideal thyristor can have a parallel resistor with the value $(1+\beta)R_p$ and the other $n-1$ thyristors can have parallel resistors of $(1-\beta)R_p$.

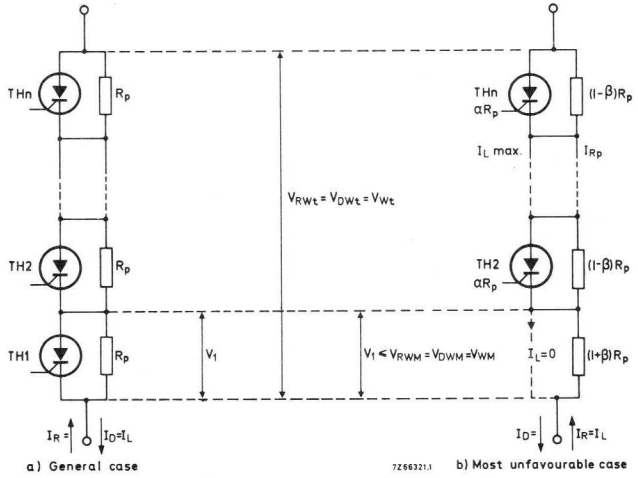


Fig. 6.3. Determination of the off-state and reverse voltage sharing resistor R_p.

In this case, the voltage (V_1) across the ideal thyristor (TH_1) will be

$$V_1 = V_{Wt}\frac{(1+\beta)\,R_p}{(1+\beta)\,R_p + (n-1)\,\alpha R_p(1-\beta)\,R_p/(\alpha R_p + (1-\beta)\,R_p)} \quad (6.1)$$

where $\beta \times 100$ is the % tolerance of the parallel resistor R_p,
$\alpha = I_{Rp}/I_{Lmax}$ is the ratio between the current through R_p (at V_W) and the maximum leakage current (at V_W) of the thyristors
V_{Wt} is the total crest working voltage across the chain.
n is the number of thyristors in the chain.

Because V_1 must not exceed the crest working voltage rating (V_{WM}) of the thyristor, we can write

$$n \geqslant 1 + \frac{V_{Wt} - V_{WM}}{V_{WM}} \cdot \frac{1 + \alpha(1 - \beta)}{\alpha(1 - \beta)}. \tag{6.2}$$

The necessary parallel resistor is then given by

$$V_{WM} \leqslant R_p(1 + \beta)(I_{Lmax} + I_{Rp}).$$

We can also see that

$$I_{Rp} \cdot R_p(1 - \beta) = I_{Lmax}\, \alpha R_p,$$

which yields

$$R_p \leqslant \frac{V_{WM}}{I_{Lmax}} \cdot \frac{1}{(1 + \beta)(1 + \alpha/(1 - \beta))}.$$

If we neglect β^2, we find

$$R_p \leqslant \frac{V_{WM}}{I_{Lmax}} \cdot \frac{1 - \beta}{1 + \alpha(1 + \beta)}, \tag{6.3}$$

R_p dissipation will be (see 6.2.4 for derivation)

$$P_{Rp} = a \frac{{V_{WM}}^2}{R_p} \tag{6.4}$$

where $a = (V_{RMS}/V_{WM})^2$ (In rectifier circuits $a = 0.5$).

For safety, the maximum leakage current (I_{Lmax}) chosen for calculation purposes is that at the specified maximum junction temperature (this eliminates the effect of different thyristor temperatures resulting from unequal forward voltage drops). A practical value for α lies between 3 and 8. (The higher α, the lower the number of series thyristors required for a particular voltage but the greater the loss in R_p.)

Controlled Avalanche Thyristors

In contrast to controlled-avalanche diodes, controlled-avalanche thyristors still need parallel resistors to equalise off-state voltage distribution. The off-state leakage current of the chain can equal the breakover current of one of the thyristors which causes it to switch on.

Calculation of the necessary parallel resistor R_p is similar to that for conventional thyristors, except that a lower value of I_B or a higher value of V_{DWM} may have to be taken into account. V_{RWM} may be exceeded without any resulting damage because the other thyristors in the chain limit the reverse avalanche current to a safe value.

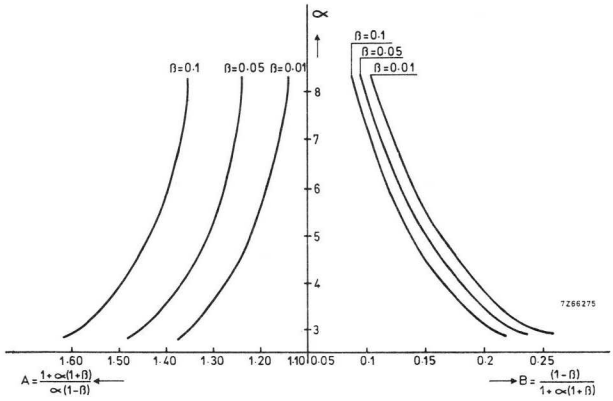


Fig. 6.4. Factors A and B as a function of α with ß (tolerance of R_p) as parameter.

Simple calculation of R_p can be effected by means of the following abbreviations of equations 6.2 and 6.3 respectively.

$$n \geqslant 1 + \frac{V_{Wt} - V_{WM}}{V_{WM}} \cdot A \tag{6.2a}$$

$$R_p \leqslant \frac{V_{WM}}{I_{Lmax}} \cdot B \tag{6.3a}$$

where

$$A = \frac{1 + \alpha(1 + \beta)}{\alpha(1 - \beta)}$$

and

$$B = \frac{1 - \beta}{1 + \alpha(1 + \beta)}.$$

Fig. 6.4 shows A and B as a function of α with β as parameter.

6.2.3 Dynamic Voltage Sharing

Dynamic voltage sharing must be accomplished in the presence of transients in both forward (off-state) and reverse directions. Such transients can be internally or externally generated. External causes are:

1. "switch-off" of an unloaded rectifier transformer on the primary side.
2. "switch-on" of a rectifier transformer – especially a step-down type.
3. "switch-off" of the inductive load of a rectifier on the secondary side of the transformer.
4. stroke of lightning on the mains.
5. switching in the supply circuit.
6. blowing of a fuse.

Internal causes are:

1. hole storage effect.
2. stray capacitance.
3. unequal switching on of thyristors – caused by differences in turn-on times.

External transients can be suppressed by the methods detailed in Chapter 4. Unequal switching on of thyristors can be minimised by the use of a trigger pulse of fast risetime and high amplitude (but even so the effect will not be negligible). The remaining transients are less harmful and can be dealt with by the provision of a capacitive path in parallel with each individual thyristor.

Before a thyristor can regain the reverse voltage blocking capability after conduction, the charge present in the thyristor at the time of commutation must be removed. This charge is removed at a rate ($\mathrm{d}i/\mathrm{d}t$) determined by the commutating inductance of the circuit. Fig. 6.5 shows the manner in which this charge extraction occurs.

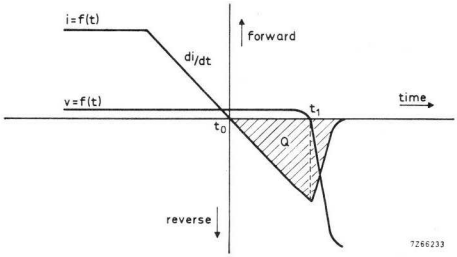


Fig. 6.5. Reverse recovery of a thyristor.

In a network of two thyristors in series, the "worst case" condition arises when one thyristor (TH_1) is a fast device (having a value of recovered charge Q_{min}) and the other (TH_2) is slow (recovered charge Q_{max}) – see Fig. 6.6.

At time t_1, TH_1 has recovered while TH_2 still has some stored charge (ΔQ which equals $Q_{max} - Q_{min}$) remaining. TH_1 assumes its reverse voltage capability and tries to take up the full voltage V_{RWt}. Additionally, it reduces the recovery current i_R for TH_2 so that it will be even longer before TH_2 can take up reverse voltage. Thus a low impedance path for recovery current must be made available to TH_2. This is achieved by the provision of a parallel capacitor C_p across each thyristor (avalanche devices do not need this as they have a low impedance in the avalanche region – though they may still have a parallel capacitor for other reasons).

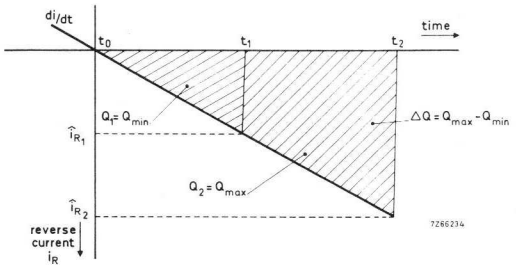


Fig. 6.6. Idealized reverse recovery of two different thyristors.

Furthermore, in the blocking state (I, IIa, Va and VI in Fig. 6.1) thyristors have their own individual capacitance (different for individual devices). Also, thyristors and their associated heatsinks have a certain capacitance C_e to earth. These capacitances contribute to unequal voltage distribution in the presence of a transient. Thus we have further need for parallel equalising capacitors.

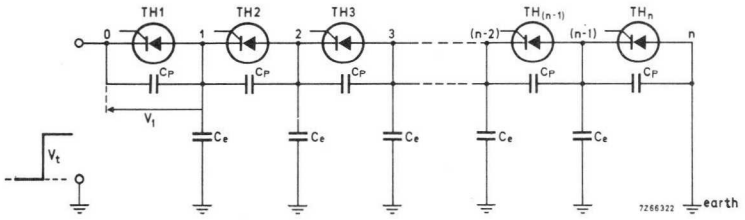


Fig. 6.7. Series connection of n thyristors with parallel capacitor C_p and earth capacitance C_e.

Conventional Thyristors

Fig. 6.7 shows n thyristors in series and the parallel capacitors connected across them. If TH_1 is fast and the other $n-1$ are equally slow, at time t the situation is that shown in Fig. 6.8.

Reverse recovery current continues to flow through C_p – charging it to a voltage V_1'. This voltage is, of course, a function of the remaining charge ΔQ. Thus

$$V_1' = \frac{\Delta Q}{C_p}. \tag{6.5}$$

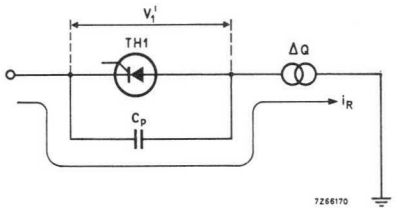


Fig. 6.8. Simplification of Fig. 6.7 at time $t_1 < t < t_2$, when only Th_1 has recovered.

After all thyristors have recovered, there will still be an unequal voltage distribution across them because of the earth capacitance C_e. When a voltage V_t is applied as shown in Fig. 6.7, the voltage V_1'' across TH_1 will be (assuming the devices have infinite leakage resistance)

$$V_1'' = \frac{C_n}{C_p + C_n} \cdot V_t \tag{6.6a}$$

where C_n is the substitutional capacitance from Point 1 to Point n (earth). If C_p is small with respect to C_n, a large part of V_t is developed across TH_1 (Fig. 6.9). The earth capacitance C_e can be determined from Fig. 6.10.

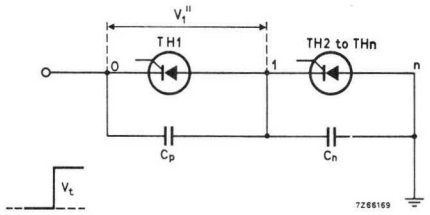


Fig. 6.9. Substitution of the capacitances between point 1 and point n by C_n.

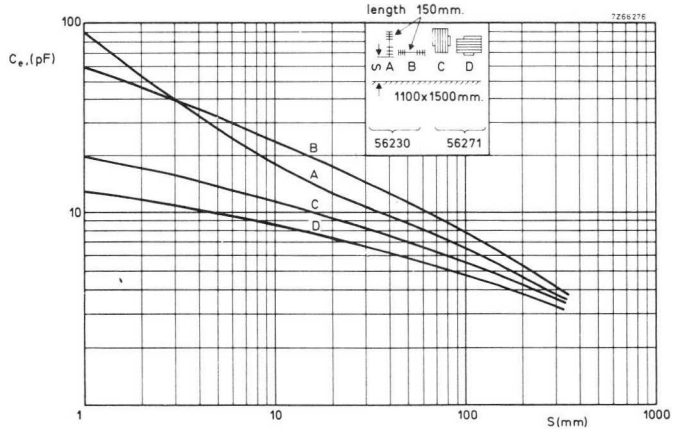


Fig. 6.10. Earth capacitance C_e of standard heatsinks as a function of the distance to earth.

The peak voltage caused by C_e occurs across the thyristor at the "hot" end of the chain, while the voltage resulting from the spread in reverse recovery charge occurs across the fastest thyristor. So the most unfavourable condition occurs if the fastest device is located at the "hot" end of the chain.

When reverse voltage is applied to the chain, a reverse recovery current flows. If TH_1 is the fastest device and TH_2 to TH_n are equally slow, when TH_1 has recovered, the reverse recovery current for the remaining devices can only flow through the C_p which is parallel to TH_1; thus C_p will be charged until the other thyristors have recovered. When the other thyristors have recovered, the voltage across TH_1 will be V_1' (Eq. 6.5). Then the remaining part of the commutation voltage V_{RWt} must be distributed across all thyristors. The part of this voltage which is picked up by TH_1 is V_1'' (Eq. 6.6a), which we can express

$$V_1'' = \frac{C_n}{C_p + C_n}(V_{RWt} - V_1'). \tag{6.6b}$$

The total voltage across TH_1 is the sum of the two partial voltages, i.e.

$$V_1 = V_1' + V_1'' = V_1' + \frac{C_n}{C_p + C_n}(V_{RWt} - V_1'). \tag{6.7}$$

If we substitute Eq. 6.5 in Eq. 6.7 and make

$$b = \frac{C_n}{C_p + C_n}, \tag{6.8a}$$

we obtain

$$V_1 = \frac{\Delta Q}{C_p}(1 - b) + V_{RWt}\, b. \tag{6.9}$$

But V_1 must not exceed the repetitive peak reverse voltage rating, V_{RRM}, of the thyristor so

$$V_{RRM} \geqslant V_1 = \frac{\Delta Q}{C_p}(1 - b) + V_{RWt}\, b. \tag{6.10a}$$

From Fig. 6.11 we can obtain C_p.

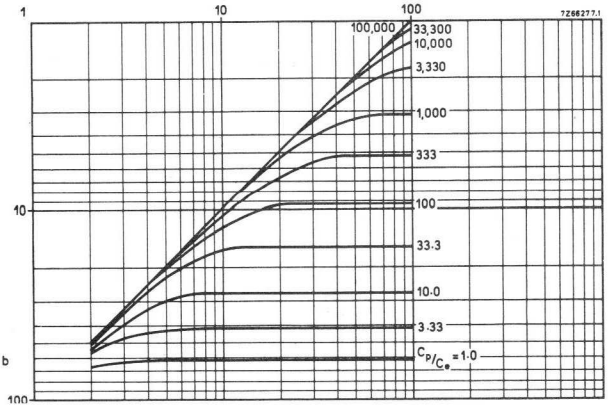


Fig. 6.11. $b = C_n/(C_n + C_p)$ as a function of the number n of devices connected in series, with the ratio between parallel capacitor and earth capacitance C_p/C_e as parameter.

As can be seen from Fig. 6.11, Eq. 6.8a will be

$$b = \frac{1}{n} \tag{6.8b}$$

for high values of C_p/C_e.

So, to a first approximation, Equation 6.10a can be written

$$C_p \geqslant \frac{\Delta Q\,(n-1)}{nV_{RRM} - V_{RWt}}. \tag{6.10b}$$

The value of C_p necessary for sharing externally generated transients may now be calculated. Transient voltage V_{tt} (off-state or reverse $V_{Rtt} = V_{Dtt} = V_{tt}$) exceeds the total crest working voltage V_{Wt} (off-state or reverse $V_{RWt} = V_{DWt} = V_{Wt}$) by $V_{tt} - V_{Wt}$. This last value $(V_{tt} - V_{Wt})$ has to be distributed across the thyristors in such a way that the thyristor at the "hot" end of the chain experiences a part equal to $b\,(V_{tt} - V_{Wt})$ as given by Eq. 6.6a. If the best thyristor is located at the "hot" end of the chain, it already has an off-state or reverse voltage which is maximum V_{WM} $(V_{RWM} = V_{DWM} = V_{WM})$. The total transient voltage across a thyristor may not exceed V_{RM} $(V_{RRM} = V_{DRM} = V_{RM})$, so

$$V_{RM} - V_{WM} \geqslant b\,(V_{tt} - V_{Wt}) \tag{6.11}$$

(see Fig. 6.12).

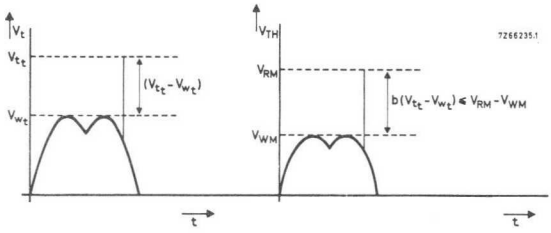


Fig. 6.12. Distribution of transient voltages across a series chain of thyristors.

We can now, by means of this relation, find the necessary value of b for a certain transient voltage V_{tt} (both off-state and reverse). Then, by means of Fig. 6.11, we can find the required value of C_p.

Now we may consider measures for sharing turn-on transients. Fig. 6.13 shows a typical thyristor turn-on characteristic. Turn-on time t_{on} is the sum of the delay time t_d and the rise time t_r ($t_{on} = t_d + t_r$). Of course,

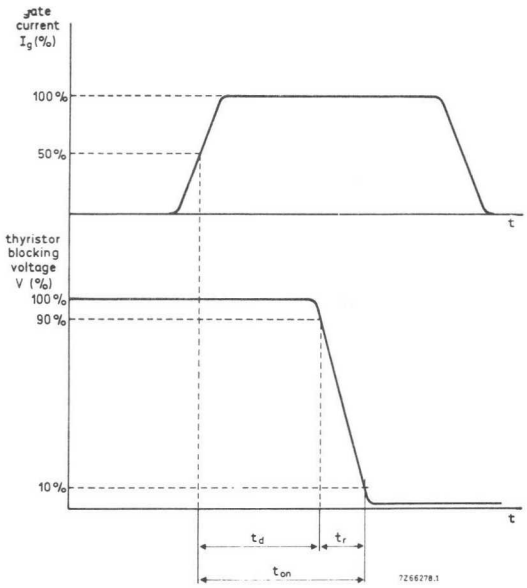


Fig. 6.13. Typical turn-on characteristic for a thyristor.

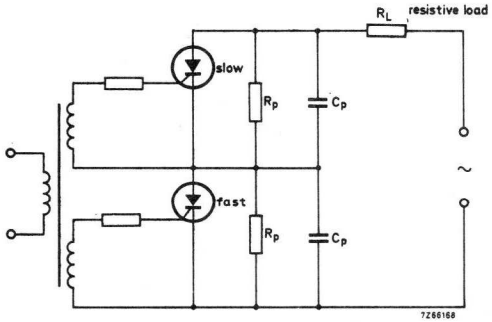


Fig. 6.14. Half-wave rectifier circuit with two thyristors connected in series – one with a fast and the other with a slow turn-on.

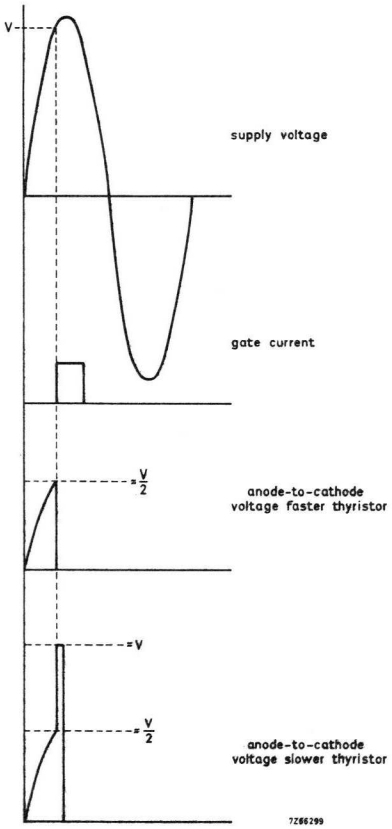


Fig. 6.15. Waveforms for Fig. 6.14.

t_{on} is liable to differ from one sample to another; Fig. 6.14 shows two thyristors, with maximum spread in t_{on}, connected in series in a half-wave rectifier circuit. The waveforms are shown in Fig. 6.15. It can be seen that a transient appears across the slower thyristor and may exceed its voltage rating. There are two standard methods of overcoming this problem – a parallel capacitor and an inductance in series with the load.

To ascertain the correct value of the parallel capacitor, we shall again consider a series chain of n thyristors. The worst case occurs when all thyristors except one turn on simultaneously at supply voltage maximum (the slow thyristor TH_1 fires after a delay Δt_{on}). Fig. 6.16 shows the equivalent circuit; the voltage across TH_1 will vary as shown in Fig. 6.17 (this is an approximation which is sufficiently accurate for the small time interval Δt_{on}). The general expression for the voltage rise across TH_1 is

$$v = V\left(1 - \exp\left(-\frac{t}{\tau}\right)\right) \tag{6.12a}$$

From Fig. 6.17 we obtain

$$V_{DRM} - V_{DWM} \geqslant (V_{DWt} - V_{DWM})\left\{1 - \exp\left(-\frac{\Delta t_{on}}{R_L C_p}\right)\right\}, \tag{6.12b}$$

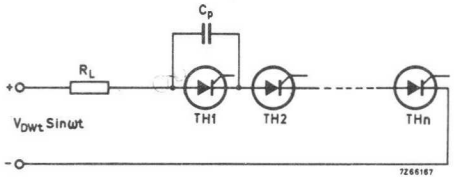


Fig 6.16. Equivalent circuit when TH_1 is off and all other thyristors (TH_2 to TH_n) are on.

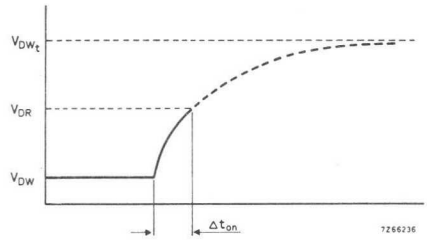


Fig. 6.17. Voltage across the slow thyristor TH_1 in Fig. 6.16.

which yields

$$C_p \geqslant \frac{\Delta t_{on}}{R_L \ln (V_{DWt} - V_{DWM})/(V_{DWt} - V_{DRM})}. \tag{6.13}$$

Usually this gives a very large value of C_p which is unacceptable because of the high switch-on currents. However, most rectifier circuits contain some inductance and an equivalent circuit can be drawn as shown in Fig. 6.18. The voltage waveform across TH_1 is shown in Fig. 6.19. (Again the short time interval Δt_{on} makes simplifications possible – $R_L = 0$ and V_{DWt} is constant – and this approximation errs on the side of safety. An exact calculation would be long and unmanageable.)

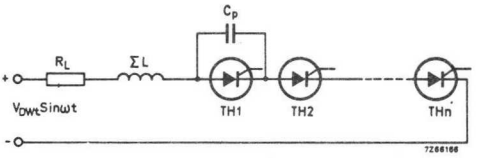


Fig. 6.18. Equivalent circuit when TH_1 is off and all other thyristors are on.

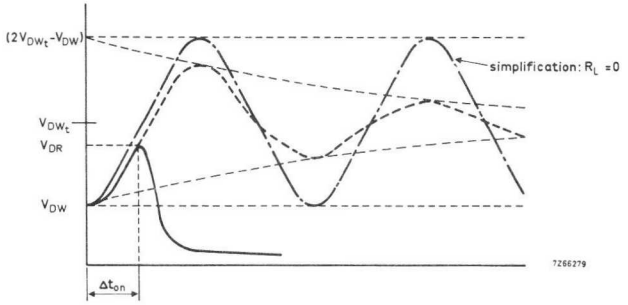


Fig. 6.19. Voltage across the slow thyristor TH_1 in Fig. 6.18.

Voltage rises across TH_1 according to the relation

$$v = V \cos \omega t. \tag{6.14a}$$

From Fig. 6.19 we obtain

$$V_{DRM} \geqslant V_{DWt} - (V_{DWt} - V_{DWM}) \cos \omega \, \Delta t_{on}. \tag{6.14b}$$

where

$$\omega^2 = \frac{1}{\Sigma L C_p}.$$

From these we obtain

$$\Sigma L \geqslant \frac{\Delta t_{on}{}^2}{C_p \, [\arccos (V_{DWt} - V_{DRM})/(V_{DWt} - V_{DWM})]^2}. \tag{6.15}$$

If C_p is chosen according to Eqs. 6.10 and 6.11, the minimum required value of ΣL can be determined. Already in the circuit are the self-inductance of the transformer and the self-inductance of the load; if ΣL is greater than the combined value of these two, an extra inductor will have to be added. A resistor, R_s (see Fig. 6.20), must be connected in series with C_p to limit the discharge rate of C_p at turn-on and thus prevent $\mathrm{d}i/\mathrm{d}t$ damage to the thyristors. R_s can be obtained from

$$\mathrm{d}i/\mathrm{d}t(C_p) = \frac{V_{DRM}}{R_s t_f'} \exp\left(-\frac{t}{R_s C_p}\right), \tag{6.16}$$

where t_f' is the idealised fall-time of the thyristor anode voltage.

In addition, the current rise introduced by commutation ($\mathrm{d}i/\mathrm{d}t_{(com)}$) must be attended to; it is given by

$$\mathrm{d}i/\mathrm{d}t_{(com)} \leqslant \frac{V_{DWt}}{L_s} \cdot \frac{t}{t_f'}. \tag{6.17}$$

The sum of these two $\mathrm{d}i/\mathrm{d}t$ values must not exceed the device rating. Thus

$$\mathrm{d}i/\mathrm{d}t_{\max} \geqslant \mathrm{d}i/\mathrm{d}t_{(Cp)} + \mathrm{d}i/\mathrm{d}t_{(com)}. \tag{6.18a}$$

Substituting Eqs. 6.16 and 6.17 in 6.18a we obtain

$$\mathrm{d}i/\mathrm{d}t_{\max} \geqslant \frac{V_{DWt}}{L_s} \cdot \frac{t}{t_f'} + \frac{V_{DRM}}{R_s t_f'} \exp\left(-\frac{t}{R_s C_p}\right), \tag{6.18b}$$

$\mathrm{d}i/\mathrm{d}t_{(com)}$ is maximum at $t = t_f'$, while $\mathrm{d}i/\mathrm{d}t_{(Cp)}$ is maximum at $t = 0$.

It is desirable for $\mathrm{d}i/\mathrm{d}t_{\max}$ to occur at $t = t_f'$ because at that moment a larger area of crystal will be in conduction and therefore the turn-on dissipation will be minimised. This condition is obtained if

$$\mathrm{d}i/\mathrm{d}t_{\max} \geqslant \frac{V_{DWt}}{L_s} + \frac{V_{DRM}}{R_s t_f'} \exp\left(-\frac{t_f'}{R_s C_p}\right) \geqslant \frac{V_{DRM}}{R_s t_f'}. \tag{6.19}$$

From this a minimum value of R_s can be calculated:

$$\left(\mathrm{d}i/\mathrm{d}t_{\max} - \frac{V_{RWt}}{L_s}\right) \frac{R_s \min t_f'}{V_{DRM}} \geqslant \exp\left(-\frac{t_f'}{R_s \min C_p}\right). \tag{6.20}$$

The maximum allowable value for R_s is governed by reverse recovery. When reverse recovery current starts to fall, the circuit inductances react to maintain $\hat{i}_R$. This current can only pass through R_s – giving a voltage drop across it equal to V_{Rs} which must not exceed the V_{RRM} rating of the thyristor. Thus

$$V_{RRM} \geqslant V_{Rs} = \hat{i}_R R_s \tag{6.21a}$$

and

$$R_s \max \leqslant \frac{V_{RRM}}{\hat{i}_R}. \tag{6.21b}$$

At the end of the reverse recovery interval an RCL circuit is energised and oscillations may occur which impose excessive voltages across the thyristors. To prevent this, we must ensure that the system is (over-)critically damped i.e.

$$R_s^2 \geqslant \frac{4 \Sigma L}{C_p}. \tag{6.22}$$

We must now find the value of the rate-of-rise of off-state voltage which occurs when the above values of C_p, R_s and ΣL are used.

If we assume a mechanical switch to be in series with the chain and that this switch closes when the supply voltage is at maximum (V_{DWt}), the voltage across the chain rises (independently of the margin of damping and thus independently of C_p) at a rate

$$\mathrm{d}V/\mathrm{d}t_{(tot)} = V_{DWt} \frac{nR_s}{\Sigma L}. \tag{6.23}$$

Because R_s is small compared with the leakage resistance of the thyristors and R_p, $\mathrm{d}V/\mathrm{d}t_{(tot)}$ will be distributed equally across the thyristors. Thus

$$\mathrm{d}V/\mathrm{d}t_{(Th)} = V_{DWt}\frac{R_s}{\Sigma L}. \tag{6.24}$$

This value must not exceed the maximum allowable value; thus

$$\mathrm{d}V/\mathrm{d}t_{\max} \geqslant V_{DWt}\frac{R_s}{\Sigma L}. \tag{6.25}$$

Another way of limiting the voltages across individual thyristors to an acceptable level is to connect controlled-avalanche diodes back-to-back across each thyristor. It is still necessary, however, to connect a series RC network across each thyristor to limit $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}V/\mathrm{d}t$. Fig. 6.20 shows all the components used; their functions are as follows:

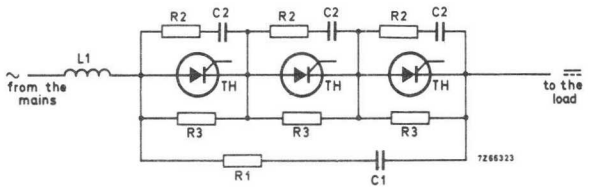


Fig. 6.20. The components used with series-connected thyristors.

L_1 is the line inductance already present. To limit $\mathrm{d}i/\mathrm{d}t$, it can be enlarged by the insertion of an additional choke.

C_1 limits $\mathrm{d}V/\mathrm{d}t$ and transient commutation overvoltage across the string.

R_1 has to be inserted in the L_1C_1 oscillatory circuit to give sufficient damping and to limit the discharge current of C_1 and associated $\mathrm{d}i/\mathrm{d}t$-value through the thyristors when string is turned-on.

R_3 serves as a shunt path for the leakage current through the thyristors and equalizes the static voltage distribution.

C_2 equalizes the spread of junction and earth capacitance, and reverse recovery charge (dynamic voltage sharing).

R_2 acts similarly to R_1, limiting the discharge current of C_2 and, therefore, the turn-on $\mathrm{d}i/\mathrm{d}t$ through the individual thyristors.

The components R_2, R_3 and C_2 are always necessary for series operation of thyristors, whereas L_1, R_1 and C_1 may be needed for certain circuit configurations and loads.

Clearly, the design procedure we have just been through is lengthy and involved; the design procedure with controlled-avalanche thyristors is much simpler and it is to this that we will now turn our attention.

Controlled-Avalanche Thyristors

When controlled-avalanche thyristors are used, reverse-recovery current can continue flowing through the fastest thyristor. However, the dissipation capability is still limited so the necessary avalanche power rating must be determined in order that suitable thyristors can be chosen. A method of determining the avalanche power rating necessary for the thyristors is given in the following analysis.

In Fig. 6.6, the idealised reverse-recovery of two different thyristors is shown. At t_1 the fast thyristor TH_1 attains its nominal reverse-blocking capability and at t_2 TH_2 does the same. During the time $\Delta t = t_2 - t_1$, the difference in charge ΔQ must be compensated. A current i_R flows in the avalanche region of the fastest device so we may express the energy

$$E = \int_{t_1}^{t_2} i_R(t)\, V_{(BR)R}\, \mathrm{d}t, \tag{6.26}$$

which, because

$$\Delta Q = \int_{t_1}^{t_2} i_R(t)\, \mathrm{d}t,$$

we may write

$$E = \Delta Q V_{(BR)R}. \tag{6.27}$$

For maximum energy, add 15% to the maximum reverse-avalanche voltage at room temperature (This will include temperature effect and influence of dynamic resistance in the avalanche region).
Time t_1 is obtained from

$$Q_{\min} = \frac{\hat{i}_{R1} t_1}{2}$$

$$= \frac{1}{2} \cdot \mathrm{d}i/\mathrm{d}t \cdot {t_1}^2 \quad \rightarrow \quad t_1 = \sqrt{\left(\frac{2Q_{\min}}{\mathrm{d}i/\mathrm{d}t}\right)} \tag{6.28}$$

and t_2 from

$$Q_{\max} = \frac{\hat{i}_{R2} t_2}{2}$$

$$= \frac{1}{2} \cdot \mathrm{d}i/\mathrm{d}t \cdot {t_2}^2 \quad \rightarrow \quad t_2 = \sqrt{\left(\frac{2Q_{\max}}{\mathrm{d}i/\mathrm{d}t}\right)}. \tag{6.29}$$

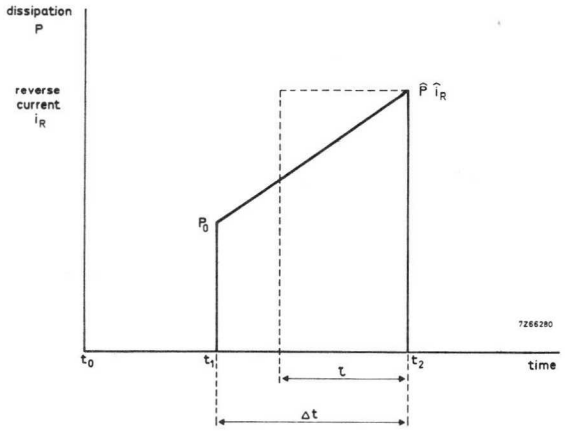


Fig. 6.21. Reverse-recovery current and avalanche power as a function of time.

The dissipation P is a function of time (see Fig. 6.21 – the solid line). A square pulse of amplitude $\hat{P}$ and duration τ (the dotted line) will give the same rise in temperature.

$\hat{P}$ is given by

$$\hat{P} = V_{(BR)R}\, \hat{i}_R. \tag{6.30}$$

From Eq. 6.29

$$Q_{\max} = \frac{\hat{i}_{R2} t_2}{2}$$

$$= \frac{{\hat{i}_{R2}}^2}{2\mathrm{d}i/\mathrm{d}t}$$

$$\therefore\ \hat{i}_{R2} = \sqrt{(2Q_{\max}\, \mathrm{d}i/\mathrm{d}t)}. \tag{6.31}$$

As $\hat{i}_R = \hat{i}_{R2}$, the peak avalanche power will be

$$P = V_{(BR)R} \sqrt{(2Q_{\max} \, \mathrm{d}i/\mathrm{d}t)} \tag{6.32}$$

and this must be dissipated during the time

$$\tau = \frac{\Delta t \, \{2 + \sqrt{(Q_{\min}/Q_{\max})}\}^2}{9}, \tag{6.33}$$

which may also be written

$$\tau = \sqrt{\left(\frac{2}{\mathrm{d}i/\mathrm{d}t}\right)} \cdot \frac{4{Q_{\max}}^{2/3} - 3{Q_{\max}}^{1/2}Q_{\min} - {Q_{\min}}^{3/2}}{9Q_{\max}} \tag{6.34}$$

Calculation with this expression is awkward; it is easier to use a graph (see Fig. 6.22) of

$$\tau \sqrt{\left(\frac{\mathrm{d}i/\mathrm{d}t}{Q_{\max}}\right)} = f\left(\frac{Q_{\min}}{Q_{\max}}\right). \tag{6.35}$$

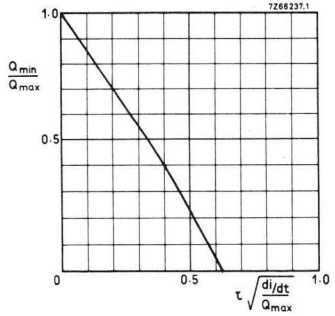


Fig. 6.22. $Q_{\min}/Q_{\max}$ *as a function of* $\tau \sqrt{(\mathrm{d}i/\mathrm{d}t)/Q_{\max}}$ *derived from Eq. 6.35.*

$$\left(\textit{note that } \tau \sqrt{\frac{\mathrm{d}i/\mathrm{d}t}{Q_{\max}}} = \frac{4\sqrt{2}}{9}\left[1 - 3/4\,\frac{Q_{\min}}{Q_{\max}} - 1/4\left(\frac{Q_{\min}}{Q_{\max}}\right)^{3/2}\right]\right)$$

If the avalanche power capacity required is greater than the published value of any otherwise suitable and available thyristor, a parallel capacitor C_p must be used to accomodate the excess power. This may be calculated as follows.

Thyristor data will give a certain permissible duration, τ', for $\hat{P}$. The charge ($\Delta Q'$) which must be absorbed by C_p can be calculated from

$$Q'_{\min} - Q_{\min} = \Delta Q' \tag{6.36}$$

after $Q'_{\min}$ has been calculated, at the existing value of $Q_{\max}$, from Eq. 6.35.
An amount

$$\Delta Q'' = Q_{\max} - Q'_{\min} \tag{6.37}$$

will be supplied by a current i_R in the avalanche region. C_p can now be found from

$$V_{(BR)R} = \frac{\Delta Q'}{C_p} \qquad \rightarrow \quad C_p = \frac{\Delta Q'}{V_{(BR)R}}. \tag{6.38}$$

If the fastest thyristor has a minimum value of $V_{(BR)R}$, $\Delta Q'$ will be small and thus $\Delta Q''$ will be relatively large; this gives rise to a large value of τ so it is important to determine at this stage whether the expected power pulse is still within the thyristor ratings.

We will now, briefly, consider the effects of external transients (both forward and reverse). A reverse transient will be distributed across all thyristors in the series chain; if the chain cannot handle this energy the limitation measures must be made more stringent. An off-state transient (forward) can either turn on the chain and dissipate its energy in the load or (if this is not permissible) be distributed across the thyristors, without exceeding their minimum breakover voltage $V_{(BO)\min}$, by means of capacitors C_p. In this latter case the calculation is similar to that for non-avalanche devices (see Eq. 6.39 and Fig. 6.12).

$$V_{(BO)\min} - V_{DWM\max} \geqslant b\,(V_{tt} - V_{DWt}). \tag{6.39}$$

Sharing of turn-on transients is not necessary because, when the slower devices reach an off-state voltage which exceeds their $V_{(BO)}$, they will be forced to turn on. However, it is still necessary to ensure that the permissible $\mathrm{d}i/\mathrm{d}t$ values for $V_{(BO)}$ are not exceeded (calculation method is the same as that for non controlled-avalanche thyristors).

6.2.4 Practical Considerations

In general, practical experience has shown that:

a. Controlled-avalanche thyristors are almost essential,

b. Off-state voltage sharing must be obtained by means of parallel resistors.

c. Calculation of the necessary parallel capacitor must be based on off-state transient sharing (mains-born and transformer-switching transients) and increase of reverse commutation capability during commutation.

d. A resistor must be connected in series with the capacitor to limit di/dt and dV/dt to safe values. (Note: if a thyristor is turned on by excessive V_{BO} or dV/dt, a smaller fall-time t_f is obtained – leading to higher di/dt – than with gate triggering. Additionally, in this case, the di/dt *rating* is lower.)

Dissipation in the Parallel Resistor

The dissipation in the parallel resistor R_p is given by

$$P_{Rp} = \frac{V_{RMS}^2}{R_p} \tag{6.40}$$

where V_{RMS} is the maximum r.m.s. voltage across the thyristor. V_{RMS}^2 can be calculated from V_{WM} for various circuit configurations if a form factor a is known. Then

$$a = \frac{V_{RMS}^2}{V_{WM}^2} \tag{6.41}$$

Substituting this in Eq. 6.40 gives

$$P_{Rp} = a \frac{V_{WM}^2}{R_p} . \tag{6.42}$$

We now need to know a for typical configurations.

In a thyristor rectifier circuit the highest r.m.s. value of blocking voltage occurs when the conduction angle is zero, i.e. the voltage is a complete sine wave (Fig. 6.23). Then

$$a = \frac{1}{2\pi} \int_0^{2\pi} \sin^2 x \, dx$$

$$= \frac{1}{2\pi} \left[\frac{x}{2} - \frac{\sin^2 x}{4} \right]_0^{2\pi} = \frac{1}{2\pi} \cdot \pi = 0.5. \tag{6.43}$$

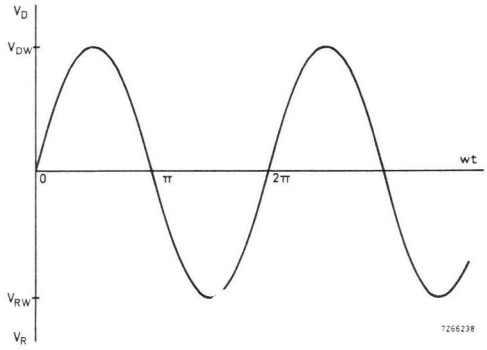


Fig. 6.23. Maximum blocking voltage in any thyristor rectifier circuit.

In square-wave inverter or chopper circuits, a is equal to the off-state duty cycle (see Fig. 6.24). Thus

$$a = \frac{t_1}{T}. \tag{6.44}$$

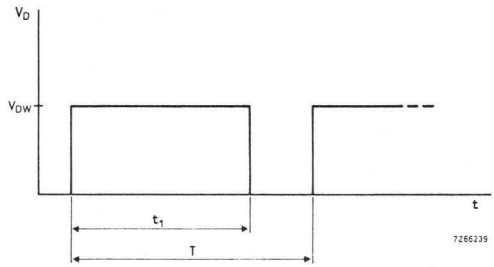


Fig. 6.24. Off-state voltage in square-wave inverter or chopper circuits.

However, if a very slow switching action is used calculation must be done as for a continuous d.c. blocking voltage. Then

$$a = 1. \tag{6.45}$$

If a sawtooth wave is applied to the series chain (Fig. 6.25), then

$$a = \frac{1}{T}\int_0^T \left(\frac{t}{t_1}\right)^2 \mathrm{d}t$$

$$= \frac{1}{T}\left[\frac{t^3}{3\,t_1{}^2}\right]_0^{t_1} = \frac{1}{T}\,\frac{t_1{}^3}{3\,t_1{}^2} = \frac{t_1}{3\,T}. \tag{6.46}$$

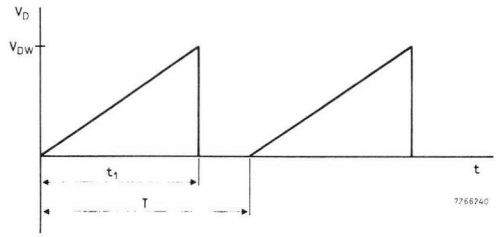


Fig. 6.25. Sawtooth wave applied to a series chain of thyristors.

Triggering

When a thyristor is turned on there is first a delay time (t_d), then a fall time (t_f), then a spreading time (t_s), and finally the normal-working time. With fast rise of trigger pulse ($\mathrm{d}I_g/\mathrm{d}t$) and high I_g peak, the thyristor switches on quickly (i.e. t_d is small); however, although t_d can be minimised by this means, t_f is very little influenced by trigger pulse characteristics.

For series operation, high fast-rising trigger pulses are needed to minimise t_d and ensure that turn-on points are as nearly coincident as possible (thus it becomes unlikely that V_{BO} will be reached across the slowest device). If avalanche types are used, this is not so important but it cannot be neglected because $\mathrm{d}i/\mathrm{d}t$ damage can result from V_{BO} turn-on.

Similarly with parallel operation – turn-on points must be as closely synchronised as possible because a slow device may have insufficient voltage across it, when parallel devices are already conducting, to turn on.

Fusing

Chapter 4 deals with fusing in detail; however, at this point it is as well to bear in mind that fusing is usually needed for the protection of thyristors in series and parallel connections. Fast-acting fuses should be provided to cope with overloads which would otherwise destroy a thyristor within one half-cycle (lesser overloads, which would not break down a thyristor until more than 10 ms had elapsed, are usually dealt with by means of overload contactors).

The I^2t rating for the fuse must, of course, be less than that for the thyristor it is protecting.

6.2.5 Worked Example

Let us assume that we have a controllable three-phase bridge rectifier which gives a d.c. output of 11 kV at 90 A. The transformer is rated at 1100 kVA and the short-circuit voltage is 10%.

Rate of change of current during commutation can be assumed to be

$$\mathrm{d}i/\mathrm{d}t \approx 0.3 \text{ A}/\mu\text{s}.$$

At the maximum junction temperature $T_{j\,\max} = 125\ ^\circ\text{C}$, the following spread in reverse recovery charge occurs in the controlled avalanche thyristor:

$$Q_{\min} = 5\ \mu\text{C}, \quad Q_{\max} = 20\ \mu\text{C}.$$

Maximum crest-working voltage, V_{Wt}, across the series chain is

$$\begin{aligned} V_{Wt} &= 1.05\ V_o \times 1.15 \\ &= 13.3 \text{ kV} \end{aligned}$$

where the factor 1.15 is provided to allow for the unloaded transformer voltage and fluctuations in the mains.

For this thyristor

$$V_{RWM} = V_{DWM} = V_{WM} = 1200 \text{ V}.$$

Thus (from Eq. 6.2) the number of thyristors required in series (assuming $\alpha = 3$ and $\beta = 0.05$) is

$$n \geqslant 1 + \frac{V_{Wt} - V_{WM}}{V_{WM}} \text{ A}$$

$$= 1 + \frac{13300 - 1200}{1200} \times 1.46$$

$$= 14.7$$

so $n = 15$.

We find, from data sheets, that

$$I_{L\,\max} = I_D = I_R = 13 \text{ mA}.$$

Thus (from Eq. 6.3) we can find R_p as follows

$$R_p \leqslant \frac{V_{WM}}{I_{L\max}} B$$

$$= \frac{1200}{0.013} \times 0.229$$

$$= 21\,200\ \Omega,$$

so a value of $R_p = 18\ \text{k}\Omega \pm 5\%$ would be suitable.

Dissipation in R_p (from Eq. 6.42) at $a = 0.5$ is

$$P_{Rp} = a \frac{{V_{WM}}^2}{R_p}$$

$$= 0.5 \frac{1200^2}{18 \times 10^2}$$

$$= 40 \text{ W}.$$

The necessary value of C_p can now be obtained.

First, from Eq. 6.32, we find

$$\hat{P} = V_{(BR)R} \sqrt{(2Q_{\max}\, \mathrm{d}i/\mathrm{d}t)}$$

$$= 1300 \sqrt{(2 \times 20 \times 0.3)}$$

$$= 4.5 \text{ kW}.$$

From Data sheets

$$\frac{Q_{\min}}{Q_{\max}} = \frac{5}{20}$$

$$= 0.25.$$

From Eq. 6.35 and using values found from Fig. 6.22,

$$\tau \sqrt{\left(\frac{\mathrm{d}i/\mathrm{d}t}{Q_{\max}}\right)} = f\left(\frac{Q_{\min}}{Q_{\max}}\right) = 0.49$$

$$\therefore \tau = 0.49 \sqrt{\left(\frac{Q_{\max}}{\mathrm{d}i/\mathrm{d}t}\right)}$$

$$= 0.49 \sqrt{\left(\frac{20}{0.3}\right)}$$

$$= 4\ \mu\mathrm{s}.$$

At 4 μs and $T_{j\,\max}$, $P_{RRM\,\max} = 12.5$ kW (extrapolated from 9 kW at 10 μs). Thus no parallel capacitor is required for the reverse recovery charge.

However, a parallel capacitor is required to ensure optimum transient distribution; it must have a much higher value than C_e, the earth capacitance of the thyristor and heatsink. If we assume a value of at least 20 pF (see Fig. 6.10) for C_e, C_p is given by (see Fig. 6.11)

$$C_p \geqslant 3330\, C_e$$

$$= 3330 \times 20$$

$$= 67\ \mathrm{nF}.$$

Now Eq. 6.8b is valid for this case and the maximum allowable input transient can be calculated by means of Eq. 6.39 as follows

$$V_{BO\,\min} - V_{DWM\,\max} \geqslant b\,(V_{tt} - V_{DWt})$$

$$\therefore 1300 - 1200 \geqslant \frac{1}{15}(V_{tt} - 13300)$$

$$\therefore V_{tt} \leqslant 14.8\ \mathrm{kV}.$$

If higher transients are expected, additional measures must be taken (e.g. filters across the transformer windings).

As the thyristors can be turned on by excessive V_{BO}, much shorter fall times may occur than would normally be expected with gate turn-on; t_f can be as little as 50 ns. Thus R_s should be calculated from

$$R_s \approx \frac{V_{BO}}{\mathrm{d}i/\mathrm{d}t \,.\, t_f}$$

$$= \frac{1300}{50 \times 0.05}$$

$$= 520\ \Omega.$$

The next higher standard value is 560 Ω. If $\mathrm{d}V/\mathrm{d}t$ is not limited sufficiently with this relatively high value of R_s, a separate RC filter must be connected across the whole chain to keep $\mathrm{d}V/\mathrm{d}t$ down to a safe level.
On the basis of these calculations we can draw the circuit of Fig. 6.26.

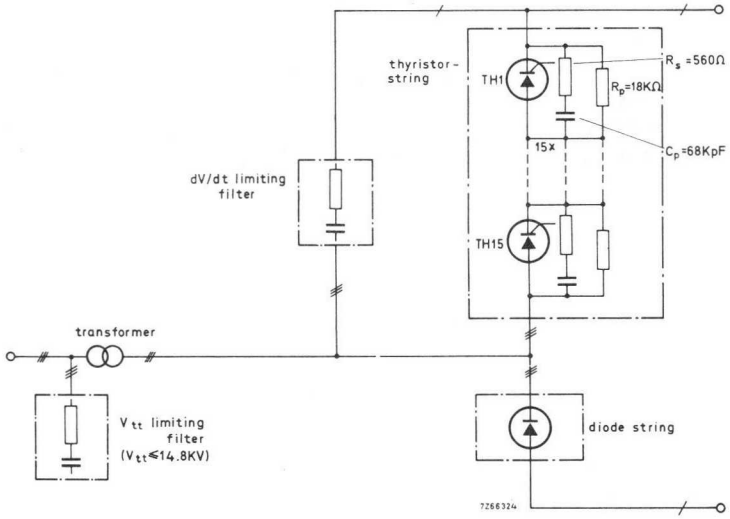


Fig. 6.26. Rectifier layout of the worked example. (There are several other methods for the V_{tt} and $\mathrm{d}V/\mathrm{d}t$ filters).

6.3 Parallel Operation

6.3.1 General

When thyristors are connected in parallel, it is essential that current is shared equally between the parallel paths. Techniques of achieving equal current distribution fall broadly into three categories

a. selection of devices with matched forward conduction characteristics
b. current and temperature derating
c. forced current sharing by external means.

Of these, the latter two are the most important as they are the easiest to use in practice. We shall consider the first one briefly and then devote most of our time to the latter two.

6.3.2 Selection of Matched Forward Characteristics

Matching of forward conduction characteristics poses problems for both the manufacturer and the user; for the latter it may be extremely difficult to replace devices in a bank consisting of many matched paralleled thyristors.

In order that current will be shared reliably under both normal and fault conditions, matching must be carried out for forward voltage at two quite different current levels. Voltage unbalance can occur (and destroy the effect of matching) if resistances and inductances of the parallel paths are not equal – so special care must be taken with these. Also, temperature differences between individual devices must be eliminated. (This is often done quite effectively by mounting the devices close together on a common heatsink.)

6.3.3 Current and Temperature Derating

There is, inevitably, a spread in the forward conduction characteristics in any unmatched batch of thyristors of a given type. Thus, if they are connected in parallel, the best thyristor (lowest forward voltage drop) will take most current. By this means, the forward dissipation rating of the best thyristor may be exceeded and the device may well be destroyed. However, this danger is avoided if the total current taken from the paralleled thyristors is decreased to a value at which (taking account of the sharing) the best device is not overloaded. The published maximum

value of the worst sample is used to estimate the maximum allowable current through the paralleled thyristors, because this gives a calculation error on the safe side. This method is known as current derating.

For calculation simplicity, we can assume the thyristor forward characteristic to be like that of a normal diode, i.e.

$$V_{in} = V_o + IR.$$

Fig. 6.27 shows histograms of spreads in forward characteristics for a

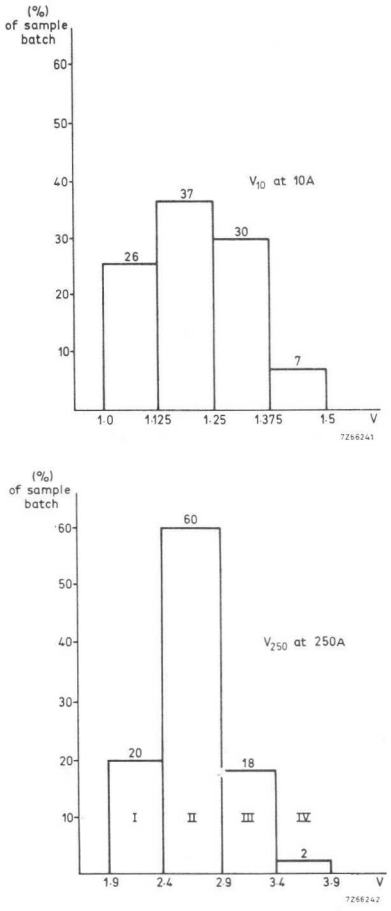


Fig. 6.27. Histograms of spreads in forward characteristics.

certain thyristor – first at 10 A forward current, then at 250 A forward current.

Dissipation of a thyristor is given by

$$P = i_{AV} \cdot V_o + i_{r.m.s.}{}^2 r.$$

So, in a six-phase rectifier circuit, the dissipation is

$$P_6 = \frac{\hat{i}}{6} V_0 + \frac{\hat{i}^2}{6} r \tag{6.47}$$

The worst sample (see Fig. 6.27) has $V_{250} = 3.9$ V and $V_{10} = 1.5$ V. From these values we will now calculate V_o and r; thus

$$V_o = \frac{25 \cdot V_{10} - 10 \cdot V_{250}}{240}$$

$$= 1.4 \text{ V}$$

and

$$r = \frac{V_{250} - V_{10}}{240}$$

$$= 0.01\ \Omega.$$

The maximum rated forward current $(\hat{i})$ is 100 A so, from Eq. 6.47, the maximum forward dissipation is 40 W.

From the histogram, we can see that the best device has $V_{250} = 1.9$ V and $V_{10} = 1.0$ V – and thus $V_o = 0.96$ V and $r = 0.00375\ \Omega$. If we had used these values for a maximum dissipation of 40 W, the peak forward current would be about 155 A; this is 55% above that allowable for the worst device. Similar calculations, for thyristors having characteristics which lie between the best and worst ones, provide the maximum allowable current values given in Table 6.1.

It is now possible to calculate the maximum allowable currents for various combinations of thyristors from the batch considered in Fig. 6.27. These are given in Fig. 6.28 and Table 6.2. In Table 6.2, Column A applies if the thyristors used come from all four groups, Column B applies if the thyristors come from Groups 2, 3 and 4, Column C applies if the thyristors come from Groups 3 and 4 and Column D applies if the thyristors come only from Group 4.

Table 6.1 Allowable forward current

V_{250}	percent of nominal maximum current	
(V)	%	
1.9	155	best sample
2.15	144	average sample of group I
2.4	135	
2.65	127	average sample of group II
2.9	120	
3.15	114	average sample of group III
3.4	109	
3.65	104	average sample of group IV
3.9	100	worst sample

Table 6.2 Allowable forward current for combinations of thyristors

group	percentage of nominal current			
	A	B	C	D
I	144	—	—	—
II	90	127	—	—
III	57	86	114	—
IV	37	61	83	100

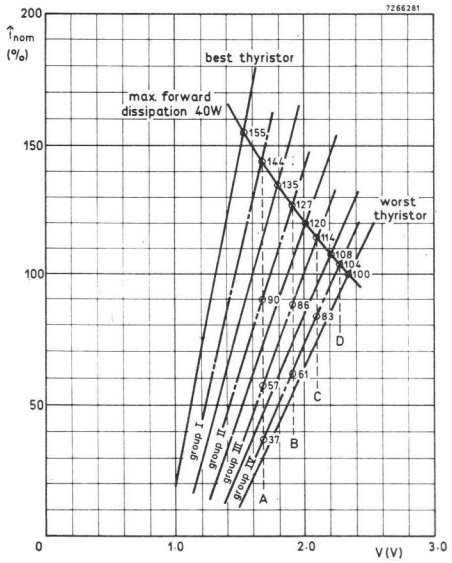


Fig. 6.28. Maximum allowable current per thyristor for various forward characteristics.

Fig. 6.29 shows the current derating factor as a function of the number of thyristors in parallel with the chance of overloading the best thyristor as parameter. The two dashed lines are the curves for chances of 0.1 % and 0.01 % and the full line represents the recommended derating

$$d = 0.65 + \frac{0.35}{n}.$$

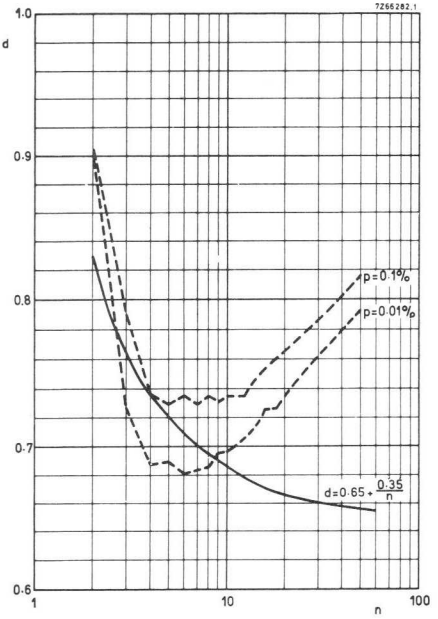


Fig. 6.29. Derating factors for 2 to 50 thyristors in parallel, for 0.1 % and 0.01 % chance p of overloading the best thyristor.

If this derating factor is used, the chance of exceeding the maximum current value (indicated in Table 6.2) in the best thyristor is 0.1 %. A rather more severe derating is required, of course, if an overload chance of only 0.01 % is required (i.e. $d = 0.55 \times 0.45/n$).

Sometimes, temperature derating rather than current derating may be used. If the base-to-ambient thermal resistance is made very low for all the parallel thyristors, it is possible to keep the junction temperature of the best thyristor below the maximum permitted level. By this means, the

maximum total current can reach the maximum rated current per thyristor times the number of thyristors in parallel without damaging any thyristor. Thus a saving can be effected by elimination of the need for extra thyristors. However, the larger heatsink(s) or increased forced-air cooling required may not be acceptable.

6.3.4 Forced Current Sharing

Forced current sharing, brought about by additional circuit components, can eliminate the need for current derating. There are two principal methods of achieving such sharing – a resistor in series with each thyristor, and a system of current balancing inductors.

Fig. 6.30 shows the circuit connection for the resistive method and illustrates the method of operation by showing the effect of the series resistors (which are of equal value) on the forward characteristics of the thyristors.

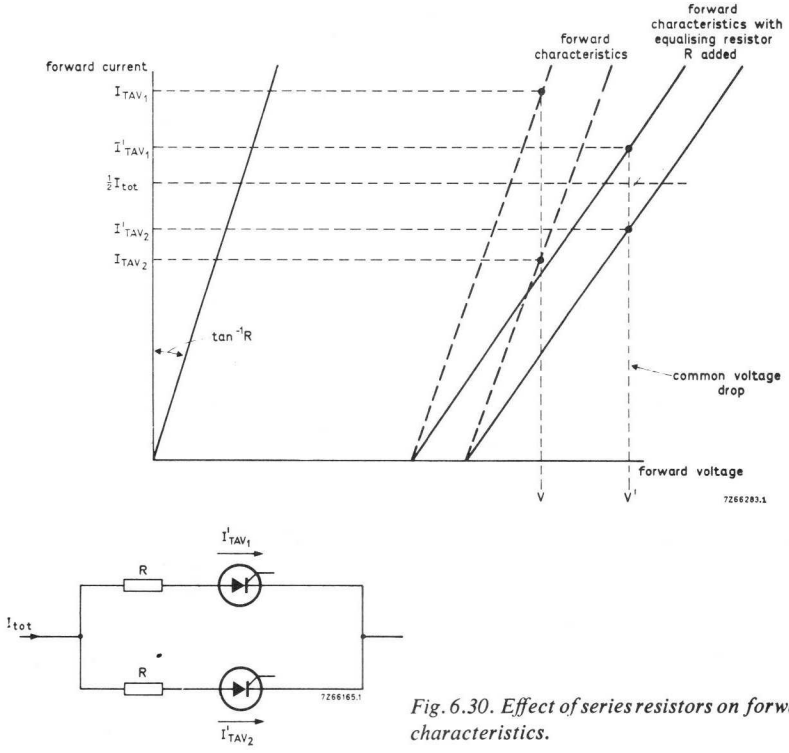


Fig. 6.30. Effect of series resistors on forward characteristics.

As can be seen in Fig. 6.30, the equal resistors in each diode branch reduce the effect of the spread in forward characteristics. Resistor tolerances must be low (usually $\pm$ 5%).

This method obviously increases power losses and affects both system efficiency and load regulation. If fuses are installed in the branches their resistances must be subtracted from the calculated values of the series resistors; all other resistances in the thyristor circuit must be minimised (or at least equalised).

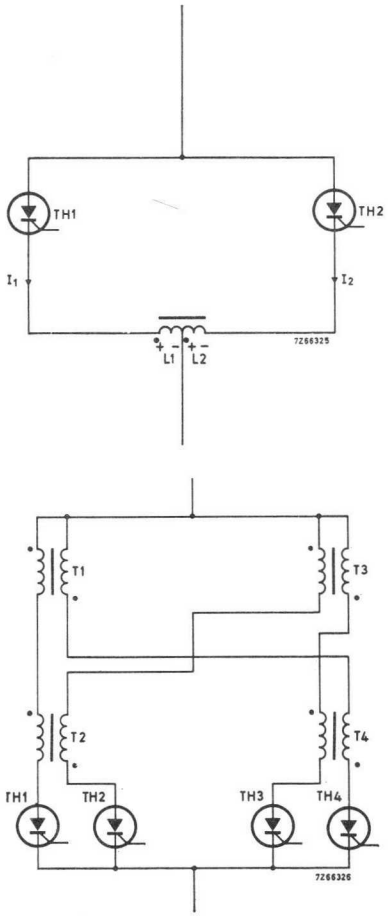


Fig. 6.31. Current balancing by inductors for (a) two thyristors, (b) four thyristors.

Current sharing by means of balancing inductors is to be preferred to the resistor method because it gives rise to little power loss. Furthermore, these inductors will equalise spreads in turn-on delay times. Fig. 6.31 shows first the basic connection (for two thyristors only) and then a suitable connection scheme for four thyristors.

The operating principle can best be understood by reference to Fig. 6.31(a). If TH_1 has the "better" forward characteristic, and/or it turns on faster than TH_2, the resulting current I_1 sets up a voltage, across L_1 and L_2 as shown; this voltage opposes I_1 and encourages I_2 – thus tending to equalise I_1 and I_2. When the conduction period ends, one current decreases first – producing a voltage which tends to equalise I_1 and I_2.

We recommend that the value of inductance (in mH) of each winding be

$$L = \frac{20\,000}{I\,\omega_{supply}}$$

where I is the repetitive peak current (in A).

Such a balancing reactor should have high saturation-flux density and low residual-flux density – to give maximum change in flux each cycle. Also, the core must not saturate during the conduction period.

Postscript

The aim of this book has been to present theory of operation, design principles, and control techniques for thyristors; some information on manufacturing technology has also been included.

Applications, (designed and developed in our own application laboratories), as a basis for practical circuits for our customers are described in separate publications.

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